Lab 1

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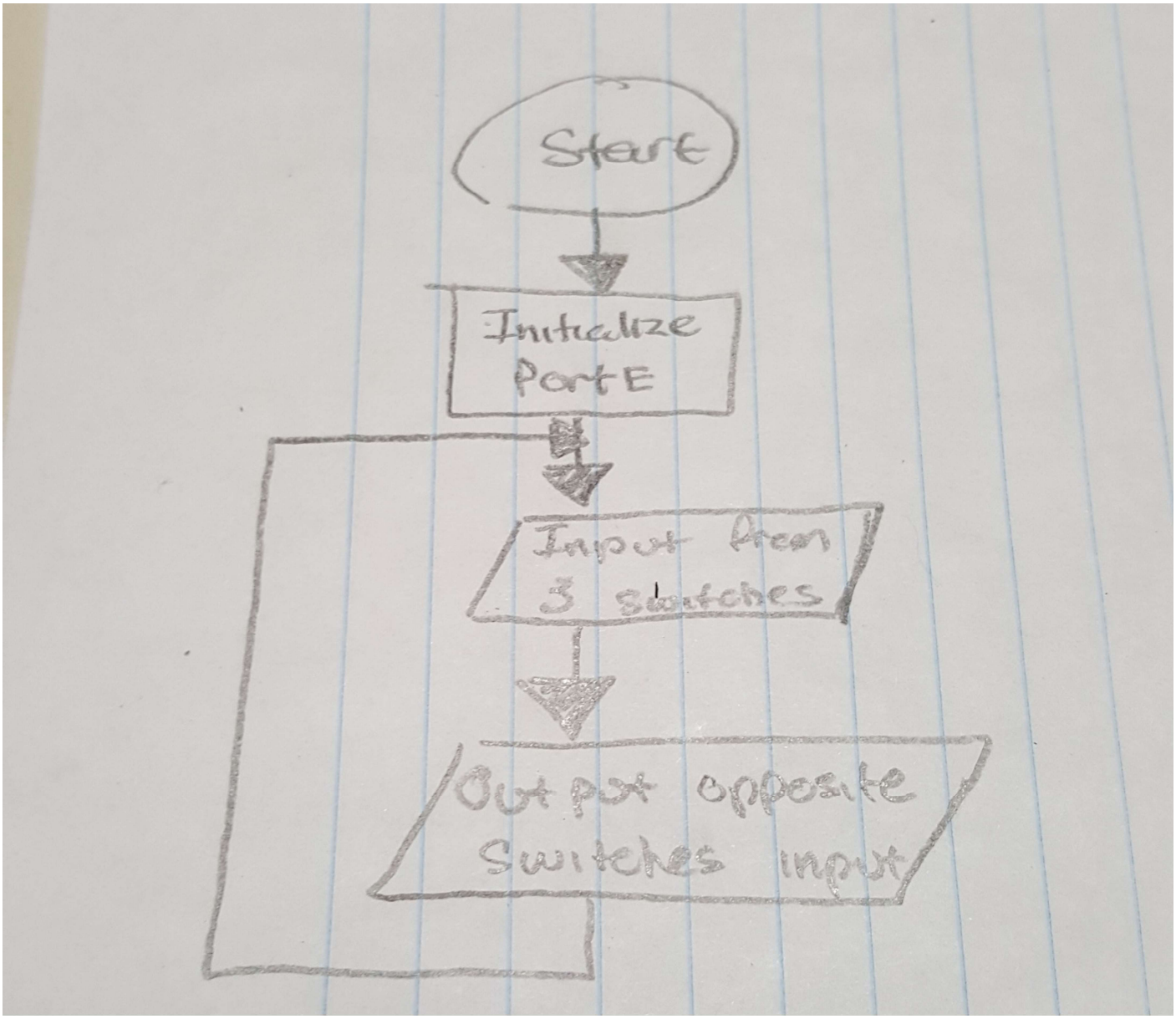
Flow Chart



Pseudo-code

Initialization
Step 1: Initialize clock, disable analog and alternate functionality, set regular digital function, set pin 2 as output, and enable digital I/O on port E

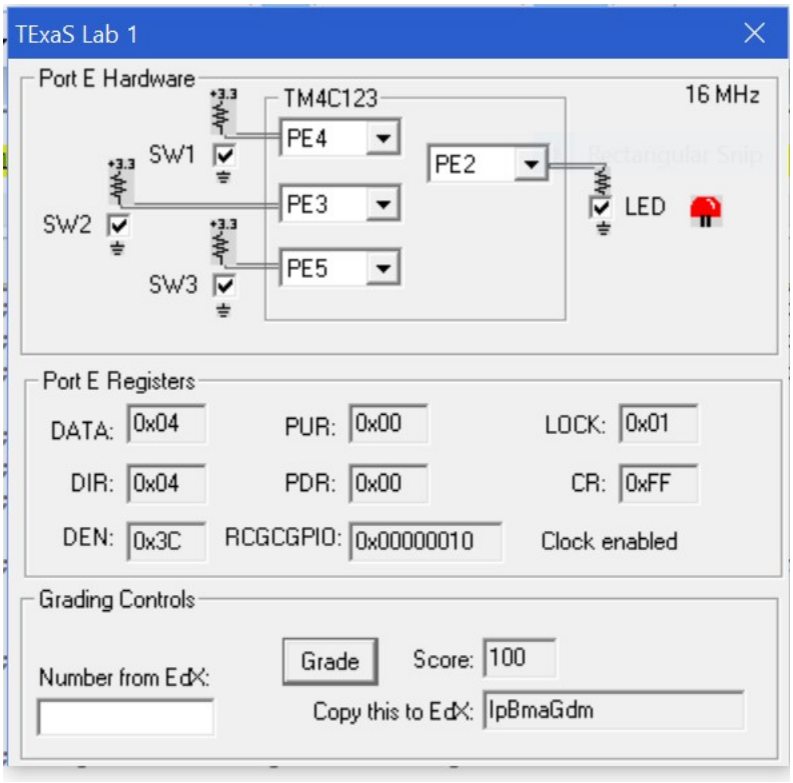
Loop
Step 2: Exclusive OR bits 3, 4, and 5 of port E data register and put solution into registers
Step 3: Logical shift each register enough for each set exclusive OR'd bit to be in bit 2 of each register
Step 4: AND one register with 2 registers with exclusive OR'd bit
Step 5: Save value of AND'd register into port E data register
Step 6: Loop back to repeat algorithm

Assembly Code

```
;****************** main.s ***************
; Program written by: Chimezie Iwuanyanwu (cci273)
; Date Created: 1/22/2015
; Last Modified: 2/3/2016
; Section Wednesday 5-6
; Instructor: Ramesh Yerraballi
; Lab number: 1
; Brief description of the program
; The overall objective of this system is a digital lock
; Hardware connections
;  PE3 is switch input  (1 means switch is not pressed, 0 means switch is pressed)
;  PE4 is switch input  (1 means switch is not pressed, 0 means switch is pressed)
;  PE5 is switch input  (1 means switch is not pressed, 0 means switch is pressed)
;  PE2 is LED output (0 means door is locked, 1 means door is unlocked)
; The specific operation of this system is to
; unlock if all three switches are pressed

GPIO_PORTE_DATA_R      EQU   0x400243FC
GPIO_PORTE_DIR_R       EQU   0x40024400
GPIO_PORTE_AFSEL_R     EQU   0x40024420
GPIO_PORTE_DEN_R       EQU   0x4002451C
GPIO_PORTE_AMSEL_R     EQU   0x40024528
GPIO_PORTE_PCTL_R      EQU   0x4002452C
SYSCTL_RCGCGPIO_R      EQU   0x400FE608

        AREA    |.text|, CODE, READONLY, ALIGN=2
        THUMB
        EXPORT  Start
Start
        LDR R1, =SYSCTL_RCGCGPIO_R
        LDR R0, [R1]
        ORR R0, #0x10
        STR R0, [R1]
        NOP
        NOP

        LDR R1, =GPIO_PORTE_AMSEL_R
        LDR R0, [R1]
```

```
        AND R0, #0xC3
        STR R0, [R1]

        LDR R1, =GPIO_PORTE_PCTL_R
        LDR R0, [R1]
        AND R0, #0xC3
        STR R0, [R1]

        LDR R1, =GPIO_PORTE_DIR_R
        LDR R0, [R1]
        AND R0, #0xC3
        ORR R0, #0x04
        STR R0, [R1]

        LDR R1, =GPIO_PORTE_AFSEL_R
        LDR R0, [R1]
        AND R0, #0xC3
         STR R0, [R1]

        LDR R1, =GPIO_PORTE_DEN_R
        LDR R0, [R1]
        ORR R0, #0x3C
        STR R0, [R1]

loop
        LDR R1, =GPIO_PORTE_DATA_R
        LDR R0, [R1]

        EOR R2, R0, #0x20
        EOR R3, R0, #0x10
        EOR R4, R0, #0x08

        LSR R2, #3
        LSR R3, #2
        LSR R4, #1

        AND R2, R3
        AND R2, R4

        AND R0, #0xFB
        ORR R0, R2
        STR R0, [R1]

        B loop

ALIGN
END
```

Screenshot


TExaS Lab 1
Port E Hardware
TM4C123
16 MHz
SW1
SW2
SW3
PE4
PE3
PE5
PE2
LED
Port E Registers
DATA: 0x04
PUR: 0x00
LOCK: 0x01
DIR: 0x04
PDR: 0x00
CR: 0xFF
DEN: 0x3C
RCGCGPIO: 0x00000010
Clock enabled
Grading Controls
Number from EdX:
Grade
Score: 100
Copy this to EdX: IpBmaGdm