SAI GIRI PS

A Graduate student mastering VLSI design and Embedded systems

A dedicated engineer, fueled by the constantly evolving landscape of technology. Proficient in VLSI design and equipped with exceptional team management and leadership abilities.

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WORK EXPERIENCE

R&D INTERN

ABB Innovation Center

01/2023 - Present *Bengaluru*

Tasks

- Responsible for the development of **remote I/O unit** modules in relay networks.
- Implementation of **CAN protocol** for communication between remote I/O modules.
- Development of drivers code, application code for communication module and sensor module in relay network
- **Integration testing** for sensor module along with its **timing analysis** using Protection and Control IED Manager software tool.

EDUCATION

M.Tech , VLSI Design & Embedded Systems

R V College of Engineering, Bengaluru

02/2022 - Present *CGPA : 8*

B.E , Electrical and Electronics Engineering

Impact College of Engineering and Applied Sciences, Bengaluru

08/2017 - 08/2021 *CGPA : 8.1*

Pre University course , PCMB

SJRC BIFR Pre university college, Bengaluru

06/2015 - 03/2017 *68.5 %*

SSLC

S L V Vidyanikethana High School, Bengaluru

04/2014 - 04/2015 *84.96 %*

LANGUAGES

English

Kannada

Telugu

Hindi

SKILLS

C programming | Python 3 | Verilog HDL | System Verilog basics | TCL scripting | UVM (basics) | Cadence Virtuoso & Genus | Xilinx Vivado | Intel Quartus prime | Digital IC Design | VLSI Testing | Analog IC design basics | Physical design | Static Timing Analysis

PROJECTS

Development of Low-End Communication Module for Remote I/O units in Control systems (Major Project) (02/2023 - Present)

- Tools used: PCM600, Keil 4, Processor Expert, CAN Analyzer.
- To develop the wired communication module for communication between user and relay network.
- Listing the specifications, selecting target uC, generating drivers code, writing application code, flashing and functional testing.

Design and implementation of magnitude comparator using Hybrid GDI logic (Published in IJRAR) (03/2022 - 05/2022)

- Tool used: Cadence Virtuoso(180nm technology)
- Impact: High speed(1.2ns) and low power consumption(1.34nW) was achieved for the design in tradeoff with area utilization.

Design and Synthesis of 16-bit Vedic Squaring digital circuit using carry save adders (Verilog HDL code) (03/2021 - 05/2021)

- Tool used: Xilinx vivado.
- Impact: The proposed Vedic squaring circuit proved to be efficient in terms of area utilization.

Design of high-speed, low-power Programmable Frequency Divider using 32|33|47|48 multi-modulus Prescalar circuit along with pre-layout and post-layout analysis (02/2023 - 05/2023)

- Tool used: Cadence Virtuoso (45 nm technology)
- Impact: The proposed design consumes average power of 46.4 uW, 97.7 nW for 32|33 and 47|48 respectively.
- The proposed design performs frequency division up to 18 GHz without distortion.

CERTIFICATES

"Analog VLSI Layout Design" certification from RV College of Engineering. (09/2022)

"Industrial environment Monitoring System using IOT" certification from Nano Robotics and Embed Systems. (12/2020)

I do hereby declare that the above information stated is true and complete to the best of my knowledge.