

# **REDUCTION OF COMMON MODE VOLTAGE USING VARIOUS CARRIER BASED PWM TECHNIQUES**

A major project report submitted in partial fulfillment of the requirements for the award of the degree of

*Bachelor of Technology*

*in*

## **Electrical and Electronics Engineering**

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***Certificate***

This is to certify that the project entitled "**REDUCTION OF COMMON MODE VOLTAGES USING VARIOUS CARRIER BASED PWM TECHNIQUES**" is a bonafide work done by **B. Sai Gowtham Teja (179X1A0208)**, **B. Suresh (179X1A0207)**, **D. Ramanjineyulu (189X5A02E3)**, **N. Lavanya (179X1A0269)** in partial fulfillment of the requirements for the award of degree of **Bachelor of Technology** in **Electrical and Electronics Engineering** during the academic year 2020-2021.

The results embodied in this major project have not been submitted to any other University or Institute for the award of any degree.

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## **ABSTRACT**

The Project is about the Reduction of Common Mode Voltage (CMV) using various Carrier Based PWM Techniques. Pulse Width Modulation (PWM) inverter has been widely applied to many ac motor drives. It is well known that conventional two-level inverters generate high-frequency common-mode voltages with high  $dv/dt$ . To reduce the common mode voltage there is an alternate solution i.e., implementing multilevel inverter employing PWM Technique. Multilevel Inverter offers high power capability, associated with lower output harmonics and lower commutation losses. In this project cascaded multilevel inverter topology is used. Similarly this multilevel inverter also generates common mode voltage. To reduce the common mode voltage Carrier Based PWM Techniques are employed. The simulation of Multilevel Inverter Topologies employing Carrier Based PWM Techniques are carried out in MATLAB Simulink.

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# **CHAPTER 1**

## **INTRODUCTION**

In today's world most of the appliances and machines work on AC power. In the absence of AC power, there should be some ways to convert DC power to AC power. This conversion is done by the power electronic circuit called the Inverter. The input voltage, output voltage and frequency, and overall power handling depend on the design of the specific device or circuitry. The inverter has been widely used in AC drive fields due to the energy saving, reliability and performance indicators of great advantage.

If the DC input voltage is fixed but not controllable, a variable output voltage is obtained by varying the pulse width of the converter which is achieved by Pulse Width Modulation Technique (PWM) control.

In recent, as Pulse Width Modulation (PWM) inverter has been widely applied to many ac motor drives, a number of problems such as motor bearing damages, electromagnetic interference (EMI), breakdown of winding insulation, and motor leakage current have been reported. It has been clarified that the common mode voltage itself as well as the  $dv/dt$  of this voltage in inverter-fed AC motor drives are responsible for the most of these problems. Also, conventional inverters generate high frequency common mode voltage.

Multilevel inverter is an alternative solution for high power & medium voltage A.C Drive. The present work explores control of common mode voltage and reduction in THD (Total Harmonic Distortion) for three-phase motor drives using different Multilevel Inverter Topologies employing various carrier based pulse width modulation techniques such as PD, POD and APOD.

# CHAPTER 2

## INVERTER

### 2.1 INTRODUCTION

A converter which converts fixed DC power to Variable AC power is called Inverter. Fig.2.1 represents the basic inverter diagram.

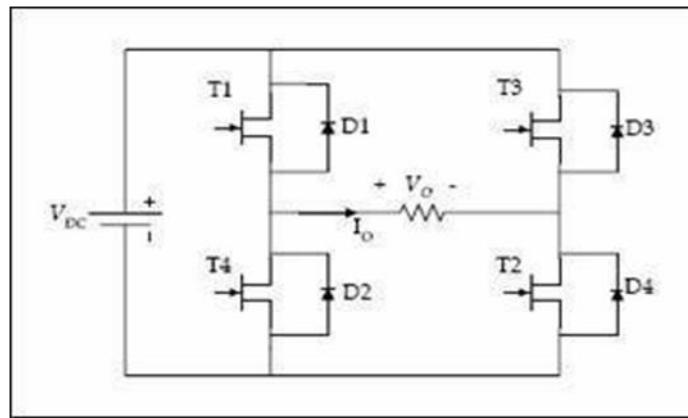


Fig.2.1. Basic Inverter Diagram

Inverters are classified into different types based on the type of commutation they are

- Load Commutated Inverters

Load Commutated Inverters are high frequency inverters in which the size of the inverter is reduced and cost of the inverter is low. Load Commutated Inverters are used in Induction heating applications.

- Line Commutated Inverters

In Line Commutated Inverters, The commutation process is done due to Line voltages. It is also a rectifier operating with firing angle greater than  $90^\circ$ .

- Forced Commutated Inverters

The forward current does not pass through zero naturally and must therefore be forced to become zero at appropriate instants by means of auxiliary circuit. These are classified into two types based on the type of source connected to it, They are 1) Voltage Source Inverter and 2) Current Source Inverter.

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Inverters are used in a wide range of applications, from small switched power supplies for a computer to large electric utility applications to transport bulk power. This makes them very suitable for when you need to use AC power tools or appliances.

### **2.2 PULSE WIDTH MODULATION**

To control the output voltage of an inverter there are two methods are there, They are 1) External Control Methods and 2) Internal Control Methods. Pulse Width Modulation comes under Internal Control method. In Pulse Width Modulation (PWM) technique, pulses of constant amplitude but different duty cycles are generated by modulating the time periods. This modulation is done by using one carrier and one reference signal. These two signals are fed to a comparator and the corresponding signals are generated based on the logic of the comparator. The reference wave is the desired signal output which may be a sine wave or a square wave. The carrier wave, on the other hand is generally saw-tooth or triangular wave having frequency significantly higher than that of the reference signal. The higher order harmonics in the load current are eliminated using a series inductor. A selected range of lower harmonics can be reduced by suitably choosing the number of pulses per half cycle.

#### **Advantages of PWM:**

- The output voltage control with method can be obtained without any additional components.
- With this method, lower order harmonic can be eliminated or minimized along with it's output voltage control.
- It reduces the filtering requirements.

There are three basic PWM techniques:

1. Single Pulse Width Modulation
2. Multiple Pulse Width Modulation
3. Sinusoidal Pulse Width Modulation

In this Project Sinusoidal PWM technique was employed.

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### Sinusoidal Pulse Width Modulation Technique

The voltage source inverter that use PWM switching techniques have a DC input voltage ( $V_{DC} = VS$ ) that is usually constant in magnitude. The inverter job is to take this DC input and to give AC output, where the magnitude and frequency can be controlled. There are several techniques of Pulse Width Modulation (PWM). The efficiency parameters of an inverter such as switching losses and harmonic reduction are principally depended on the modulation strategies used to control the inverter.

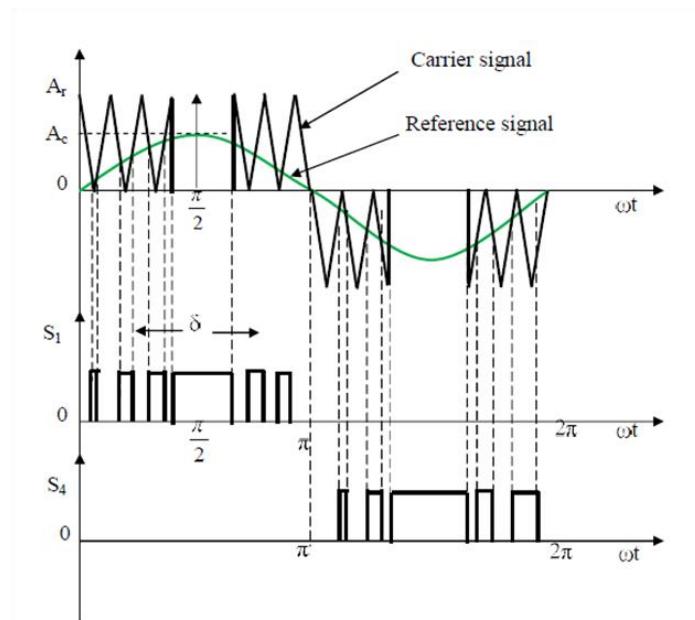


Fig.2.2. Sinusoidal Pulse width modulation diagram

In this design the Sinusoidal Pulse Width Modulation (SPWM) technique has been used for controlling the inverter as it can be directly controlled the inverter output voltage and output frequency according to the sine functions. Sinusoidal pulse width modulation (SPWM) is widely used in power electronics to digitize the power so that a sequence of voltage pulses can be generated by the on and off of the power switches. The PWM inverter has been the main choice in power electronic for decades, because of its circuit simplicity and rugged control scheme. Sinusoidal Pulse Width Modulation switching technique is commonly used in industrial applications or solar electric vehicle applications SPWM techniques are characterized by constant amplitude pulses with different duty cycles for each period. The width of these pulses are modulated to obtain inverter output voltage control and to reduce its harmonic content. Sinusoidal pulse width modulation is the mostly used method in motor control and inverter application.

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In SPWM technique, carrier comparison approach is used for getting sequence of control signals. In carrier comparison approach there will be a reference signal and carrier signal both will be compared to get the resultant pulse as shown in Fig.2.2. Here the reference signal is sinusoidal signal and the carrier signal is a triangular signal. Output signal or reference signal frequency should be same. In a VSI output voltage depends on amplitude of the reference signal , output frequency depends on the frequency of reference signal. Always reference signal should be within the carrier signal. By changing the amplitude of reference signal pulse width is varied.

### **MODULATION INDEX**

It is defined as the ratio of peak value of the reference signal to the amplitude of carrier signal. It is also called as Amplitude modulation. The range of the Modulation Index is 0 to 1. If Modulation index is greater than 1 Output Voltage cannot be controlled. For same input voltage or same Modulation Index SPWM will give higher Output Voltage.

### **FREQUENCY MODULATION**

It is defined as the ratio of carrier signal frequency to the reference signal frequency. It is given by

$$\text{Frequency Modulation} = \frac{f_c}{f_s}$$

Number of pulses per half cycle are decided by carrier signal frequency and it is given by

$$\text{Number of pulses (N}_p\text{)} = \frac{\text{carrier signal frequency}}{2 * \text{reference signal frequency}}$$

$$N_p = \frac{\text{Frequency Modulation}}{2}$$

## 2.3 TWO LEVEL INVERTER

An inverter whose pole voltages can have two levels of voltages is called Two level Inverter. The most common type of inverter which is used to generate AC voltage from DC Voltage is Two level Inverter. A two-level Inverter creates two different voltages for the load i.e, suppose we are providing  $V$  as an input to a two level inverter then it will provide either  $+V/2$  and  $-V/2$  or  $V$  and  $0$  on output. The Circuit Diagram of three phase two level inverter is shown in Fig.2.3.

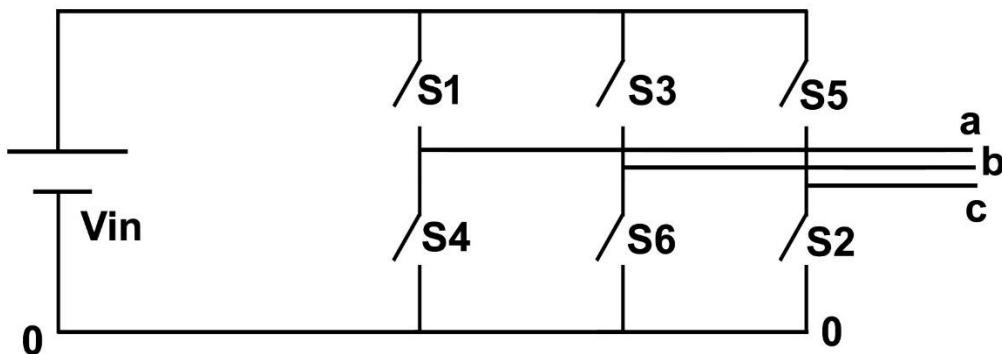


Fig.2.3. Two Level Inverter Circuit

Fig.2.3 represents the general circuit topology of the three phase two-level VSI. It comprises of six active switches, each equipped with an antiparallel freewheeling diode. Switches from the same leg should not be turned on. All the switches are in Forward bias. Switches S1,S2,S3 are positive group switches and S4,S6,S2 are negative group switches. S1-S4, S3-S6 and S5-S2 complementary pairs of switches. All positive group switches should not be turned ON at same time. Based on turning time of switches it can be operated in two modes of operation, They are 1)  $180^\circ$  mode of operation or six step mode of operation 2)  $120^\circ$  mode of operation. By operating two level inverter with above two modes of operation lower order harmonics are encountered. To overcome this disadvantage PWM technique is employed, the purpose of operating any VSI with a PWM scheme is to shift the low order harmonics near the fundamental frequency to higher frequencies to reduce the ripple in the output current, thereby reducing torque ripple and motor losses. In this topology SPWM technique was used, where sinusoidal signal was compared with triangular signal for getting resultant pulse. Here the level is two so sinusoidal signal is compared with N-1 carrier signals where N is number of levels i.e, sinusoidal signal is compared with one carrier signal. If we consider a single

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leg then the carrier comparison approach is shown in Fig.2.4, where  $V_{ref}$  is reference signal and  $V_{T1}$  is carrier signal.  $V_{ref}$  and  $V_{T1}$  are compared to get a resultant pulse which is given to switch S1.

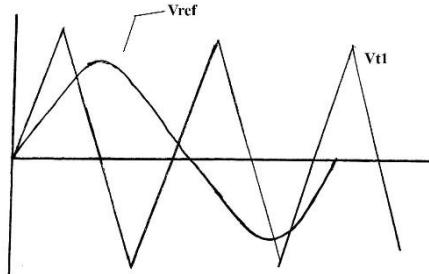


Fig.2.4. Carrier Comparison Approach

### 2.4 OPERATION OF TWO LEVEL INVERTER

The operation of two level inverter will be explained by considering single leg in the above circuit diagram shown in Fig.2.3. Two level inverter single leg circuit is shown in Fig.2.5.

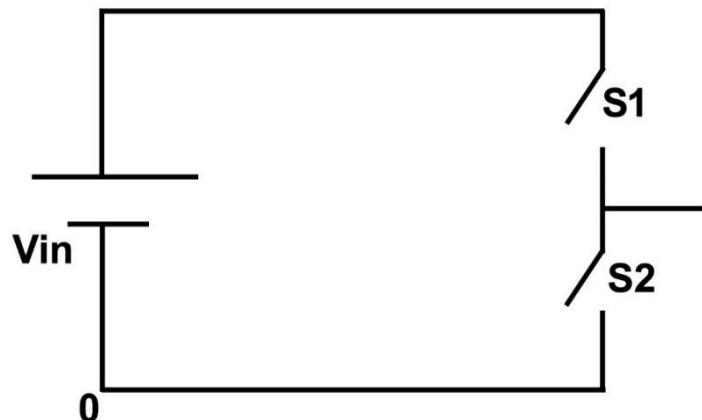


Fig.2.5. Single leg circuit of Two level Inverter

Here  $S_1-S_2$  are complementary pair of switches. If switch  $S_1$  is in ON condition then  $S_2$  will be in OFF condition vice versa. Here the input voltage is  $V_{in}$ . When  $S_1$  is turned ON the pole voltage will be  $V_{in}$  and when  $S_2$  is turned ON then the pole voltage will be 0. For remaining legs also the operation is same. Voltage between output point of legs and mid potential of the dc bus is called as pole voltage referred to the mid potential of the dc bus. Harmonic content in the output waveform of two level inverter will be high. Total Harmonic Distortion was calculated by performing Fast Fourier Transform Analysis.

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Common mode voltage ( $V_{no}$ ) is nothing but it is the voltage measured between neutral point to the reference point. If common mode voltage is high, unwanted voltages passes through the windings of the machine and damages the windings and losses also get increased. Common mode voltage is given by

$$\text{Common Mode Voltage } (V_{no}) = \frac{V_{ao} + V_{bo} + V_{co}}{3}$$

Two level inverter has the following disadvantages:

- 1) High THD in output voltage.
- 2) More switching losses on devices.
- 3) Not applicable for high voltage applications.
- 4) Higher common mode voltages.
- 5) Since  $dv/dt$  is high, the EMI from the system is high.
- 6) Higher switching frequency is used hence switching losses is high.

## 2.5 SIMULATION RESULTS

The circuit diagram of Two level Inverter fed Induction Motor Drive shown in Fig.2.6.

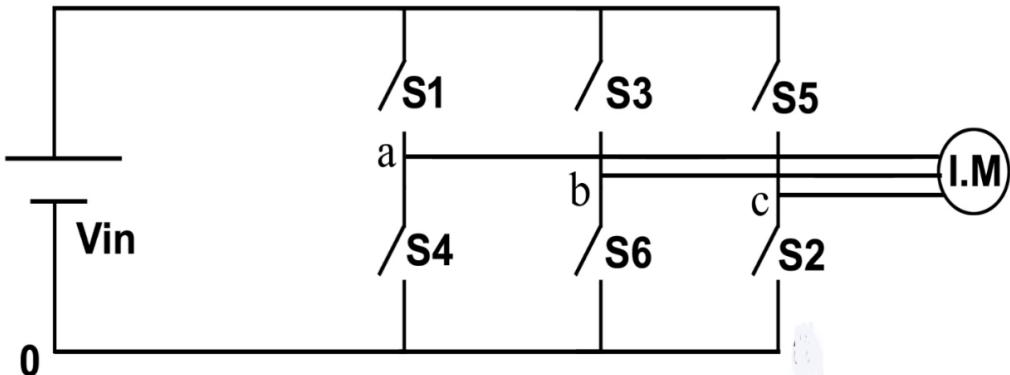


Fig.2.6. Two Level Inverter fed Induction Motor Drive

### SIMULATION PARAMETERS

Input DC Voltage ( $V_{DC}$ ) = 510V

Modulation Index = 0.9

Switching Frequency = 3000 Hz

Frequency of Sinewave ( $F_{sw}$ ) = 50 Hz

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## SIMULATION MODEL

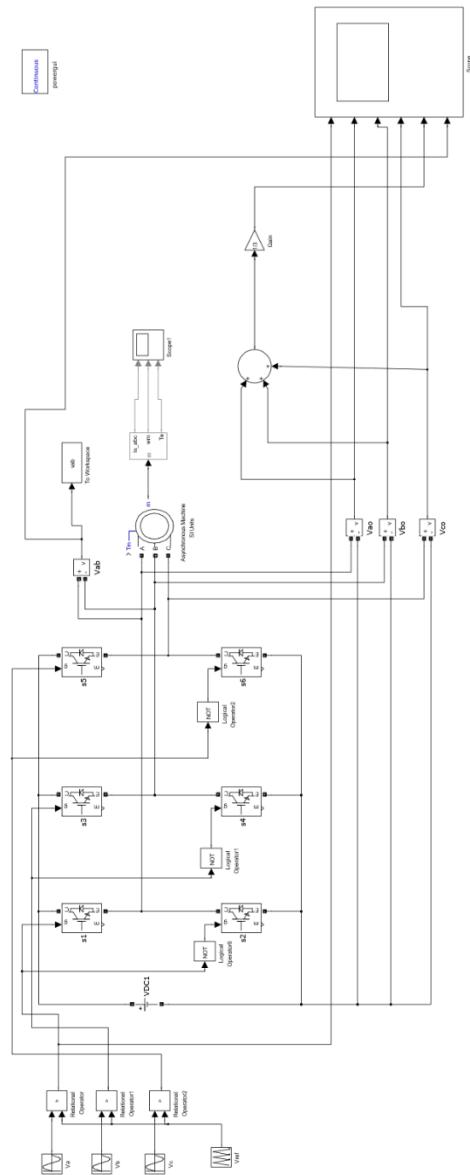
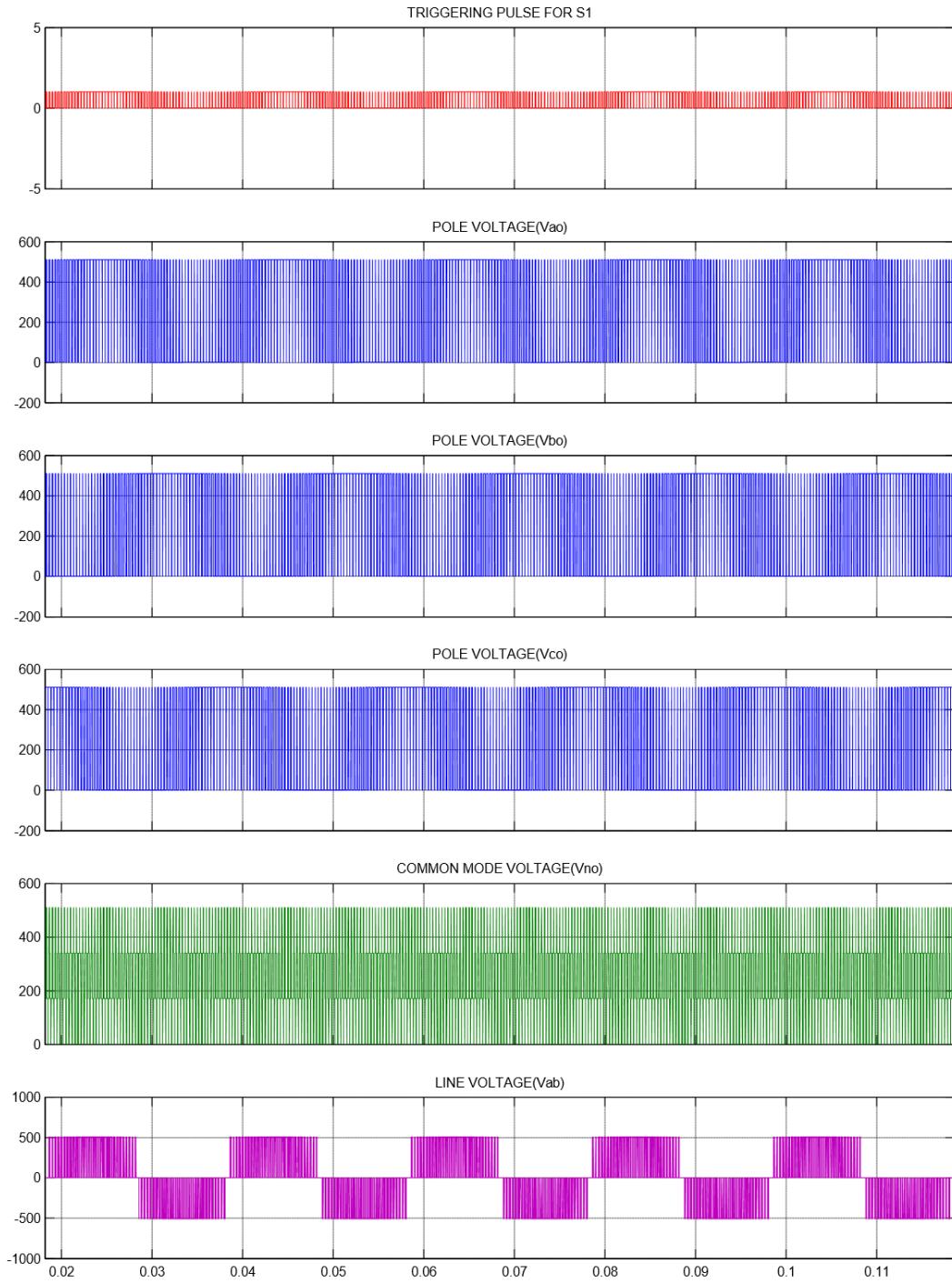


Fig.2.7. Simulation model of Two level Inverter

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For an input voltage of  $V_{DC}$ , Pole voltage comprising of levels  $V_{DC}$  and 0, Line voltage comprising of levels  $V_{DC}$ , 0 and  $-V_{DC}$  and common mode voltage comprising of levels 0,  $\frac{V_{DC}}{3}$ ,  $\frac{2V_{DC}}{3}$  and  $V_{DC}$  are obtained.



**Fig.2.8. Pole and Line Voltages of Two Level Inverter**

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Here, The machine runs at no load condition, So the Electromagnetic Torque ( $T_e$ ) is zero.

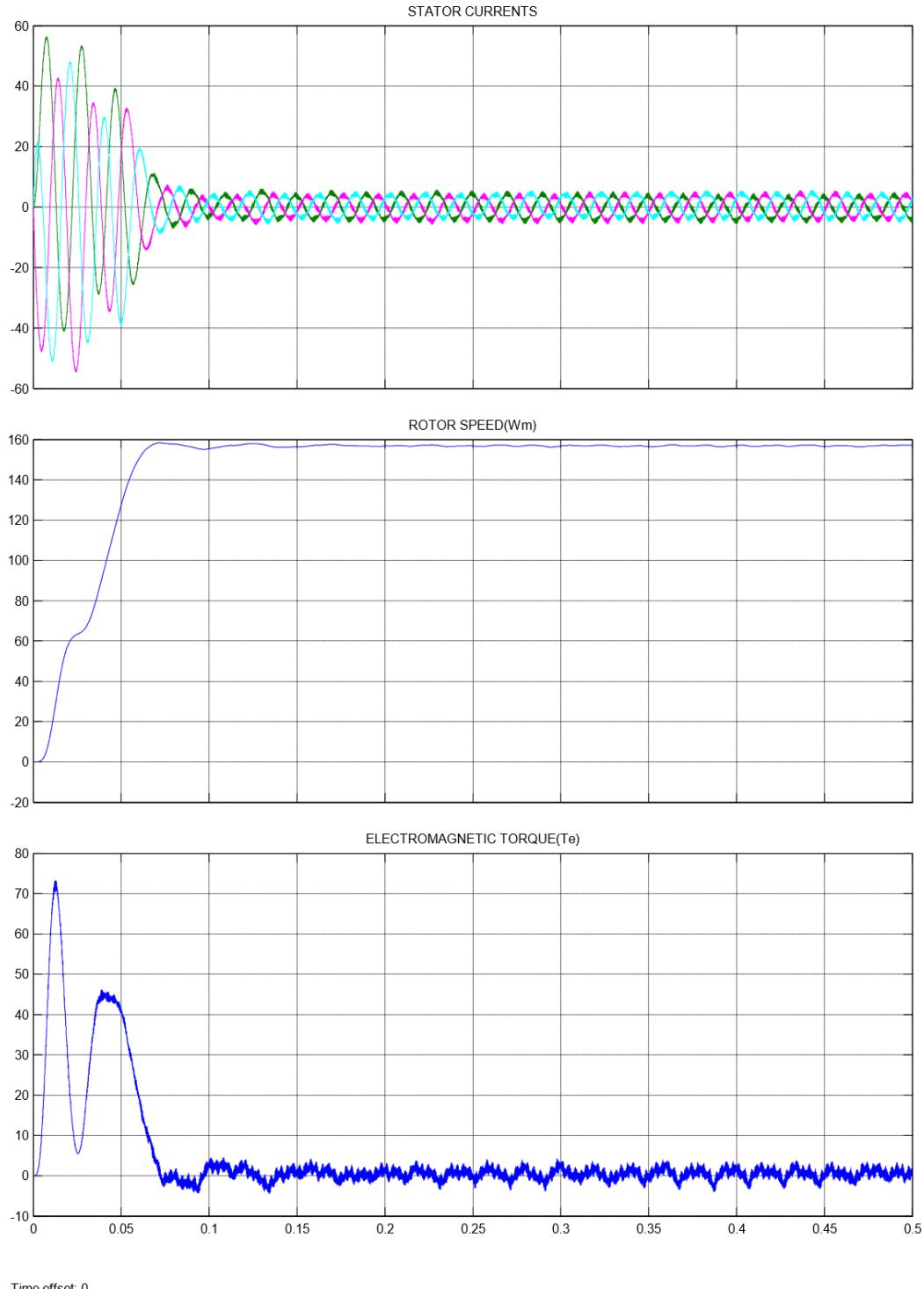


Fig.2.9. Two Level inverter fed Induction Motor Drive results

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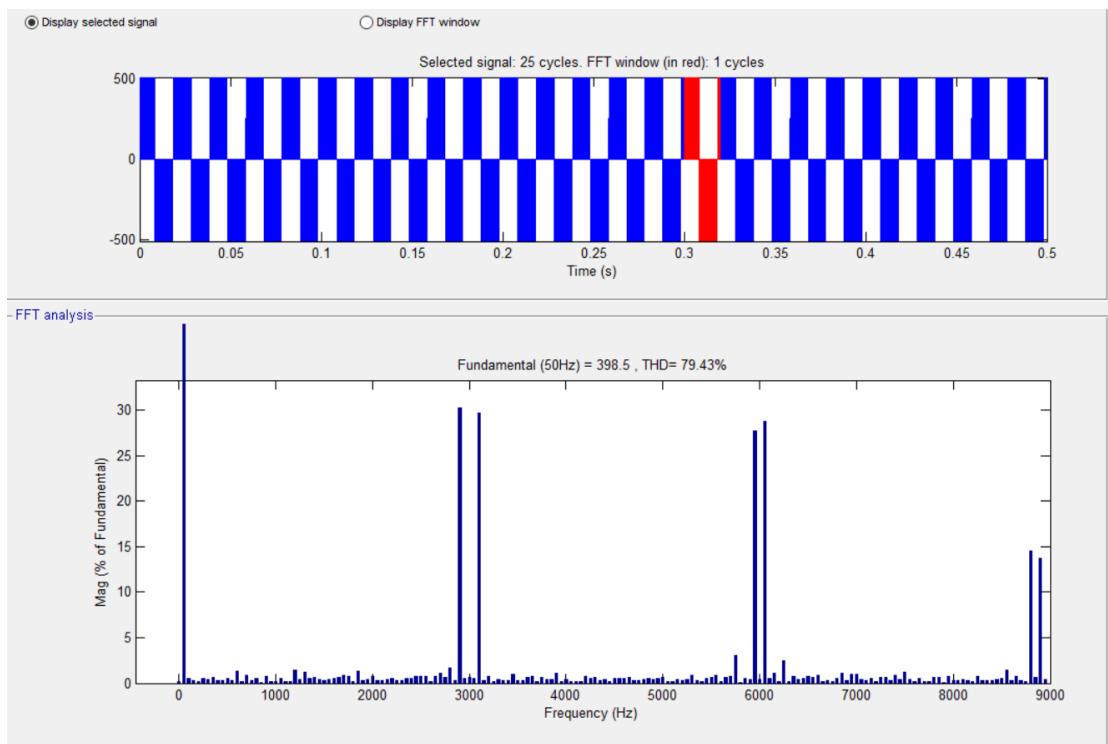


Fig.2.10. FFT Analysis of Two Level inverter

Table 2.1: Results of Two level Inverter

LEVEL	SPWM TECHNIQUE	COMMON MODE VOLTAGE (V <sub>no</sub> )	THD (%) (Line Voltage)
TWO	PD	$0, \frac{V_{DC}}{3}, \frac{2V_{DC}}{3}, V_{DC}$	79.43

## CHAPTER 3

### MULTILEVEL INVERTER

#### 3.1 INTRODUCTION

The most common type of inverter which is used to generate AC voltage from DC Voltage is two level inverter. A two-level Inverter creates two different voltages for the load i.e, suppose we are providing  $V$  as an input to a two level inverter then it will provide  $+V/2$  and  $-V/2$  or  $V$  and  $0$  on output. In order to build an AC voltage, these two newly generated voltages are usually switched. Although this method of conversion of voltage is effective but it has some limitations as it causes disturbance in the output voltage. Normally this method works but in some applications it creates problems specifically where high distortion in the output voltage is not required. To overcome the disadvantages of two level inverter Multilevel Inverter is employed.

The concept of multilevel converters has been introduced since 1975. The term multilevel began with the three-level converter. Subsequently, several multilevel converter topologies have been developed. The concept of multilevel Inverter (MLI) is kind of modification of two-level inverter. In multilevel inverters we don't deal with the two level voltages instead in order to create a smoother stepped output waveform, more than two voltage levels are combined together. Smoothness of the waveform is directly proportional to the voltage levels, as we increase the voltage level, the waveform becomes more smoother but the complexity will be increased. However, the elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected. A multilevel inverter has several advantages over a conventional two-level inverter that uses high switching frequency pulse width modulation (PWM).

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Multilevel inverters have the advantage of producing high voltage high power with improved power quality of the supply. It also eliminates the use of problematic series-parallel connections of switching devices. However, multilevel PWM inverters generate common mode voltages as in the case of conventional 2-level inverters. The problem of common mode voltage generation in multilevel inverters has been studied extensively during last decade.

There are different types in Multilevel Inverter which are shown in Fig.3.1.

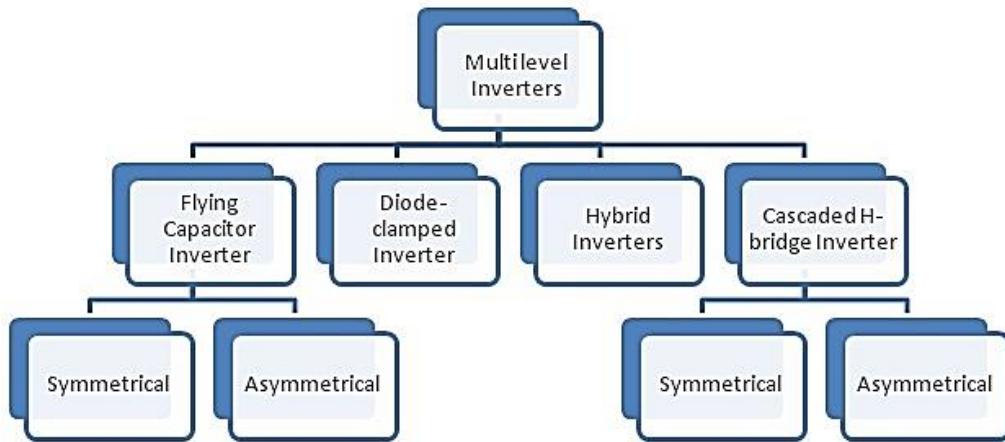


Fig.3.1. Classification of Multilevel Inverters

The Features of Multilevel Inverter are given below

- Higher Voltage operating capability
- Lower Common Mode Voltage
- Reduced Voltage Derivatives ( $\frac{dv}{dt}$ )
- Voltages with reduced harmonic contents
- Size of input and output filters are reduced
- Increased Efficiency
- Fault tolerant operation

### **3.2 THREE LEVEL INVERTER**

An inverter that produces three levels in the output pole voltage is called Three level Inverter. A Three level Inverter creates three different voltages for the load i.e, suppose if  $V$  is the input voltage to three level inverter then it will provide either  $V$ ,  $+V/2$  and  $0$  on output. The circuit diagram of three level inverter is shown in Fig.3.2.

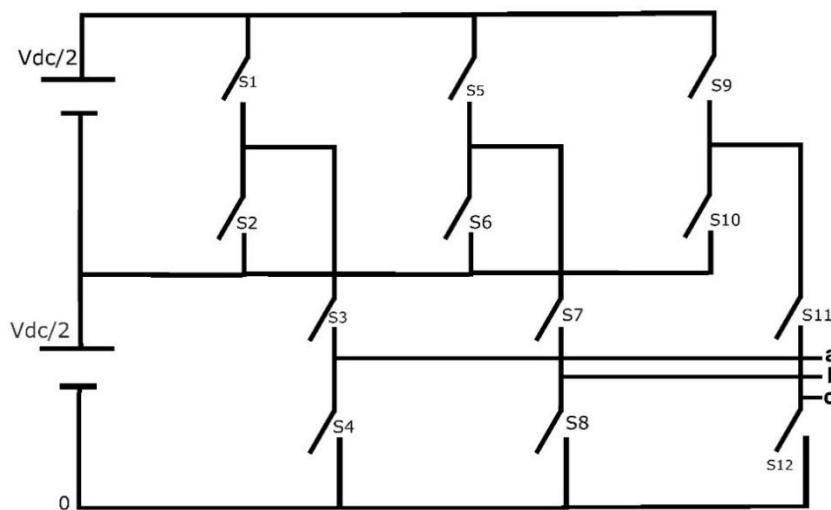


Fig.3.2. Three Level Inverter circuit

It comprises of 12 active switches, each equipped with an antiparallel freewheeling diode. Above circuit comes under Cascaded Multilevel Inverter Topology. Suppose if one leg was considered from the above circuit then  $S1-S2$  and  $S3-S4$  are the complementary pairs of switches. In this topology SPWM technique was used, where sinusoidal signal was compared with triangular signal for getting resultant pulse. Here the level is three so sinusoidal signal is compared with  $N-1$  carrier signals where  $N$  is number of levels i.e, sinusoidal signal is compared with two carrier signals. If single leg was considered then the carrier comparison approach is shown in Fig.3.3, where  $V_{ref}$  is reference signal and  $V_{T1}$  and  $V_{T2}$  are carrier signals.  $V_{ref}$  and  $V_{T1}$  are compared to get a resultant pulse which is given to the switch  $S1$ .  $V_{ref}$  and  $V_{T2}$  are compared to get a resultant pulse which is given to the switch  $S3$ . In Phase Disposition (PD) all the carrier signals are in same phase. In Phase Opposition Disposition (POD) all the carrier signals above zero are out of phase with those below the zero by  $180^\circ$ .

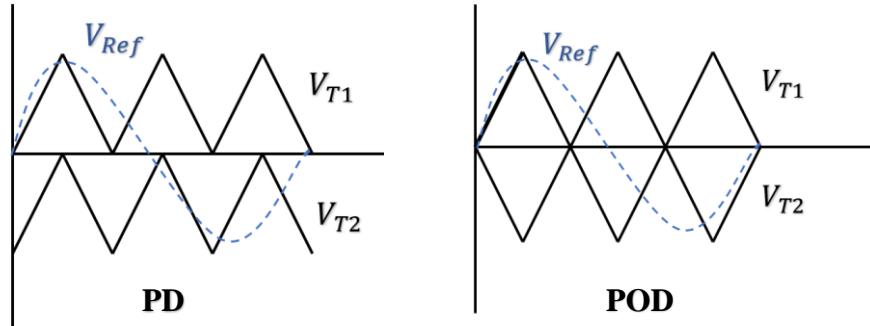


Fig.3.3. Carrier Comparison Approach

### 3.3. OPERATION OF THREE LEVEL INVERTER

Operation of three level inverter is explained by considering the single leg from the above circuit shown in Fig.3.2. The single leg circuit of the three level inverter is shown in Fig.3.4.

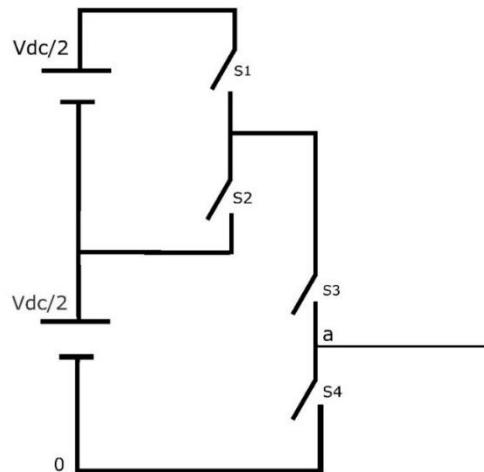


Fig.3.4. Single leg circuit of Three level Inverter

Here S1-S2 and S3-S4 are the complementary pairs of switches. Consider an instant 1 with S1 in ON/OFF, S2 is complementary pair of S1 so S2 also in ON/OFF. S3 was in ON condition so that S4 will be in OFF condition as it is complementary pair of S3. When S1 and S3 in ON condition then the pole voltage is Vdc as output. When S2 and S3 in ON condition then the pole voltage is Vdc/2 as output. In this instant S4 will be in OFF condition. Consider an instant 2 with S1 in OFF condition, S2 is complementary pair of S1 so S2 is in ON condition. S3 was in ON/OFF condition so that S4 will be in ON/OFF condition as it is complementary pair of S3. When S2 and S3 in ON condition then the pole voltage is Vdc/2 as output. When S2 and S4 in ON condition then the pole voltage is 0 as output. In this instant S1 will be in OFF condition. Here three levels of voltages occurred which are Vdc, Vdc/2, 0. For remaining legs also the operation is

## REDUCTION OF COMMON MODE VOLTAGE USING VARIOUS CARRIER BASED PWM TECHNIQUES

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same. Voltage between output point of legs and mid potential of the dc bus is called as pole voltage referred to the mid potential of the dc bus. Harmonic content in the output waveform of three level inverter will be low compared to Two level Inverter. Total Harmonic Distortion was calculated by performing Fast Fourier Transform Analysis. As the level of an Inverter increases the harmonic content and common mode voltage will be reduced.

Common mode voltage ( $V_{no}$ ) is nothing but it is the voltage measured between neutral point to the reference point. If common mode voltage is high, unwanted voltages passes through the windings of the machine and damages the windings and losses also get increased which will effect the efficiency of the machine. Common mode voltage is given by

$$\text{Common Mode Voltage } (V_{no}) = \frac{V_{ao} + V_{bo} + V_{co}}{3}$$

### 3.4 SIMULATION RESULTS

The Three Phase Three level Inverter fed induction motor drive is shown in Fig.3.5.

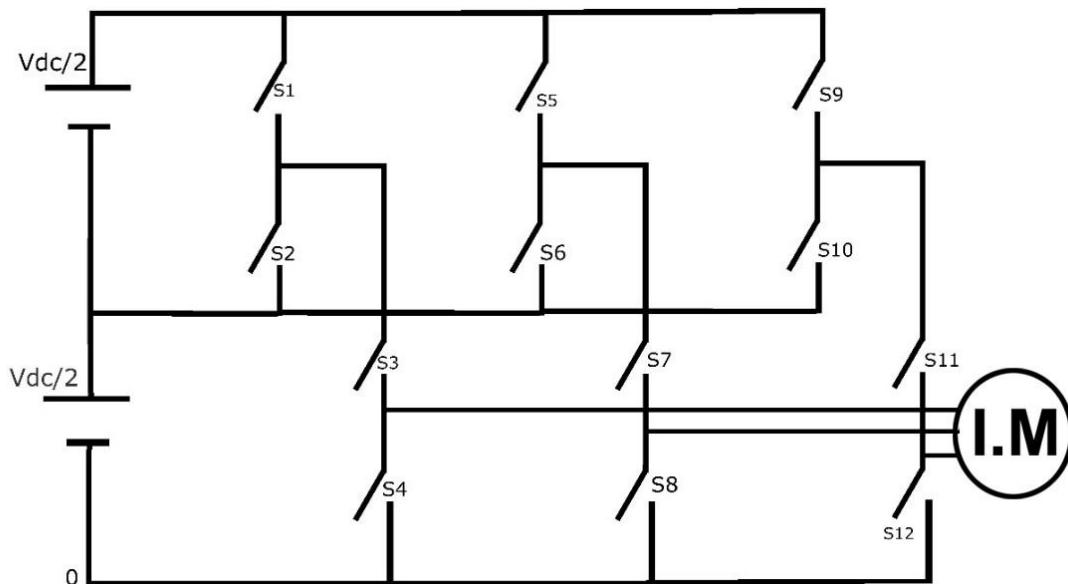


Fig.3.5. Three Level Inverter fed Induction Motor Drive

# REDUCTION OF COMMON MODE VOLTAGE USING VARIOUS CARRIER BASED PWM TECHNIQUES

## SIMULATION PARAMETERS

Input DC Voltage ( $V_{DC}$ ) = 510V

Modulation Index = 0.9

Switching Frequency = 3000 Hz

Frequency of Sinewave ( $F_{sw}$ ) = 50 Hz

## SIMULATION MODEL

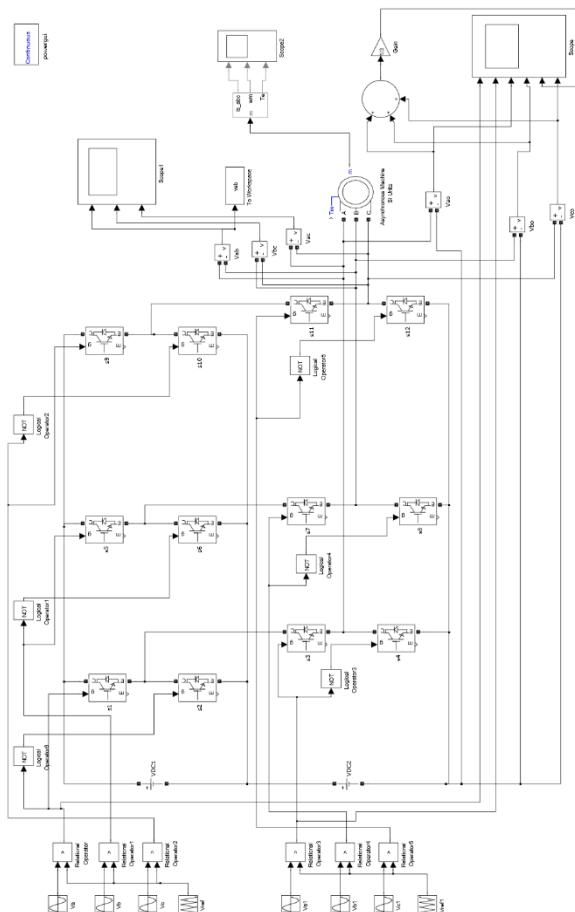


Fig.3.6. Simulation Model of Three Level Inverter

## REDUCTION OF COMMON MODE VOLTAGE USING VARIOUS CARRIER BASED PWM TECHNIQUES

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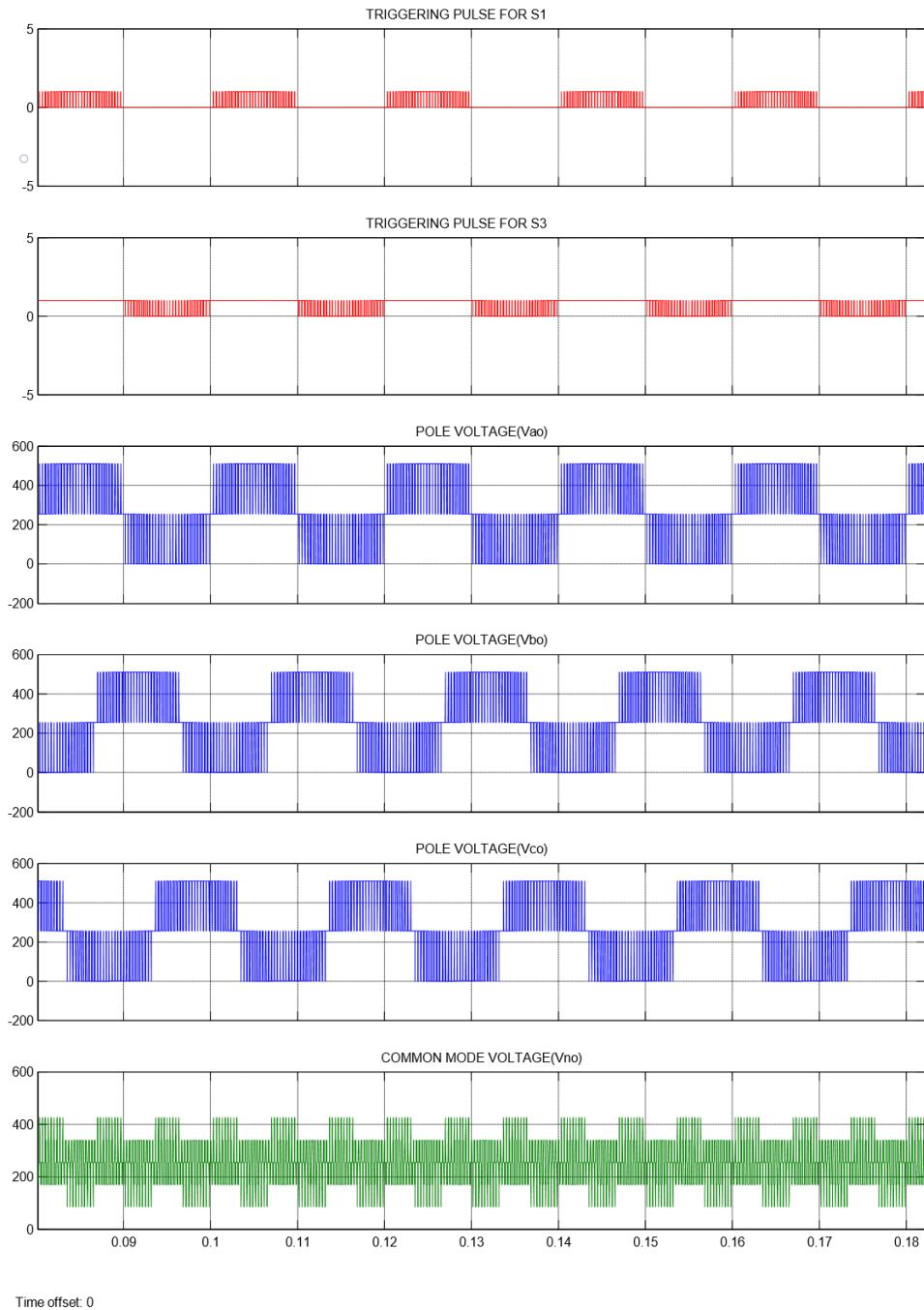


Fig.3.7. Pole voltage and Common mode voltage of Three Level Inverter  
for PDSPWM

## REDUCTION OF COMMON MODE VOLTAGE USING VARIOUS CARRIER BASED PWM TECHNIQUES

For an input voltage of  $V_{DC}$ , Pole voltage comprising of levels  $V_{DC}$ ,  $\frac{V_{DC}}{2}$  and 0, Line voltage comprising of levels  $V_{DC}$ ,  $\frac{V_{DC}}{2}$ , 0,  $-\frac{V_{DC}}{2}$ ,  $-V_{DC}$  and common mode voltage comprising of levels  $\frac{V_{DC}}{6}$ ,  $\frac{V_{DC}}{3}$ ,  $\frac{2V_{DC}}{3}$  and  $\frac{5V_{DC}}{6}$  are obtained.

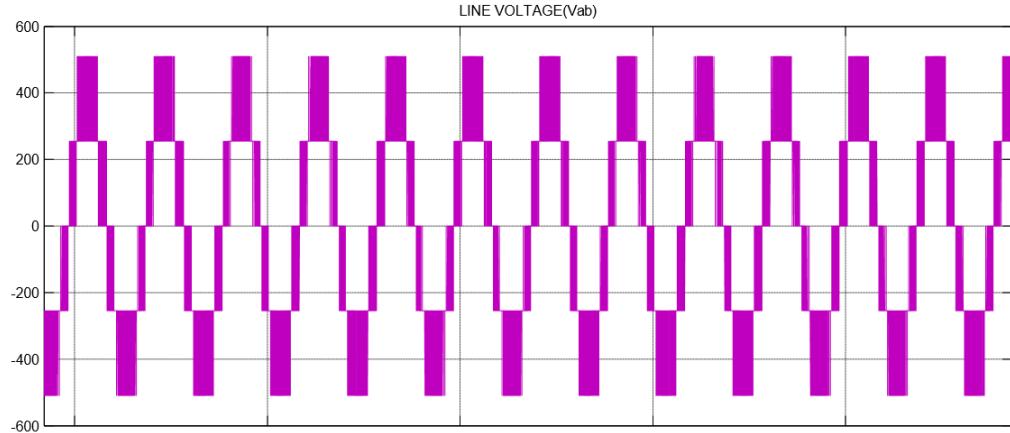


Fig.3.8. Line Voltage of Three level inverter for PDSPWM

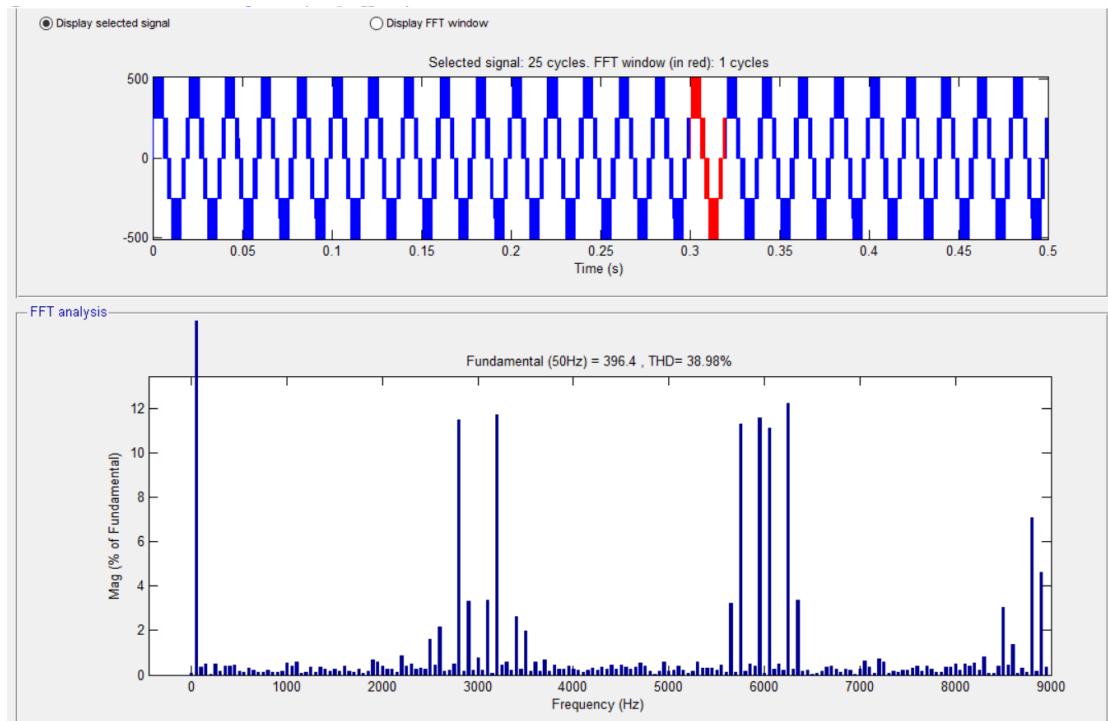


Fig.3.9. FFT Analysis of Three Level Inverter for PDSPWM

## REDUCTION OF COMMON MODE VOLTAGE USING VARIOUS CARRIER BASED PWM TECHNIQUES

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Here, The machine runs at no load condition, So the Electromagnetic Torque ( $T_e$ ) is zero.

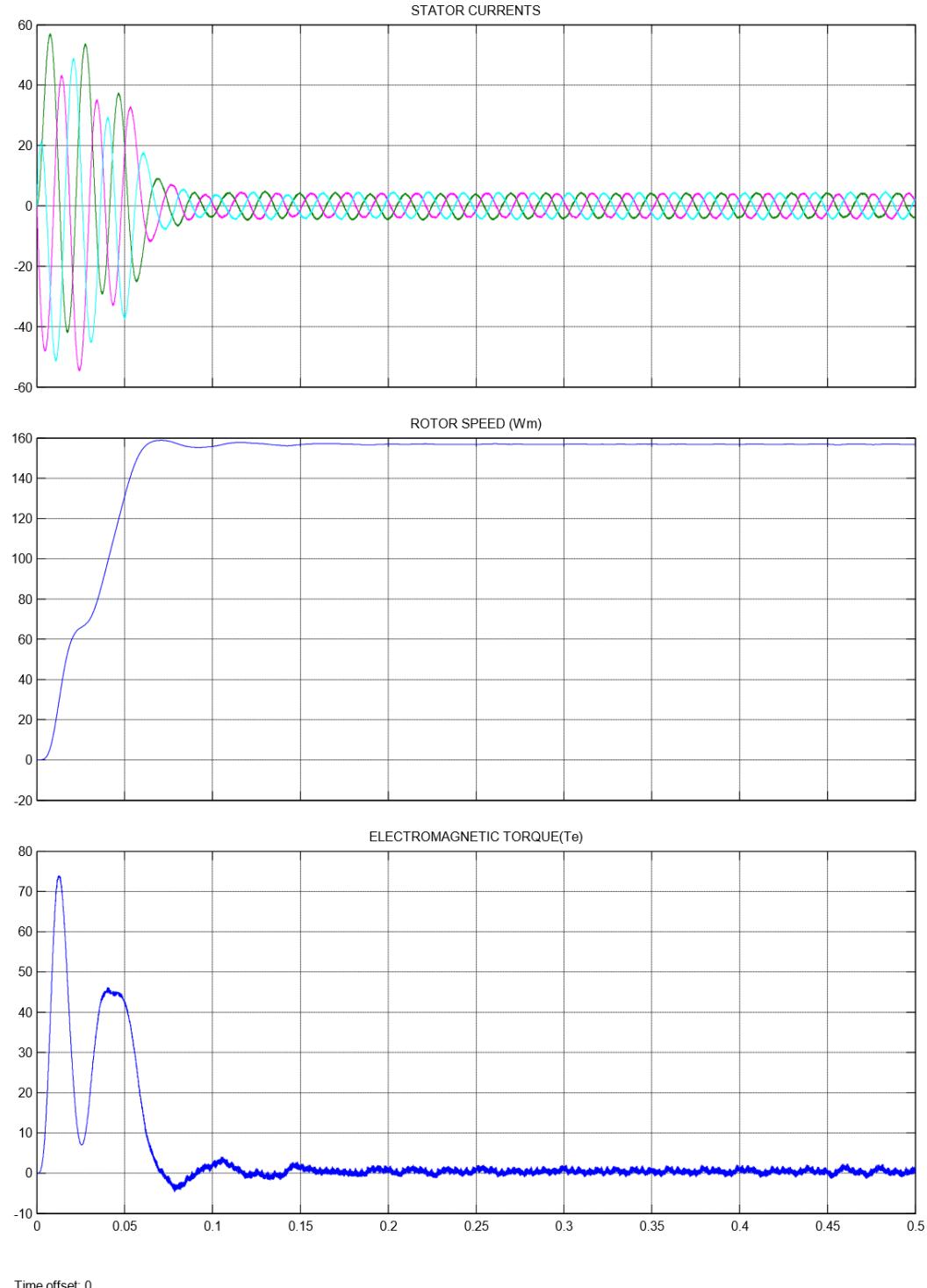
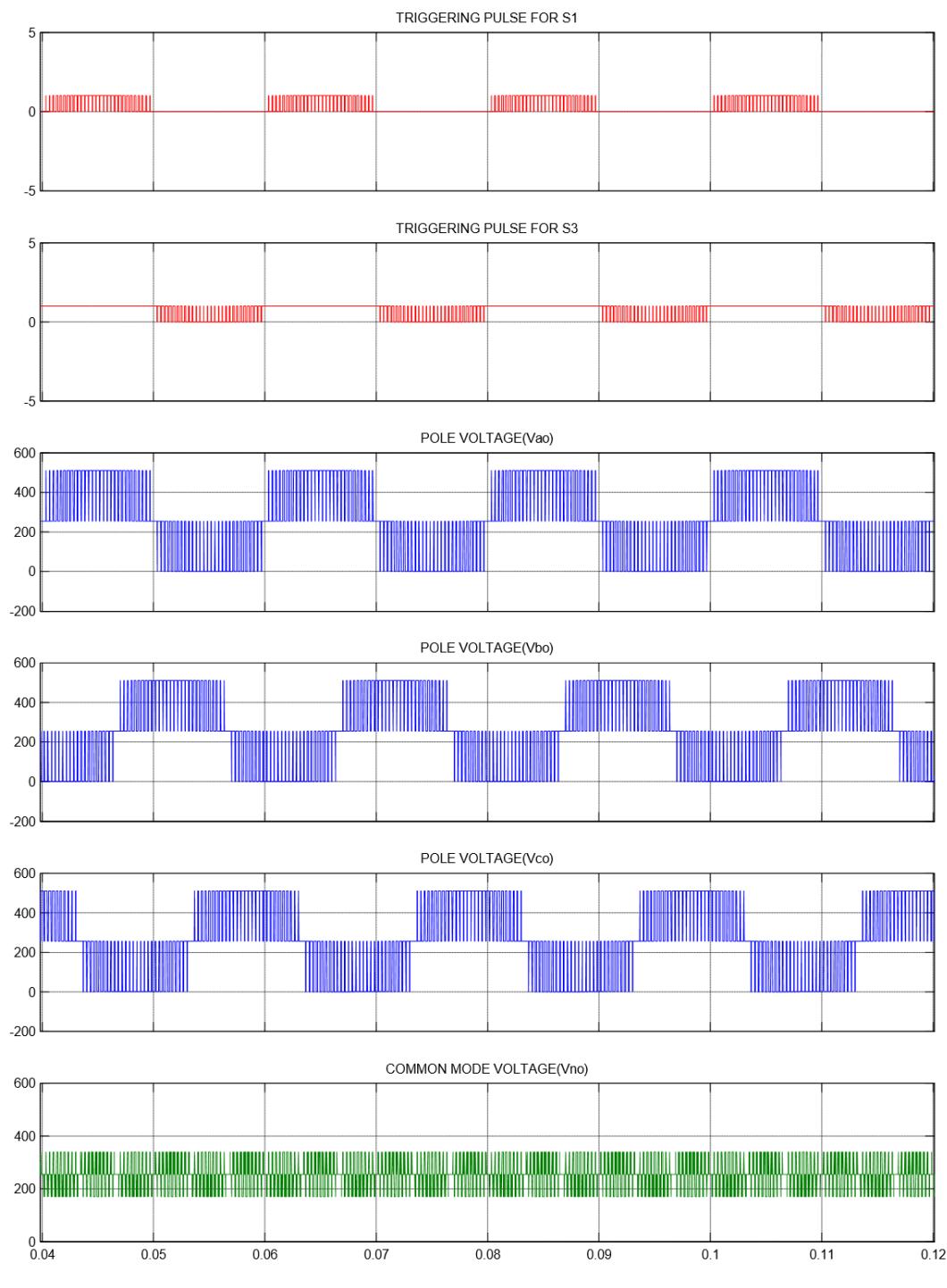


Fig.3.10. Three level Inverter fed Induction Motor Drive results for PDSPWM

## REDUCTION OF COMMON MODE VOLTAGE USING VARIOUS CARRIER BASED PWM TECHNIQUES

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Time offset: 0

Fig.3.11. Pole voltage and Common mode voltage of Three Level Inverter  
for PODSPWM

## REDUCTION OF COMMON MODE VOLTAGE USING VARIOUS CARRIER BASED PWM TECHNIQUES

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For an input voltage of  $V_{DC}$ , Pole voltage comprising of levels  $V_{DC}$ ,  $\frac{V_{DC}}{2}$  and 0, Line voltage comprising of levels  $V_{DC}$ ,  $\frac{V_{DC}}{2}$ , 0,  $-\frac{V_{DC}}{2}$ ,  $-V_{DC}$  and common mode voltage comprising of levels  $\frac{V_{DC}}{3}$ ,  $\frac{2V_{DC}}{3}$  are obtained.

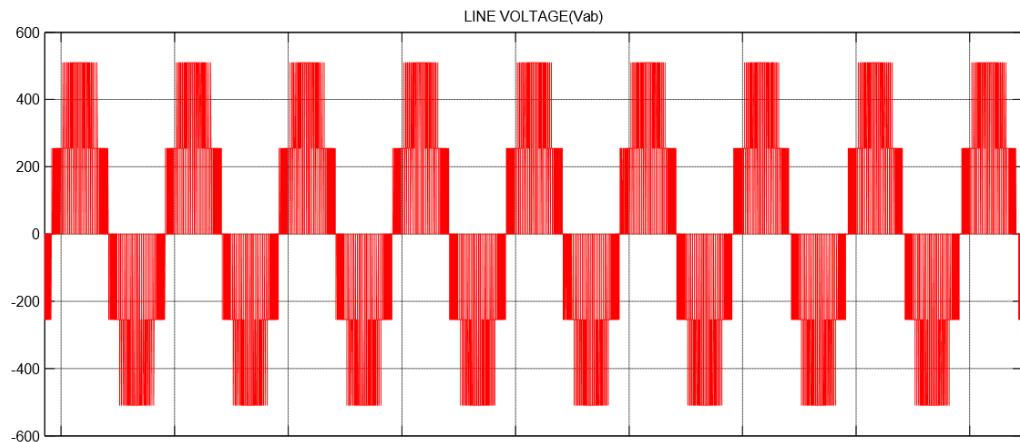


Fig.3.12. Line Voltage of Three level inverter for PODSPWM

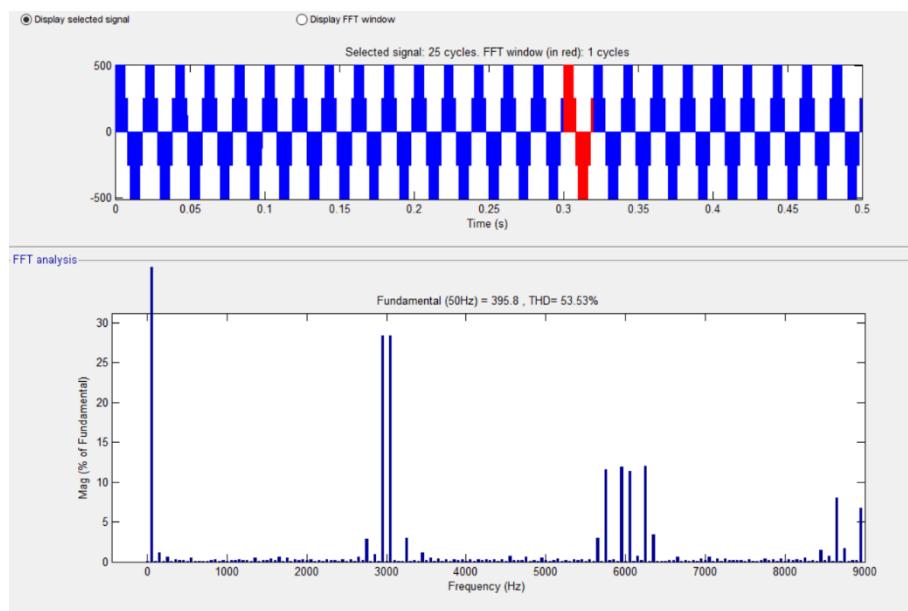


Fig.3.13. FFT Analysis of Three Level Inverter for PODSPWM

## REDUCTION OF COMMON MODE VOLTAGE USING VARIOUS CARRIER BASED PWM TECHNIQUES

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Here, The machine runs at no load condition, So the Electromagnetic Torque ( $T_e$ ) is zero.

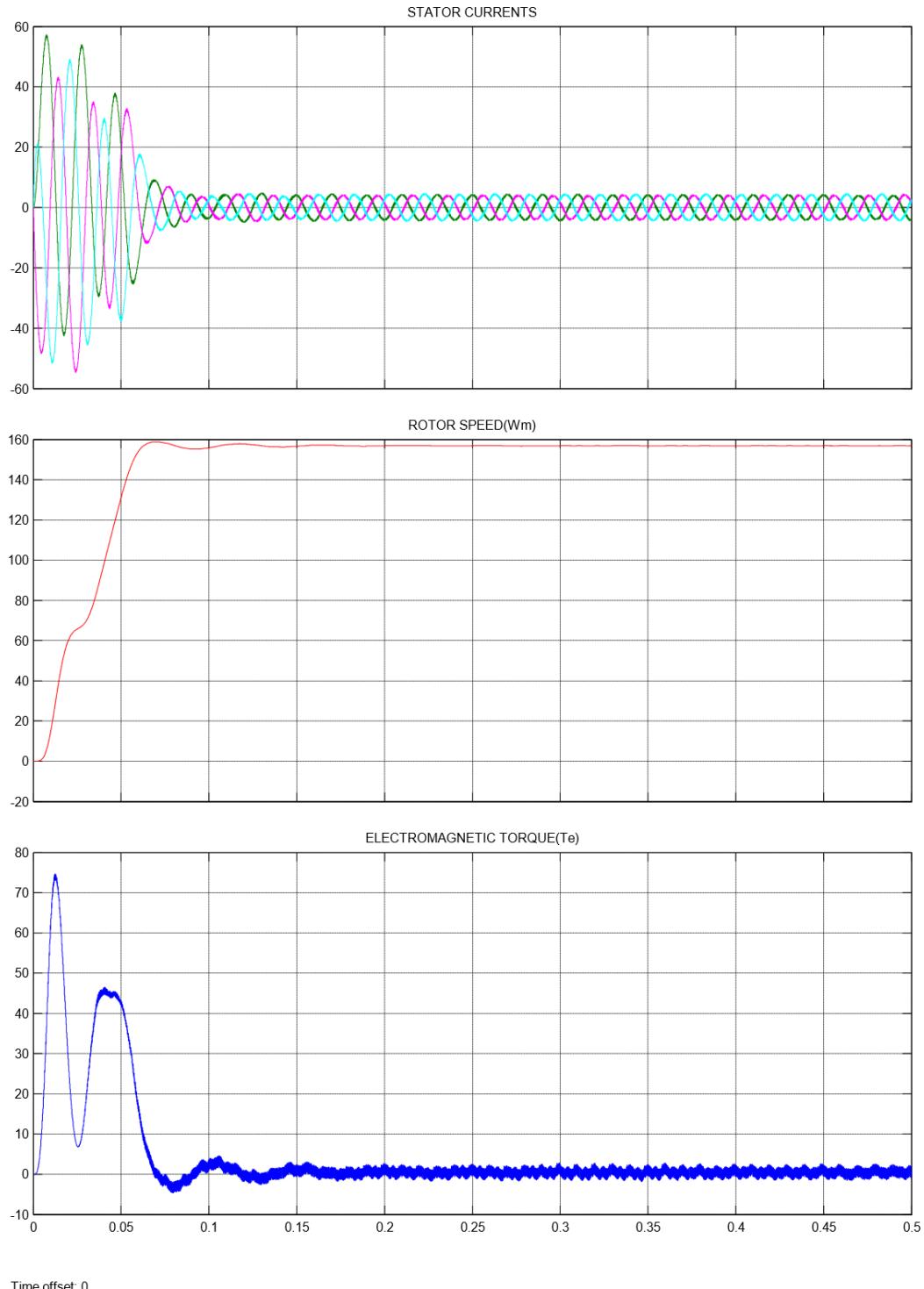


Fig.3.14. Three level Inverter fed Induction Motor Drive results for PODSPWM

**REDUCTION OF COMMON MODE VOLTAGE USING VARIOUS  
CARRIER BASED PWM TECHNIQUES**

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Table 3.1. Results of Three Level Inverter

<b>LEVEL</b>	<b>SPWM TECHNIQUE</b>	<b>COMMON MODE VOLTAGE (<math>V_{no}</math>)</b>	<b>THD (%) (Line Voltage)</b>
<b>THREE</b>	PD	$\frac{V_{DC}}{6}, \frac{V_{DC}}{3}, \frac{2V_{DC}}{3}, \frac{5V_{DC}}{6}$	38.98
	POD	$\frac{V_{DC}}{3}, \frac{2V_{DC}}{3}$	53.53

## CHAPTER 4

# FOUR AND HIGHER LEVEL INVERTER TOPOLOGIES

### 4.1 FOUR LEVEL INVERTER

An inverter that produces Four levels in the output pole voltage is called Four level Inverter. A Four level Inverter creates four different voltages for the load i.e, suppose we are providing  $V$  as an input to a four level inverter then it will provide either  $V$ ,  $2V/3$ ,  $V/3$  and 0 on output. A Four level Inverter creates four different voltages for the load. The circuit diagram of four level inverter is shown in Fig.4.1.

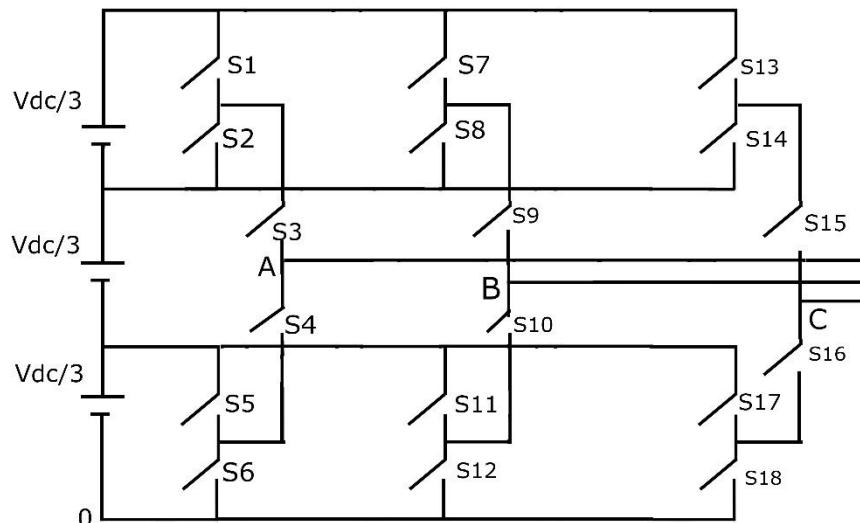


Fig.4.1. Four Level Inverter circuit

It comprises of 18 active switches, each equipped with an antiparallel freewheeling diode. Above circuit comes under Cascaded Multilevel Inverter Topology. Suppose if one leg was considered from the above circuit then S1-S2, S3-S4 and S5-S6 are the complementary pairs of switches. In this topology SPWM technique was used, where sinusoidal signal was compared with triangular signal for getting resultant pulse. Here the level is four so sinusoidal signal is compared with  $N-1$  carrier signals where  $N$  is number of levels i.e, sinusoidal signal is compared with three carrier signals. If single leg was considered then the carrier comparison approach is shown in Fig.4.2., where

## REDUCTION OF COMMON MODE VOLTAGE USING VARIOUS CARRIER BASED PWM TECHNIQUES

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$V_{ref}$  is reference signal and  $V_{T1}$ ,  $V_{T2}$  and  $V_{T3}$  are carrier signals.  $V_{ref}$  and  $V_{T1}$  are compared to get a resultant pulse which is given to the switch S1.  $V_{ref}$  and  $V_{T2}$  are compared to get a resultant pulse which is given to the switch S3.  $V_{ref}$  and  $V_{T3}$  are compared to get a resultant pulse which is given to the switch S5.

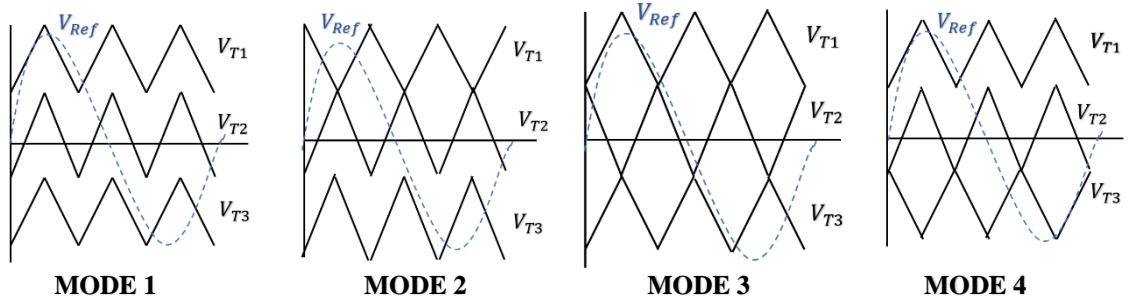


Fig.4.2. Carrier Comparison Approach

In mode 1 all the carrier signals are in same phase. In mode 2,  $V_{T1}$  is in out of phase with other two carrier signals by  $180^\circ$ . In mode 3,  $V_{T2}$  is in out of phase with other two carrier signals by  $180^\circ$ . In mode 4,  $V_{T3}$  is in out of phase with other two carrier signals by  $180^\circ$ .

### 4.2 OPERATION OF FOUR LEVEL INVERTER

Operation of four level inverter is explained by considering the single leg from the above circuit shown in Fig.4.1. The single leg circuit of the four level inverter is shown in Fig.4.3.

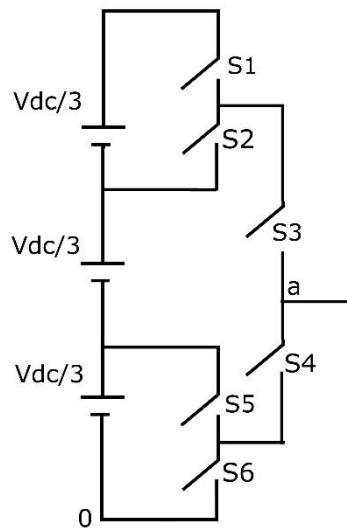


Fig.4.3. Single leg circuit of Four level Inverter

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## REDUCTION OF COMMON MODE VOLTAGE USING VARIOUS CARRIER BASED PWM TECHNIQUES

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Here S1-S2, S3-S4 and S5-S6 are the complementary pairs of switches. Consider S1 is in ON condition so that S2 will be in OFF condition if S3 is in ON condition in this case the pole voltage is Vdc as output. Consider S2 is in ON condition so that S1 will be in OFF condition if S3 is in ON condition in this case the pole voltage is 2Vdc/3 as output. Consider S5 is in ON condition so that S6 will be in OFF condition if S4 is in ON condition in this case the pole voltage is Vdc/3 as output. Consider S6 is in ON condition so that S5 will be in OFF condition if S4 is in ON condition in this case the pole voltage is 0 as output. Here four levels of voltages occurred which are Vdc, 2Vdc/3, Vdc/3 and 0. For remaining legs also the operation is same. Voltage between output point of legs and mid potential of the dc bus is called as pole voltage referred to the mid potential of the dc bus. Harmonic content in the output waveform of Four level inverter will be less compared to Three level Inverter. Total Harmonic Distortion was calculated by performing Fast Fourier Transform Analysis. As the level of an Inverter increases the harmonic content and common mode voltage will be reduced.

Common mode voltage ( $V_{no}$ ) is nothing but it is the voltage measured between neutral point to the reference point. If common mode voltage is high, unwanted voltages passes through the windings of the machine and damages the windings and losses also get increased which will effect the efficiency of the machine. Common mode voltage is given by

$$\text{Common Mode Voltage } (V_{no}) = \frac{V_{ao} + V_{bo} + V_{co}}{3}$$

### 4.3 SIMULATION RESULTS

The Three Phase Four Level Inverter fed induction motor drive is shown in Fig.4.4.

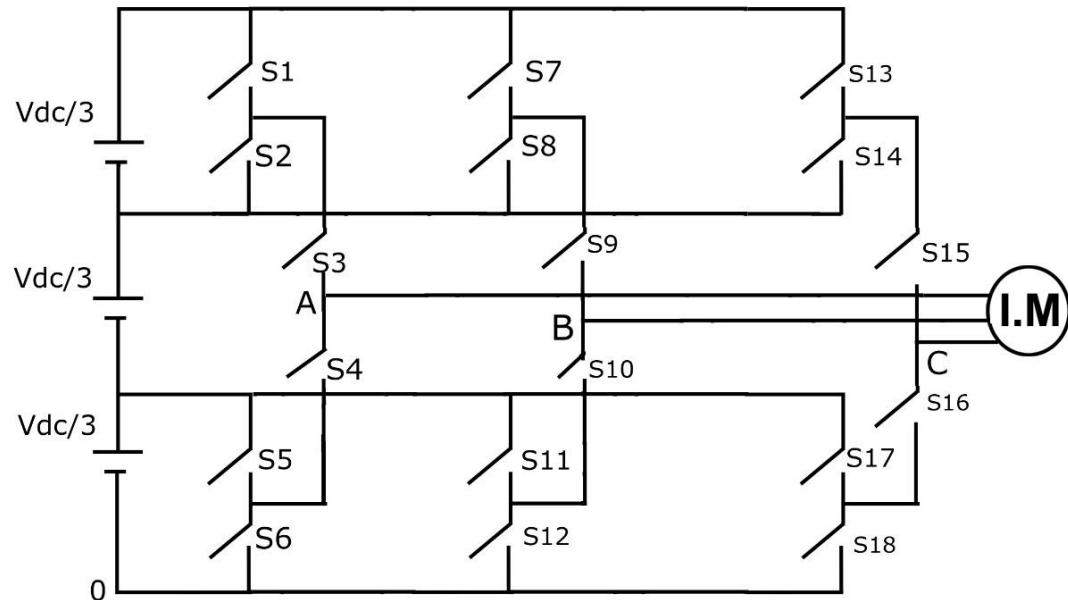


Fig.4.4. Four Level Inverter fed Induction Motor Drive

### SIMULATION PARAMETERS

Input DC Voltage ( $V_{DC}$ ) = 510V

Modulation Index = 0.9

Switching Frequency = 3000 Hz

Frequency of Sinewave ( $F_{sw}$ ) = 50 Hz

# REDUCTION OF COMMON MODE VOLTAGE USING VARIOUS CARRIER BASED PWM TECHNIQUES

## SIMULATION MODEL

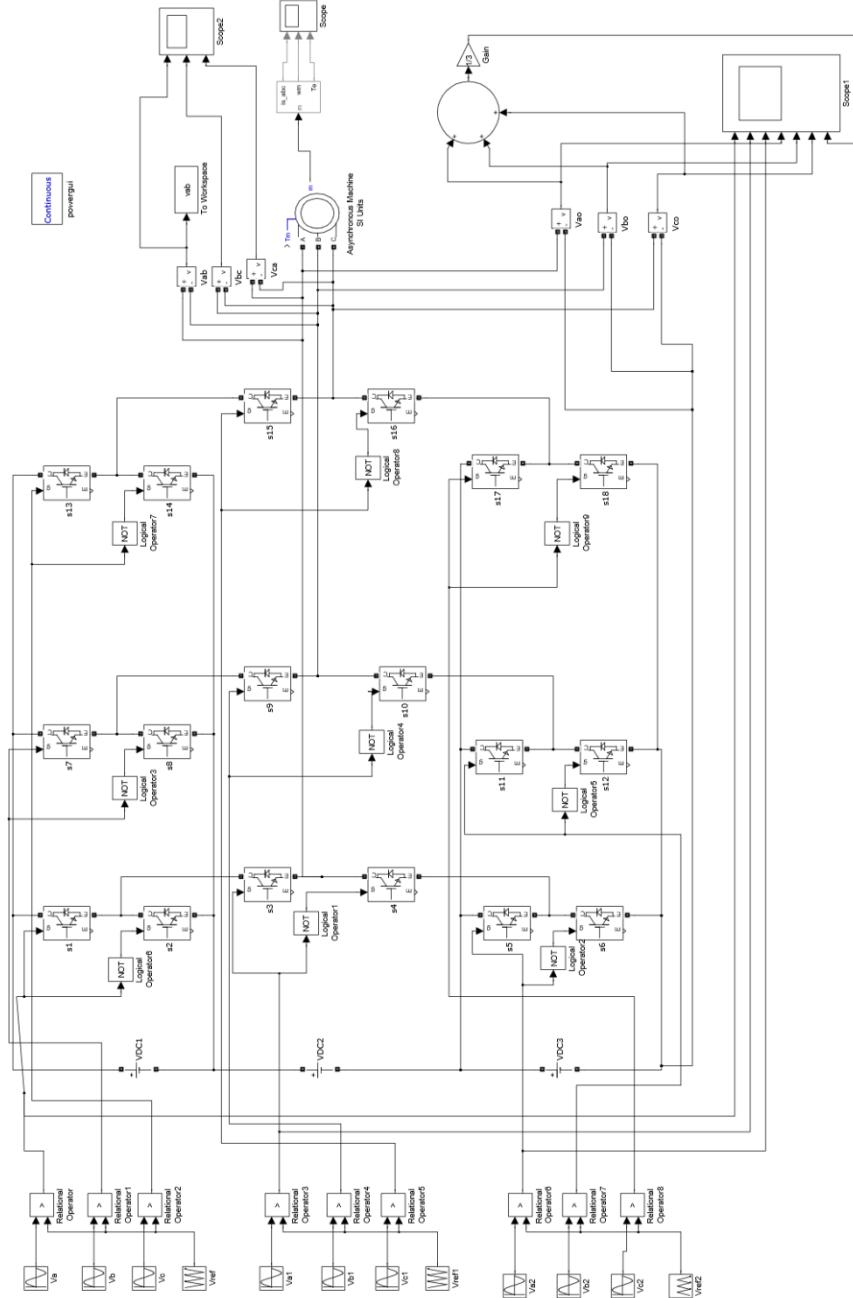


Fig.4.5. Simulation Model of Four Level Inverter

## REDUCTION OF COMMON MODE VOLTAGE USING VARIOUS CARRIER BASED PWM TECHNIQUES

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For an input voltage of  $V_{DC}$ , Pole voltage comprising of levels  $V_{DC}$ ,  $\frac{2V_{DC}}{3}$ ,  $\frac{V_{DC}}{3}$ , 0, Line voltage comprising of levels  $V_{DC}$ ,  $\frac{2V_{DC}}{3}$ ,  $\frac{V_{DC}}{3}$ , 0,  $\frac{-V_{DC}}{3}$ ,  $\frac{-2V_{DC}}{3}$ ,  $-V_{DC}$  and common mode voltage comprising of levels  $\frac{23V_{DC}}{102}$ ,  $\frac{V_{DC}}{3}$ ,  $\frac{15V_{DC}}{34}$ ,  $\frac{28V_{DC}}{51}$ ,  $\frac{2V_{DC}}{3}$  and  $\frac{40V_{DC}}{51}$  are obtained.

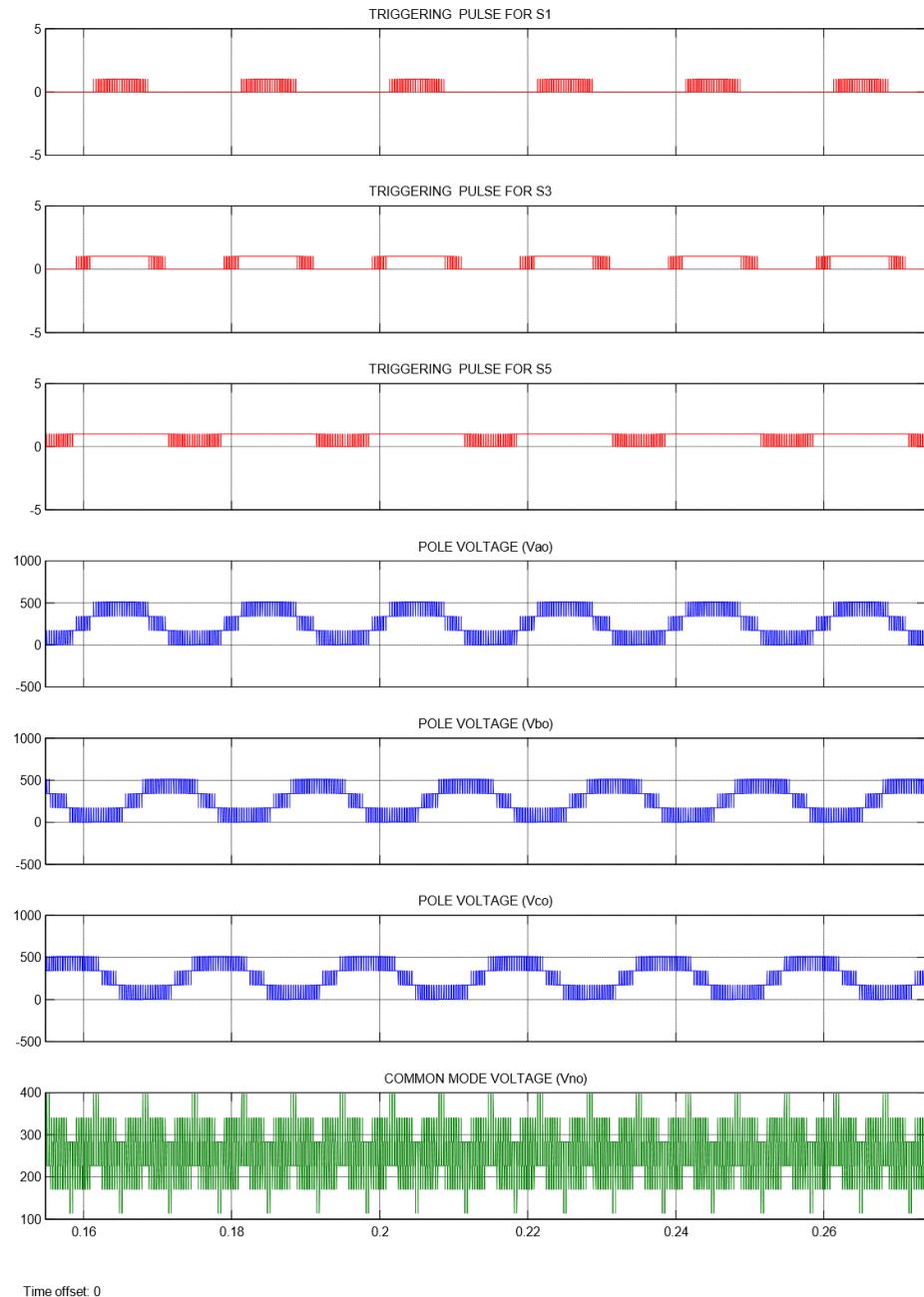


Fig.4.6. Pole voltage and common mode voltage of Four level Inverter for Mode 1

## REDUCTION OF COMMON MODE VOLTAGE USING VARIOUS CARRIER BASED PWM TECHNIQUES

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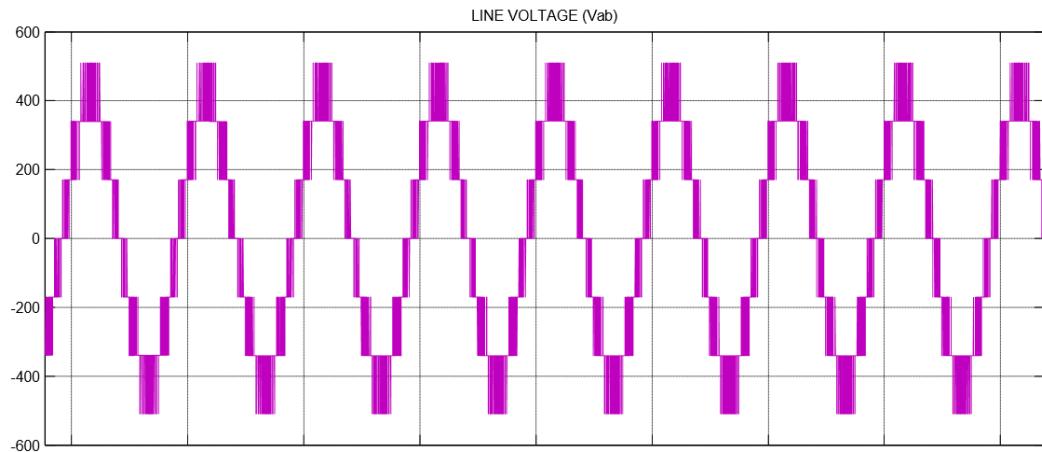


Fig.4.7. Line voltage of Four Level Inverter for Mode 1

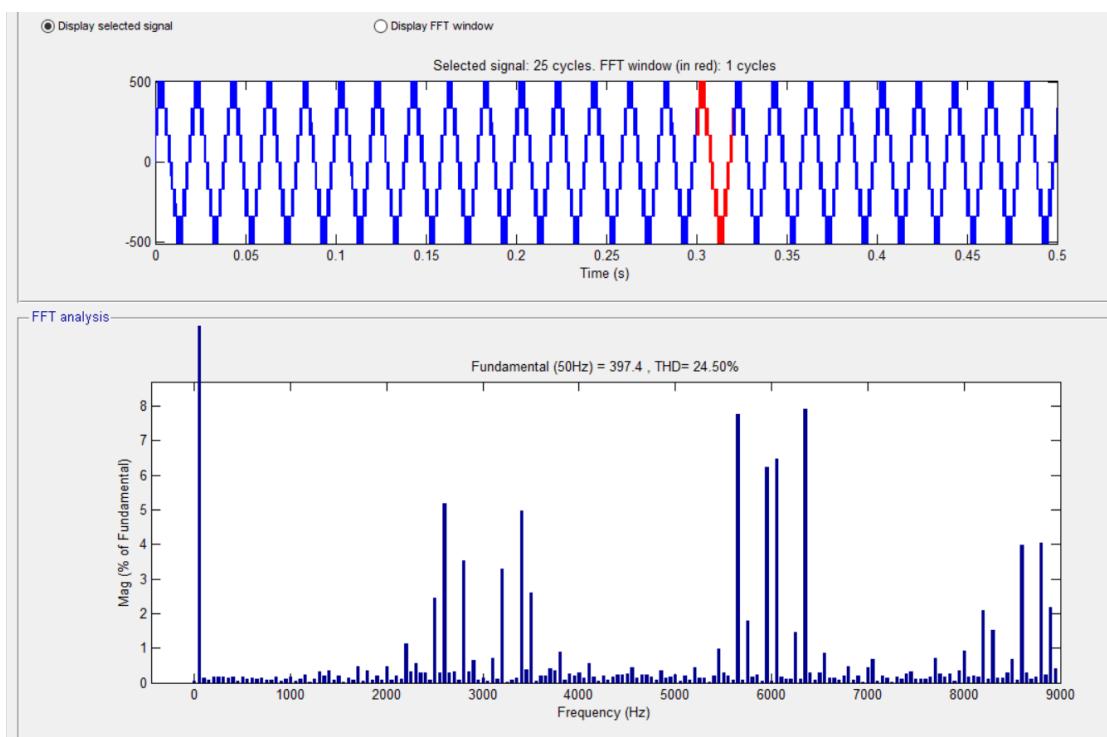


Fig.4.8. FFT Analysis of Four Level inverter for Mode 1

## REDUCTION OF COMMON MODE VOLTAGE USING VARIOUS CARRIER BASED PWM TECHNIQUES

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Here, The machine runs at no load condition, So the Electromagnetic Torque ( $T_e$ ) is zero.

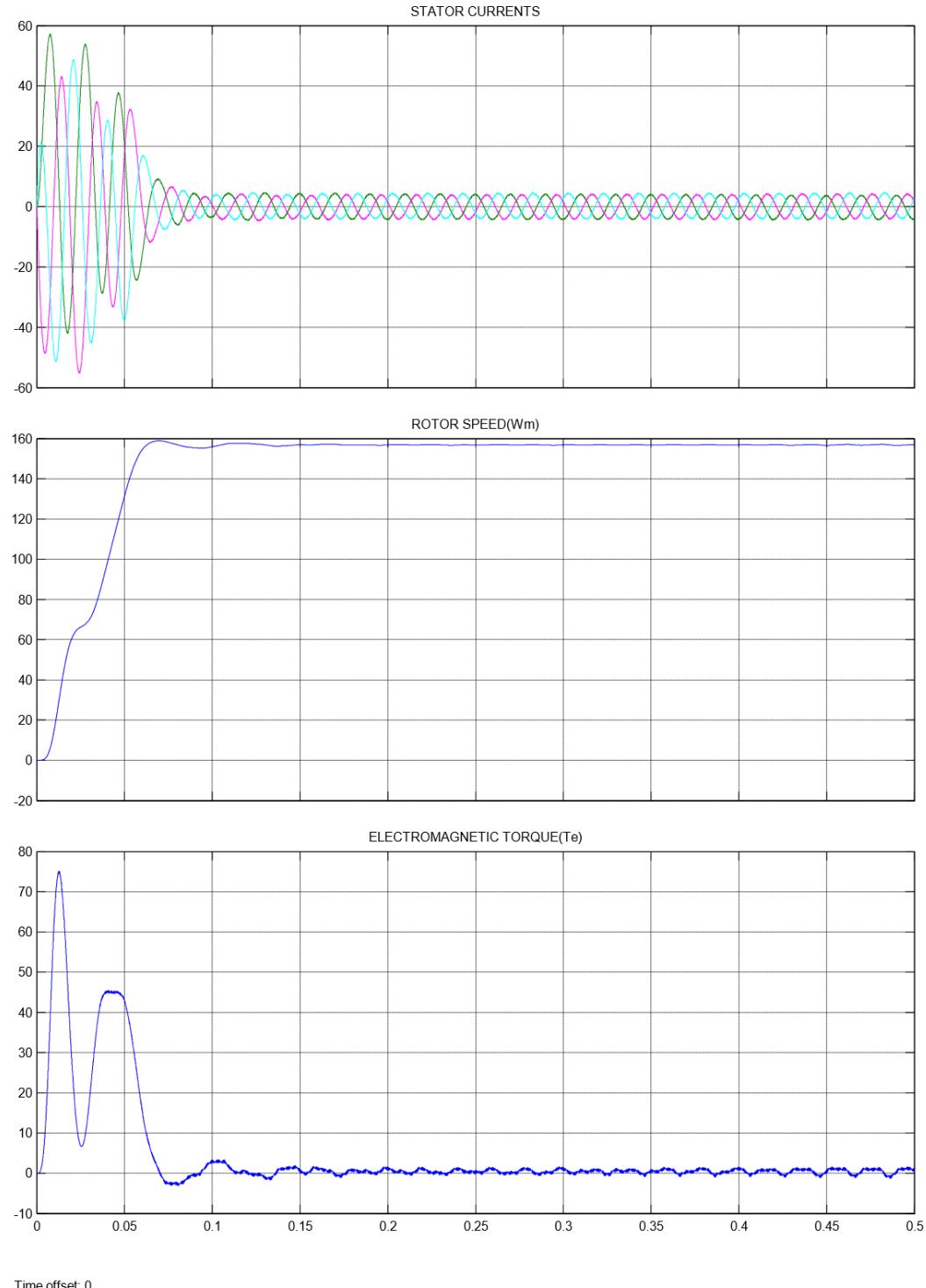
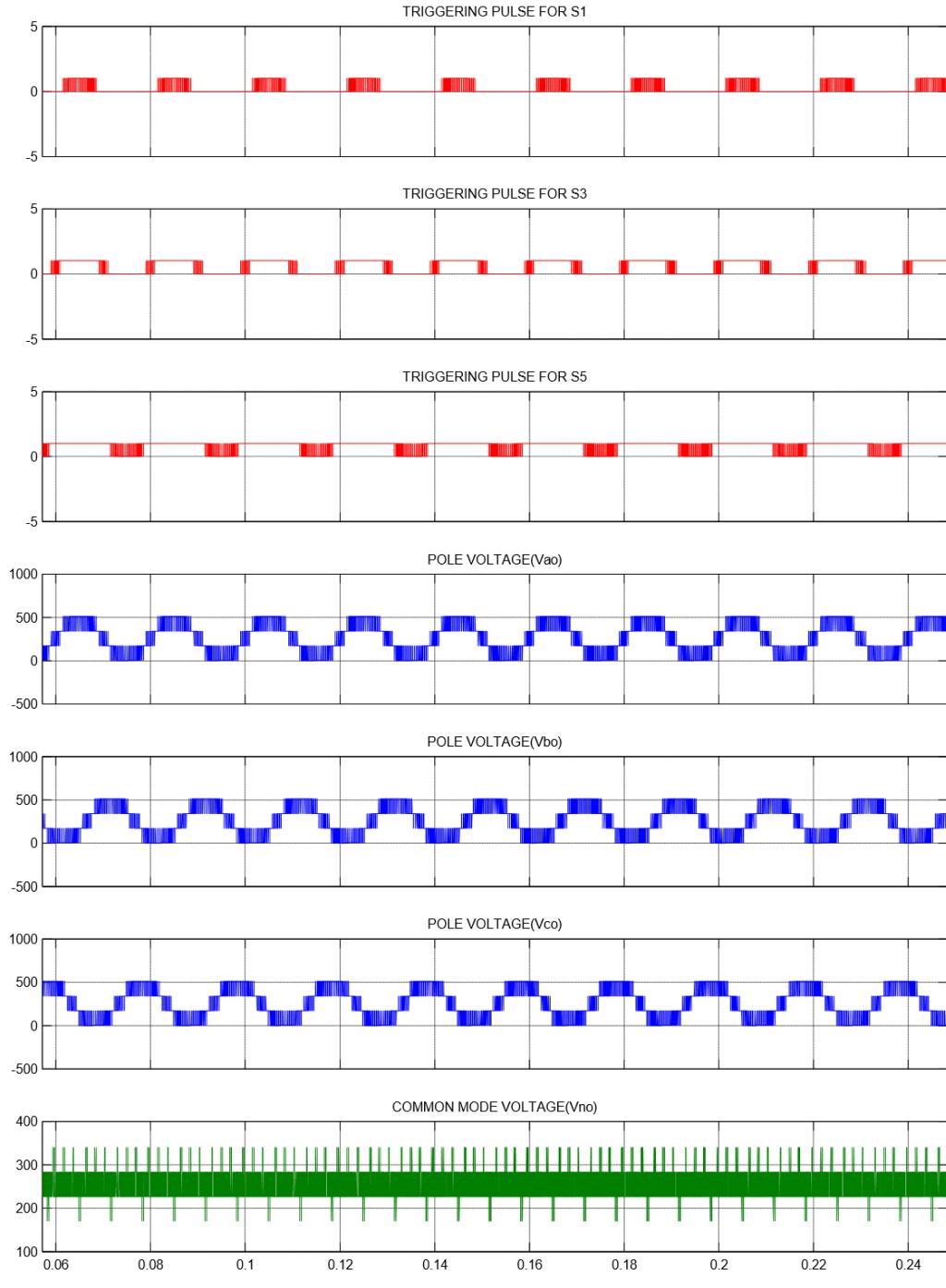


Fig.4.9. Four level Inverter fed Induction Motor Drive results for Mode 1

## REDUCTION OF COMMON MODE VOLTAGE USING VARIOUS CARRIER BASED PWM TECHNIQUES

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Time offset: 0

Fig.4.10. Pole voltage and common mode voltage of Four level Inverter for Mode 2

For an input voltage of  $V_{DC}$ , Common mode voltage comprising of levels  $\frac{V_{DC}}{3}$ ,  $\frac{15V_{DC}}{34}$ ,  $\frac{28V_{DC}}{51}$ ,  $\frac{2V_{DC}}{3}$  are obtained.

## REDUCTION OF COMMON MODE VOLTAGE USING VARIOUS CARRIER BASED PWM TECHNIQUES

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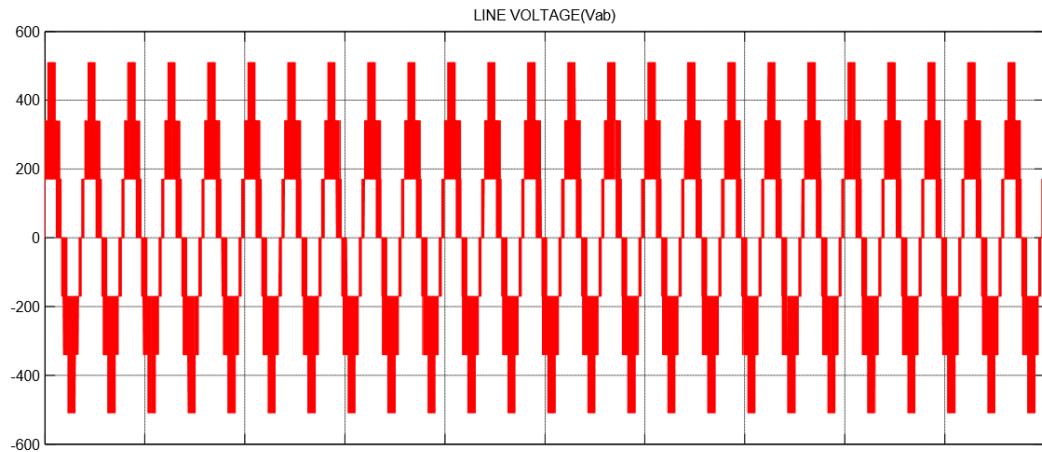


Fig.4.11. Line voltage of Four Level Inverter for Mode 2

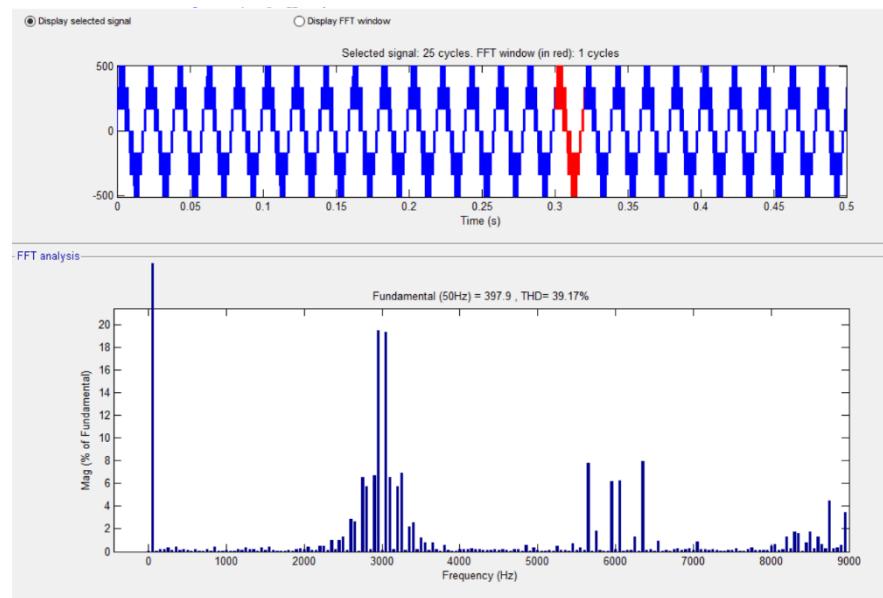


Fig.4.12. FFT Analysis of Four Level Inverter for Mode 2

## REDUCTION OF COMMON MODE VOLTAGE USING VARIOUS CARRIER BASED PWM TECHNIQUES

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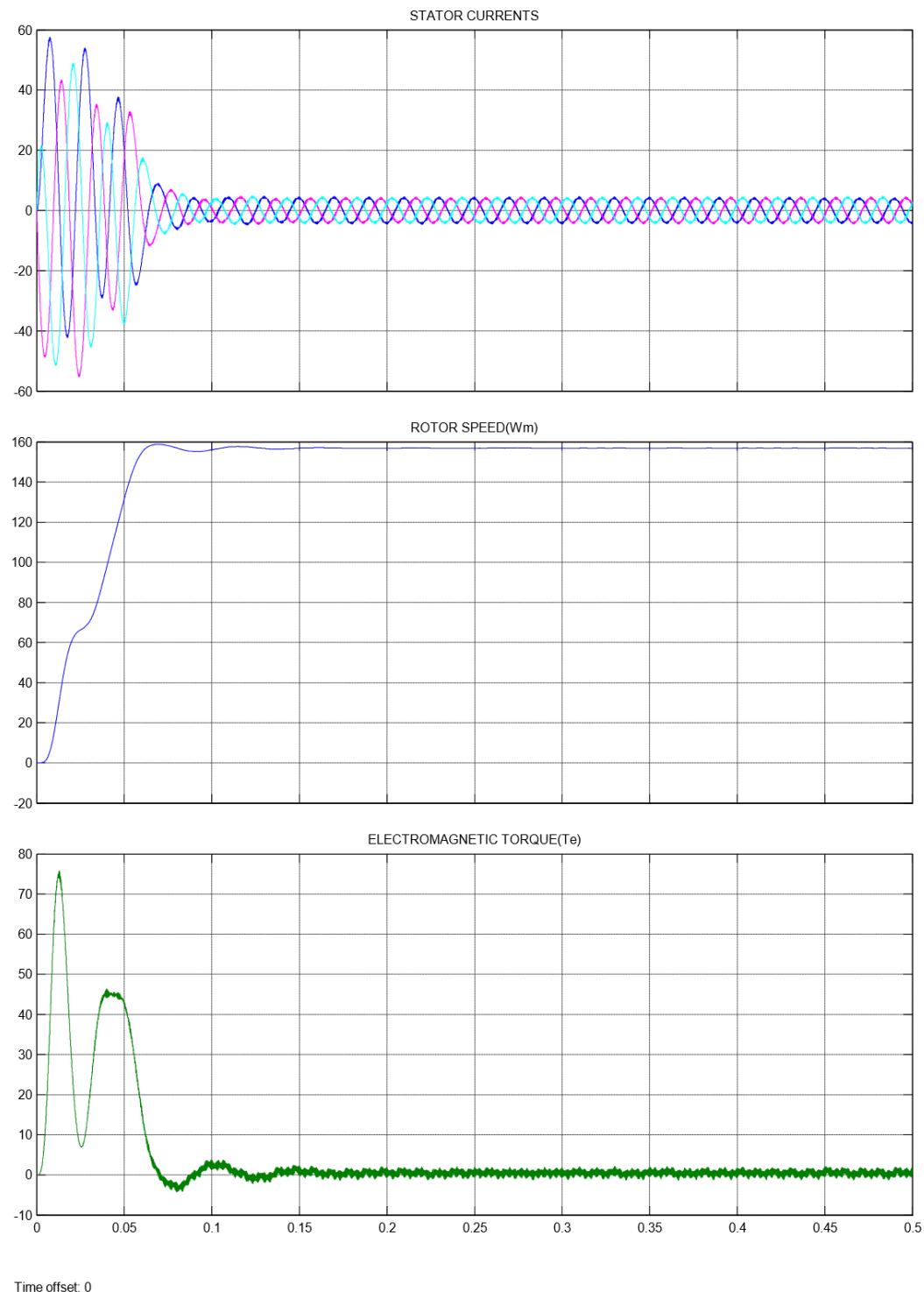


Fig.4.13. Four level Inverter fed Induction Motor Drive results for Mode 2

Here, The machine runs at no load condition, So the Electromagnetic Torque ( $T_e$ ) is zero.

## REDUCTION OF COMMON MODE VOLTAGE USING VARIOUS CARRIER BASED PWM TECHNIQUES

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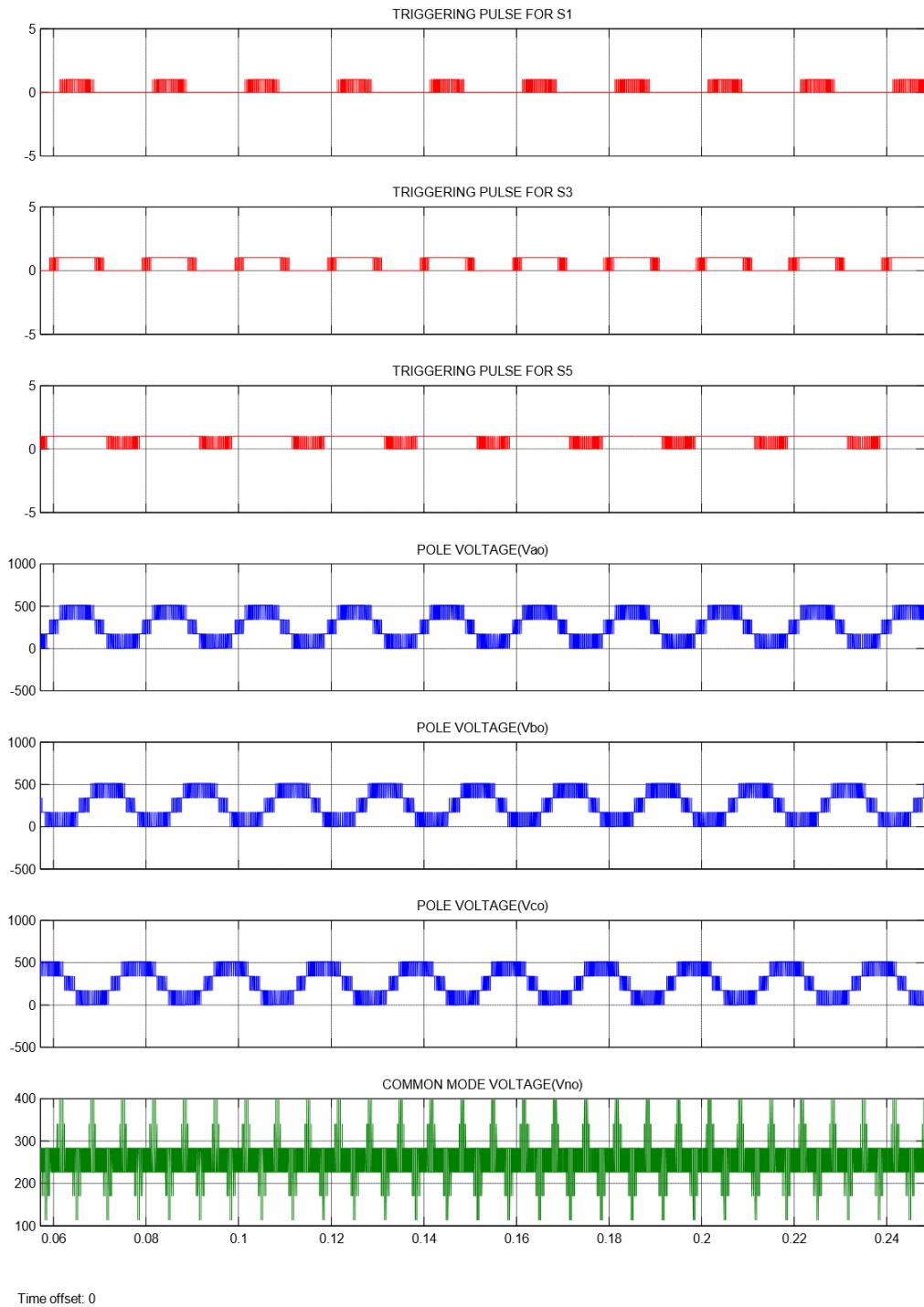


Fig.4.14. Pole voltage and common mode voltage of Four level Inverter for Mode 3

For an input voltage of  $V_{DC}$ , Common mode voltage comprising of levels  $\frac{23V_{DC}}{102}$ ,  $\frac{V_{DC}}{3}$ ,  $\frac{15V_{DC}}{34}$ ,  $\frac{28V_{DC}}{51}$ ,  $\frac{2V_{DC}}{3}$  and  $\frac{40V_{DC}}{51}$  are obtained.

## REDUCTION OF COMMON MODE VOLTAGE USING VARIOUS CARRIER BASED PWM TECHNIQUES

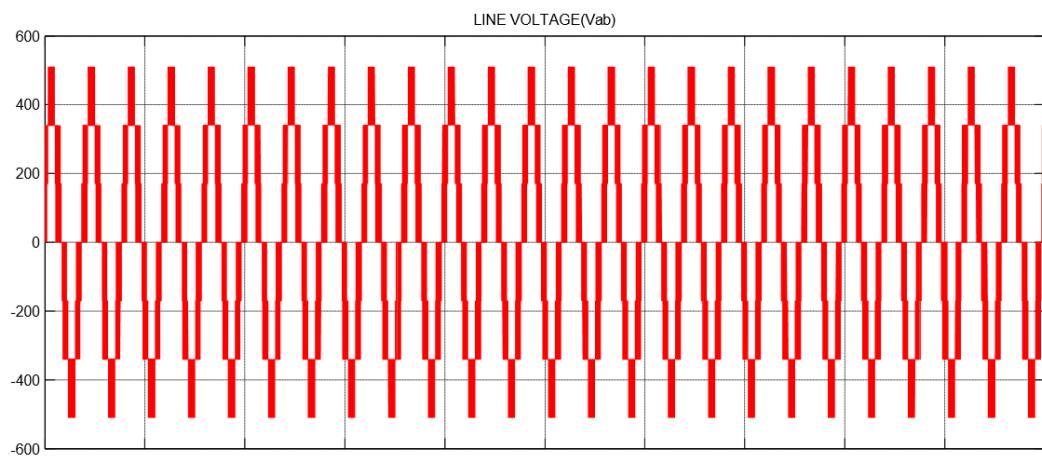


Fig.4.15. Line voltage of Four Level Inverter for Mode 3

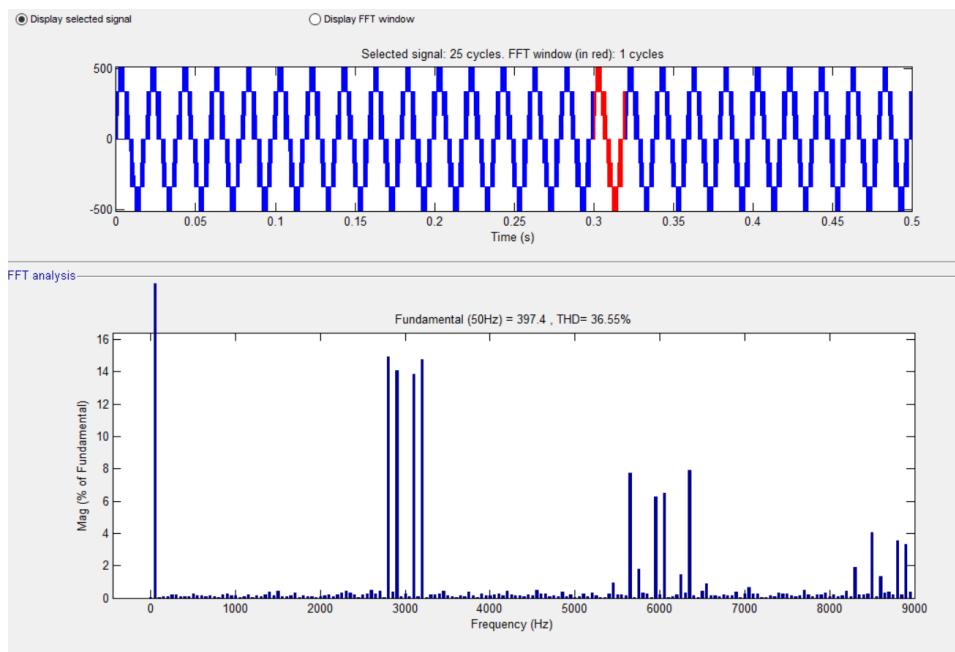


Fig.4.16. FFT Analysis of Four Level Inverter for Mode 3

## REDUCTION OF COMMON MODE VOLTAGE USING VARIOUS CARRIER BASED PWM TECHNIQUES

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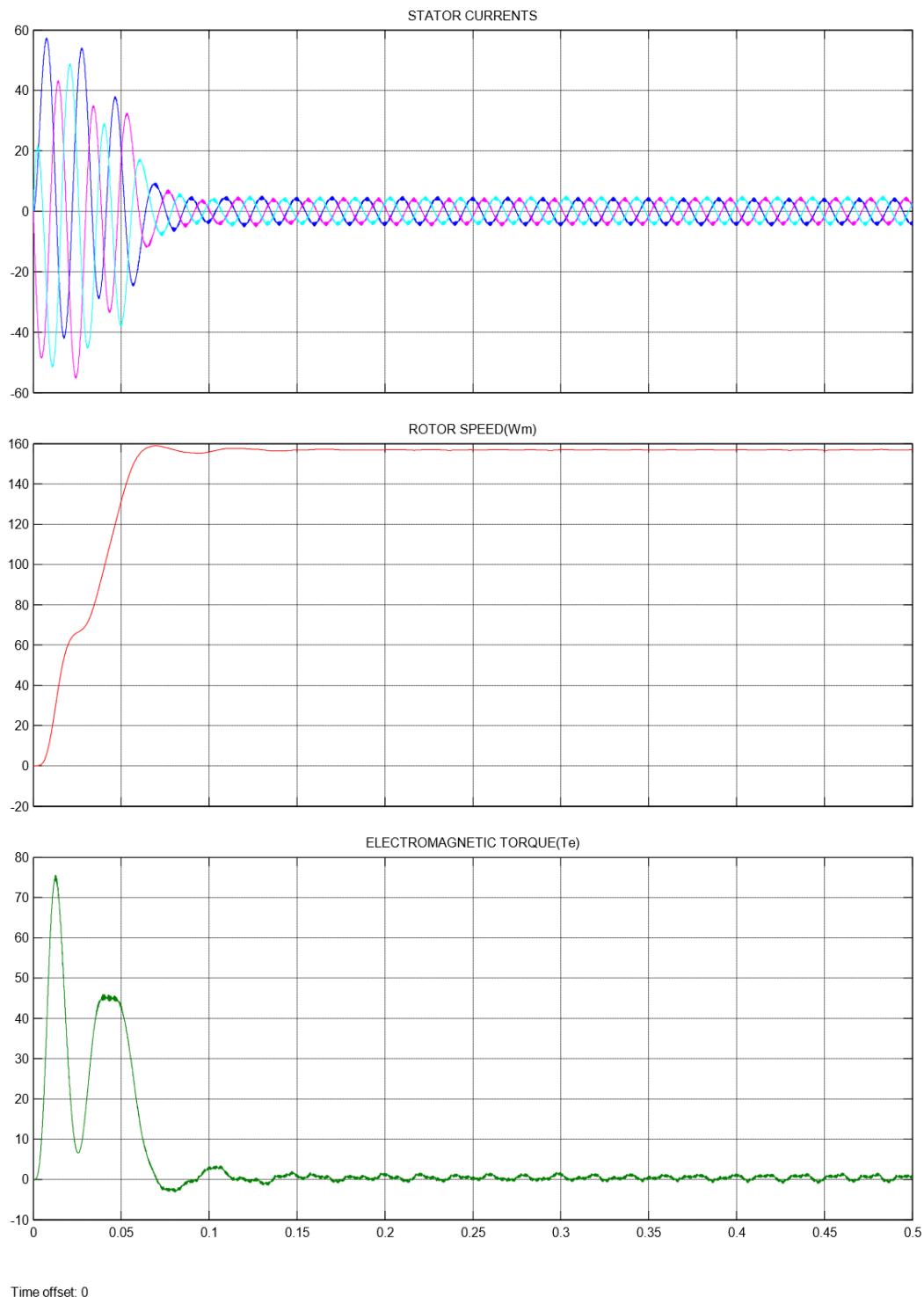


Fig.4.17. Four level Inverter fed Induction Motor Drive results for Mode 3

Here, The machine runs at no load condition, So the Electromagnetic Torque ( $T_e$ ) is zero.

## REDUCTION OF COMMON MODE VOLTAGE USING VARIOUS CARRIER BASED PWM TECHNIQUES

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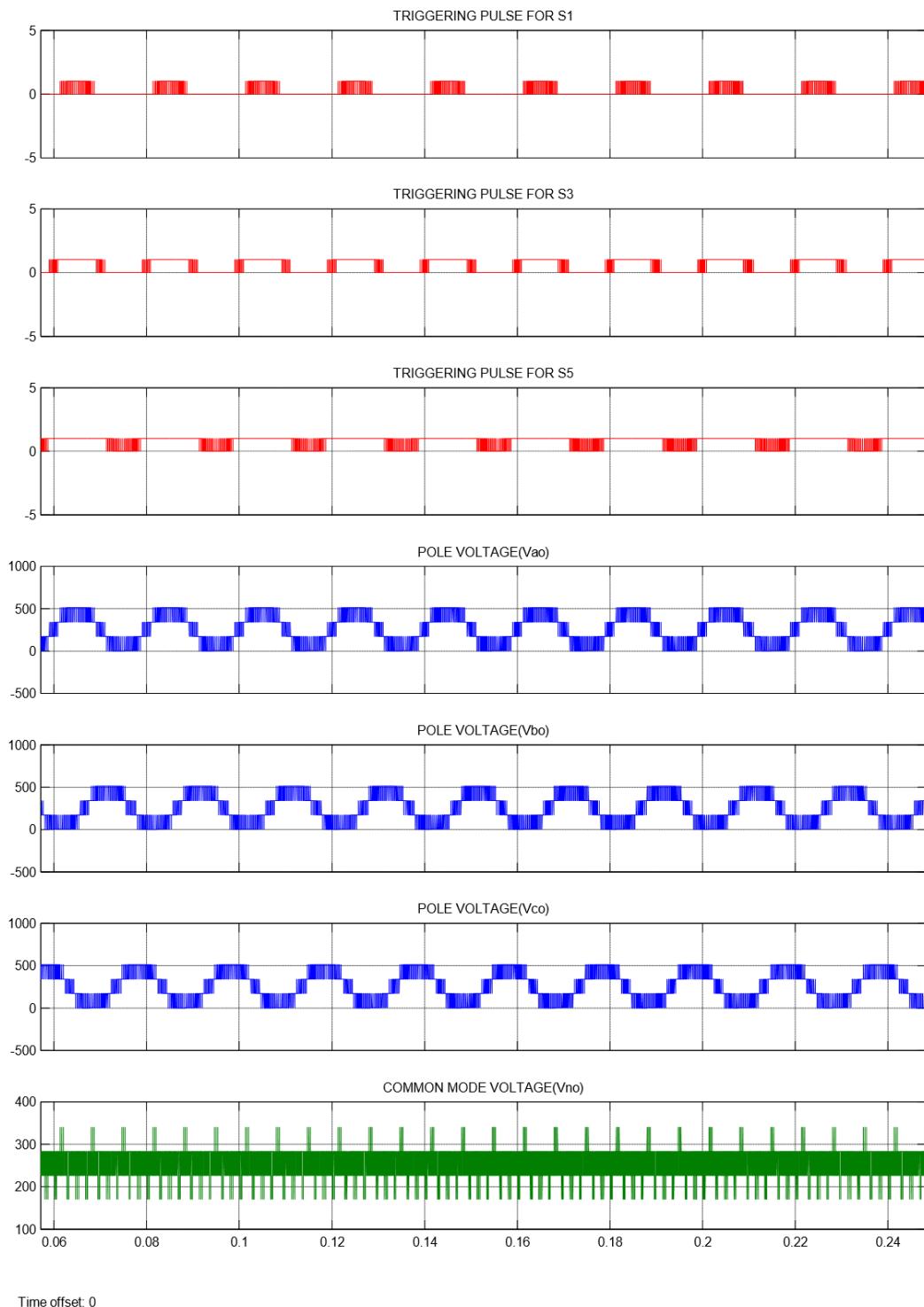


Fig.4.18. Pole voltage and common mode voltage of Four level Inverter for Mode 4

For an input voltage of  $V_{DC}$ , Common mode voltage comprising of levels

$$\frac{V_{DC}}{3}, \frac{15V_{DC}}{34}, \frac{28V_{DC}}{51}, \frac{2V_{DC}}{3}$$

## REDUCTION OF COMMON MODE VOLTAGE USING VARIOUS CARRIER BASED PWM TECHNIQUES

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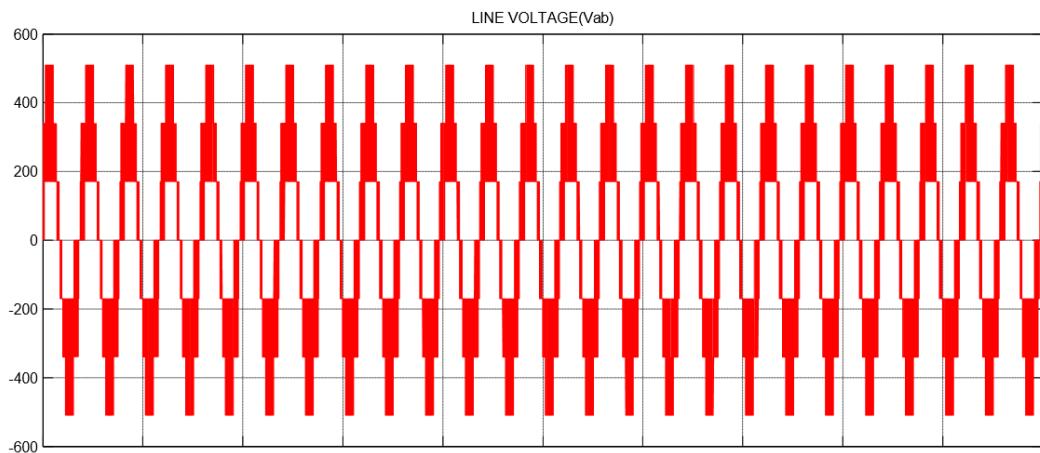


Fig.4.19. Line voltage of Four Level Inverter for Mode 4

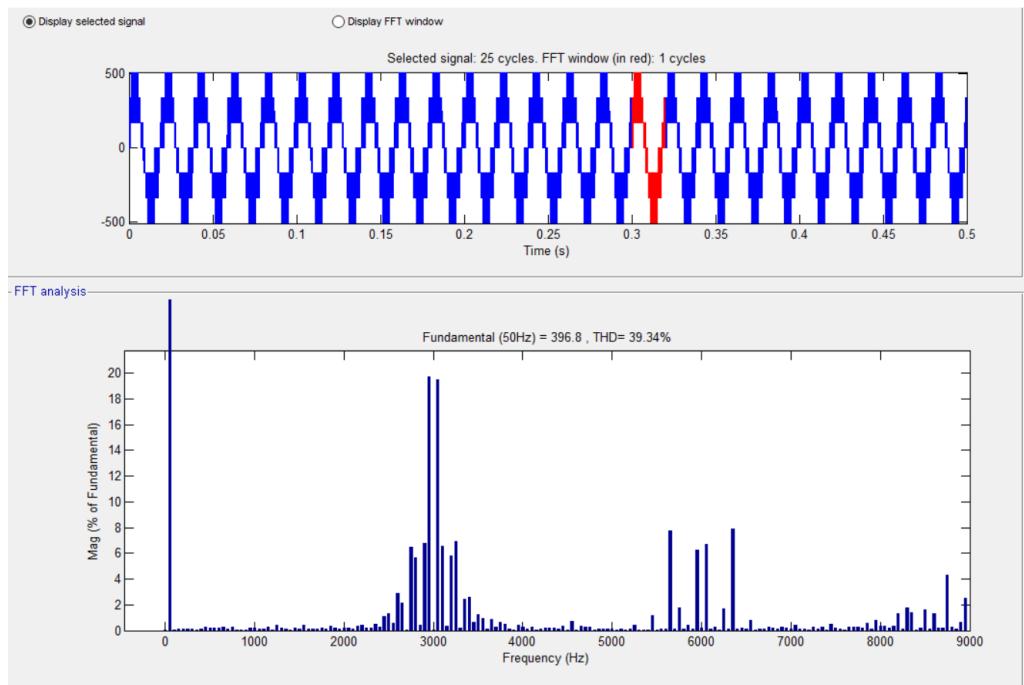


Fig.4.20. FFT Analysis of Four Level Inverter for Mode 4

## REDUCTION OF COMMON MODE VOLTAGE USING VARIOUS CARRIER BASED PWM TECHNIQUES

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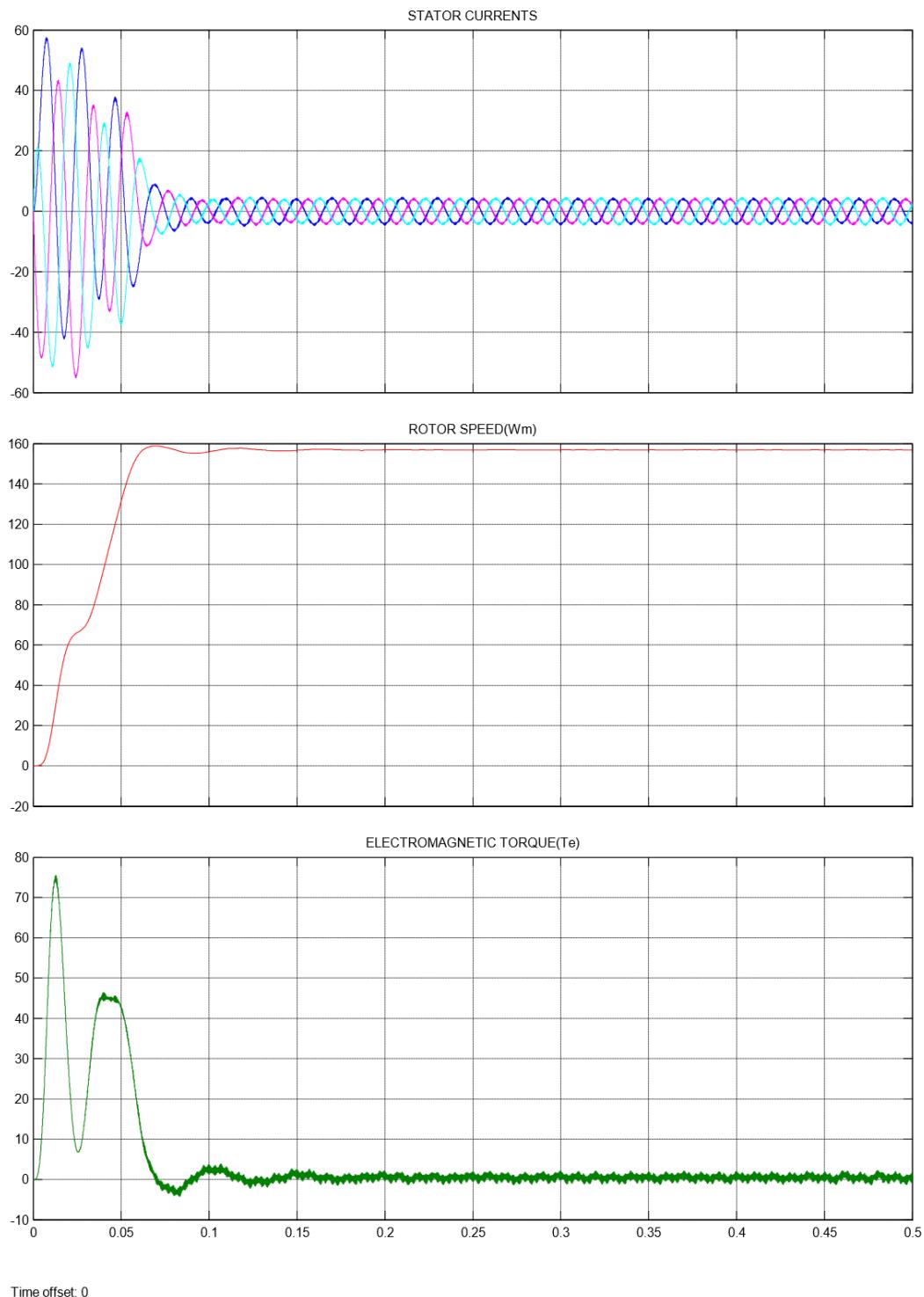


Fig.4.21. Four level Inverter fed Induction Motor Drive results for Mode 4

Here, The machine runs at no load condition, So the Electromagnetic Torque ( $T_e$ ) is zero.

**REDUCTION OF COMMON MODE VOLTAGE USING VARIOUS  
CARRIER BASED PWM TECHNIQUES**

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Table 4.1: Results of Four level Inverter

<b>LEVEL</b>	<b>SPWM TECHNIQUE</b>	<b>COMMON MODE VOLTAGE (V<sub>no</sub>)</b>	<b>THD (%) (Line Voltage)</b>
<b>FOUR</b>	MODE 1	$\frac{23V_{DC}}{102}, \frac{V_{DC}}{3}, \frac{15V_{DC}}{34}, \frac{28V_{DC}}{51}, \frac{2V_{DC}}{3},$ $\frac{40V_{DC}}{51}$	24.50
	MODE 2	$\frac{V_{DC}}{3}, \frac{15V_{DC}}{34}, \frac{28V_{DC}}{51}, \frac{2V_{DC}}{3}$	39.17
	MODE 3	$\frac{23V_{DC}}{102}, \frac{V_{DC}}{3}, \frac{15V_{DC}}{34}, \frac{28V_{DC}}{51}, \frac{2V_{DC}}{3},$ $\frac{40V_{DC}}{51}$	36.55
	MODE 4	$\frac{V_{DC}}{3}, \frac{15V_{DC}}{34}, \frac{28V_{DC}}{51}, \frac{2V_{DC}}{3}$	39.34

## REDUCTION OF COMMON MODE VOLTAGE USING VARIOUS CARRIER BASED PWM TECHNIQUES

### 4.4 FIVE LEVEL INVERTER

An inverter that produces five levels in the output pole voltage is called Five level Inverter. A Five level Inverter creates five different voltages for the load. The circuit diagram of five level inverter is shown in Fig.4.22.

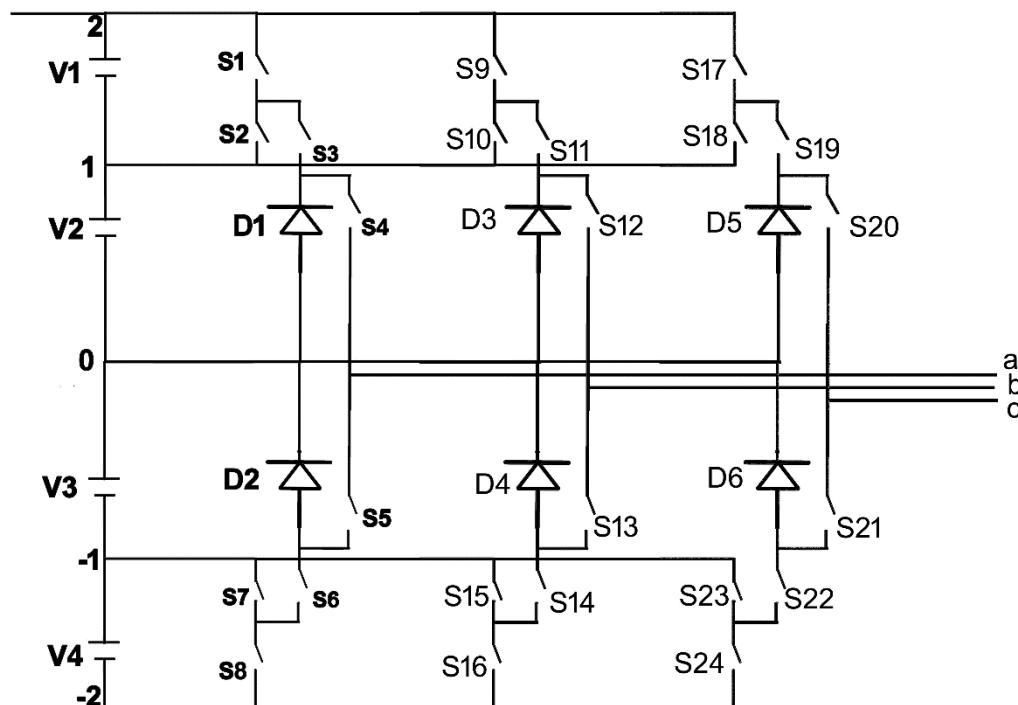


Fig.4.22. Five Level Inverter circuit

It comprises of 24 active switches, each equipped with an antiparallel freewheeling diode. Above circuit comes under Cascaded Multilevel Inverter Topology. Suppose if one leg was considered from the above circuit then S1-S2, S3-S5, S4-S6 and S7-S8 are the complementary pairs of switches. In this topology SPWM technique was used, where sinusoidal signal was compared with triangular signal for getting resultant pulse. Here the level is five so sinusoidal signal is compared with N-1 carrier signals where N is number of levels i.e., sinusoidal signal is compared with four carrier signals. If single leg was considered then the carrier comparison approach is shown in Fig.4.10, where  $V_{ref}$  is reference signal and  $V_{T1}$ ,  $V_{T2}$ ,  $V_{T3}$  and  $V_{T4}$  are carrier signals.  $V_{ref}$  and  $V_{T1}$  are compared to get a resultant pulse which is given to the switch S1.  $V_{ref}$  and  $V_{T2}$  are compared to get a resultant pulse which is given to the switch S3.  $V_{ref}$  and  $V_{T3}$  are compared to get a resultant pulse which is given to the switch S4.  $V_{ref}$  and  $V_{T3}$  are compared to get a resultant pulse which is given to the switch S7.

## REDUCTION OF COMMON MODE VOLTAGE USING VARIOUS CARRIER BASED PWM TECHNIQUES

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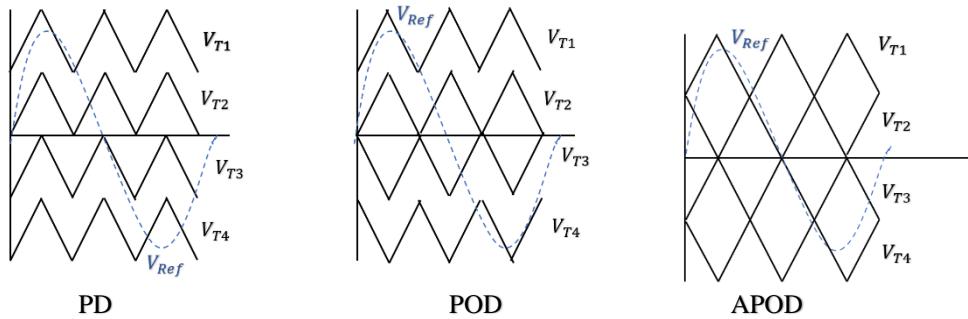


Fig.4.23. Carrier Comparison Approach

In Phase Disposition (PD) all the carrier signals are in same phase. In Phase Opposition Disposition (POD) all the carrier signals above the zero are out of phase with those below the zero by  $180^\circ$ . In Alternate Phase Opposition Disposition (APOD) all the adjacent carrier signals are out of phase by  $180^\circ$

### 4.5 OPERATION OF FIVE LEVEL INVERTER

Operation of five level inverter is explained by considering the single leg from the above circuit shown in Fig 4.22. The single leg circuit of the five level inverter is shown in Fig 4.24.

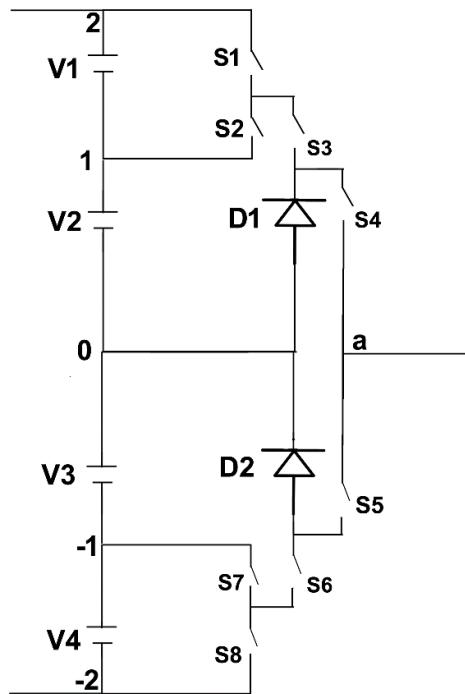


Fig.4.24. Single leg circuit of Five level Inverter

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## REDUCTION OF COMMON MODE VOLTAGE USING VARIOUS CARRIER BASED PWM TECHNIQUES

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Here S1-S2, S3-S5, S4-S6 and S7-S8 are the complementary pairs of switches. Consider an instant where S1 is in OFF condition so that S2 will be in ON condition. Switches S3 and S5 are in ON/OFF condition. S4 will be in ON condition so that S6 will be in OFF condition. S7 will be in ON condition so that S8 will be in OFF condition. If S2, S3, S4 are in ON condition then V2 will be the pole voltage. If S4 and S5 will be in ON condition then 0 will be the pole voltage. Consider an instant where S1, S2 are in ON/OFF condition. S3 will be in ON condition so that S5 will be in OFF condition. S4 will be in ON condition so that S6 will be in OFF condition. S7 will be in ON condition so that S8 will be in OFF condition. Switches S1, S3, S4 and S7 are in ON condition then V1 will be the pole voltage. Switches S2, S3, S4 and S7 are in ON condition then V2 will be the pole voltage. Consider an instant S2 will be in ON condition so that S1 will be in OFF condition. S5 will be in ON condition so that S3 will be in OFF condition. S7 will be in ON condition so that S8 will be in OFF condition. Switches S4, S6 will be in ON/OFF condition. If S4, S5 and S7 are in ON condition then the pole voltage will be 0. If S6, S5 and S7 are in ON condition then the pole voltage will be If S4, S5 and S7 are in ON condition then the pole voltage will be V3. Consider an instant in which S2 will be in ON condition so that S1 will be in OFF condition. S5 will be in ON condition so that S3 will be in OFF condition. S6 will be in ON condition so that S4 will be in OFF condition. Switches S7, S8 will be in ON/OFF condition. If switches S2, S5, S6 and S7 are in ON condition then the pole voltage will be V3. If switches S2, S5, S6 and S8 are in ON condition then the pole voltage will be V4. Here five levels of voltages occurred which are V1, V2, 0, V3 and V4. For remaining legs also the operation is same. Voltage between output point of legs and mid potential of the dc bus is called as pole voltage referred to the mid potential of the dc bus. Harmonic content in the output waveform of five level inverter will be less compared to four level inverter. Total Harmonic Distortion was calculated by performing Fast Fourier Transform Analysis. As the level of an Inverter increases the harmonic content and common mode voltage will be reduced. Common mode voltage ( $V_{no}$ ) is nothing but it is the voltage measured between neutral point to the reference point. If common mode voltage is high, unwanted voltages passes through the windings of the machine and damages the windings and losses also get increased which will effect the efficiency of the machine. Common mode voltage is given by

$$\text{Common Mode Voltage } (V_{no}) = \frac{V_{ao} + V_{bo} + V_{co}}{3}$$

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#### 4.6 SIMULATION RESULTS

Three Phase Five Level fed Induction motor drive shown in Fig.4.25.

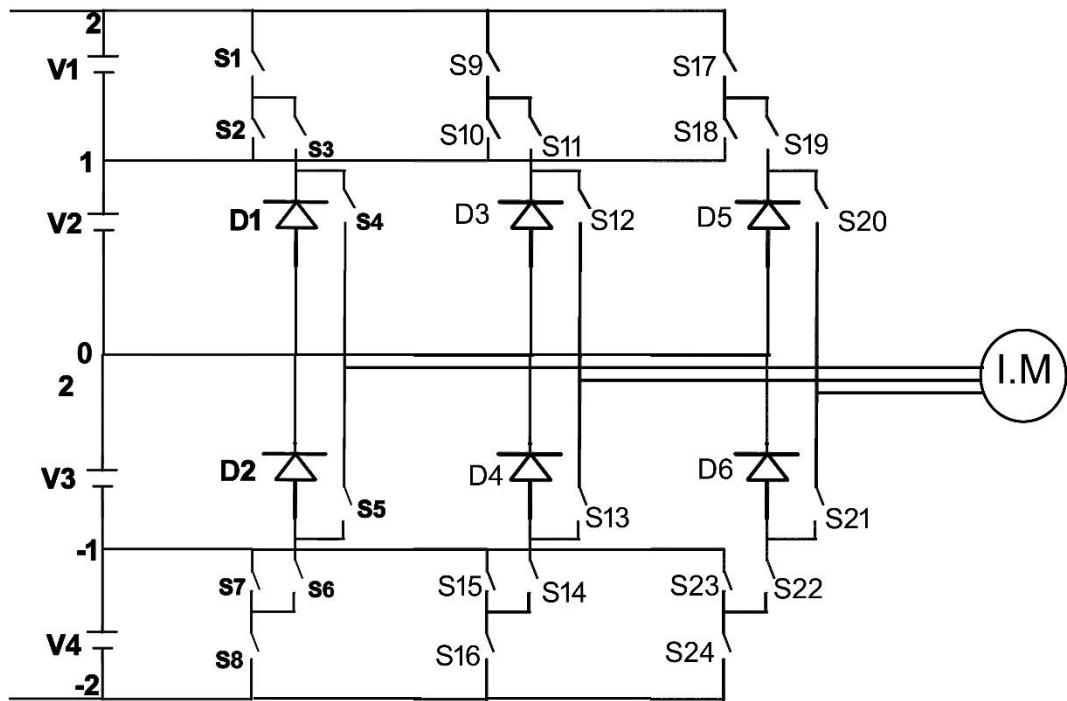


Fig.4.25. Five Level Inverter fed Induction Motor Drive

#### SIMULATION PARAMETERS

Input DC Voltage ( $V_{DC}$ ) = 510V

Modulation Index = 0.9

Switching Frequency = 3000 Hz

Frequency of Sinewave ( $F_{sw}$ ) = 50 Hz

# REDUCTION OF COMMON MODE VOLTAGE USING VARIOUS CARRIER BASED PWM TECHNIQUES

## SIMULATION MODEL

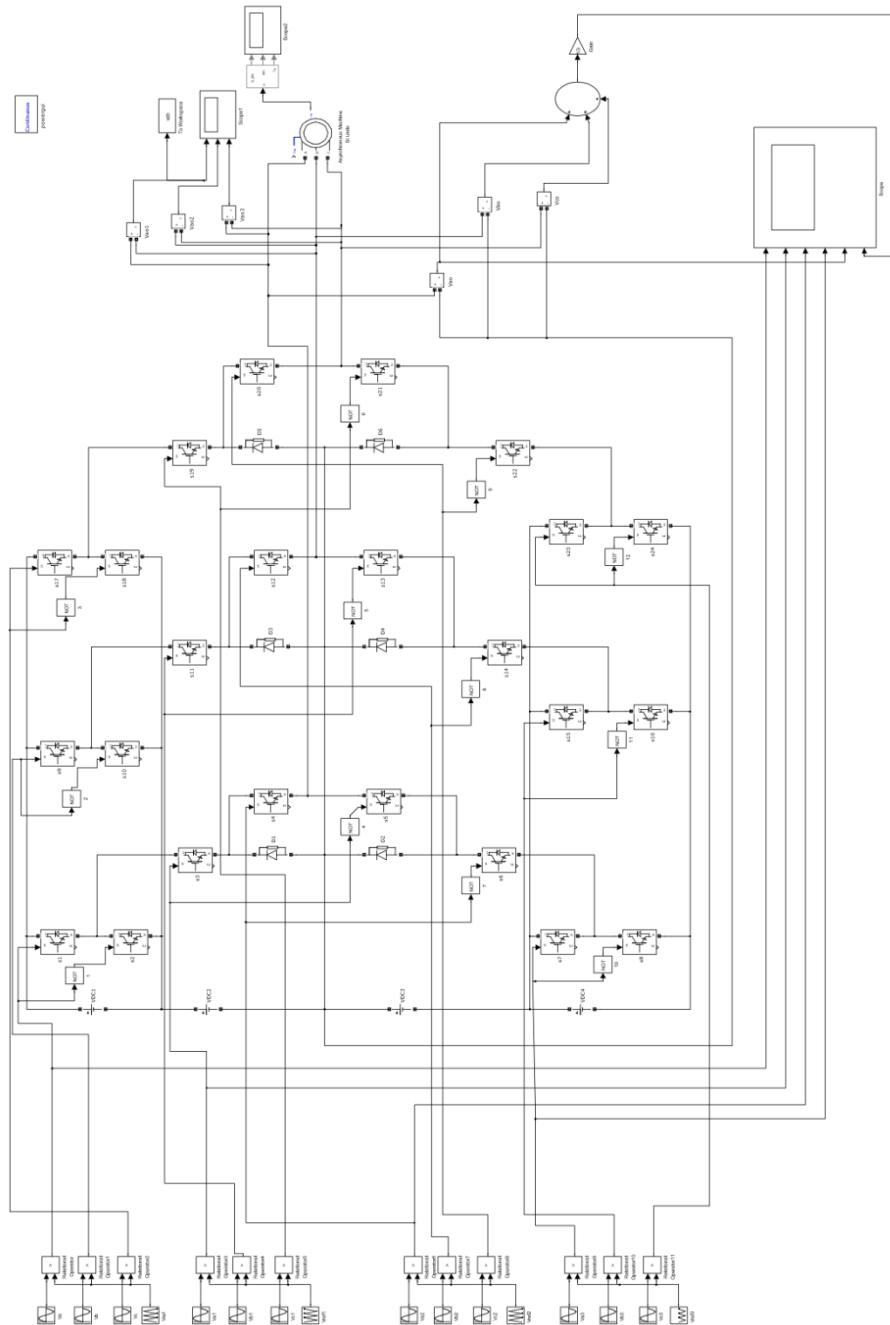


Fig.4.26. Simulation Model of Five Level inverter

## REDUCTION OF COMMON MODE VOLTAGE USING VARIOUS CARRIER BASED PWM TECHNIQUES

For an input voltage of  $V_{DC}$ , Pole voltage comprising of levels  $\frac{V_{DC}}{2}, \frac{V_{DC}}{4}, 0, -\frac{V_{DC}}{4}, -\frac{V_{DC}}{2}$ , Line voltage comprising of levels  $V_{DC}, \frac{38V_{DC}}{51}, \frac{V_{DC}}{2}, \frac{V_{DC}}{4}, 0, -\frac{V_{DC}}{4}, -\frac{V_{DC}}{2}, \frac{-38V_{DC}}{51}, -V_{DC}$  and common mode voltage comprising of levels  $\frac{V_{DC}}{6}, \frac{V_{DC}}{12}, -\frac{V_{DC}}{12}, -\frac{V_{DC}}{6}$  are obtained.

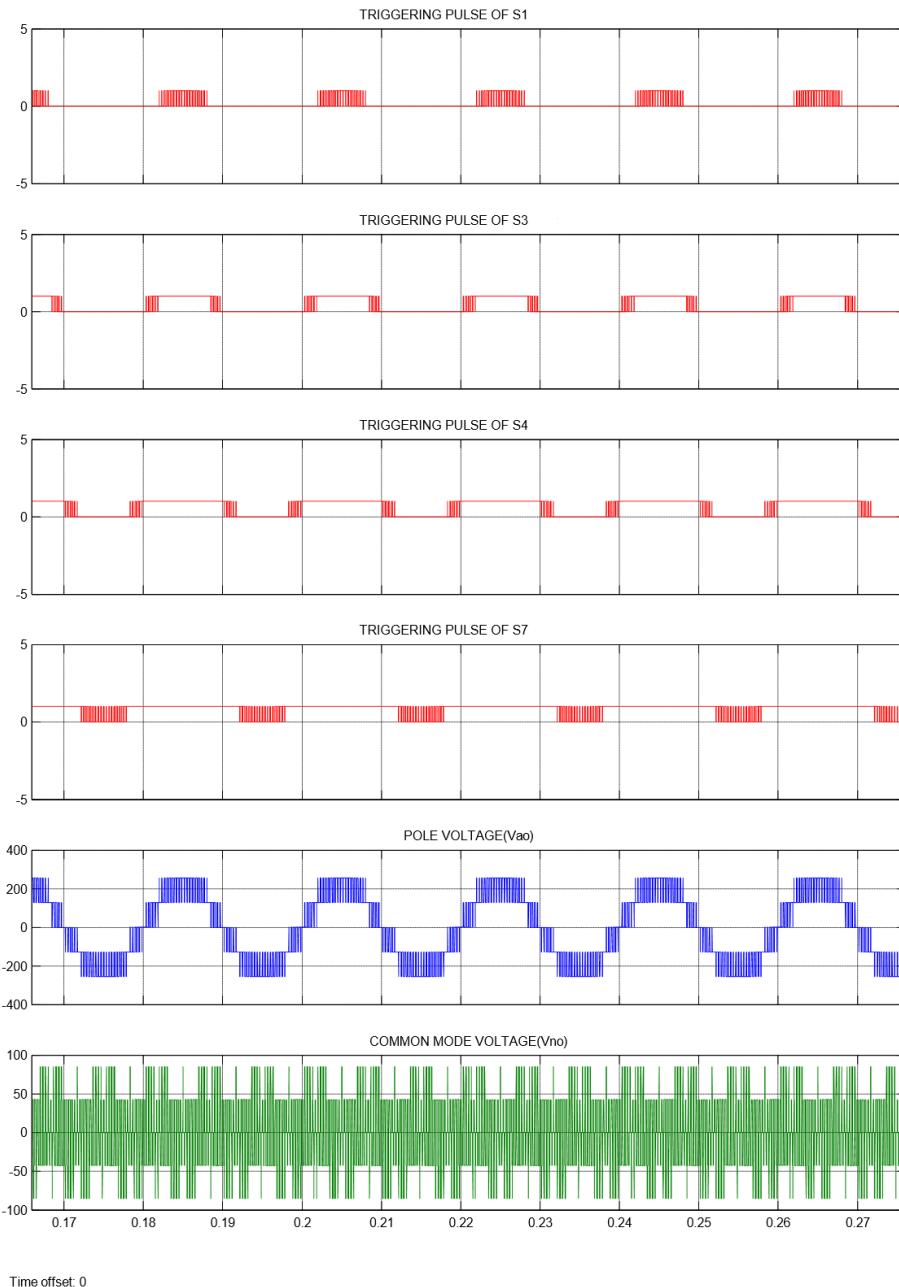


Fig.4.27. Common mode voltage of Five Level Inverter for PDSPWM

## REDUCTION OF COMMON MODE VOLTAGE USING VARIOUS CARRIER BASED PWM TECHNIQUES

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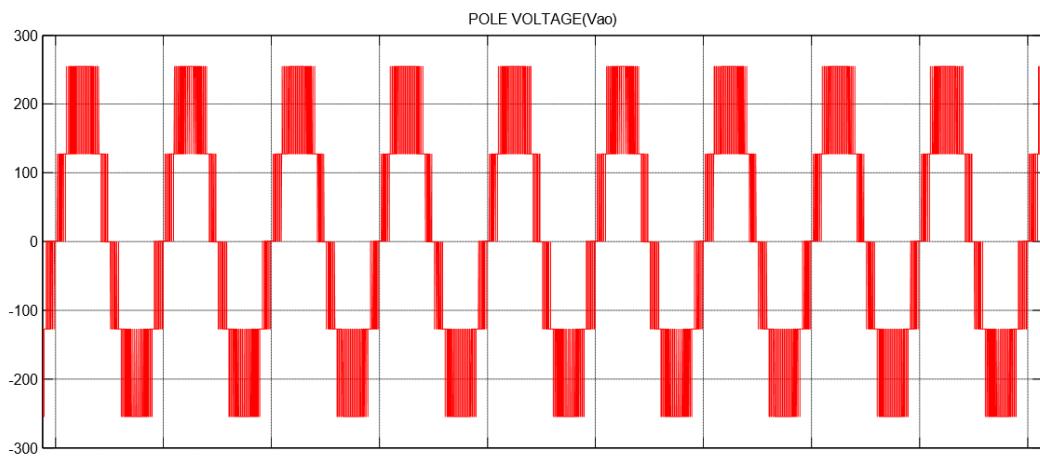


Fig.4.28. Pole Voltage of Five Level Inverter for PDSPWM

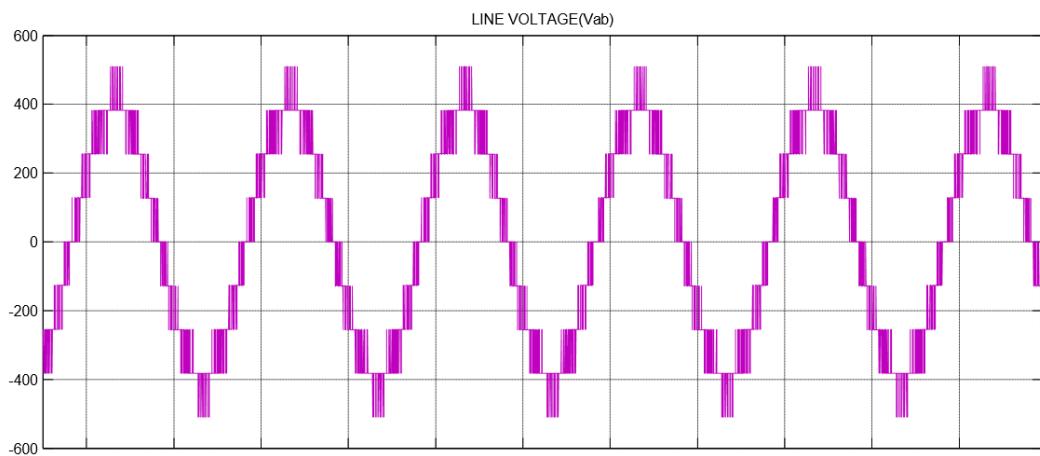


Fig.4.29. Line Voltage of Five Level Inverter for PDSPWM

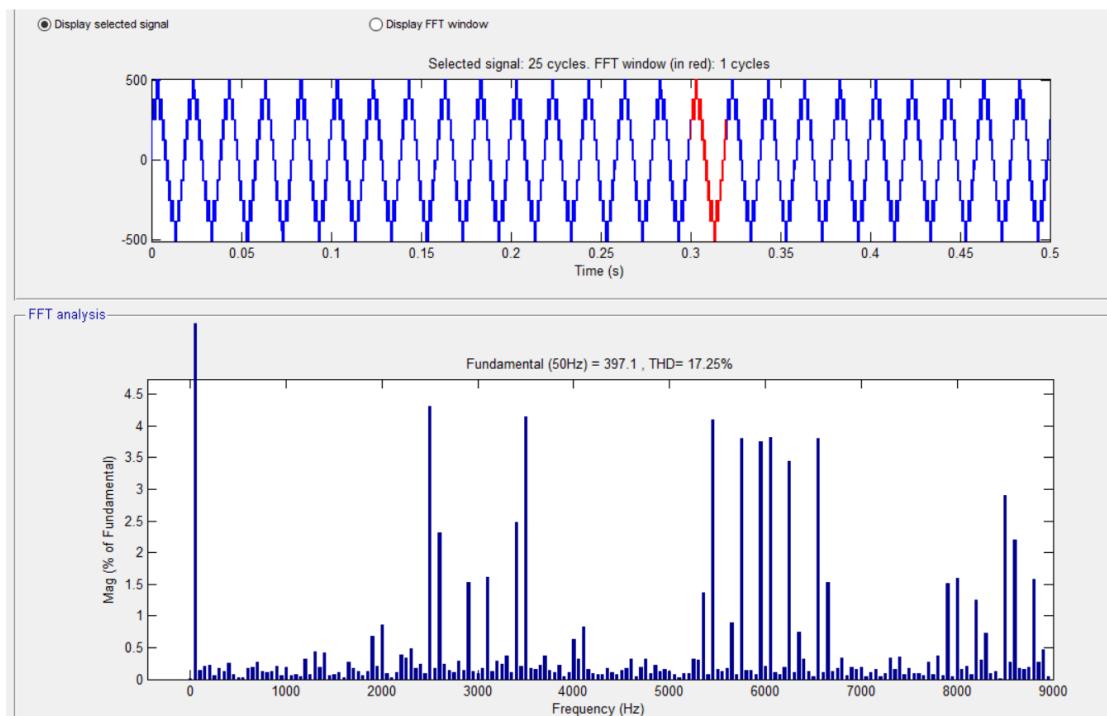


Fig.4.30. FFT Analysis of Five Level Inverter for PDSPWM

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## REDUCTION OF COMMON MODE VOLTAGE USING VARIOUS CARRIER BASED PWM TECHNIQUES

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Here, The machine runs at no load condition, So the Electromagnetic Torque ( $T_e$ ) is zero.

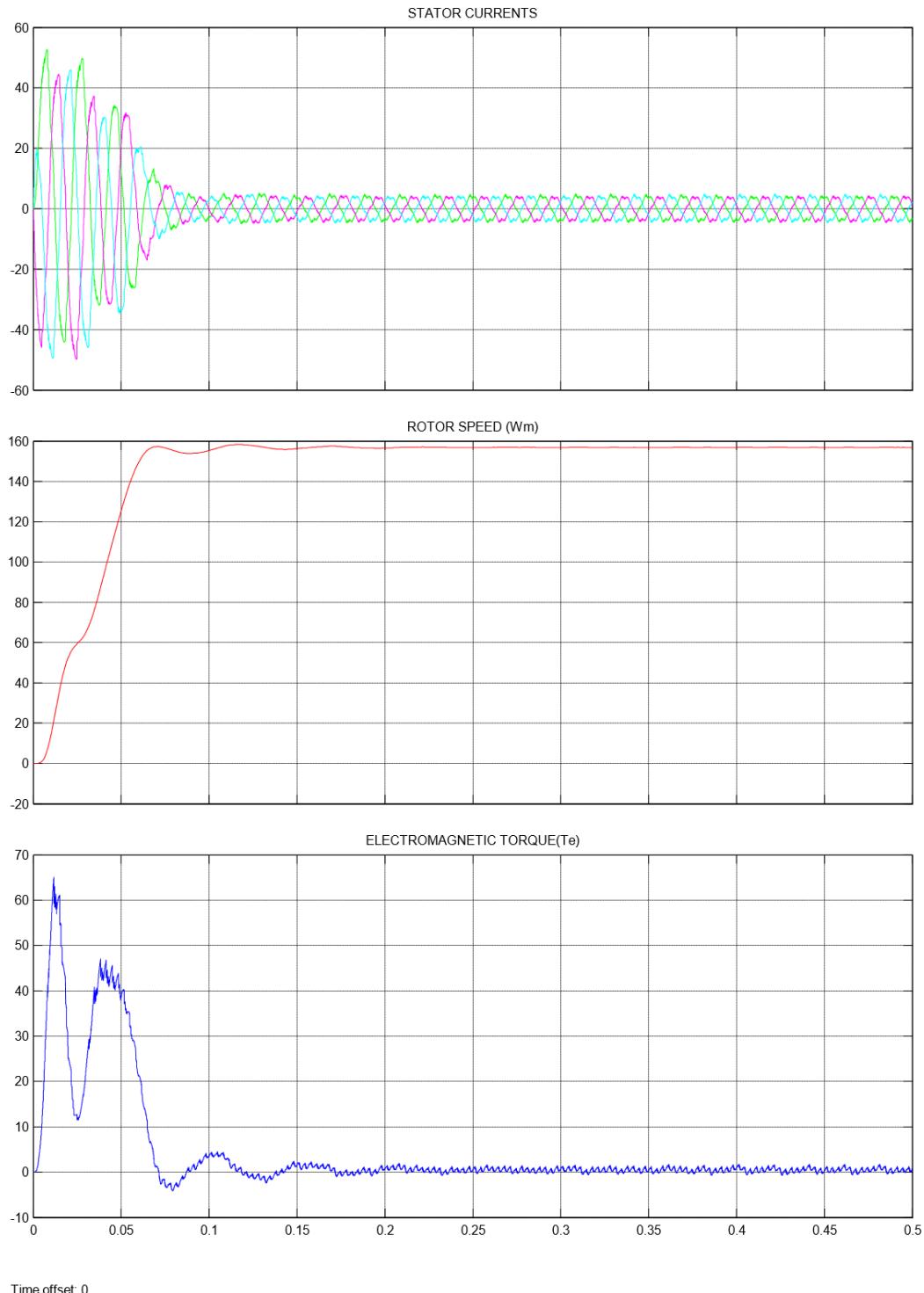


Fig.4.31. Five Level Inverter fed Induction Motor Drive results for PDSPWM

## REDUCTION OF COMMON MODE VOLTAGE USING VARIOUS CARRIER BASED PWM TECHNIQUES

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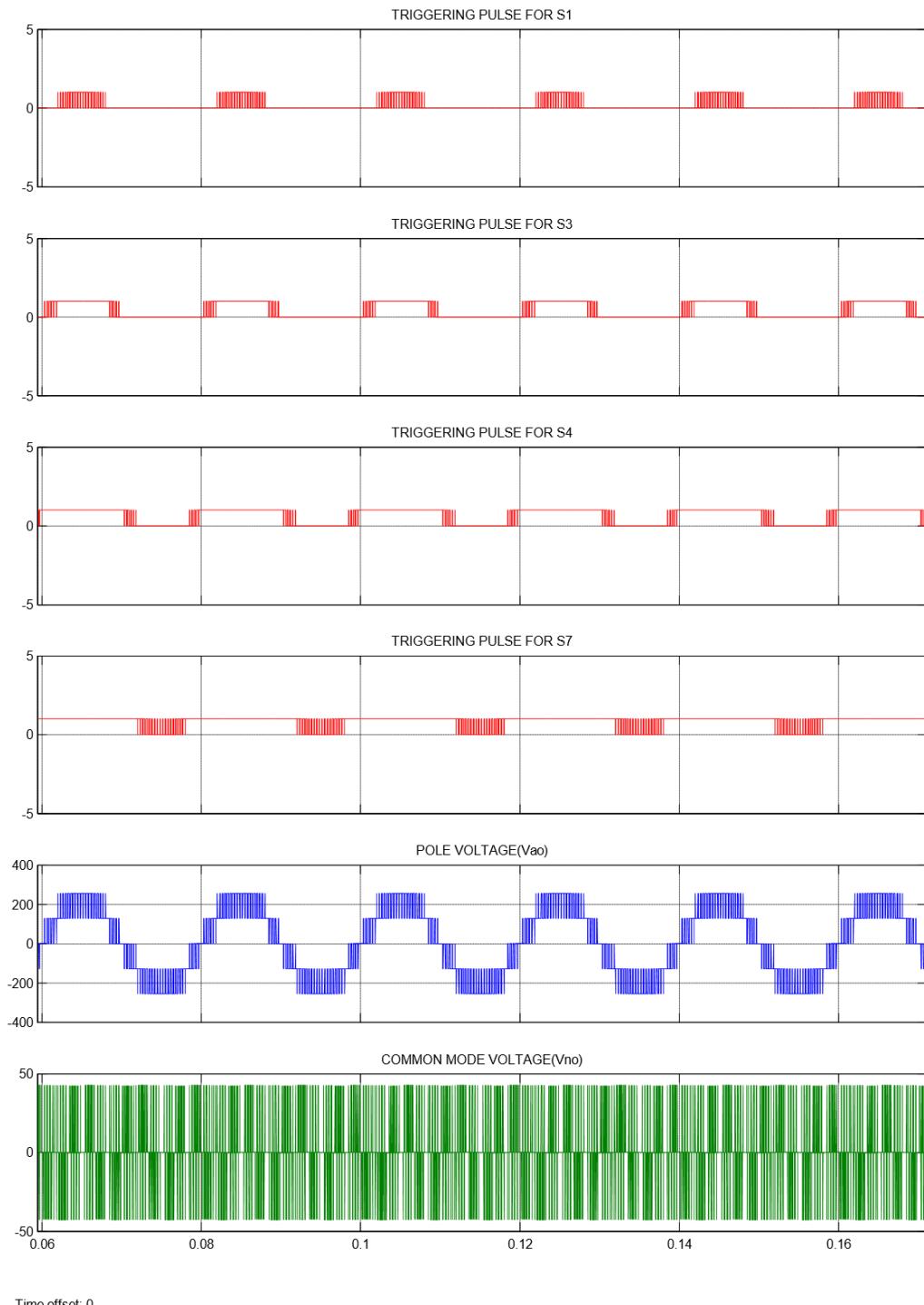


Fig.4.32. Pole voltage & Common mode voltage of Five Level Inverter  
for PODSPWM

For an input voltage of  $V_{DC}$ , common mode voltage comprising of level  $\frac{V_{DC}}{12}$ ,  $-\frac{V_{DC}}{12}$  are obtained.

## REDUCTION OF COMMON MODE VOLTAGE USING VARIOUS CARRIER BASED PWM TECHNIQUES

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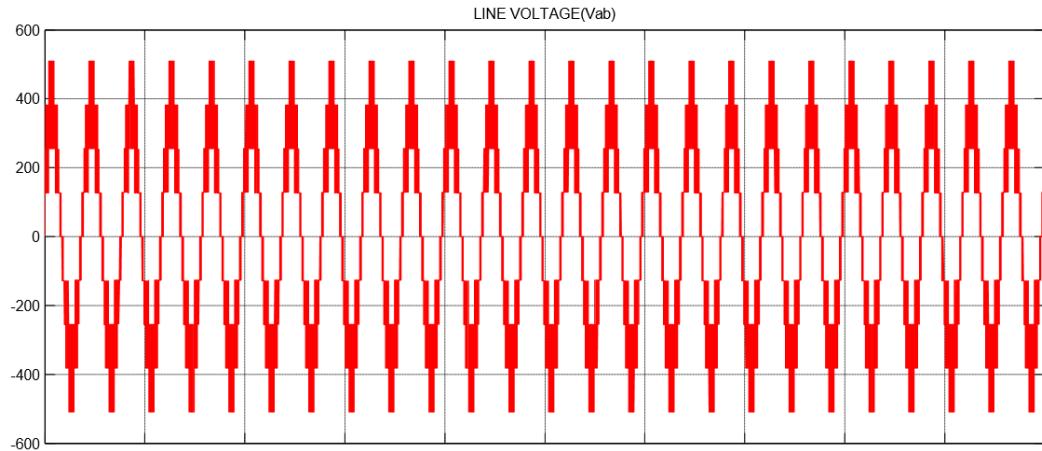


Fig.4.33. Line Voltage of Five Level Inverter for PODSPWM

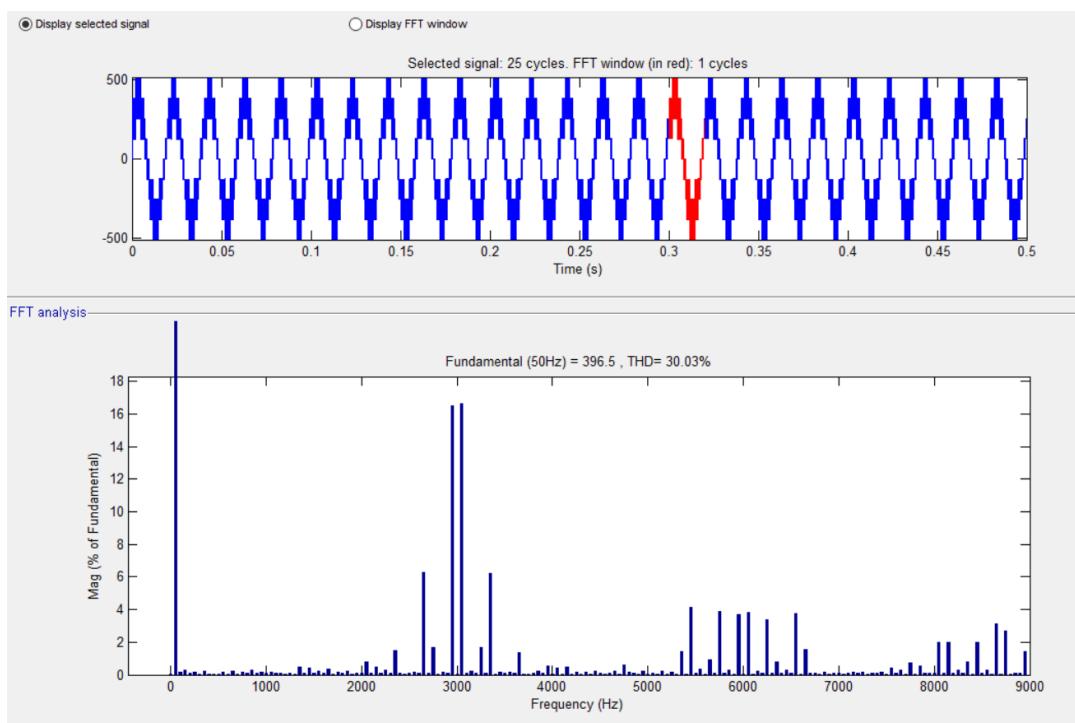


Fig.4.34. FFT Analysis of Five Level Inverter for PODSPWM

## REDUCTION OF COMMON MODE VOLTAGE USING VARIOUS CARRIER BASED PWM TECHNIQUES

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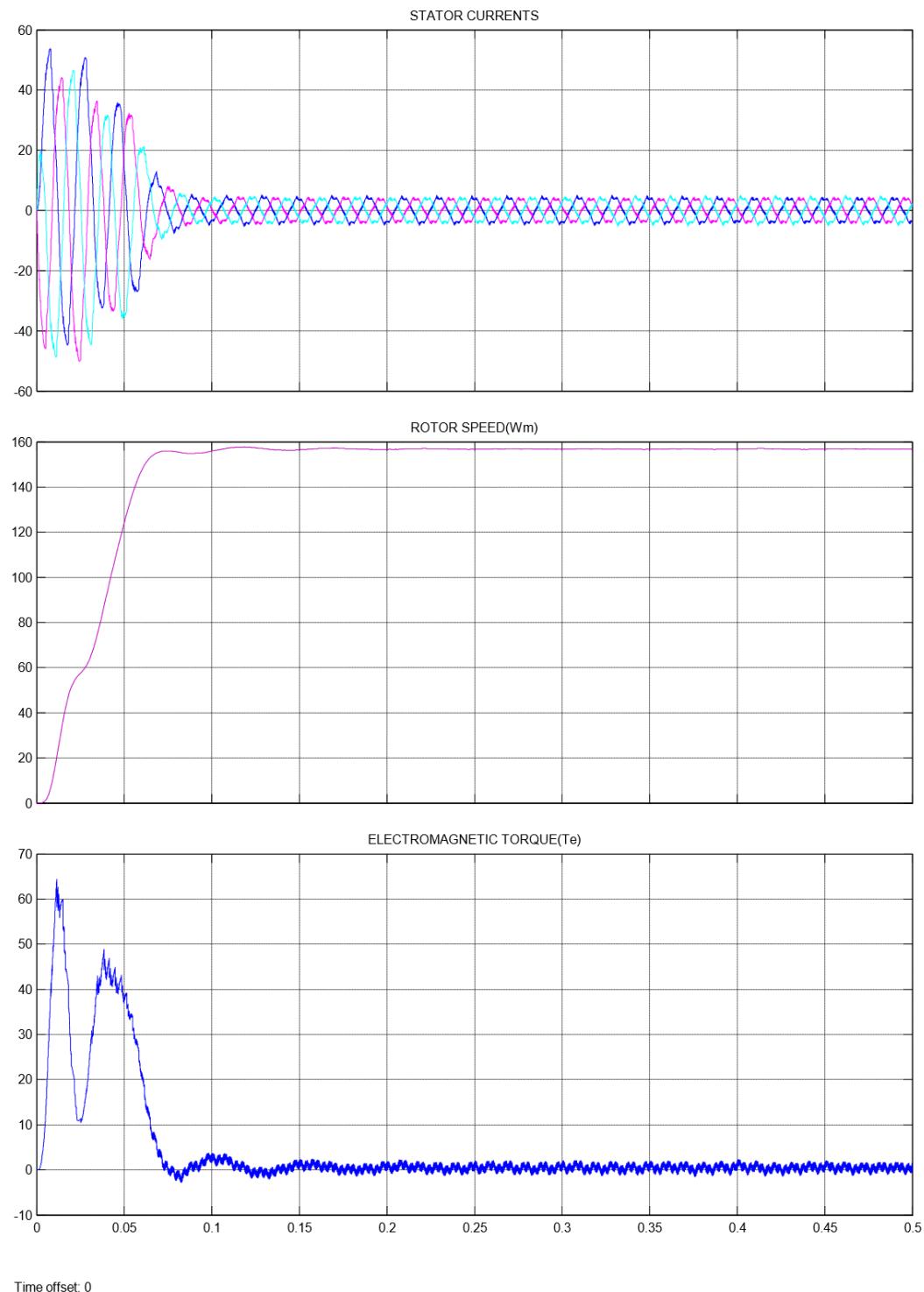
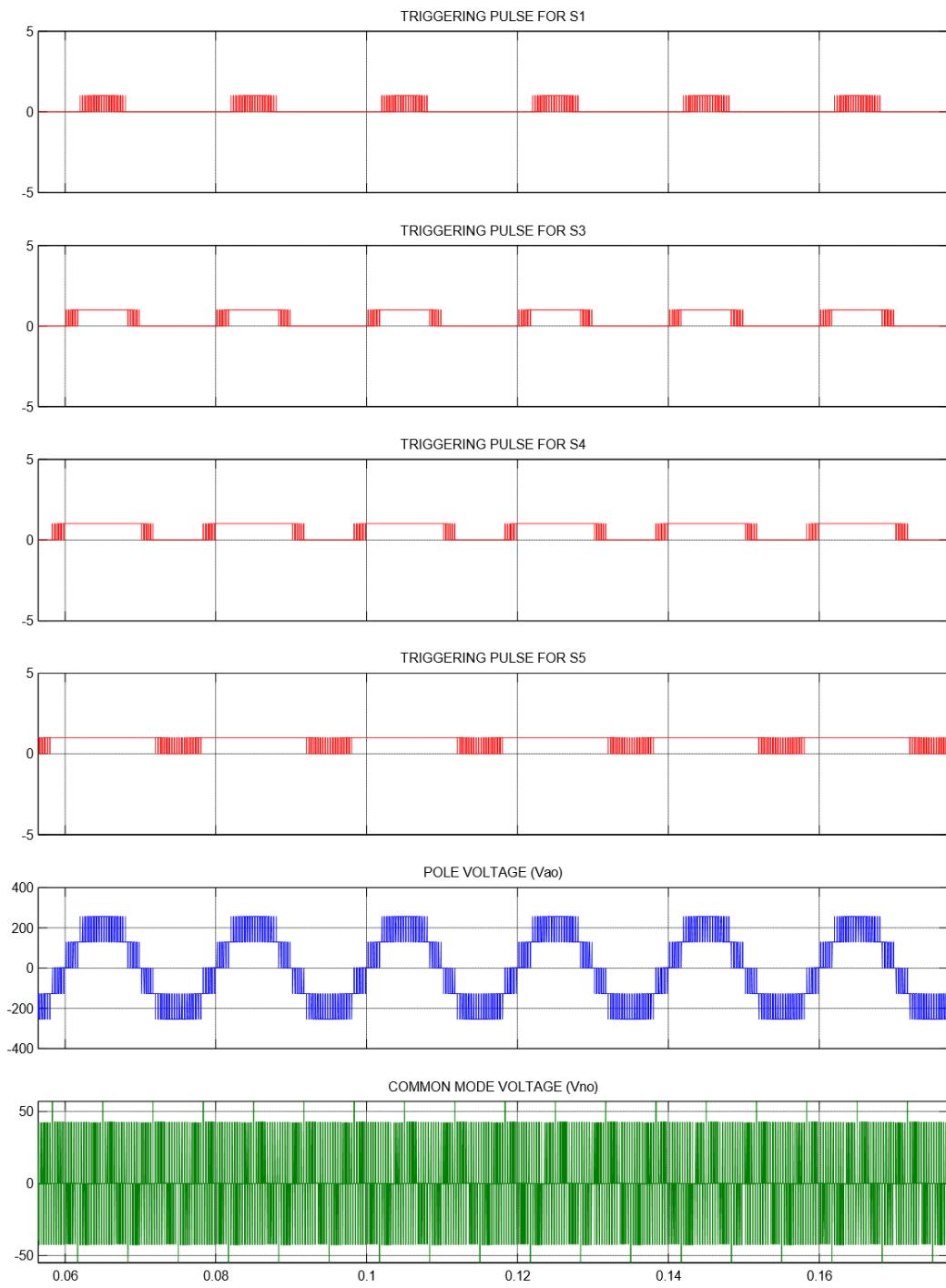


Fig.4.35. Five Level Inverter fed Induction Motor Drive results for PODSPWM  
Here, The machine runs at no load condition, So the Electromagnetic Torque ( $T_e$ ) is zero.

## REDUCTION OF COMMON MODE VOLTAGE USING VARIOUS CARRIER BASED PWM TECHNIQUES

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Time offset: 0

**Fig.4.36. Pole voltage & Common mode voltage of Five Level Inverter for APODSPWM**

For an input voltage of  $V_{DC}$ , common mode voltage comprising of level  $\frac{V_{DC}}{12}$ ,  $-\frac{V_{DC}}{12}$  are obtained.

## REDUCTION OF COMMON MODE VOLTAGE USING VARIOUS CARRIER BASED PWM TECHNIQUES

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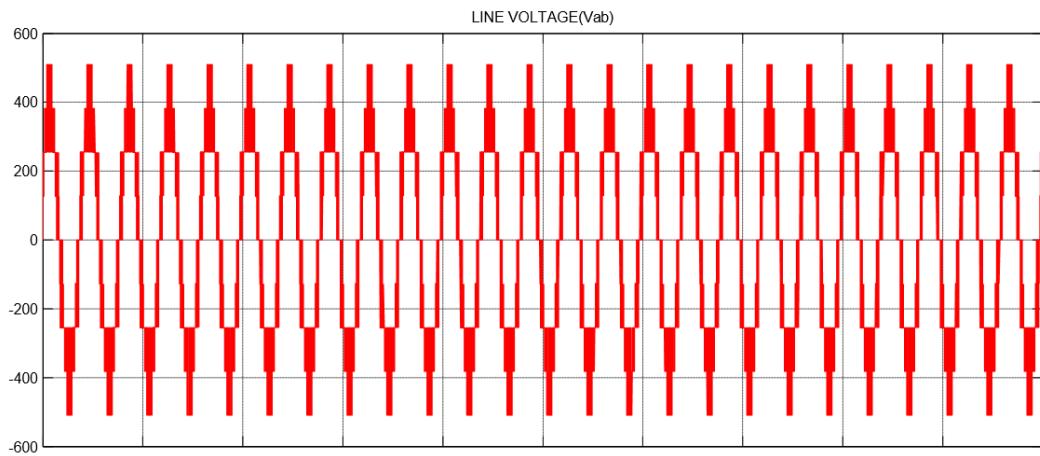


Fig.4.37. Line Voltage of Five Level Inverter for APODSPWM

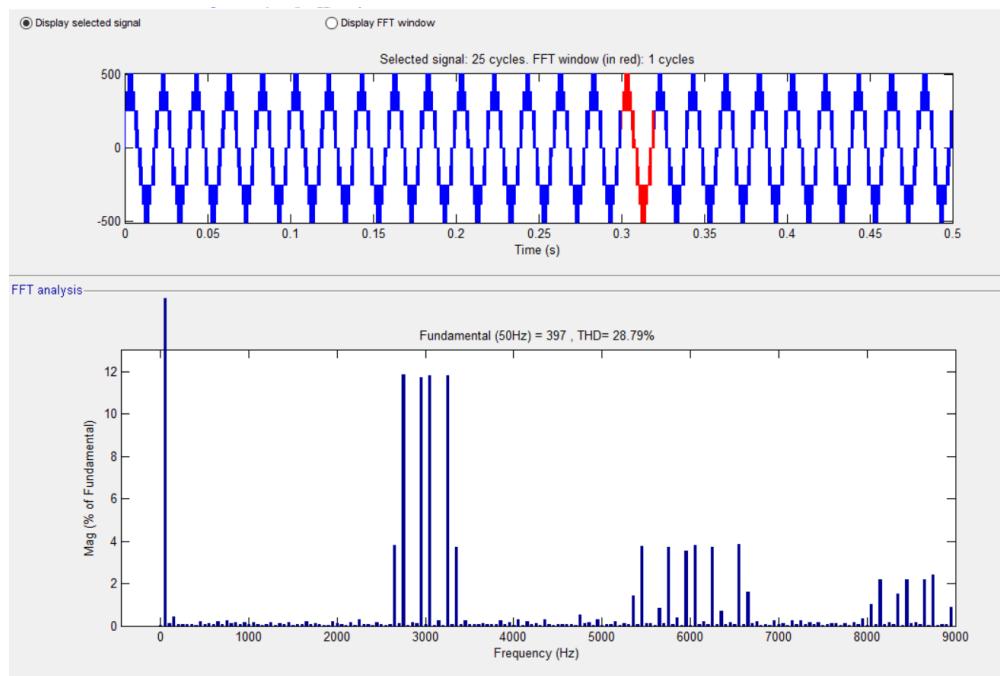
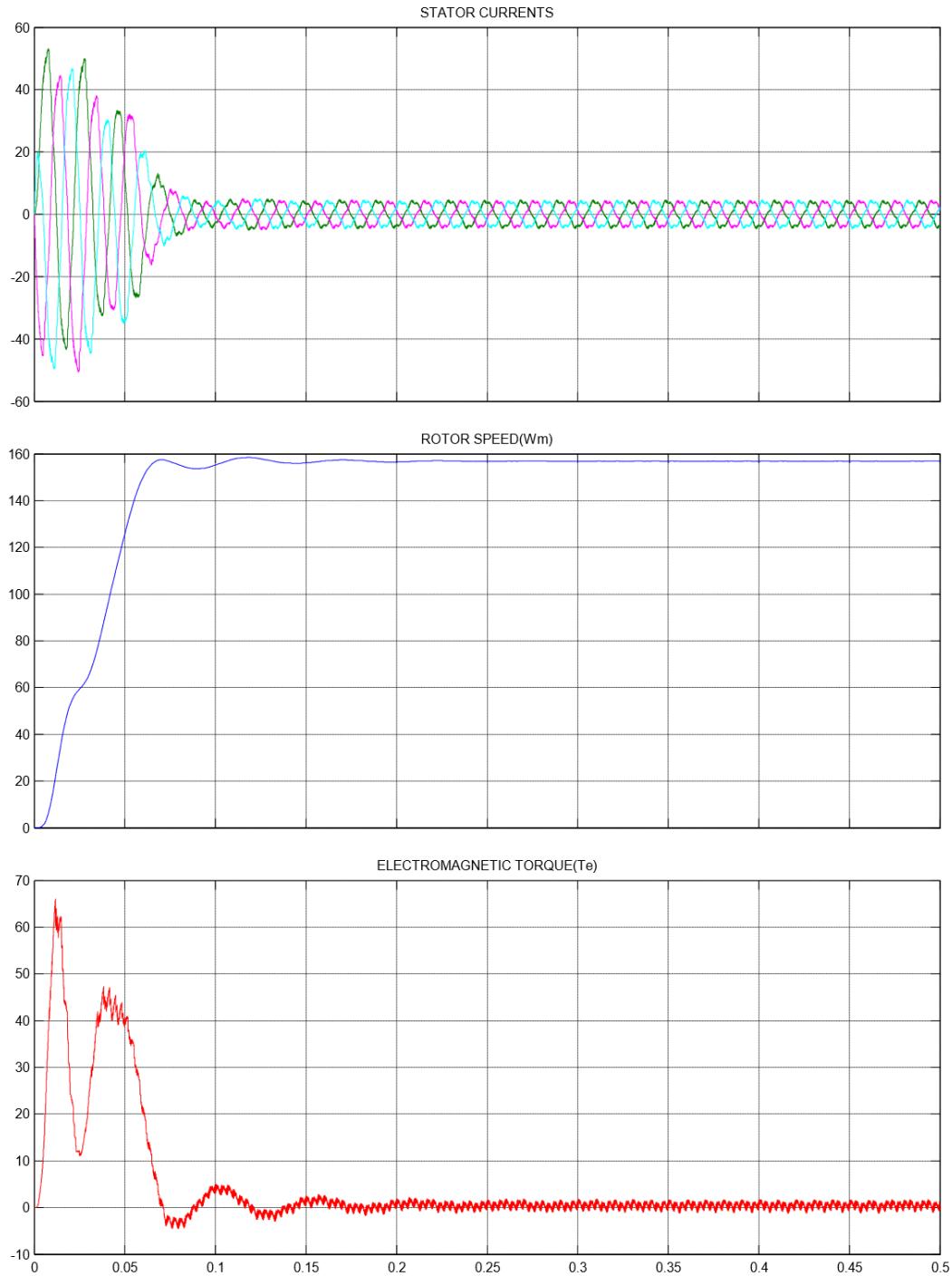


Fig.4.38. FFT Analysis of Five Level Inverter for APODSPWM

## REDUCTION OF COMMON MODE VOLTAGE USING VARIOUS CARRIER BASED PWM TECHNIQUES

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Time offset: 0

Fig.4.39. Five Level Inverter fed Induction Motor Drive results for APODSPWM  
Here, The machine runs at no load condition, So the Electromagnetic Torque ( $T_e$ ) is zero.

**REDUCTION OF COMMON MODE VOLTAGE USING VARIOUS  
CARRIER BASED PWM TECHNIQUES**

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Table 4.2: Results of Five level Inverter

<b>LEVEL</b>	<b>SPWM TECHNIQUE</b>	<b>COMMON MODE VOLTAGE (<math>V_{no}</math>)</b>	<b>THD (%) (Line Voltage)</b>
FIVE	PD	$\frac{V_{DC}}{6}, \frac{V_{DC}}{12}, \frac{-V_{DC}}{12}, \frac{-V_{DC}}{6}$	17.25
	POD	$\frac{V_{DC}}{12}, \frac{-V_{DC}}{12}$	30.03
	APOD	$\frac{V_{DC}}{12}, \frac{-V_{DC}}{12},$	28.82

## CHAPTER 5

### CONCLUSION

Table 5.1: Comparison of results of MLI Topologies

LEVEL	SPWM TECHNIQUE	COMMON MODE VOLTAGE (Vno)	THD (%) LINE VOLTAGE (Vab)
TWO	PD	$0, \frac{V_{DC}}{3}, \frac{2V_{DC}}{3}, V_{DC}$	79.43
THREE	PD	$\frac{V_{DC}}{6}, \frac{V_{DC}}{3}, \frac{2V_{DC}}{3}, \frac{5V_{DC}}{6}$	38.98
	POD	$\frac{V_{DC}}{3}, \frac{2V_{DC}}{3}$	53.53
FOUR	MODE 1	$\frac{23V_{DC}}{102}, \frac{V_{DC}}{3}, \frac{15V_{DC}}{34}, \frac{28V_{DC}}{51}, \frac{2V_{DC}}{3}, \frac{40V_{DC}}{51}$	24.50
	MODE2	$\frac{V_{DC}}{3}, \frac{15V_{DC}}{34}, \frac{28V_{DC}}{51}, \frac{2V_{DC}}{3}$	39.17
	MODE 3	$\frac{23V_{DC}}{102}, \frac{V_{DC}}{3}, \frac{15V_{DC}}{34}, \frac{28V_{DC}}{51}, \frac{2V_{DC}}{3}, \frac{40V_{DC}}{51}$	36.55
	MODE 4	$\frac{V_{DC}}{3}, \frac{15V_{DC}}{34}, \frac{28V_{DC}}{51}, \frac{2V_{DC}}{3}$	39.34
FIVE	PD	$\frac{V_{DC}}{6}, \frac{V_{DC}}{12}, \frac{-V_{DC}}{12}, \frac{-V_{DC}}{6}$	17.25
	POD	$\frac{V_{DC}}{12}, \frac{-V_{DC}}{12}$	30.03
	APOD	$\frac{V_{DC}}{12}, \frac{-V_{DC}}{12}$	28.82

In this project Simulation of Two level, Three level, Four level and Five level Inverter employing different carrier based pulse width modulation techniques such as PD, POD and APOD is implemented. The analysis and variation of Total Harmonic Distortion (THD) and Common Mode Voltage (CMV) of different Multilevel Inverters topologies are plotted and tabulated.

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- <https://microcontrollerslab.com/multilevel-inverters-types-applications/>
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