ABSTRACT

The Project is about the Reduction of Common Mode Voltage (CMV) using various Carrier Based PWM Techniques. Pulse Width Modulation (PWM) inverter has been widely applied to many ac motor drives. It is well known that conventional two-level inverters generate high-frequency common-mode voltages with high dv/dt. To reduce the common mode voltage there is an alternate solution i.e., implementing multilevel inverter employing PWM Technique. Multilevel Inverter offers high power capability, associated with lower output harmonics and lower commutation losses. In this project cascaded multilevel inverter topology is used. Similarly this multilevel inverter also generates common mode voltage. To reduce the common mode voltage Carrier Based PWM Techniques are employed. The simulation of Multilevel Inverter Topologies employing Carrier Based PWM Techniques are carried out in MATLAB Simulink.

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