Asynchronous Counters

1. Asynchronous counters are those whose output is free from the clock signal. Because the flip flops in asynchronous counters are supplied with different clock signals, there may be delay in producing output.

2. The required number of logic gates to design asynchronous counters is very less. So they are simple in design. Another name for Asynchronous counters is “Ripple counters”.

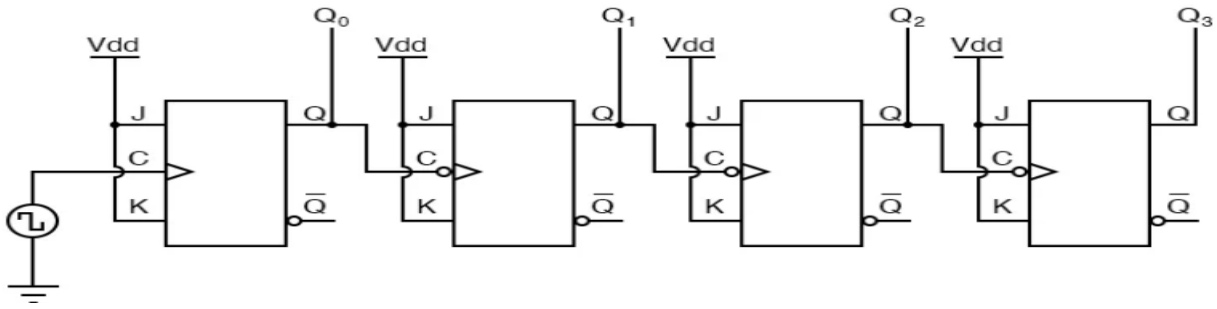
3. The number of flip flops used in a ripple counter is depends up on the number of states of counter (ex: Mod 4, Mod 2 etc). The number of output states of counter is called “Modulus” or “MOD” of the counter. The maximum number of states that a counter can have is 2n where n represents the number of flip flops used in counter

Different types of Asynchronous counters

- N bit synchronous UP counter
- N bit synchronous DOWN counter
- N bit synchronous UP / DOWN counter

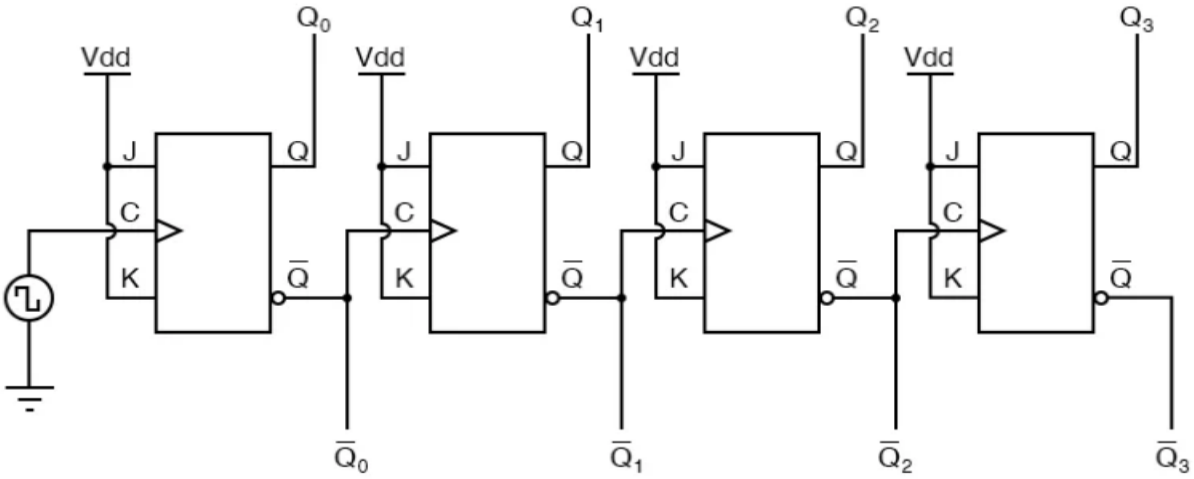
Four-bit “Up” Counter

A four-bit “up” counter

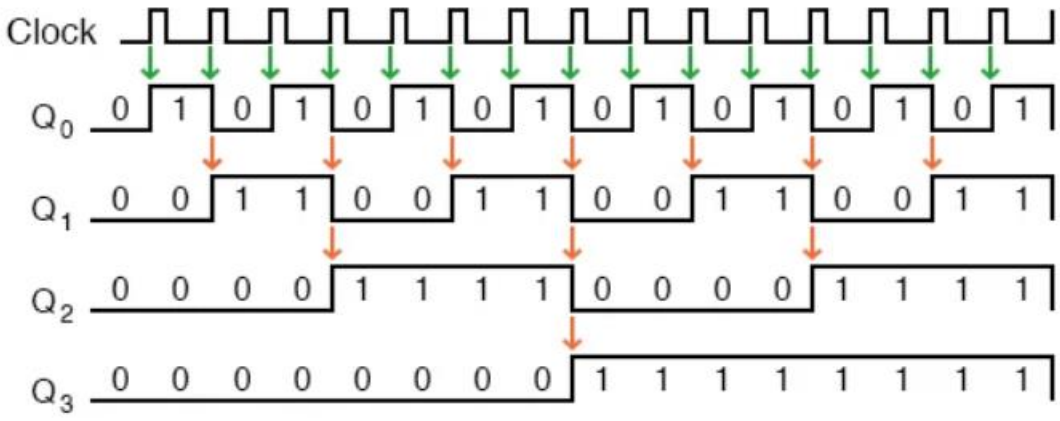


Simultaneous “Up” and “Down” Counter

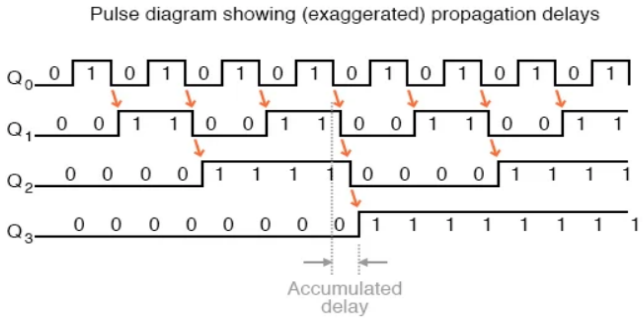
A simultaneous “up” and “down” counter

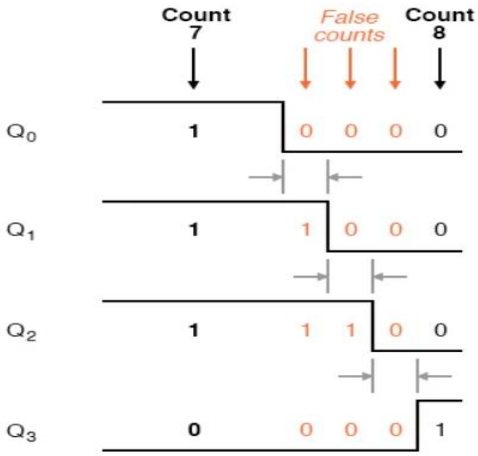


This circuit would yield the following output waveforms, when "clocked" by a repetitive source of pulses from an oscillator:



Disadvantage of Asynchronous Counter Circuit: Propagation Delay





Disadvantage of Asynchronous Counter Circuit: Limited Speed

Another disadvantage of the asynchronous, or ripple, counter circuit is limited speed.

While all gate circuits are limited in terms of maximum signal frequency, the design of asynchronous counter circuits compounds this problem by making propagation delays additive.

Thus, even if strobing is used in the receiving circuit, an asynchronous counter circuit cannot be clocked at any frequency higher than that which allows the greatest possible accumulated propagation delay to elapse well before the next pulse.

The solution to this problem is a counter circuit that avoids ripple altogether.

Such a counter circuit would eliminate the need to design a "strobing" feature into whatever digital circuits use the counter output as an input, and would also enjoy a much greater operating speed than its asynchronous equivalent.

This design of counter circuit is the subject of the next section.

REVIEW:

- An “up” counter may be made by connecting the clock inputs of positive-edge triggered J-K flip-flops to the Q’ outputs of the preceding flip-flops. Another way is to use negative-edge triggered flip-flops, connecting the clock inputs to the Q outputs of the preceding flip-flops. In either case, the J and K inputs of all flip-flops are connected to V_{cc} or V_{dd} so as to always be “high.”

- Counter circuits made from cascaded J-K flip-flops where each clock input receives its pulses from the output of the previous flip-flop invariably exhibit a *ripple effect*, where false output counts are generated between some steps of the count sequence. These types of counter circuits are called *asynchronous counters*, or *ripple counters*.

- *Strobing* is a technique applied to circuits receiving the output of an asynchronous (ripple) counter, so that the false counts generated during the ripple time will have no ill effect. Essentially, the *enable* input of such a circuit is connected to the counter’s clock pulse in such a way that it is enabled only when the counter outputs are not changing, and will be disabled during those periods of changing counter outputs where ripple occurs.

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