AMAN JESWANI

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EDUCATION

TANDON SCHOOL OF ENGINEERING, NEW YORK UNIVERSITY New York, NY
Master of Science in Computer Engineering, GPA: 3.74/4.0 January 2023 - December 2024
Relevant Coursework: Computer Architecture, Embedded Systems, Digital Signal Processing, Advanced Hardware Design, Hardware Security, Analog Circuit Design, Serial Communication Protocols (UART, CAN, Ethernet), Schematic Entry and Simulation, Firmware Debugging

WORK EXPERIENCE

GRADUATE ASSISTANT - STUDENT IMPACT INNOVATION LAB Brooklyn, NY
Tandon School of Engineering, New York University September 2024 – Present
- Contributed to the development of prototypes, collaborating on hardware design, accelerating project timelines by 15%
- Facilitated the creation of innovative solutions in smart agriculture and healthcare, targeting a potential reduction in resource usage by 10% and improved patient care

HEAD GRADUATE COURSE ASSISTANT - REAL TIME EMBEDDED SYSTEMS Brooklyn, NY
Tandon School of Engineering, New York University September 2023 - Present
- Supervised the recruitment, training, and performance of a team of 8 CAs, supporting over 300 graduate and 50 undergraduate students in two embedded systems courses
- Headed interactive recitations and demonstrations on advanced embedded programming topics such as UART, I2C, SPI, and real-time interrupt handling, fostering hands-on learning with the STM32F429I-DISC1 Board and Mbed OS

GRADUATE ASSISTANT - DIGITAL LOGIC AND STATE MACHINE DESIGN Brooklyn, NY
Tandon School of Engineering, New York University September 2023 – December 2023
- Spearheaded lab sessions on Verilog HDL programming for undergraduate students, including grading assignments and projects, fostering their understanding and application of digital design principles

SUMMER INTERN - SoC DESIGN ON FPGA Ahmedabad, GJ
Institute of Technology, Nirma University June 2020 – July 2020
- Modeled custom hardware block designs such as an LED Controller on the ZedBoard with the ZYNQ-7000 SoC
- Created training videos regarding System-On-Chip Design for more than 50 graduate students

UNIVERSITY PROJECTS

PIPELINE IMPLEMENTATION OF MIPS32 PROCESSOR | *Verilog, Digital Logic Design, Simulation* June 2024
- Designed and implemented a 5-stage instruction pipeline in Verilog, achieving a 25% increase in instruction throughput by optimizing instruction flow and reducing hazards
- Produced testbenches to simulate over 50 test cases, validating the functional correctness of pipeline stages and ensuring minimal data hazards and control stalling

VERIFICATION OF AXI BUS PROTOCOL | *SystemVerilog, Functional Coverage, Verification* June 2024
- Developed a SystemVerilog verification environment for the AXI bus protocol, achieving 95% functional coverage across key protocol features to ensure specification compliance
- Implemented modular testbench architecture, improving reusability and reducing test case development time by 20%

PUBLICATIONS

BLIND SCRAMBLING CODE IDENTIFICATION FOR SYNCHRONOUS AND SELF-SYNCHRONOUS SCRAMBLER Spring 2021
Advancement in Communication, Electronics, Computer and Automation Technology *Conference*

TECHNICAL SKILLS, CERTIFICATIONS AND AWARDS

Programming and Hardware Description Languages: C, C++, Python, TCL, SystemVerilog, Verilog HDL, VHDL
Tools and Technologies: VS Code, MATLAB, GitHub, Platform IO, Mbed Studio, FreeRTOS, Linux, Vivado, Quartus Prime, Cadence Virtuoso, ModelSim, LabVIEW, Oscilloscopes, Logic Analyzers, Digital Multimeters
Certifications and Awards: Embedded System Essentials with ARM ESE101 and ESE102 (edX), Hardware Description Languages (Coursera), Smart India Hackathon 2020 (Winner)
FPGA Boards: Xilinx Artix-7 Basys 3, HiFive Rev1 B, ZedBoard ZYNQ-7000