Research of 4T SRAM/SOI Memory Cell Structure at 0.5V Supply Voltage

Abstract

A high-drive current and low-static power four transistor (4T) SOI-SRAM memory cell with 0.5V supply voltage is proposed. This structure adopts Cross-shaped gate、ultra thin self-body-bias (SBB) resistor and Dynamic Threshold MOSFET(DTMOS). The Cross-shaped gate and DTMOS increase the on-state current at low voltage and the latter also reduces the off-state current effectively. Furthermore, the process of SBB resistor is compatible with SOI-CMOS process and the proposed memory cell's performance and process are simulated by MEDICI and T-SUPREM4. Results show that the ultra thin SBB resistor has a 4.3×10^{4} on/off-state current ratio with the shift of gate voltage and its on-state current is comparable to the N type DTMOS. At 0.5V supply voltage, the memory cell's static power dissipation is 1.6×10^{-7}mw and the dynamic power dissipation of writing and reading is respectively 4.4×10^{-3}mw and 3.7×10^{-3}mw.

Keywords: SRAM/SOI; SBB; Cross-shaped gate; DTMOS; on/off-state current ratio

1. Introduction

SOI technology can enhance the SRAM cell's performance and compress the cell area, because SOI has low power dissipation, low noise, high resistance to radiation, no latch-up effect and high density integration [1]-[3].

In order to reduce power dissipation and layout area, classic 6T SRAM cells are always improved into 4T cells by SOI technology [4]. However, with low supply voltage, most of 4T cells have some instable problems [5]-[9] or complicated process [10]-[12]. In this paper, a high-drive current and low-static power 4T SRAM cell based on the three-dimensional structure of Cross-shaped gate、ultra thin SBB resistor [13] and DTMOS [14]-[15] with 0.5V supply voltage is presented, as show in Fig.1. This structure's simulation and analysis are carried out with MEDICI and T-SUPREM4.

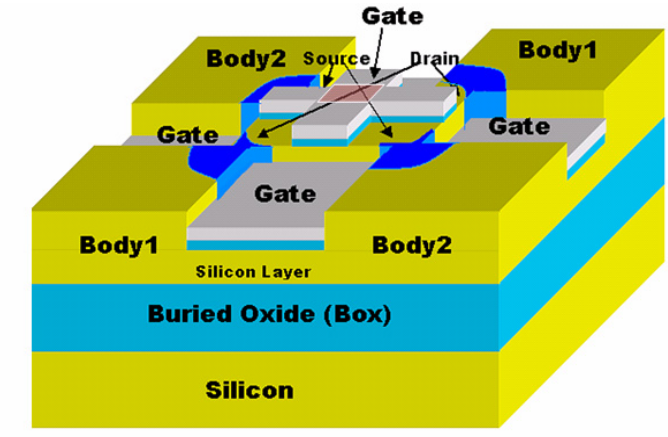

Fig.1 Three-dimensional structure of Cross-shaped gate、ultra thin SBB resistor and DTMOS

2. Basic structure and mechanism

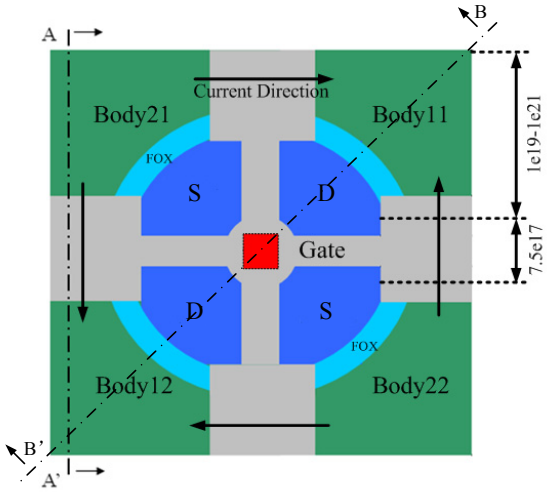

Fig.2 The plan view of the three-dimensional structure

Fig.2 shows the plan view of SBB and DTMOS with a Cross-shaped gate electrode. In order to increase on-state current and save the area of cell, the center area of structure has two drain and two source electrodes to form four N-MOSFETs equivalent to a big N-MOSFET and the circumference has two body1 and two body2 electrodes to form four SBB resistors equivalent to a big P-MOSFET. An isolation cirque isolates N-MOSFETs and SBB resistors; Fig.3 shows the size of cross-section view of ultra thin SBB modified the plane marked AA' in Fig.2. A ladder groove is under the gate.

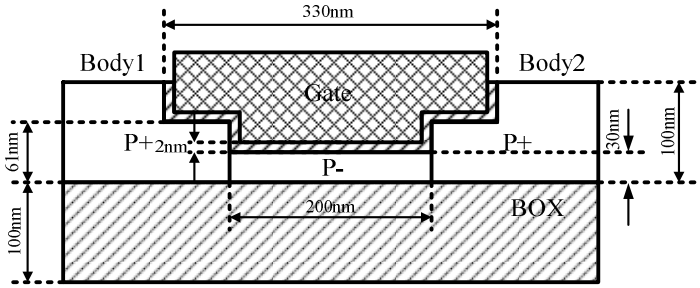

Fig.3 The size of cross-section view of ultra thin SBB

The body resistor P- is beneath the gate from terminal Body1 to terminal Body2. When a high gate voltage is applied, the P- area is absolutely depleted, so greatly enhancing the resistance and shutting down the current between Body1 and Body2 [16], as shown in Fig.4.

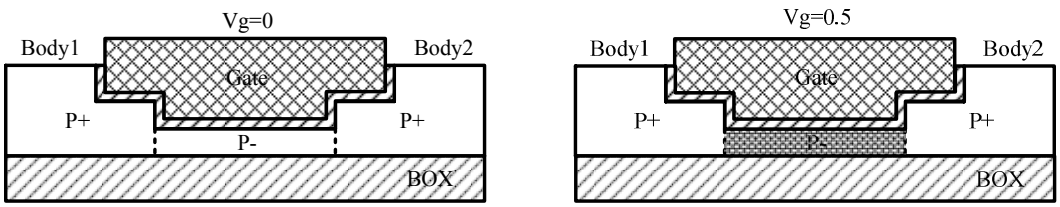

Fig.4 Operation of the SBB resistor

In the circuit of whole SRAM cell, all of NMOS are DTMOS. DTMOS has not SOI Floating body effect and its on-state threshold voltage is low and off-state threshold voltage is high, because its body voltage is tied to the gate voltage. Especially, as show in Fig.1 and Fig.2, at the center of gate, there is a body contact of DTMOS, its cross-section view modified the plane marked BB' in Fig.2 is shown in Fig 5. At 0.5V supply voltage, the performance of DTMOS is stable and effective.

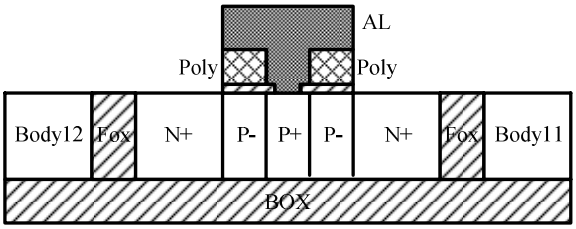

Fig.5 Cross-section view of body contact of DTMOS

3. Design of ultra thin SBB resistor

The parameters of ultra thin SBB resistor are designed and simulated by MEDICI and T-SUPREM4. Fig.6 shows the dependence of the current through the resistor on Vg for various P- film thicknesses. B concentration of P- area is $7.5\times10^{17}/cm^3$. B concentration of P+ area is $1\times10^{19}/cm^3$～$1\times10^{21}/cm^3$. When P- film thickness is 40-60nm, SBB resistor can't shut down the current and When P- film thickness is 20nm, the on-state current is so small. According to the tradeoff between on -state current and off-state current, 30nm is suitable.

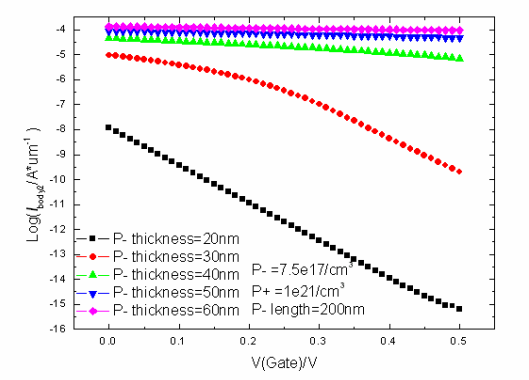

Fig.6 I_{body2} versus Vg for various P- film thicknesses

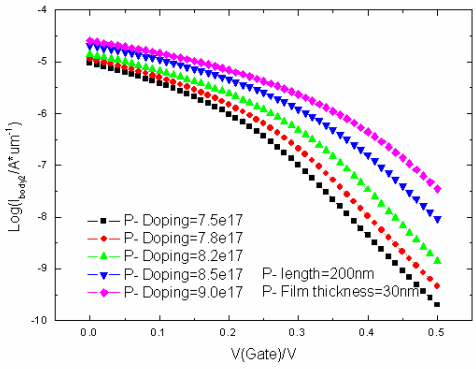

Fig.7 I_{body2} versus Vg for various P- doping

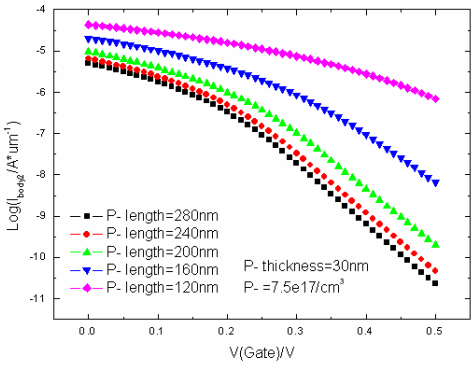

Fig.8 I_{body2} versus Vg for various P- lengths

Fig.7 shows the dependence of the current through the resistor on Vg for various P- doping. It is evident that the off-state current changes much faster than the on-state current with the variation of P- doping. In order to maintain the low static power dissipation of 4T SRAM cell, $7.5\times10^{17}/cm^3$ is suitable.

Fig.8 shows the dependence of the current through the resistor on Vg for various P- lengths. When P- length is 120-160nm, the SBB resistor can not shut down the current and when P- length is 240-280nm, the on-state current is not enough big. Choosing the 200nm is suitable.

Basic parameters is designed by MEDICI, the following step is the simulation of process. The steps of process simulation by T-SUPREM4 are shown in Fig.9.

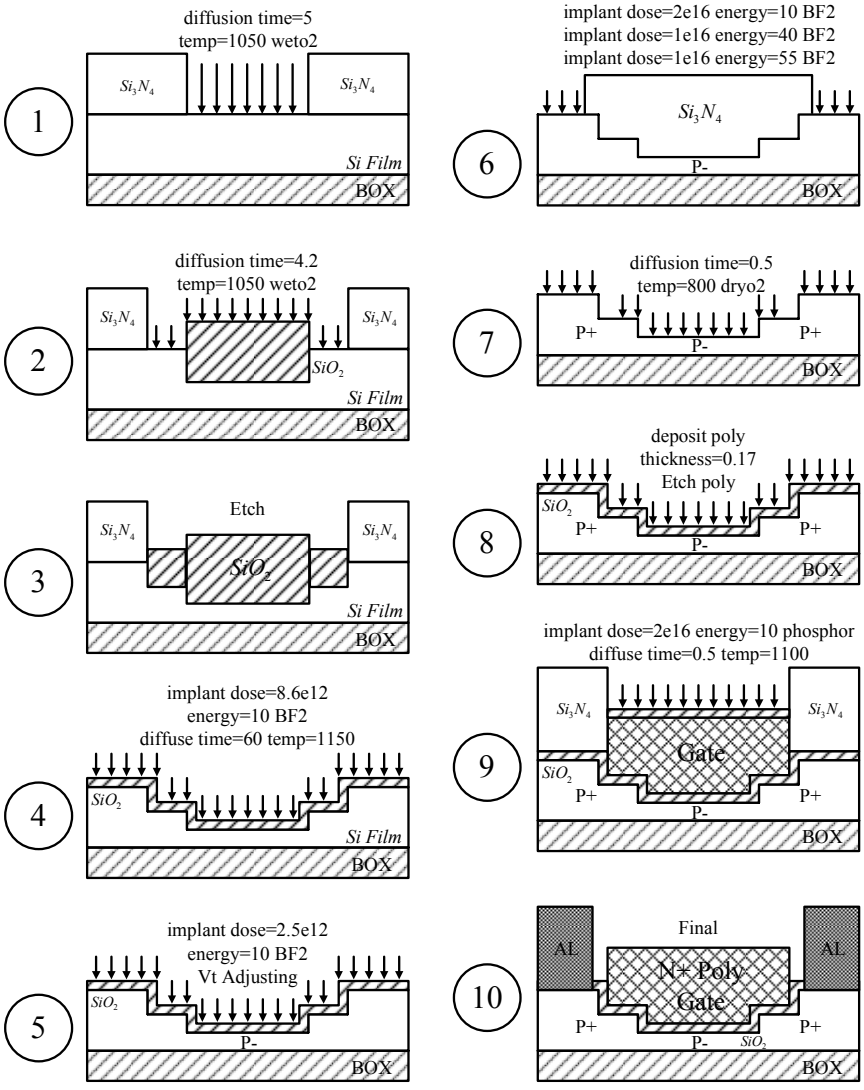

Fig.9 Steps of process simulation of ultra thin SBB resistor

According to the steps, the ladder groove is made by twice thermal oxidation of wet O_2. The thickness of ladder is another factor for further improvement, as shown in Fig.10.

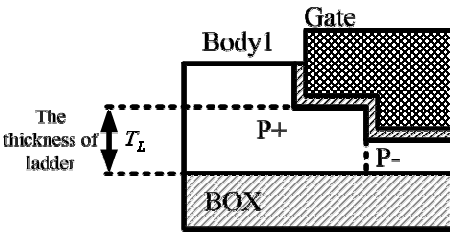

Fig.10 Define of the thickness of ladder

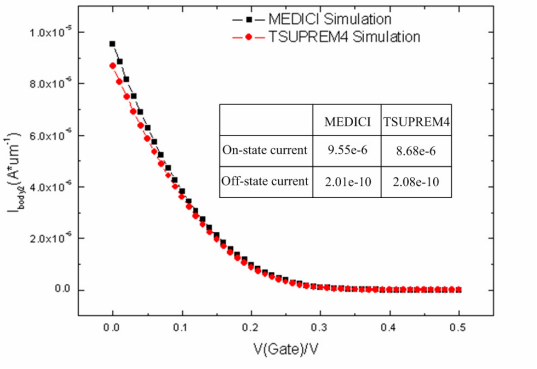

Fig.11 Simulation results of MEDICI and T-SUPREM4

Table.1 The influence of various T_L on the on/off current (by T-SUPREM4)

Time of twice thermal oxidation (min)	T_{OX} (nm)	T_L (nm)	On/off-state current (A/um)
2/7.7	29.9-30.1	43	$8.6\times10^{-6}/4.0\times10^{-10}$
3/6.4	29.2-30.1	49	$8.6\times10^{-6}/2.6\times10^{-10}$
4/5.2	29.7-30.3	53	$8.3\times10^{-6}/1.9\times10^{-10}$
5/4.2	29.8-30.1	61	$8.7\times10^{-6}/2.1\times10^{-10}$
6/3.2	29.3-30.4	69	$8.2\times10^{-6}/3.6\times10^{-10}$

If T_L is much thick, the off-current will become big and if T_L is much thin, the on-state current will become small. After adjusting the doping for various T_L, the optimized results of on/off currents are shown in Table.1. According to the tradeoff between on -state current and off-state current, 61nm is suitable.

In conclusion, the size parameters of SBB resistor are shown in Fig.3. Its performance of process simulation by T-SUPREM4 is little different from the performance of ideal device simulation by MEDICI, as show in Fig.11. Its on-state current closed to 10uA is comparable to N type DTMOS and its off-state current is enough small to maintain the low static power dissipation.

4. Global performance of 4T SRAM cell

The circuit of 4T SRAM cell is shown in Fig.12 and the channel length of DTMOS is 0.13um.

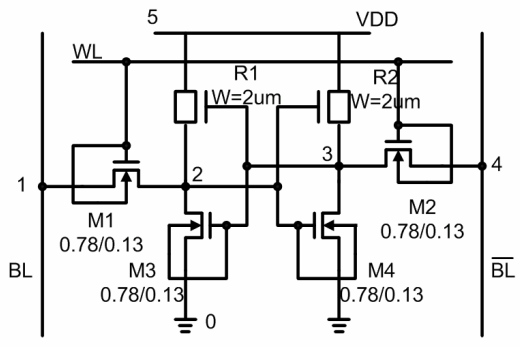

Fig.12 Proposed 4T SRAM cell circuit

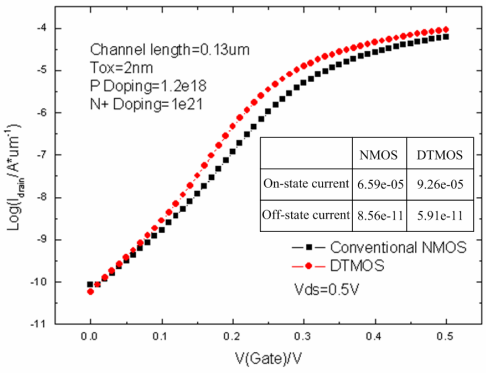

Fig.13 Performance simulation of DTMOS

In the circuit, DTMOS device is simulated by MEDICI. Comparing with conventional NMOS, its on-state current is 1.4 times bigger and its off-state current is 1.45 times smaller with 0.5V supply voltage, as shown in Fig.13.

The transfer characteristics of cell described in Fig.14 prove that the 4T SRAM cell functions stably and its static noise margin is about 200mv at 0.5V supply voltage. But the point of intersection of transfer curves is not at 0.25V, because the current of SBB resistor is a little smaller than the current of DTMOS.

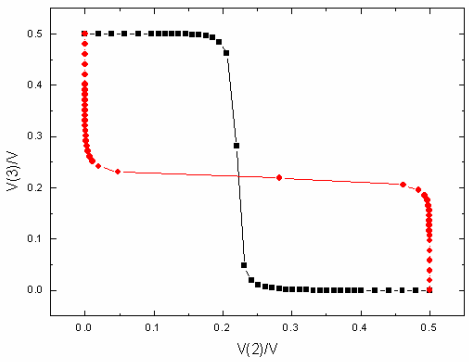

Fig.14 Transfer curve of the 4T SRAM cell

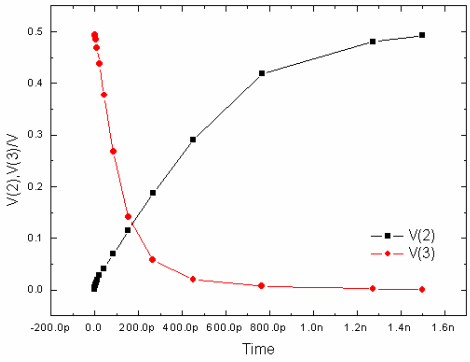

Fig.15 Transient voltage of 4T SRAM's writing mode

In order to measure the writing delay, BL is short to VDD and $\overline{BL}$ is short to GND. The initial voltage of node (2) is 0V and node (3) is 0.5V. Fig.15 shows the writing delay of node (2) and node (3) in the circuit. According the transient transfer curve of writing state, the 50%-50% delay of node (2) is about 100ps and node (3) is about 400ps.

In order to measure the reading time, BL is connected with a NMOS (13/0.13) which is equivalent the capacitance of BL [17], as shown in Fig.16. Fig.17 shows the reading time of the 4T SRAM cell. According the transient transfer curve of reading state, the reading time of 0.5V-0.1V is about 330ps.

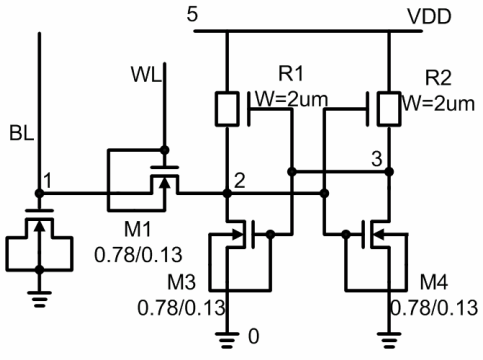

Fig.16 Testing circuit of Reading state

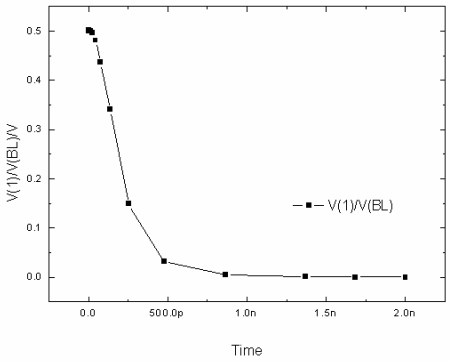

Fig.17 Transient voltage of 4T SRAM's reading mode

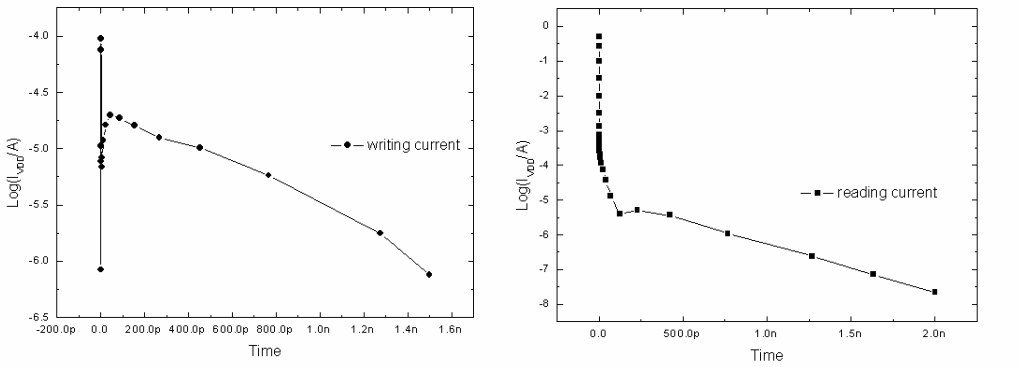

Fig.18 Transient current of 4T SRAM

Fig.18 shows the transient current of 4T SRAM. The total currents of writing and reading are integrated in 1.5ns of simulation time with a result of 13*fA·S* and 11*fA·S*. So the power dissipations of writing and reading are 4.4×10^{-3}mw and 3.7×10^{-3}mw at 0.5V supply voltage, which is much smaller than the conventional 6T SRAM cell [17]. Finally the static current though the VDD is about 3.3×10^{-7}mA, thus the static power dissipation is about1.6×10^{-7}mw.

5. Layout of 4T SRAM cell

The layout of 4T SRAM cell is shown in Fig.20. The width of isolation cirque is 0.13um and the area of body contact of DTMOS is $0.13\times0.13\text{um}^2$. According to the size as shown in Fig.12, the width of single SBB resistor is 0.5um and the width of single DTMOS is 0.195um. In order to reduce the cell area, four corners of the square are cut, as shown in Fig.19, thus the area of a single inverter is just 2.5 um^2.

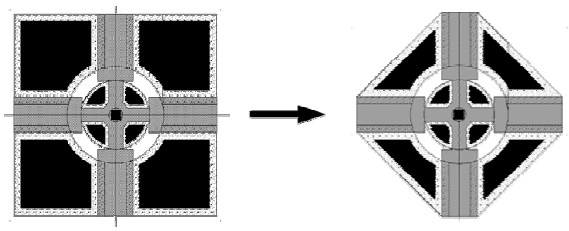

Fig.19 Improvement of a single inverter

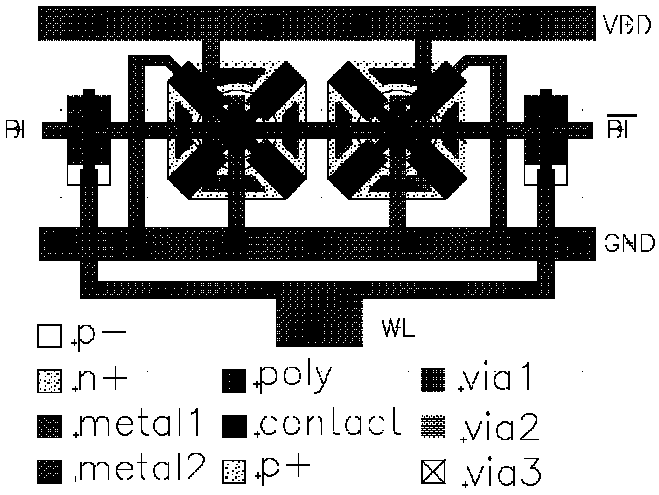

Fig.20 Layout of the proposed 4T SRAM cell

6. Conclusion

A high-drive current 4T SRAM structure with 0.5V supply voltage is proposed. Using the Cross-shaped gate, the area of the structure doesn't add a lot with the increasing of the drive current. Furthermore, the ultra thin SBB resistor and DTMOS have a low off-state current, so the structure has much low static power dissipation.

The ultra thin SBB resistor is the key of the device performance. Thus, the optimizing of p- area is illustrated including thickness modification, impurity concentration adjustment and length alteration. Eventually, the resistor has a 4.3×10^4 on/off current ratio with the shifting of gate voltage, and its on-state current is comparable to DTMOS.

The transfer speed and power dissipation of the proposed 4T SRAM cell are also simulated. The results show that the memory cell's static power dissipation is 1.6×10^{-7}mw and the dynamic power dissipation of writing and reading is respectively 4.4×10^{-3}mw and 3.7×10^{-3}mw at 0.5V supply voltage. Because of 0.5V supply voltage, the speed is a little slower than conventional 6T SRAM, but the area and the power dissipation are much smaller than conventional 6T SRAM cell [17].

In a word, the novel structure of 4T SRAM cell proposed in this paper increases the drive current、save the area、improves the on/off-state current ratio of SBB resistor and reduces the static power dissipation, which is suitable for low-voltage and low-power IC development needs. With the development of process technology, the layout structure and process technology of cell still have a big potential for further in-depth research.

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