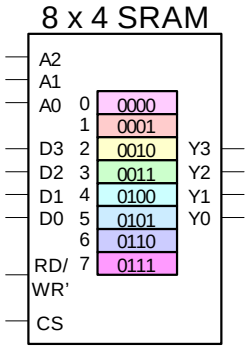
SRAM Arrays



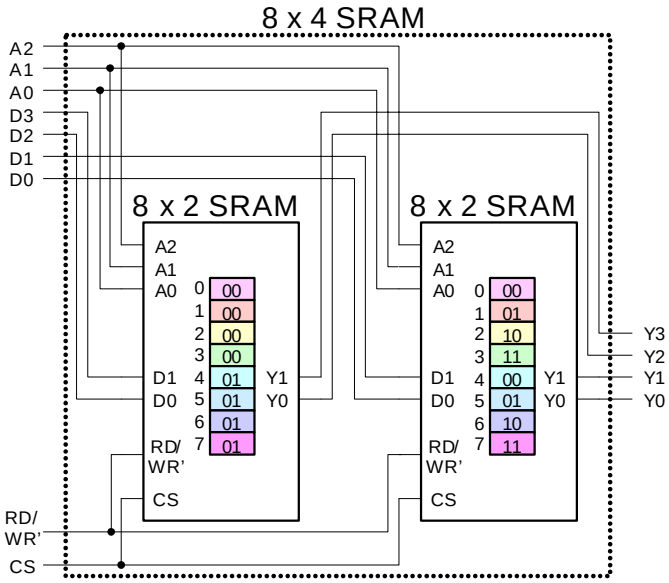
Larger SRAM arrays can be constructed from smaller ones. For this example, we want to build an 8x4 SRAM array. The external interface of the array should be as if it were a single SRAM structure, as shown at right.

To see where different parts of the data are stored for each design, values are given inside the RAM structures for each address location (address at right in decimal, binary data at right in the colored boxes). All designs of the 8x4 SRAM hold the same 4-bit data at the same 3-bit address locations.

Building Wider SRAMS

We can use multiple SRAMs to make a wider device. The data inputs/outputs are split between the SRAM components. The address, chip select, and RD/WR' signals are the same for all devices.

Each device contains a subset of the bit positions for all of the memory's words.



Building SRAMs w/More Words

We can use multiple SRAMs to make a device with more row locations. The input data lines, RD/WR' signal, and lower address bits are the same for all chips. The upper address bits and the CS input generate the individual chip selects.

Each device contains all bits (full width) of a subset of the memory's words.

NOTE: The SRAM outputs can only be directly connected like this if individual chip outputs are High-Z when that chip's CS input is low. Otherwise, multiplexers would have to choose between different chip outputs for each bit position to avoid contention.