Sensing Margin Enhancement Techniques for Ultra-Low-Voltage SRAMs Utilizing a Bitline-Boosting Current and Equalized Bitline Leakage

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***Abstract*—A small bitline sensing margin is one of the most challenging design obstacles for reliable ultra-low-voltage static random access memory (SRAM) implementation. This paper presents design techniques for bitline sensing margin enhancement using decoupled SRAMs. The proposed bitline-boosting current scheme improves the bitline sensing margin at a given bitline configuration. The bitline sensing margin can be further augmented by equalizing bitline leakage. Simulation using a 40-nm CMOS process shows that the proposed techniques achieve larger bitline sensing margin, wider operating temperature and supply range, and a larger number of cells per bitline.**

***Index Terms*—Bitline sensing, equalized bitline leakage, MTCMOS, static random access memory (SRAM).**

I. Introduction

ULTRA-LOW-power circuits are becoming increasingly popular in many green computing systems where subthreshold or near-threshold operation has been desirable with a moderation in performance [1]. However, ultra-low-voltage operation generates various challenging issues such as a small noise margin, large device variations, etc. While digital logic circuits can be implemented with acceptable operation reliability, the design of ultra-low-voltage static random access memory (SRAMs) is extremely challenging due to additional design parameters including cell stability, sensing margin, write margin, and leakage current. Various circuit techniques have been presented to address the above challenges. One of the most significant changes made for ultra-low-voltage SRAM design is the employment of decoupled SRAM cells with additional devices [2]–[4]. Decoupled SRAM cells improve cell stability by isolating the SRAM cell nodes from the read bitlines (RBLs) during read operation. The write margin has been improved by utilizing a collapsed cell supply [2], and boosted wordline voltage schemes [2]. Boosted wordline voltage schemes and negative bitlines augment the strength of write access devices, while a collapsed cell supply weakens the cross-coupled latches. To tackle a small sensing margin, sense amplifier redundancy and data-independent bitline leakage have been explored. Finally, leakage-reduction techniques have been explored since the leakage power is significant in ultra-low-power SRAMs [3].

In this paper, we present design techniques that can enhance the bitline sensing margin at a given structure. The novel techniques are 1) utilizing an optimal device available in the MTCMOS technology for better bitline voltage swing, 2) equalizing bitline leakage, and 3) utilizing the boosting current to maximize the bitline sensing margin at a given bitline structure.

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II. Bitline Sensing Challenges in Conventional Ultra-Low-Voltage SRAMs

Decoupled 8T SRAM cells have been widely accepted in ultra-low-power and low-voltage SRAMs due to the significantly improved stability. The 8T SRAM cell comprises a typical 6T SRAM cell for writing and storing data and a dedicated read port for disturbance-free read operation. Read operation is enabled by activating a read wordline and RBLs are conditionally discharged in accordance with the accessed cell data. The bitline sensing is conducted by differentiating the RBL discharging speed of data "0" from that of data "1." However, following the aggressive device scaling trend as well as the ultra-low-voltage operation requirement, the amount of the RBL leakage becomes considerable compared to the cell read current.

The RBL discharging is determined by the combination of the cell read current and the RBL leakage current. RBL is always discharged since both the cell read current and the RBL leakage are pulling down. RBL always shows a positive sensing margin when the amount of RBL leakage is fixed. However, when comparing the RBL level of data "0" with minimum RBL leakage with that of data "1" with maximum RBL leakage, the RBL level of data "1" can be lower than that of data "0." This makes the RBL sensing through a single reference level impossible. Therefore, a leakage-aware bitline structure design is highly required.

III. RBL Sensing Margin Enhancement Techniques

A. Effect of MTCMOS Technology on RBL Sensing

The RBL sensing margin is primarily determined by the I_{on}-to-I_{off} ratio of an SRAM cell. In MTCMOS technology, various

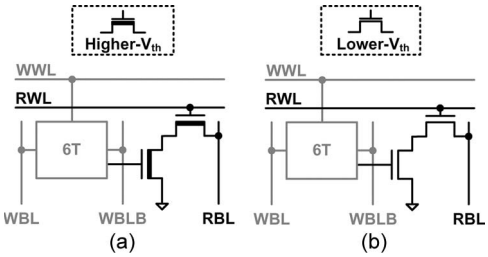


Fig. 1. Schematic of decoupled 8T SRAM cells with four different read port configurations using MTCMOS technology: (a) HVT-HVT, (b) LVT-LVT. Note that HVT and LVT represent higher$V_{\rm th}$ devices and lower$V_{\rm th}$ devices.

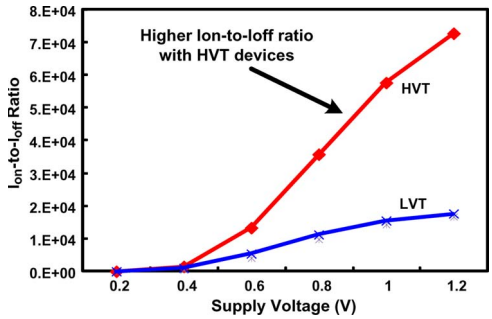


Fig. 2. Simulated $I_{\rm on}$-to-$I_{\rm off}$ ratio of four different read ports shown in Fig. 1.

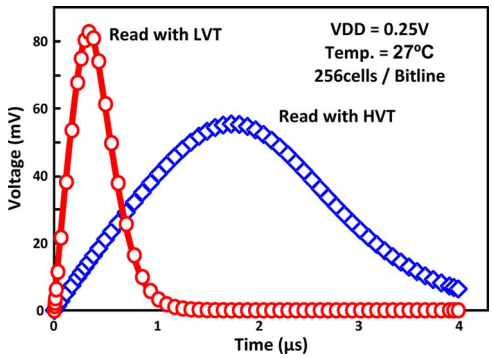


Fig. 3. Simulated RBL swing of the SRAM cells in Fig. 1.

devices with different threshold voltages are available, and each device type shows a different $I_{\rm on}$-to-$I_{\rm off}$ ratio.

Therefore, an optimal device can be chosen by investigating the characteristics of each device. Fig. 1 shows two different read port configurations (HVT and LVT) to be analyzed in this work. The simulated $I_{\rm on}$-to-$I_{\rm off}$ ratios of the two configurations are illustrated in Fig. 2. At the higher supply region, HVT shows better $I_{\rm on}$-to-$I_{\rm off}$ ratios while the difference becomes less prominent at the near- or sub-threshold region. Fig. 3 demonstrates RBL swings of the SRAM cells in Fig. 1. LVT shows a larger RBL swing but has a narrower RBL sensing window. This is due to the exponentially increased leakage current and sub-threshold current at LVT. Since no device simultaneously produces a larger bitline swing and a wider sensing margin, careful tradeoffs in device selection, operation temperature, and the number of cells per bitline have to be considered at the design stage.

B. Boosting Current for the Maximizing RBL Sensing Margin

To realize reliable RBL sensing, it is desirable to provide both a larger RBL swing and a wider sensing window. In this

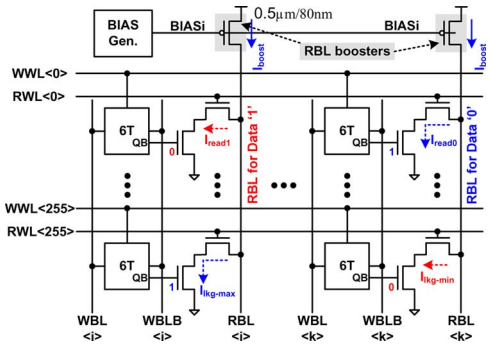


Fig. 4. Proposed bitline-boosting current scheme for enhancing the RBL sensing margin.

paper, we propose a novel bitline-boosting current scheme to achieve this goal.

Fig. 4 illustrates the proposed boosting current scheme employed in the sample bitlines. The basic read/write operation is the same as the conventional 8T SRAM. The main difference is to eliminate precharge operation and provide boosting current for RBL during read operation. This can be realized by turning on strength-controlled devices (RBL boosters). During the read operation, the RBL boosters are activated supplying a pull-up boosting current to RBL. The RBL level for data "1" is formed at the level where the pull-up boosting current $(I_{\rm boost})$ is balanced with the summation of the cell read current and the RBL leakage. This prevents RBL from being fully discharged down to GND by the pull-down leakage current, which expands the RBL sensing window. Compared to the conventional read operation where RBL is always pulled down, forming a narrow RBL sensing window, the proposed scheme enables RBL to be sensed at any time after the RBL setup. This scheme is different from [5] whereby each individual BL leakage is measured separately. Although the scheme in [5] gives a more accurate compensation to each BL, it significantly affects the performance as the leakage current must be measured each cycle. Furthermore, its area overhead is much larger. In our design, $V_{\rm bias}$ is applied to only boosting PMOSs and there is no precharge. Thus, both area and performance efficiency are improved.

Fig. 5 compares the proposed boosting scheme with the conventional RBL. As expected, the proposed RBL boosting scheme shows a larger bitline swing and a wider sensing window. However, at high temperatures [Fig. 5(b) and (d)] where the data-dependent bitline leakage is larger than the cell read current, the proposed bitline-boosting scheme also fails. This indicates that the data-dependent bitline leakage should always be maintained to be smaller than the cell read current by constraining the operating temperature, supply voltage, number of cells per bitline, etc. To overcome this limitation, we propose an SRAM cell with equalized bitline leakage, which will be discussed in the following section.

C. Effect of Equalized Bitline Leakage on the RBL Sensing Margin

The principle of bitline equalization is illustrated in Fig. 6. In conventional SRAMs, the worst case RBL of data "0" is determined by the pull-down current of "$I_{\rm cell} + I_{\rm leak\_min}$" while the worst case RBL of data "1" is the amount of the bitline leakage is governed by "$I_{\rm leak\_max}$." When "$I_{\rm cell} + I_{\rm leak\_min}$" is larger

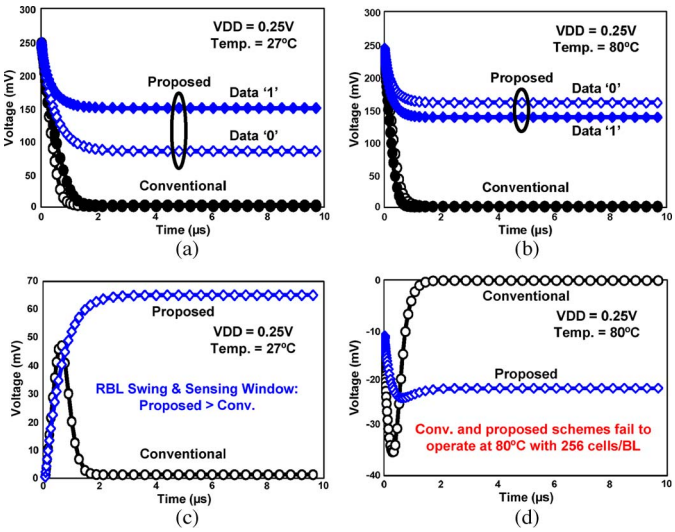


Fig. 5. Simulated RBL waveforms show a sensing margin improvement of the proposed boosting scheme. (a) RBL levels of data "1" and data "0" at room temperature, (b) RBL levels of data "1" and data "0" at high temperature, (c) RBL swing [V(RBL of data "1")—V(RBL of data "0")] at room temperature, and (c) RBL swing [V(RBL of data "1")—V(RBL of data "0")] at high temperature. Note that 256 cells are used in each column.

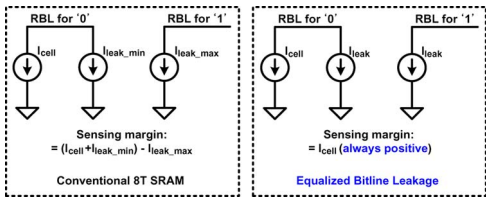


Fig. 6. Principle of the equalized bitline.

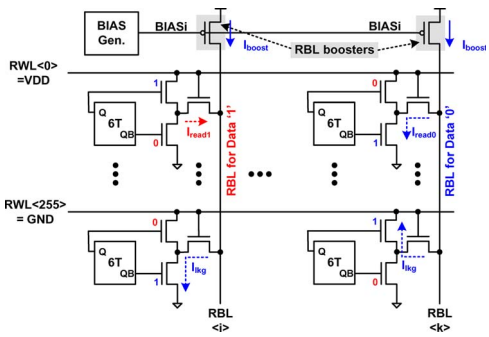


Fig. 7. Proposed boosting current scheme combined with equalized bitline leakage for enhancing the RBL sensing margin.

than "$I_{\mathrm{leak\_max}}$," RBL can be correctly sensed. Otherwise, read failure occurs as explained in Fig. 5(b) and (d). However, in the equalized bitline leakage scheme, the amount of the bitline leakage is constant, consequently providing positive sensing margins regardless of the number of cells per bitline and the data pattern stored in a column. Fig. 7 shows a simplified schematic of the 9T SRAM cell with equalized bitline leakage and the bitline-boosting current scheme. In unselected rows, one of two NMOS devices connected to cell storage nodes (Q and QB) is always on, equalizing the amount of the leakage. It is similar to that in [6] but we use that for a decoupled single-ended cell. Furthermore, it does not affect the RBL parasitic capacitance and thus has more advantages when compared to that in [6]. Since the equalized bitline leakage generates

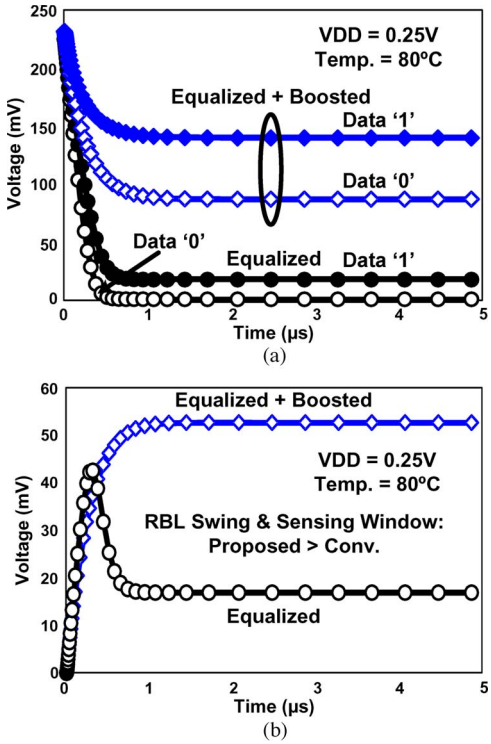


Fig. 8. Simulated equalized RBL waveforms and RBL swing before and after employing the proposed boosting current scheme to the equalized bitline scheme. (a) RBL levels of data "1" and data "0" at high temperature and (b) the corresponding RBL swings.

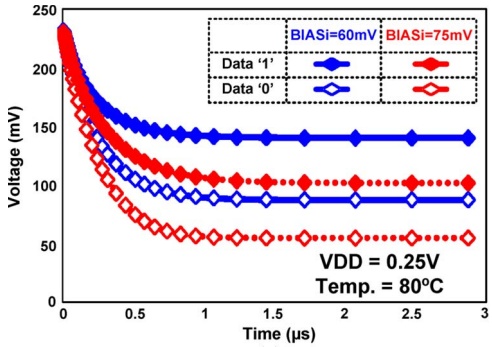
positive sensing margins, the bitline-boosting current scheme will always increase the sensing margin further.

Fig. 8 demonstrates the boosting effect of the proposed techniques with equalized bitline leakage. While the leakage equalization offers a static bitline swing of 20 mV at 80 °C with 256 cells per column, the boosting scheme improves the bitline swing over 50 mV. Note that the conventional 8T SRAM design fails at the same operating condition.

Even though the static RBL level improves the sensing window substantially, the RBL swing should also be large enough to be reliably sensed. To accomplish this, the strength of the RBL boosters needs to be carefully controlled. For example, if the RBL boosters are too strong, it prevents RBL from being discharged when reading data "0." On the other hand, if they are too weak, they will fail to raise RBL up to the level of data "1" due to the substantial pull-down RBL leakage when reading data "1." As shown in Fig. 4, the worst RBL level for data "1" occurs when the RBL leakage is at the maximum. Similarly, the worst case RBL level for data "0" is found when the RBL leakage is at the minimum. The strength of the RBL boosters should be positioned so that it can maximize the bitline voltage difference between the RBL of data "1" and that of data "0." Fig. 9 illustrates the impact of using different biasing voltage for the same array at the same operating condition. It can be seen that a different biasing voltage generates different RBL voltage levels and swings. Thus, a PVT-tracking bias generator should be implemented to maximize the boosting effect.

D. PVT-Tracking Bias Generation Scheme

The generator must ensure that V_{bias} is high enough so that I_{cell} can discharge RBL to ground while it is low enough to fight



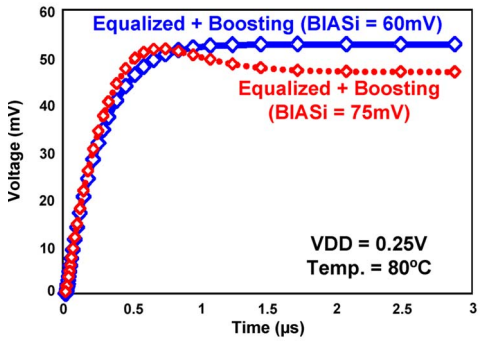


Fig. 9. Simulated equalized RBL waveforms and RBL swing with different biasing voltages for the booster devices. (a) RBL levels of data "1" and data "0" at high temperature and (b) the corresponding RBL swings.

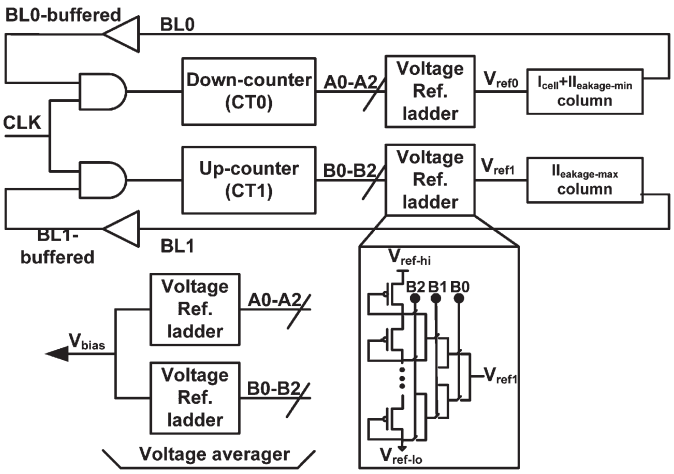


Fig. 10. Simplified schematic of the proposed PVT-tracking biasing generator.

against the maximum leakage current. Fig. 10 shows the simplified schematic of our proposed bias-generation scheme. It consists of two hard wired dummy columns, four voltage reference ladder, and two counters. The first dummy column represents the worst-case read zero (i.e., $I_{\mathrm{RBL}} = I_{\mathrm{cell}} + I_{\mathrm{leakage-min}}$), while the other represents the worst-case read one.

Initially, the down-counter (CT0) is at maximum, thus V_{ref0} is at V_{DD} and V_{RBL0} is at ground. As the CT0 counts, V_{ref0} steps down and I_{boost0} increases. This process continues until $V_{\mathrm{BL0-buffered}}$ turns high. This defines the minimum allowable value of V_{bias}. It also blocks the clock to CT0 and locks the output bits (A0–A2). Similarly, the bottom loop tracks the maximum allowable value of V_{bias} by using an Up-counter. The locked values of A0–A2 and B0–B2 are fed to two additional reference ladder to generate the final V_{bias} whose value is $(V_{ref0} + V_{ref1})/2$. The area overhead of this circuit is less than 5% (including the dummy column).

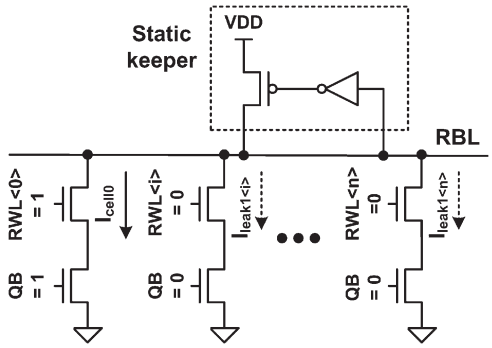


Fig. 11. Simplified schematic of the conventional static keeper for improving bitline swing [6].

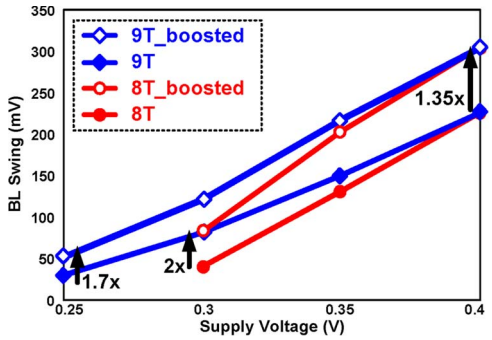


Fig. 12. Simulated RBL voltage swing at different operating supply voltages. All simulations were performed at 256 cells per column, 80 °C.

Compared to the conventional static BL keeper (Fig. 11), our proposed scheme is much more robust against PVT variation as it uses two worst-case scenarios to track the allowable boundaries. Furthermore, one can see that the conventional design is a special case of our proposed scheme when V_{bias} is fixed to ground at the initial state. Another advantage of our design is that the counters (and thus V_{bias}) can be reset and tuned again if the operating condition changes abruptly.

IV. Simulation Results and Remarks

In this section, we present comprehensive simulation results for validating the robustness of the proposed RBL-boosting scheme and the bitline leakage equalization scheme. Two SRAM arrays similar to those in Figs. 4 and 7 were used in our simulations (one for the 8T cell and the other for the 9T cell). Each RBL column has N SRAM cells ($N = 32, 64, 128, 256$). The data patterns of columns are based on the worst and best cases. Parametric variations in supply voltage, biasing voltage, temperature, number of cells per column, and process corners will be evaluated and compared between the four schemes in consideration (8T, 9T, 8T_boosted, and 9T_boosted).

Fig. 12 compares the RBL swing during the read operation of the four designs in consideration at different supply voltages. At high-voltage operating points (e.g., 0.4 V), applying the boosting current improves the RBL voltage swing by only 35% for both 8T and 9T designs. However, when supply voltage scales down, this improvement increases significantly, as also shown in Fig. 12. It is also worth noting that the 8T designs

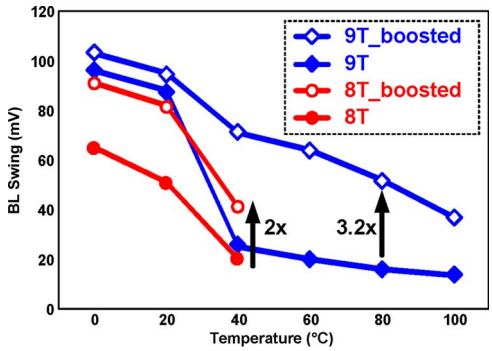


Fig. 13. Simulated RBL voltage swing at different temperature. All simulations were performed at 256 cells per column, 0.25-V supply.

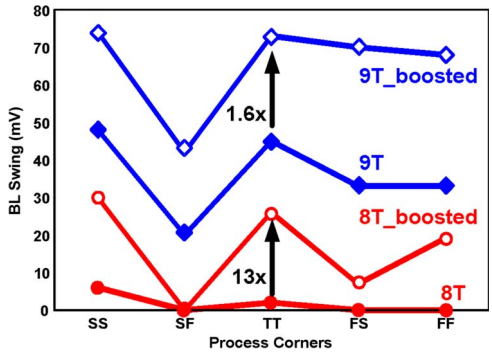


Fig. 14. Simulated RBL voltage swing at different process corners. All simulations were performed at 256 cells per column, 0.25-V supply, 50 °C.

ceases to work at 0.3 V supply, due to the diminishing $I_{\rm on}$-to-$I_{\rm off}$ ratio at low voltage (Fig. 2). The 9T designs continue to work at 0.25 V thanks to its equalized bitline leakage.

In Fig. 13, we study the impact of temperature on the operability of the designs in comparison. At low temperature, all four schemes offer reasonable RBL swing with the 9T_boosted the best and 8T the worst. With increasing temperature, the leakage current increases exponentially, and thus the RBL swings are reduced. The 8T and 8T_boosted cannot work at 60 °C or above, due to the high bitline leakage. The 9T and 9T_boosted schemes can operate with a positive RBL swing even at 100 °C. Another observation is that when the boosting current is applied to the 9T design, the slope of the 9T_boosted curve in Fig. 13 is less than that of the 9T curve (20 °C $\rightarrow$ 40 °C transition), indicating that the proposed boosting current scheme is less sensitive to temperature variation.

When considering different process corners, the 9T_boosted scheme continues to outperform the other designs. Fig. 14 illustrates the RBL swings of these designs at 50 °C, 256 cells per column, 0.25 V supply voltage. Since 50 °C is quite close to 60 °C, the 8T designs work quite badly, which agrees with the data shown in Fig. 13.

Finally, we investigate the effect of different numbers of cells per RBL. When fewer cells are attached to one RBL, with all others equal, it leads to a less leakage current. As a result, the corresponding RBL will be able to achieve higher bitline swing, as shown in Fig. 15, at 80 °C, the 8T schemes can only support 128 cells per RBL. On the contrary, the 9T and 9T_boosted designs are able to support 256 cells per column.

In general, the 9T designs outperform the 8T designs due to their constant RBL leakages. This also extends their operating

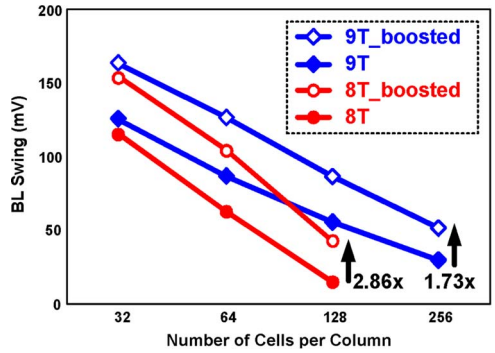


Fig. 15. Simulated RBL voltage swing at different process corners. All simulations were performed at 0.25 V supply, TT corner.

range with higher number of cells per column and can be sustained even at higher temperatures. It can also be seen that the boosting current significantly enhances the RBL swing by at least 35% in both 8T and 9T schemes. In some extreme cases, this number can go up to several times, as noted in Figs. 12–15. Since the boosting current is used to compensate for the excessive leakage current on a RBL, its impact is more noticeable when the total leakage current is comparable to $I_{\rm on}$. It is therefore a good candidate to improve the performance of ultra-low-voltage SRAMs.

V. Conclusion

This paper has explored circuit techniques for enhancing RBL sensing margin for ultra-low-power SRAMs. The proposed boosting current technique compensates the excessive bitline leakage at ultra-low-voltage condition, thus enhancing the available bitline voltage swing during the read operation. It also widens the sensing time window since the compensation current prevents the the read "1" RBL to be discharged completely to ground. When applied to the 8T and 9T cells, it improves their bitline swing performance by at least 35%. At 256 cells per column, 0.25-V supply voltage, 27 °C, our simulations using a commercially available 40-nm CMOS process showed that the proposed scheme boosts the bitline swing of the 8T and 9T cells from 30 mV and 61 mV to 56 mV and 90 mV, respectively.

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