# BSIM4 Gate Leakage Model Including Source-Drain Partition

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## Abstract

Gate dielectric leakage current becomes a serious concern as sub-20Å gate oxide prevails in advanced CMOS processes. Oxide this thin can conduct significant leakage current by various direct-tunneling mechanisms and degrade circuit performance. While the gate leakage current of MOS capacitors has been much studied, little has been reported on compact MOSFET modeling with gate leakage. In this work, an analytical intrinsic gate leakage model for MOSFET with physical source/drain current partition is developed. This model has been implemented in BSIM4.

## Introduction

As the gate length of MOSFETs is reduced to the sub-100nm regime, gate oxide thickness of sub-20Å prevails in CMOS processes [1]. Besides the benefits of high drive current and low DIBL effect, such thin oxide yields significant gate leakage current by various direct tunneling mechanisms [2], with undesirable effects on standby current and memory operation [3]. Comparing to the compact leakage current models for MOS capacitors [4,5], less research has been conducted on the compact MOSFET models. C.-H. Choi [6] proposed a gate leakage model for MOSFET but the model is not accurate under low bias condition (in direct-tunneling regime) and the current partition scheme is unphysical. In this work, a physical gate leakage model for MOSFET is developed and implemented in BSIM4. Firstly, we propose an accurate gate leakage model for the MOS capacitor. Then a physical source-drain current partition model is introduced. The model is verified with experimental data and 2D simulation.

## MOS Capacitor Leakage Model

Lee and Hu proposed an accurate dielectric leakage model for MOS capacitors [5]. A simplified version of this model with little compromises on accuracy is the basis of the MOSFET gate leakage model.

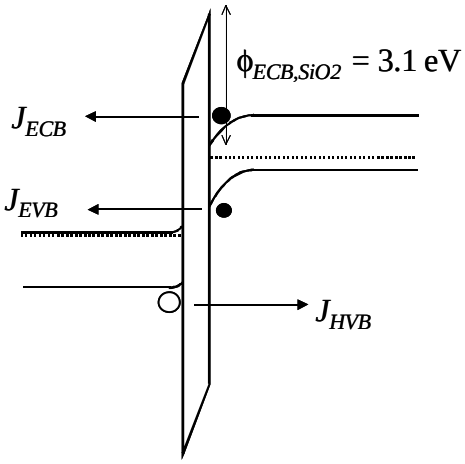


**Figure 1** Three mechanisms of gate dielectric direct tunneling leakage.

There are three major leakage mechanisms for a MOS structure, namely, electron conduction-band tunneling (ECB), electron valence-band tunneling (EVB), and hole valence-band tunneling (HVB), as illustrated in Fig. 1. Each mechanism is dominant or important in different regions of operation for PMOS and NMOS as shown in Table 1. For each

**Table 1** Major mechanisms (as shown in Fig.1) contributing to current components illustrated in Fig. 2. The mechanism governing $I_{gso}$ and $I_{gdo}$ under all bias conditions is ECB.

| Current Component | Igc | Igb | |
|---|---|---|---|
| Region of Operation | inversion | $V_g>0$ | $V_g<0$ |
| PMOS | HVB | ECB | EVB |
| NMOS | ECB | ECB | EVB |

mechanism, the leakage current density can be modeled by:

$$J_g = A \cdot \left( \frac{T_{oxref}}{t_{ox}} \right)^{ntox} \cdot \frac{V_g \cdot V_{aux}}{t_{ox}^2} \cdot e^{-B(a - b|V_{ox}|)(1+g|V_{ox}|)t_{ox}}$$

where $A = q^2/8ph f_b$, $B = 8p\sqrt{2qm_{ox}} f_b^{3/2}/3h$, $m_{ox}$ is the effective carrier mass in oxide, $f_b$ is the tunneling barrier height (shown in Fig. 1), $t_{ox}$ is the oxide thickness, $T_{oxref}$ is the reference oxide thickness at which all the parameters are extracted, *ntox* is a fitting parameter that defaults to 1, and $V_{aux}$ is an auxiliary function which approximates the density of tunneling carriers as well as available states and tabulated in Table 2.

**Table 2** The $V_{aux}$ function, which models the density of tunneling carriers and available states.

| Region of Operation | Current | $V_{aux}$ |
|---|---|---|
| acc. | $I_{gb}$ | $nigbacc \cdot V_{tm} \cdot \log\left(1 + \exp\left(-\frac{V_{gb} - V_{fb}}{nigbacc \cdot V_{tm}}\right)\right)$ |
| inv.+dep. | $I_{gb}$ | $nigbinv \cdot V_{tm} \cdot \log\left(1 + \exp\left(\frac{V_{oxdepinv} - eigbinv}{nigbinv \cdot V_{tm}}\right)\right)$ |
| | $I_{gc}$ | $nigc \cdot V_{tm} \cdot \log\left(1 + \exp\left(\frac{V_{gs\_eff} - V_{th0}}{nigc \cdot V_{tm}}\right)\right)$ |
| both | $I_{gso}$ | $\lvert V_{gs} \rvert$ |
| both | $I_{gdo}$ | $\lvert V_{gd} \rvert$ |

## MOSFET Gate Leakage Model

As illustrated in Fig. 2, the gate tunneling current is composed of several components. $I_{gb}$ is the gate-to-substrate leakage current; $I_{gso}$ and $I_{gdo}$ are parasitic leakage currents through gate-to-S/D extension overlap region; and $I_{gc}$ is the gate-to-inverted channel tunneling current. Part of $I_{gc}$ is collected by the source ($I_{gcs}$) while the rest goes to the drain ($I_{gcd}$). $I_{gb}$, $I_{gso}$, $I_{gdo}$, and $I_{gc}$ can be easily determined from the MOS capacitor model introduced in the previous section. The remaining challenge is modeling $I_{gc}$ for nonzero $V_{ds}$ and partitioning $I_{gc}$ into $I_{gcs}$ and $I_{gcd}$.

To derive $I_{gcs}$ and $I_{gcd}$, current continuity equation is solved for the voltage along the channel as a function

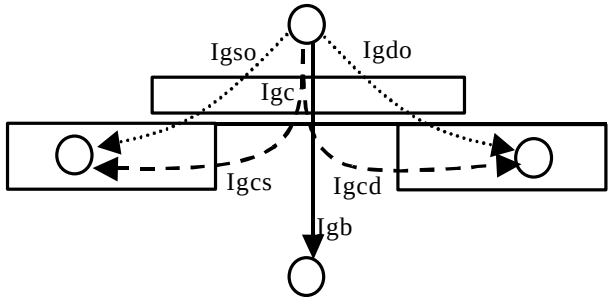


**Figure 2** Components of tunneling current. $I_{gso}$ and $I_{gdo}$ are parasitic tunneling currents through gate-source/drain overlap regions. $I_{gb}$ flows between gate and substrate. $I_{gc}$ is the gate-to-channel tunneling current. It is partitioned into $I_{gcs}$, which flows to the source, and $I_{gcd}$, which flows to the drain.

of x, which is 0 at the source and L at the drain. From drift equation, the channel current density in source-drain direction is $mC_{ox}(V_{gs} - V_{th} - V) \cdot dV/dx$.

Current continuity requires:

$$d\left((V_{gs} - V_{th} - V)dV/dx\right)\Big/_{dx} + J_g(x)/mC_{ox} = 0 \quad (2)$$

where *V(x)* is the channel potential relative to the source. The gate tunneling current density at *x* can be approximated with

$$J_g \approx AE_{ox}^2 e^{-B/E_{ox}} \approx AE_{oxs}^2 e^{-BT_{ox}/(V_{oxs}-V)} \equiv J_{g0} \cdot e^{-B^* V} \quad (3)$$

where $J_{go}$ is the gate tunneling current density with $V_{ds}=0$ (can be modelled by Eq. 1), $B^* \approx P_{igcd} \cdot BT_{ox}/V_{oxs}^2$ and $V_{oxs} \approx V_{gs}$ is the voltage across the gate oxide at $x=0$. $P_{igcd}$ is a fitting parameter added for flexibility with a default value of 1.

Assuming the gate leakage current is small compared to the drain current, the perturbation of $J_g$ on $V(x)$ is small,

$$V(x) = V_0(x) + V_1(x) \quad (4)$$

where $V_0(x)$ is the solution of Eq. (2) with $J_g(x)=0$ and $V_0(x) >> V_1(x)$. $V_0(x)$ can be solved and approximated to be:

$$V(x) = V_{gs} - V_{th} - \sqrt{(V_{gs} - V_{th})^2 - 2(V_{gs} - V_{th} - V_{ds}/2) \cdot V_{ds} \cdot x/L} \approx K \cdot x \quad (5)$$

where $K = (V_{gs} - V_{th} - V_{ds}/2) \cdot V_{ds}/(V_{gs} - V_{th})L$. This approximation is not very accurate when *x* and $V_{ds}$ are both large compared to *L* and $V_{gs}$-$V_{th}$ respectively. However, in that case $J_g$ is large only at small *x*, where the approximation is accurate. Therefore, the simplification is reasonable.

Eq. (2) can be further simplified considering $V_0(x) >> V_1(x)$.

$$\left(V_{gst}-V_0\right)d^2V_1/dx^2 - V_1 d^2V_0/dx^2 - 2dV_0/dx \cdot dV_1/dx + J_{g0}\cdot e^{-B^*V_0}\Big/ mC_{ox} = 0, \quad V_1(0)=V_1(L)=0 \tag{6}$$

$V_1$ can then be solved as

$$V_1 = -\frac{J_{g0}\left\{\left(e^{-B^*Kx}-1\right)+\frac{x}{L}\left(1-e^{-B^*KL}\right)\right\}}{mC_{ox}B^{*2}K^2\left(V_{gst}-Kx\right)} \tag{7}$$

and $I_{gcs}$ and $I_{gcd}$ can be derived as:

$$I_{gcs} = mC_{ox}V_{gst}W\left.\frac{dV_1}{dx}\right|_{x=0} = \frac{J_{g0}WL\left(B^*KL+e^{-B^*KL}-1\right)}{B^{*2}K^2L^2}$$
$$I_{gcd} = -mC_{ox}\left(V_{gst}-KL\right)W\left.\frac{dV_1}{dx}\right|_{x=L} = -\frac{J_{g0}WL\left(B^*KLe^{-B^*KL}+e^{-B^*KL}-1\right)}{B^{*2}K^2L^2} \tag{8}$$

Using the same derivation, better accuracy but more complex equation can be obtained by including the second order term in the exponent of Eq. (3).

From Eq. (8), the $I_{gc}$-$V_{ds}$ function can then be easily calculated as:

$$I_{gc} = \frac{J_{g0}WL\left(1-e^{-B^*KL}\right)}{B^*KL} \tag{9}$$

Parameter extraction can follow two steps. The first step is to extract the parameters in Eq. 1 from the tunneling currents $I_{gc}$ (from shorted source and drain) and $I_{gb}$. The second step is to extract $P_{igcd}$ from the gate-to-channel tunneling current as a function of drain and gate bias using Eq. (9). Afterwards, the gate-to-channel current partition can be calculated using Eq. (8) without any parameter. The proposed partition model is based on physical derivation and requires no empirical parameters. This is especially important because the partition ratio is extremely difficult or impossible to measure.

## Verification of the Model

We found that the proposed tunneling model (Eq. 1) for MOS capacitors works well for all major mechanisms (Fig. 3) and for a wide range of oxide thickness (Fig. 8). Our simple $I_{gc}$-$V_{ds}$ model (Eq. 9) also agrees with simulation results and experimental data very well as shown in Fig. 4,5, and 11. The proposed partition model (Eq. 8) is verified by simulation data as a function of $V_{gs}$(Fig. 6) and oxide thickness (Fig. 7). Fig. 9 shows the model agrees well with $I_{gc}$-$V_{ds}$ data for different $V_{gs}$.

## Summary

We have developed a simple gate dielectric leakage current model suitable for compact MOSFET models. This model considers all three major leakage components and is accurate in direct-tunneling regime with excellent $T_{ox}$ scaling capability. Physical gate-to-channel current partition models are developed for the first time. With its great accuracy and satisfying test results from the member companies of the Compact Modeling Council (CMC), the proposed models have been implemented into the BSIM4 and can already help to address the impacts of gate leakage current on circuit performance.

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## References

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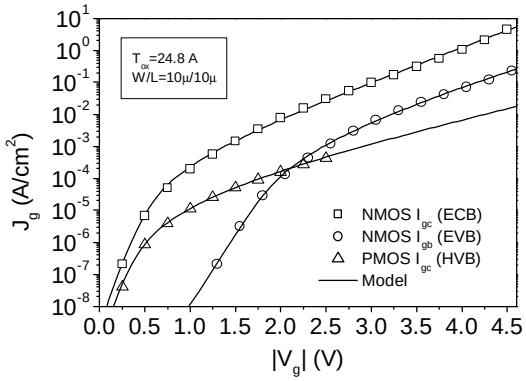


**Figure 3** The proposed MOS model agrees with measured data for tunneling mechanisms ECB, EVB, and HVB.

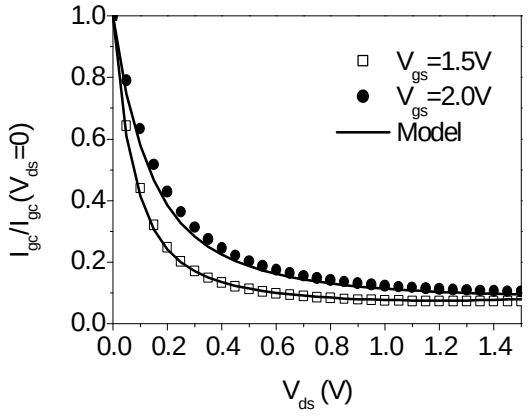


**Figure 4** The model and normalized $I_{gc}$-$V_{ds}$ 2D simulation data at different $V_{gs}$.

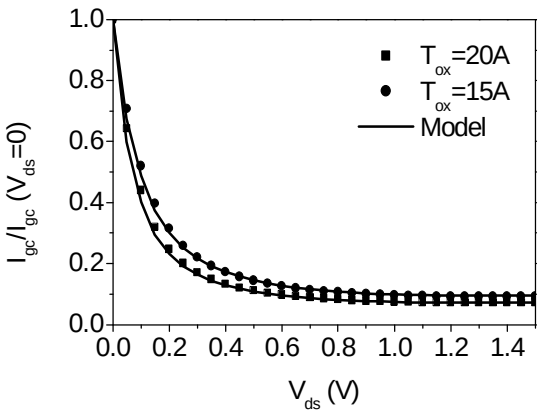


**Figure 5** The model and normalized $I_{gc}$-$V_{ds}$ 2D Simulation data at different oxide thickness.

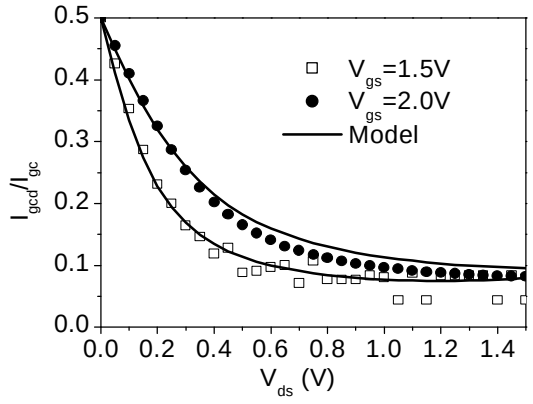


**Figure 6** The current partition model agrees with simulation data at different $V_{gs}$ bias.

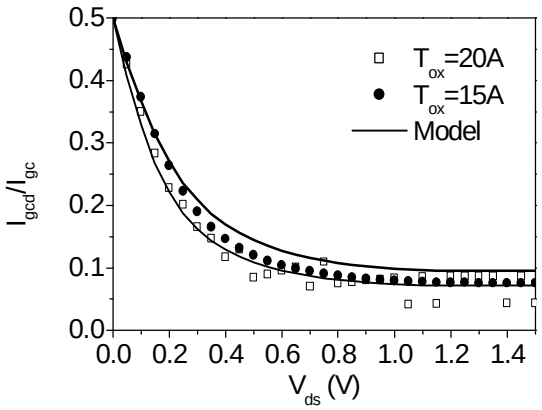


**Figure 7** The current partition model agrees with simulation data at different oxide thickness.

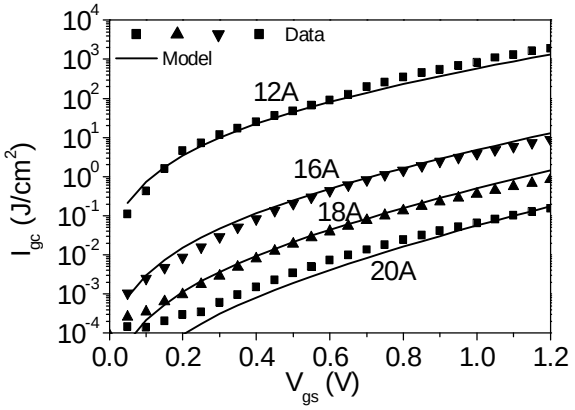


**Figure 8** The proposed MOS tunneling model is scalable with oxide thickness (NMOS).

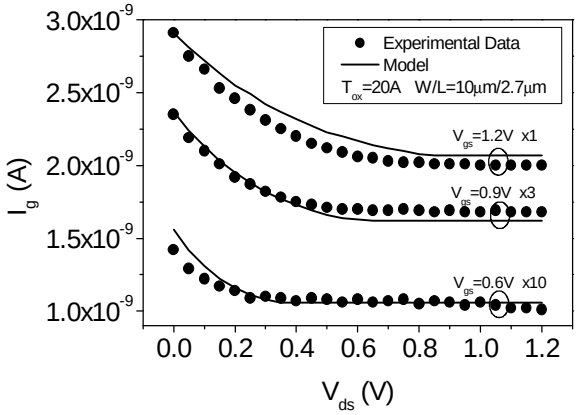


**Figure 9** Agreement of the model with experimental $I_g$-$V_{ds}$ data at different $V_{gs}$ bias.