A Read-Static-Noise-Margin-Free SRAM Cell for Low-VDD and High-Speed Applications

Koichi Takeda, Yasuhiko Hagihara, Yoshiharu Aimoto, Masahiro Nomura, *Member, IEEE*, Yoetsu Nakazawa, Toshio Ishii, and Hiroyuki Kobatake

***Abstract*—To help overcome limits to the speed of conventional SRAMs, we have developed a read-static-noise-margin-free SRAM cell. It consists of seven transistors, several of which are low-Vth nMOS transistors used to achieve both low-VDD and high-speed operations. For the same speed, the area of our proposed SRAM is 23% smaller than that of a conventional SRAM. Further, we have fabricated a 64-kb SRAM macro using 90-nm CMOS technology and have obtained with it a minimum VDD of 440 mV and a 20-ns access time with a 0.5-V supply.**

***Index Terms*—Static random access memory (SRAM), SRAM scaling, static noise margin.**

I. Introduction

ADVANCES in process technologies are leading to steady increases in the speeds of microprocessors and system LSIs. The speeds of SRAMs, which are needed to serve as cache memories, must keep pace with these increases. Unlike the situation with the threshold voltage (Vth) of CMOS logic transistors, however, since the read-static-noise-margin (SNM) deteriorates with decreases in supply voltage (VDD) and increases with the transistor mismatch accompanied by geometry scaling [1]–[3], there are severe limits to the degree to which the Vth of nMOS transistors in SRAM cells can be lowered. The SNM problem also makes it difficult to apply, to SRAMs, dynamic voltage scaling techniques that have been proposed for reducing the active power consumption of microprocessors and system LSIs. This is because the minimum supply voltage of LSIs is limited by their SRAMs for the following two reasons: 1) with decreasing VDD, SRAM delay increases at a higher rate than does CMOS logic circuit delay, and 2) Read operations at low-VDD levels result in storage data destruction in SRAM cells. While techniques for boosting VDD in SRAMs have been proposed in order to achieve both high-speed data access and stable data retention during Read operations [4], [5], the use of these techniques can result in the deterioration of transistor reliability.

In response to this, the use of a dual-port SRAM cell as a single-port SRAM cell with 32-nm CMOS process technology has been proposed [6]. By separating data retention elements and data output elements, Read operations can be performed without read-disturb. This makes it possible to lower the Vth of nMOS transistors in SRAM cells to the same degree as the Vth of CMOS logic transistors can be lowered. The proposed dual-port SRAM cell (8T-cell), however, is composed of eight transistors and has 30% greater area than that of a conventional six-transistor SRAM cell (6T-cell).

To overcome the SNM problem and to reduce the area overhead incurred by an 8T-cell, we have developed a read-SNM-free seven-transistor SRAM cell (7T-cell) [7]. In it, a single transistor for loop-cutting is added to a 6T-cell. This makes it possible to reduce the area overhead from 30%

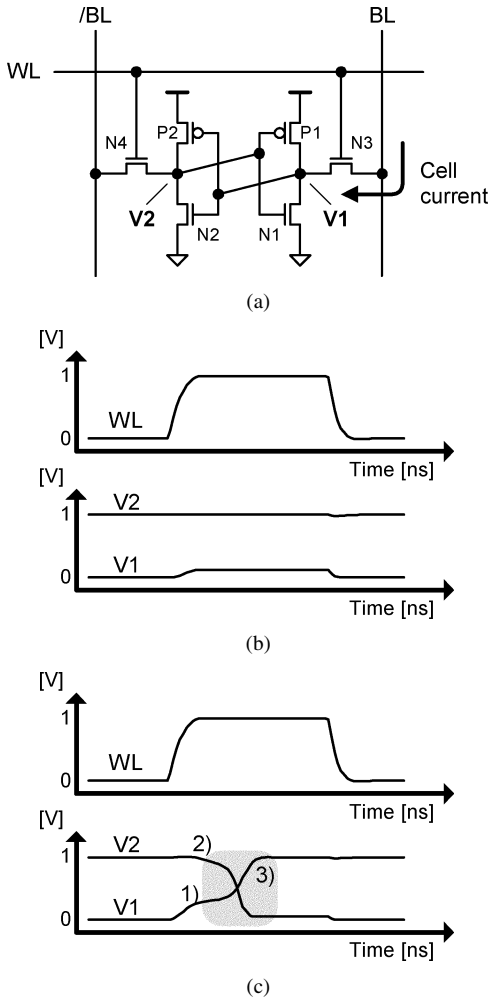

Fig. 1. (a) Conventional SRAM cell. (b) Waveforms of conventional SRAM cell for SNM $>$ 0 V. (c) Waveforms of conventional SRAM cell for SNM $<$ 0 V.

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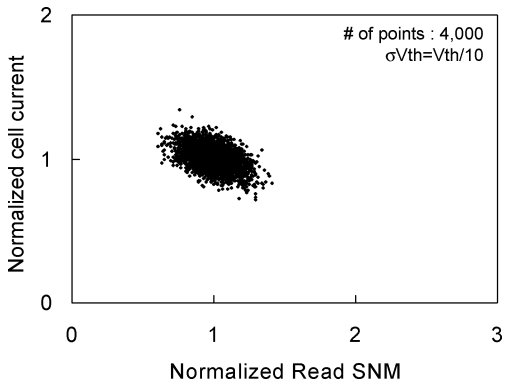

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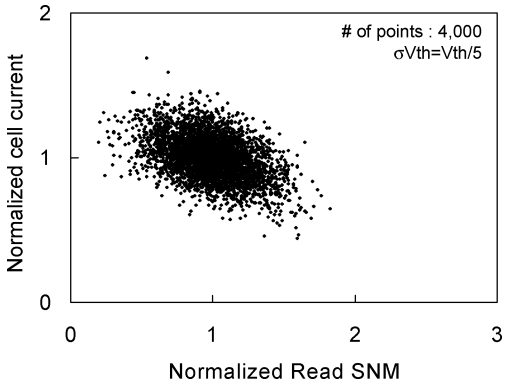
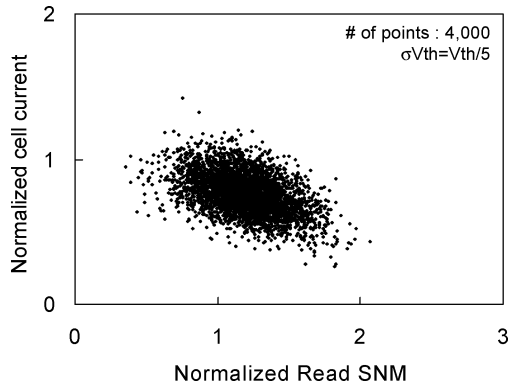


(b)

Fig. 2. (a) Monte Carlo simulation results for $\sigma\mathrm{Vth} = \mathrm{Vth}/10$. (b) Monte Carlo simulation results for $\sigma\mathrm{Vth} = \mathrm{Vth}/5$.



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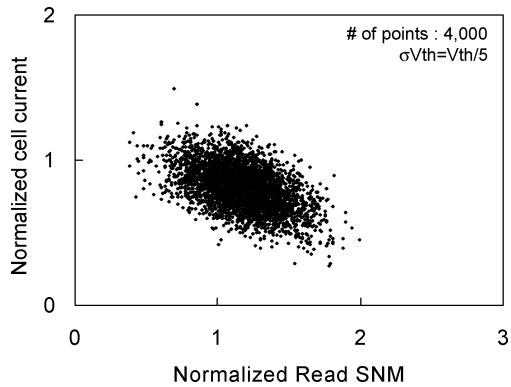


(b)

Fig. 3. (a) Monte Carlo simulation results for nMOS Vth raised by 0.1 V. (b) Monte Carlo simulation results for WL voltage lowered to 0.9 V.

to 13%. In our proposed 7T-cell, Vth in the nMOS transistor can be reduced to the Vth of the logic transistor, making it possible to achieve both low-VDD and high-speed operations. In addition, a large-signal sensing scheme is used [8] which, unlike a small-signal sensing scheme, has the advantage that its delay improves with the same device-scaling that is applied to CMOS logic circuits.

This paper is organized as follows. In Section II, the Read SNM and SRAM cell current in conventional SRAM cell is described. Section III introduces our proposed Read-SNM-free seven-transistor SRAM cell and peripheral circuit architectures. In Section V, chip fabrication and measurement results are described.

II. Static Noise Margin and SRAM Cell Current in Conventional SRAM Cells

Transistor mismatch degrades both the read SNM and SRAM cell current (Icell) of the conventional SRAM cell shown in Fig. 1(a). Although Icell degradation simply increases bit-line (BL) delay time, Read SNM degradation results in data destruction during Read operations. When SNM > 0 V [Fig. 1(b)], stable data retention is still achieved even though the voltage at Node V1 may slightly exceed "0". When SNM < 0 V [Fig. 1(c)], however, reversal data is overwritten. Specifically:

1) Node V1 voltage greatly exceeds "0".
2) Node V2 voltage falls below "1" because Node V1 voltage reaches the CMOS inverter logical threshold voltage (P2, N2).
3) The fall in Node V2 voltage raises Node V1 voltage further, resulting in the overwriting of reversal data.

To determine the influence due to transistor mismatch, we performed Monte Carlo simulations for Read SNM and Icell under the condition of $\sigma\mathrm{Vth} = \mathrm{Vth}/10$. Fig. 2(a) shows the results. Here, Read SNM values have been normalized to that of a typical SRAM cell, and Icell values have been normalized to the Icell value of a typical SRAM cell. Both Read SNM and Icell values are highly dependent on the driving capability of the access nMOS transistor: Read SNM decreases with increases in driving capability, while Icell increases. That is, the dependence of the two is in an inverse correlation. The worst normalized Read SNM and normalized Icell values are, respectively, 0.60 and 0.72. The figure represents 4000 points. In consideration of the possibility of future advances in process technologies, we also performed Monte Carlo simulations for $\sigma\mathrm{Vth} = \mathrm{Vth}/5$. As shown in Fig. 2(b), the worst normalized Read SNM and normalized Icell values then deteriorate to 0.20 and 0.44, respectively.

We further extended our simulations to include two techniques which have been proposed for improving Read SNM, which is a more significant parameter than Icell. The first technique is that of increasing the Vth of the nMOS transistors in SRAM cells [1]. Increasing the Vth of access nMOS transistors prevents Node V1 voltage from greatly exceeding "0", while increasing the Vth of drive nMOS transistors increases the CMOS inverter logical threshold voltage. The second technique is that of dropping the word-line (WL) voltage level from VDD at Read

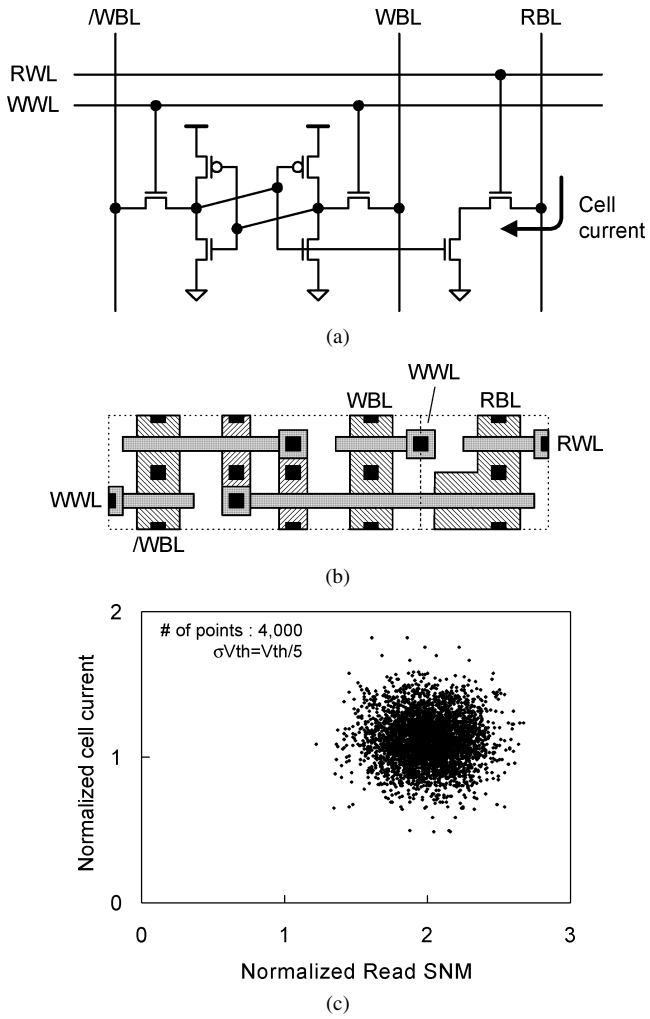


Fig. 4. (a) 8T-cell. (b) 8T-cell layout. (c) Monte Carlo simulation results.

operations [9]. This has the same effect as increasing the Vth of access nMOS transistors. In Monte Carlo simulations that included these Read SNM improvement techniques, the worst normalized Read SNM value improved from 0.20 to 0.36, but the worst normalized Icell value decreased from 0.44 to 0.26, as may be seen in Fig. 3(a). Here we used nMOS transistors whose Vth was 0.1 V higher than that of conventional SRAM cell transistors. When the WL voltage level was dropped from 1.0 V to 0.9 V, the worst normalized Read SNM value improved to 0.38, but the worst normalized Icell value decreased to 0.27, as shown in Fig. 3(b). In order to avoid increased BL delay time, Icell degradation could be compensated for by reducing the number of SRAM cells per BL, but to do so would result in increased area overhead in the sensing circuit. If the area of the sensing circuit were increased so much as to exceed that of the SRAM cell array, it would no longer be possible to maintain BL delay time levels.

To avoid this limitation, the use of a dual-port SRAM cell as a single-port SRAM has been proposed [6]. A dual-port cell (8T-cell) is created by adding two data output transistors to a conventional 6T-cell, as shown in Fig. 4(a) and (b). Separation of data retention element and data output element means that there will be no correlation between Read SNM and Icell [see Fig. 4(c)]. In contrast to the worst normalized Read SNM value

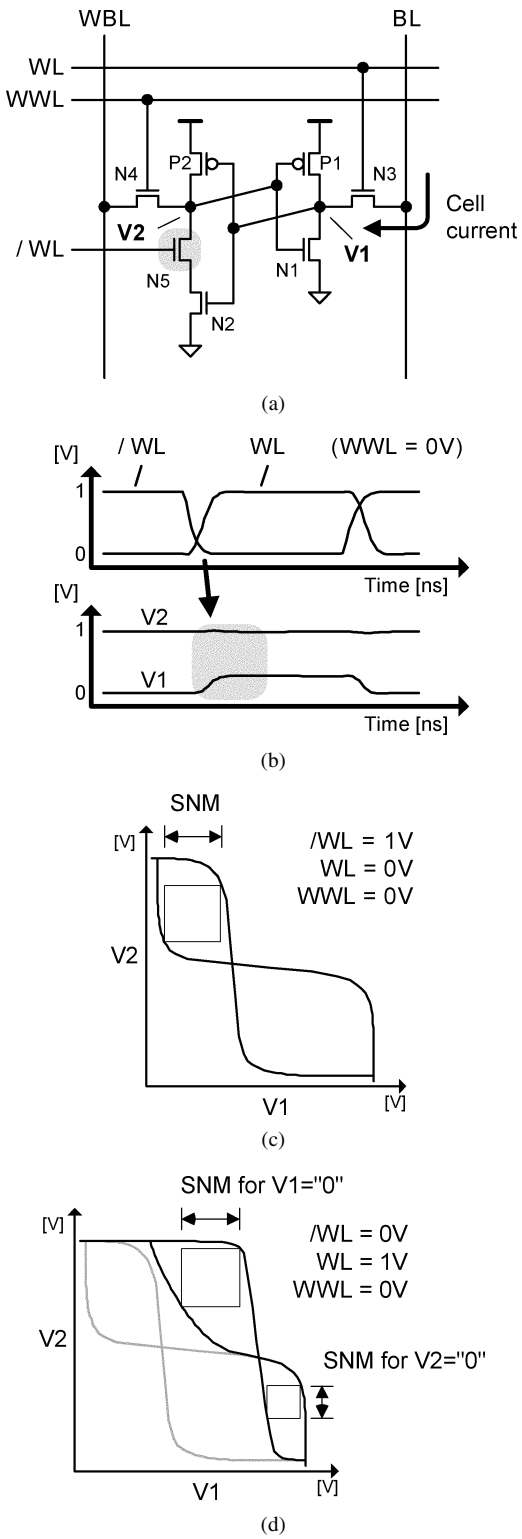
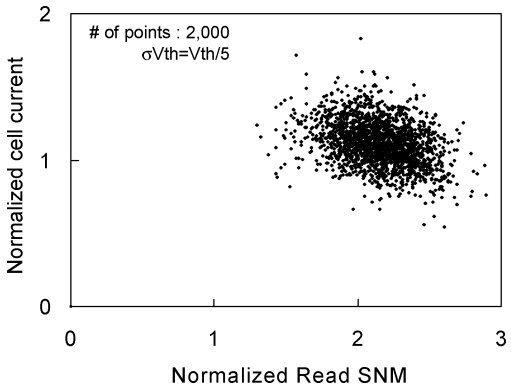


Fig. 5. (a) 7T-cell. (b) Waveforms of 7T-cell. (c) Butterfly curve during data retention period. (d) Butterfly curve during read operations.

of 0.20 for a conventional 6T-cell [see Fig. 2(b)], here the value is 1.22, and there is no Icell degradation. It is also possible here to lower the Vth of the nMOS transistors in a SRAM cell in order to improve Icell. This 8T-cell has 30% more area than a conventional 6T-cell, however. The 30% area overhead is composed of not only the two added transistors but also of the contact area of the WWL, the word-line for Write operations. While



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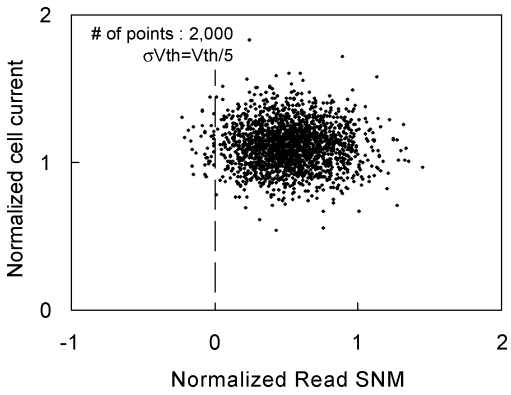

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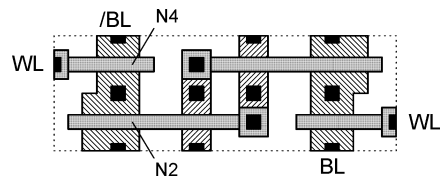
Fig. 6. (a) SNM Monte Carlo simulation results for V1 = "0". (b) SNM Monte Carlo simulation results for V2 = "0".



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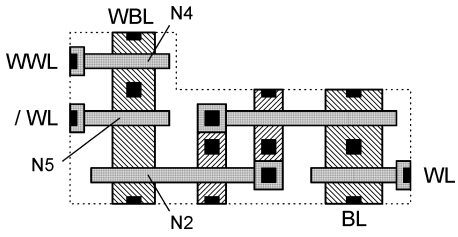


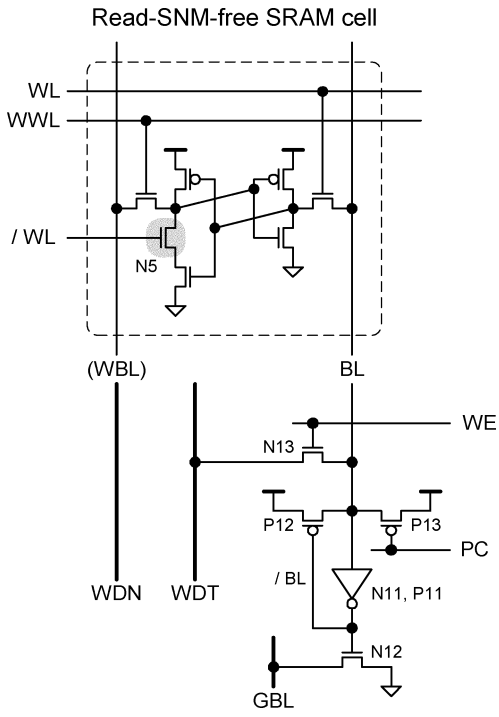
(b)

Fig. 7. (a) Conventional 6T-cell layout. (b) Proposed 7T-cell layout.

WL contact area is conventionally assigned to the boundary line between two SRAM cells, in this SRAM cell the WWL contact area is assigned to within a cell, as shown in Fig. 4(b).

III. Proposed Seven-Transistor SRAM Cell

We have developed a read-SNM-free seven-transistor SRAM cell [Fig. 5(a)] with the purpose not only of obtaining the same effect as that of using an 8T-cell but also of reducing the 30% area overhead that results from use of an 8T-cell. Data



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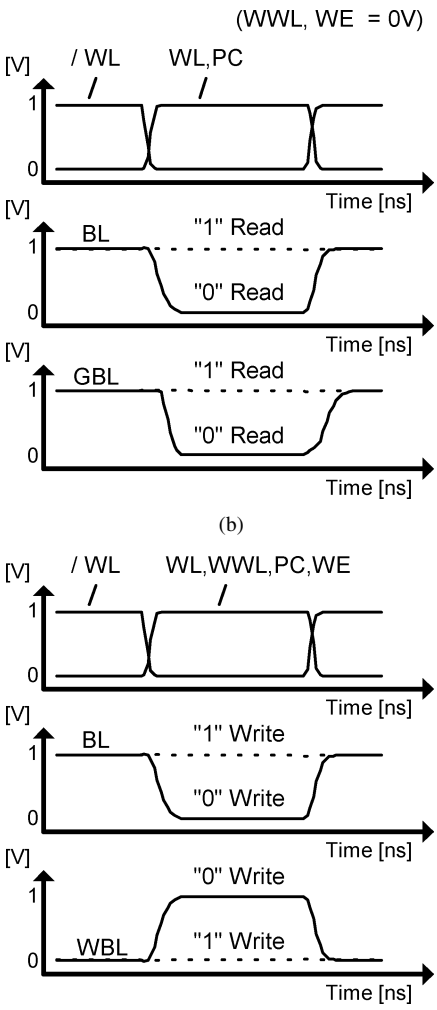

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Fig. 8. (a) Sensing circuit. (b) Waveforms for read operations. (c) Waveforms for write operations.

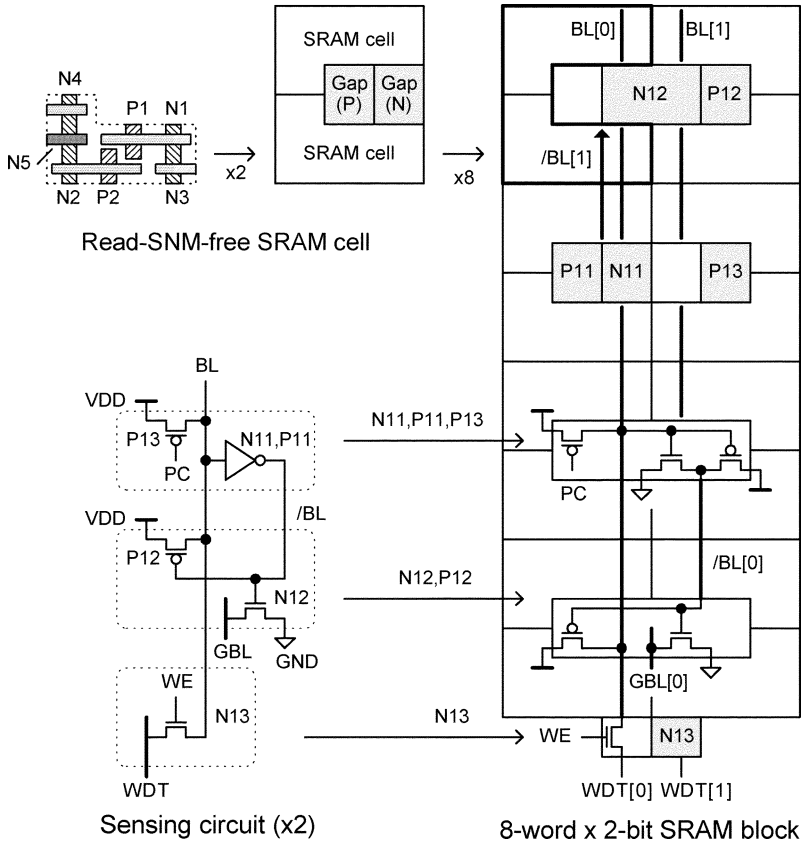


Fig. 9. Sensing-circuit-combined layout design.

protection nMOS transistor N5 has been added between Node V2 and nMOS transistor N2. While the SRAM cell is being accessed, /WL is in the activated state, "0", and N5 is OFF. Since N5 prevents the voltage at Node V2 from decreasing, the data bit is not reversed even if Node V1 voltage greatly exceeds [Fig. 5(b)].

During data retention period, when the SRAM cell is not being accessed, word line signal /WL is "1", and nMOS transistor N5 is ON. The use of two CMOS inverters results in high cell stability [Fig. 5(c)]. During Read operations, the logical threshold voltage of the CMOS inverter driving Node V2 increases greatly when the data protection nMOS transistor N5 is turned off [Fig. 5(d)]. For this reason, the Read SNM value at V1 = "0" remains large even when access nMOS transistor N3 is turned on and Node V1 voltage increases.

The worst normalized Read SNM and normalized Icell values improve, respectively, to 1.24 and 0.54, as may be seen in Fig. 6(a). With our 7T-cell, the same Read SNM and Icell values are obtained as with the 8T-cell. Its use, however, means that three issues must be addressed:

1) area overhead due to the addition of transistor N5;
2) control of WL, WWL and /WL;
3) dynamic retention of V2 = "0" during "1" read.

In the case in which Node V2 is "0", while the SRAM cell is being accessed, Node V2 will be in a high-impedance state. Therefore, the worst SNM value for V2 = "0" will be lower than 0 V, as may be seen in Fig. 6(b).

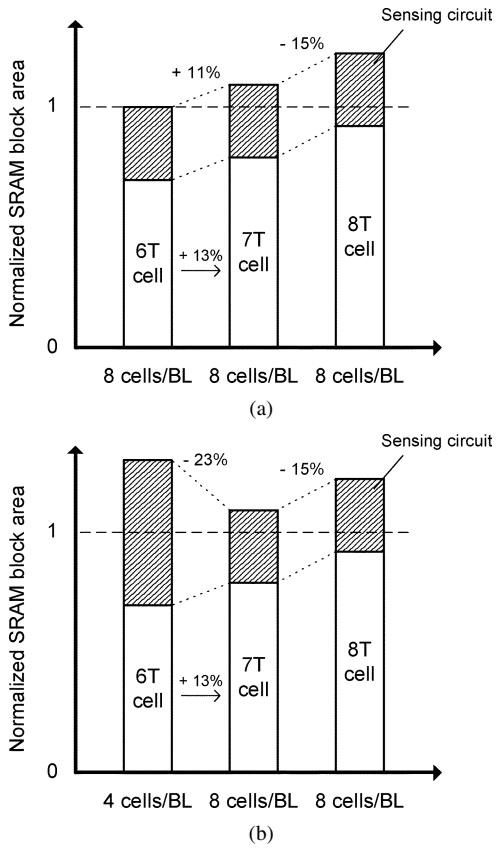


Fig. 10. (a) Area comparison for the same configuration. (b) Area comparison for same speed.

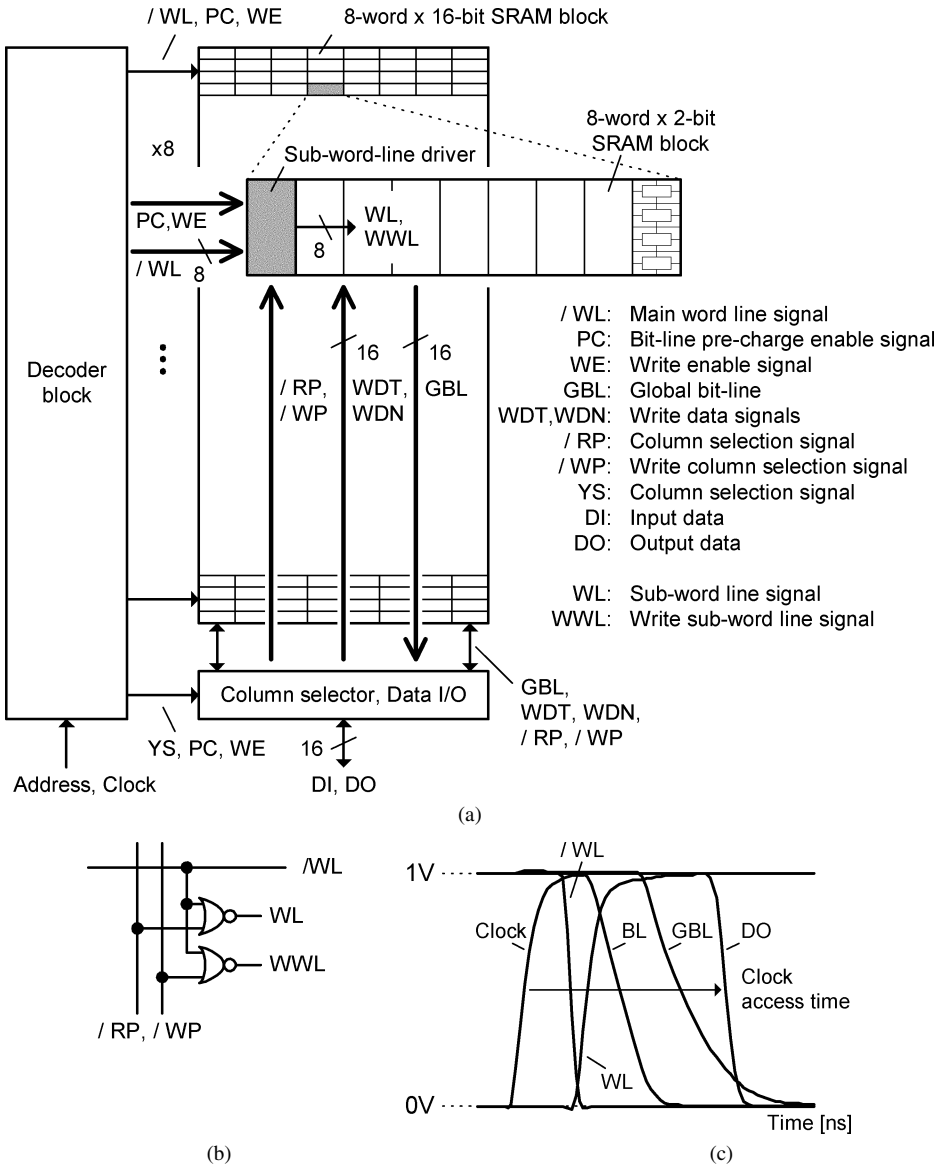


Fig. 11. (a) Floor plan for proposed 7T-cell (64 Kb). (b) Sub-word-line driver. (c) Waveforms of 64 Kb SRAM.

A. Cell Layout

Fig. 7(a) and (b) show, respectively, a conventional 6T-cell layout and our proposed 7T-cell layout. In the proposed 7T-cell, a data protection nMOS transistor N5 is inserted between access nMOS transistor N4 and drive nMOS transistor N2. In contrast to a conventional 6T-cell design, N4 is shifted upward, giving the proposed 7T-cell an L-shape. This results in an increase in area of 13% over that of a 6T-cell designed with the same rules.

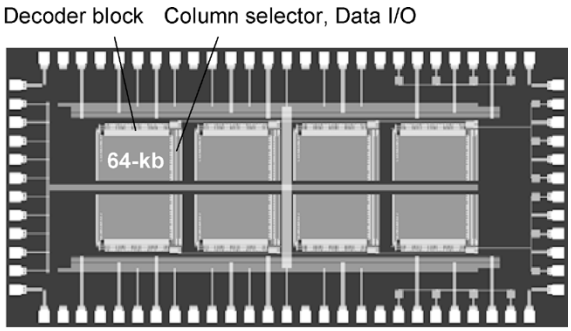
B. Sensing Circuit

Fig. 8(a) shows the sensing circuit for our proposed 7T-cell. It consists of a CMOS inverter (P11 and N11), data output nMOS transistor N12, keeper pMOS transistor P12, pre-charge pMOS transistor P13, and write nMOS transistor N13. In Read operations, shown in Fig. 8(b), the pre-charge enable signal PC is activated to "1". The CMOS inverter amplifies the data output to the BL, and N12 outputs Read data to a global bit-line (GBL). In Write operations, shown in Fig. 8(c), the pre-charge enable signal PC and the write enable signal WE are activated to "1". The sensing circuit outputs Write data WDT to the BL through N13. The WBL is connected directly to the WDN signal line and is controlled by a column selector [see Fig. 11(a)].

C. Sensing-Circuit-Combined Layout Design

Fig. 9 shows an 8-word $\times$ 2b-SRAM block composed of 16 SRAM cells and two sensing circuits. While high density is conventionally achieved with a rectangular design, in this SRAM cell a useless gap, equivalent to one transistor, would result, since seven is a prime number and cannot be factored. To avoid such a useless gap, the layout design combines the SRAM cell and the sensing circuit. A pMOS and an nMOS transistor are placed, respectively, in GAP (P) and GAP (N), between two L-shaped SRAM cells. N11, N12, P11, P12 and P13 of the sensing circuit are placed into these otherwise useless gaps. This is possible because the source terminal of these transistors is either GND or VDD.

Fig. 10(a) contrasts the areas of 8-word $\times$ 2b-SRAM blocks, in which the number of SRAM cells per BL is 8. The area of



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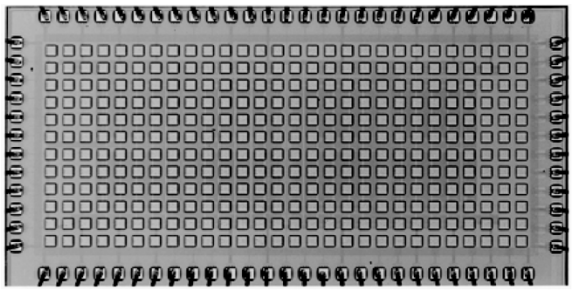

(b)

Fig. 12. (a) SRAM macro layout. (b) Microphotograph

the SRAM block with 7T-cells is 15% smaller than that of the SRAM block with 8T-cells, but is 11% larger than that of the SRAM block with 6T-cells.

Fig. 10(b) shows the areas of SRAM blocks which are designed to achieve the same speed. Because the Read SNM improvement techniques decrease Icell to as small as half of its original value [Fig. 3(a) and (b)], the number of SRAM cells per BL can be reduced to 4 while maintaining the same access time as with other SRAMs, and the number of sensing circuit can be doubled. In this way, the area of the SRAM block with 7T-cells will be 23% smaller than that of the SRAM block with 6T-cells for the same speed [Fig. 10(b)].

D. Sub-Word-Line Driver

Fig. 11(a) shows the word line control scheme of the SRAM cell. Since the activation of word line signal WWL, which is newly added, triggers Write operations in the SRAM cell, column selection must be performed not per BL but per 8-word×16 bit SRAM block. This 8-word×16 bit SRAM block is composed of eight 8-word×2-bit SRAM blocks and eight sub-word-line drivers. Word line /WL is assigned to the main word line, and word lines WL and WWL are assigned to sub-word lines. Sub-word lines are controlled by CMOS NORs, for which the inputs are the main word line /WL and the column selection lines, /RP and /WP, as shown in Fig. 11(b). Since WL is activated after /WL is activated, as may be seen in Fig. 11(c), the data protection nMOS transistor N5 always performs its function before cell access. While there is a 10% area overhead due to the addition of the sub-word-line drivers, this column selection scheme reduces the number of active BLs, and it is superior to conventional SRAMs in terms of active power reduction.

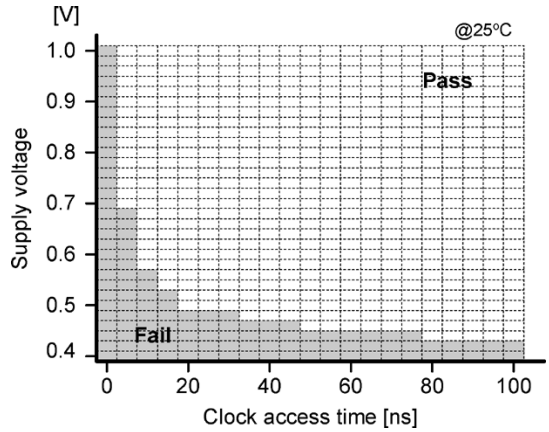

Fig. 13. Shmoo plot.

TABLE I
MACRO CHARACTERISTICS

Organization:	4Kword x 16b
Clock access time:	1.2 ns, at 1.0 V
	20 ns, at 0.5 V
Power consumption:	12.9 mA/GHz, at 1.0 V
Supply voltage:	1.0V to 0.44 V
Process technology:	90-nm ASPLA CMOS, NMOS Vth: 0.32V, PMOS Vth: -0.33V
Macro size:	0.4 mm x 0.7 mm

E. Bit-Line Replica Circuit

In our proposed 7T-cell, a Node V2 voltage of "0" is retained by parasitic capacitance during "1" Read. Therefore, if the activated period of WL were longer than the data retention time of V2 = "0", the storage data would be destroyed due to the charging of Node V2 by the leakage current of pMOS transistor P2. On the other hand, if the activated period of WL were shorter than the BL delay time, Read operations could not be completed. That is why, in order to achieve stable Read operations, the relationships expressed in (1) below should be maintained in the driving of the WL.

$$\text{BL delay time} < \text{WL pulse width} < \text{Retention time of V2} = \text{"0"} \quad (1)$$

BL delay time is 0.2 ns@1 V. When the capacitance of Node V2, the leakage current of P2 and the Vth of nMOS transistor N1 are, respectively, 1.0 fF, 10 nA and 0.32 V, the retention time of Node V2 will be 32 ns ($= 1.0\,\text{fF} \times 0.32\,\text{V}/10\,\text{nA}$), far larger than the BL delay time. In order to satisfy (1), WL is controlled by using a BL replica circuit [10]. Unlike with a conventional SRAM, with our SRAM the accuracy of the BL replica circuit does not influence access time. In addition, since the BL voltage level changes from VDD to GND in our SRAM, the BL replica circuit is easier to design than it would be for a conventional SRAM.

IV. CHIP FABRICATION AND MEASUREMENT RESULTS

For the purpose of confirming that the SRAM macro works correctly, we used a 90-nm CMOS process technology to fabricate the 64-kb SRAM macro shown in Fig. 12(a) and (b). Fig. 13 and Table I show the measurement results obtained for

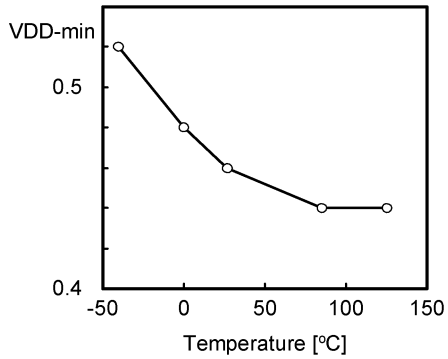

Fig. 14. VDD-min dependence on temperature.

the macro. As shown in the shmoo plot, both a minimum supply voltage (VDD-min) of 440 mV and a 20 ns access time are achieved with a 0.5 V supply voltage. In our SRAM, VDD-min is limited by the following two factors: 1) Write operations at low-VDD levels cannot be performed, since write margin decreases with decreasing VDD, and 2) Read operations at low-VDD levels result in storage data destruction in SRAM cells due to the leakage current of pMOS transistor P2. Since BL delay time increases exponentially with decreasing VDD, the relation between BL delay time and data retention time of V2 = "0" is reversed at low-VDD levels.

Fig. 14 shows VDD-min dependence on temperature. Below 85 °C, VDD-min decreases with increasing temperature. This occurs because VDD-min is determined by factor 1). Write margin, unlike Read SNM, improves with decreasing Vth levels in nMOS transistors, and Vth decreases with increasing temperature. VDD-min, which will not improve even if the temperature exceeds 85 °C, will be determined by factor 2). The leakage current of pMOS transistor P2 increases with increasing temperature. This reverses the relationship between BL delay time and retention time. Since both Write margin and SRAM cell current improve with decreasing Vth levels in nMOS transistors, it will be possible to achieve even higher speeds and lower-VDD operations by reducing Vth levels below 0.32 V, the value currently achieved.

V. Conclusion

In order to overcome the SNM problem encountered with conventional six-transistor SRAM cells and to avoid the area overhead of conventional eight-transistor SRAM cells, we have developed a read-SNM-free seven-transistor SRAM cell. Dynamic inverter-loop-cutting helps achieve Read SNM without causing degradation of SRAM cell current, while need for the addition of just a single transistor for loop-cutting making it possible to reduce area overhead from 30% to 13%. We have fabricated a 64-kb SRAM macro using 90-nm CMOS technology and have obtained, with a 0.5-V supply, a minimum VDD of 440 mV, and a 20-ns access time.

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