A Novel Low Power SRAM/SOI Cell Design

Abstract

A four transistor (4T) Self-Body-Bias (SBB) structured SRAM/SOI cell is proposed. The structure improvements and its parameters' specifications are based on its performance simulations on TSUPREM4 and MEDICI. The structure saves area and simplifies its process by using the parasitic resistor beneath the gate of NMOS to supersede PMOS of conventional 6T CMOS SRAM. Furthermore, this structure can safely operates with 0.5 V supply voltage, which may be prevalent in nearby future. Finally, compare to conventional 6T CMOS SRAM, this structure's transient responses are normal and it has 10 times lower power dissipation.

Keywords: *4T SRAM, Self Body Bias, Low power*

1. Introduction

SOI technology is broadly used in IC designs, nowadays. Its performance is merited with low power dissipation, low noise, high rejection to radiation, and no latch-up effect in contrast with conventional CMOS technology[1]~[3]. Thus, SRAM cell's performances can be enhanced based on SOI technology.

In an attempt to reduce power dissipation and layout area, many researches have done to change classic 6T SRAM cell into 4T one. Some are based on circuit level modifications, but their stabilities are always poor[4]~[7]. Others are based on device modifications, but their processes are always too complicated[8][9]. In this paper, a novel 4T SRAM cell is presented based on Self-Body-Biased (SBB)[10] and Dynamic Threshold MOS (DTMOS)[11][12] structures. Except that 6T SRAM model and simulations are based on Cadence tool suits, other models are constructed using TSUPREM4, and devices' simulations are based on MEDICI.

In section 2, the basic structure and mechanism of SBB structure SRAM cell is introduced

In section 3, the stability of the SBB structure is analyzed. It proves that the 4T SRAM cell can be safely operated with 0.5 V supply voltage. Conclusion is also made that further improvement of the parasitic resistor will not change function of normal NMOS.

In section 4, the gate voltage controlled resistor is optimized by changing p- area's length, thickness, and impurity concentration, as well as by ion implanting the NMOS channel.

In section 5, transient analyses are described. It is concluded that in contrast with conventional 6T SRAM cell, this design has a bit slower transfer speed but great lower power dissipation.

In section 6, A different SBB structure is proposed. It has smaller cell area and similar characteristics to H-gate one.

In section 7, both the two structure's layouts are displayed.

2. Basic Structure and Mechanism

Figure 1 displays the plan view of the SBB SOI MOSFET with an H-shaped gate[13] electrode, figure 2 shows the cross-section view of AA' direction marked in figure 1, and figure 3 is its equivalent circuit. A parasitic body resistor beneath the gate from terminal BODY1 to terminal BODY2 marked in figure3 generally functions like a PMOS. One part of the resistor area is doped more lightly than the other part, thus, when a high voltage is applied to gate, the p- area quickly depletes, thereby greatly enhancing the resistance and shut down current between BODY1 and BODY2, as shown in figure 4[10]. The whole SRAM cell circuit is demonstrated in figure 5.

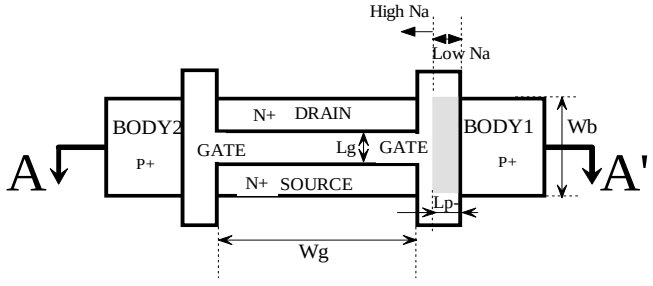

Fig. 1 Plan view of H-gate SBB SOI MOSFET

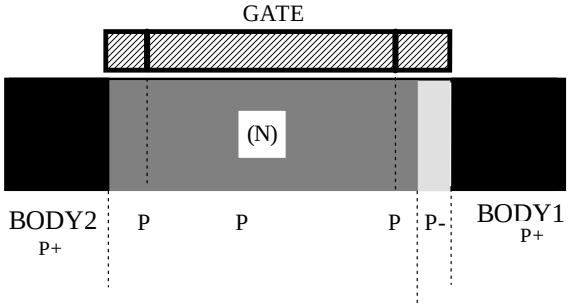

Fig. 2 Cross-section view of H-gate SBB SOI MOSFET

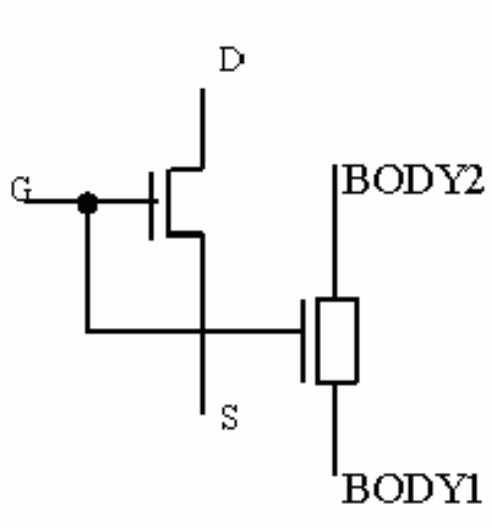

Fig.3 Equivalent circuit of SBB structure

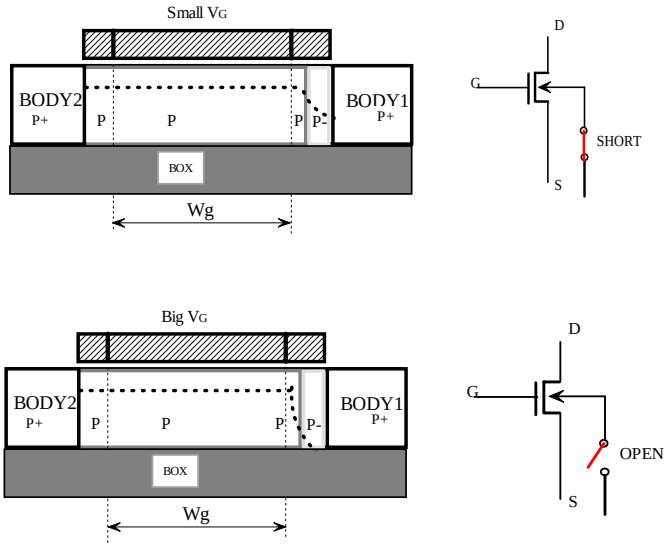

Fig. 4 Operation of the parasitic resistor

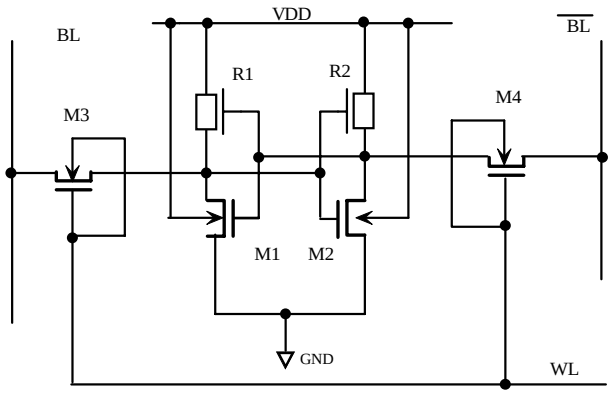

Fig.5 Proposed 4T SRAM cell circuit

In figure 5, transistors M3 and M4 have their substrates tied to gates, therefore, the back-gate effect of the two transistors cause the threshold voltage varies with the gate voltage. This kind of MOS structure is named Dynamic Threshold MOS or DTMOS. DTMOS's on-state threshold voltage is low and off-state one is high. This attribute facilitates the transfer speed of the device. The limitation of DTMOS is that the maximum gate voltage should be no higher than 0.5V to guarantee that no current flows through PN junction between substrate and source. Because this research is based on 0.5V supply voltage, the application of DTMOS is safe and effective.

3. Stability Analysis of Basic Structure

One problem must be resolved before further research. In conventional 6T SRAM cell, the substrate of NMOS should be tied to ground or connected to source. However, in the proposed H-gate NMOS, current flows through the substrate beneath the gate, and BODY2 terminal of the substrate is tied to VDD. Therefore, there might be disastrous current flowing from substrate to source, although the supply voltage is only 0.5V. Thus, characteristics of PN junction under 0.5V forward voltage are simulated using MEDICI. Table 1 shows the result of the relationship between forward current and temperature. It reveals that if current flowing between BODY2 and BODY1 is larger than several nano Amps, the influence of current flowing between BODY2 and source can

be omitted.

Table 1 Forward PN junction currents at various temperatures

T（K）	I（A/um）
300	9.46×10^{-11}
310	2.46×10^{-10}
320	5.84×10^{-10}
330	1.35×10^{-9}
340	2.99×10^{-9}
350	6.31×10^{-9}

Another problem should also be cared about. In the cell schematic, BODY2 is connected to 0.5V, and BODY1 varies from 0.5V to a value near 0V. Whether this variation affects the NMOS is also simulated. Figure 6 and 7 [14][15]illustrate the Log(I_{DS})-V_G and the I_{DS}-V_{DS} relationships of the NMOS with SBB structure. Apparently, the variation of BODY1 voltage does not change the characteristics of NMOS, the operation of the parasitic resistor and the operation of the H-gate NMOS are independent. This conclusion definitely facilitates further research.

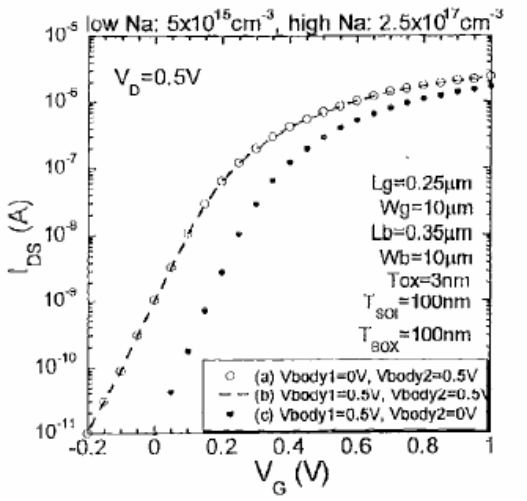

Fig.6 V_G dependence of I_{DS} of the proposed device with (V_{BODY1},V_{BODY2}) configuration

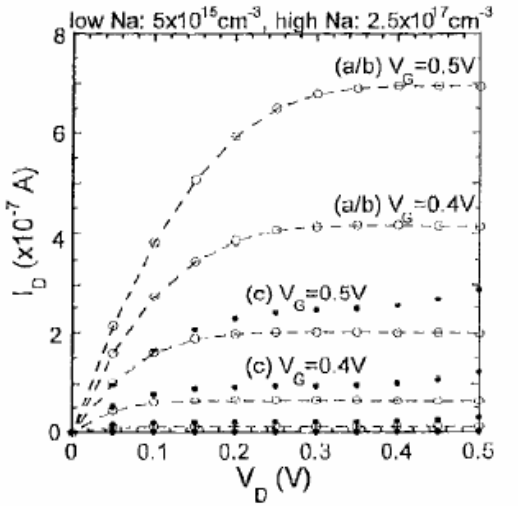

Fig.7 I_{DS}-V_{DS} relationship with the same (V_{BODY1},V_{BODY2}) configuration in Fig.6

4. Structure and performances of the Parasitic Resistor

Since modification of parasitic resistor parameters does not influence performance of the NMOS, and because NMOS/SOI structure is mature enough in technology nowadays, the main purpose of this paper is to describe several skills that optimize performance of the resistor other than the NMOS or the DTMOS.

4.1 p- concentration's influence on performances

Figure 8 demonstrates the V_G dependence of current flowing through the resistor under conditions of various p- area boron concentrations. Lb is the length of p- area and assumed to be fixed as 0.30 um. The conductivity of the resistor varies greatly if the impurity concentration of the p- area changes. Curve *e* and curve *f* indicate that, if the impurity concentration is too high, the resistance can not be controlled by the gate voltage. And Curves *a*, *b* and *c* prove that if the impurity concentration is too low, even the on-state current can be as low as several nano Amps, which is comparable to PN junction forward current. It is concluded that if other parameters are fixed,

the p- area impurity concentration can be designed to make the resistor perform like a PMOS.

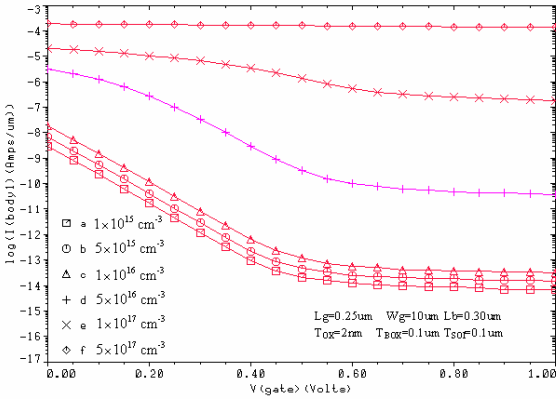

Fig. 8 $I_{body2\text{-}body1}$—V_G relationship with different impurity concentrations in p- area

4.2 p- length's influences on performances

Simulation results of p- area length's influence on the performance of the resistor are displayed in figure 9. With the variation of factor *Lb*, the off state current changes much faster than the on state current. If on state current doubles, the on/off current ratio may decline 10 times. This relationship of compromise causes certain difficulty in device improvements.

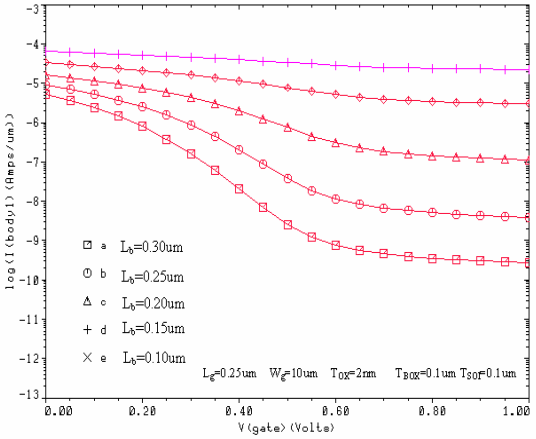

Fig. 9 $I_{body2\text{-}body1}$—V_G relationship with variation of length of p- area

4.3 p- thickness' influences on performances

The simulations above indicate that the parasitic resistor's performance is determined primarily by the impurity concentration in the p- area. And the compromising relationship mentioned above makes the device's characteristics hard to be improved. Thus, a third degree of freedom is required for further improvements——the thickness of p- area. In simulations above, the thickness of p- area is 0.1 um, the same value as the epitaxy layer. This parameter can also be adjusted.

To ensure that the p- area can be pinched off under 0.5V gate voltage, the thickness of this area has a maximum value *dmax*.

$$dmax=\left[\frac{2\varepsilon_0\varepsilon_{Si}V_G}{qN_A}\right]^{1/2} \qquad (1)$$

The following results can be derived from function 1, while N_A is the impurity concentration of p- area:

⑴When $N_A=10^{15}cm^{-3}$, $d_{max}=0.8\ \mu m$

⑵When $N_A=10^{16}cm^{-3}$, $d_{max}=0.25\ \mu m$

⑶When $N_A=6.6\times10^{16}cm^{-3}$, $d_{max}=0.1\ \mu m$

⑷When $N_A=2.5\times10^{17}cm^{-3}$, $d_{max}=0.05\ \mu m$

The theory is that if the p- area is doped with impurity concentration as high as $2.5\times10^{17}cm^{-3}$, the p- area will not be fully depleted under 0.5V controlling voltage. Local Oxidization is applied on the p- area using a wet oxidization for about 20 minutes, then, the SiO_2 are removed leaving shapes around former p- area like figure 10. The surface of the p- area is smooth and it has a thickness of 0.05 um at its thinnest point marked *Hlow* in figure 10. It is assumed that the equivalent p- area after oxidization is defined to be area that has its thickness smaller than 0.075, as shown in figure 10. Figure 11 displays the $I_{body2\text{-}body1}$—V_G relationship with 4 different p- area impurity concentrations, assuming that the equivalent length of p- area (*Lb*) equals 0.3 um. Figure 12 displays the $I_{body2\text{-}body1}$—V_G relationship with various value of *Lb*, assuming that the impurity concentration of p- area is 10^{17} cm^{-3}. Curve *c* in figure 12 may be the best situation so far, it has on-state current close to 10 micro Amps and several nano Amps off-state current, which is similar to characteristics of NMOS/SOI shown in figure 6.

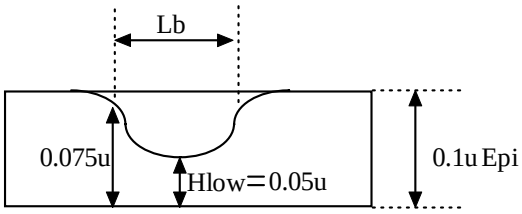

Fig. 10 P- shape after local oxidization

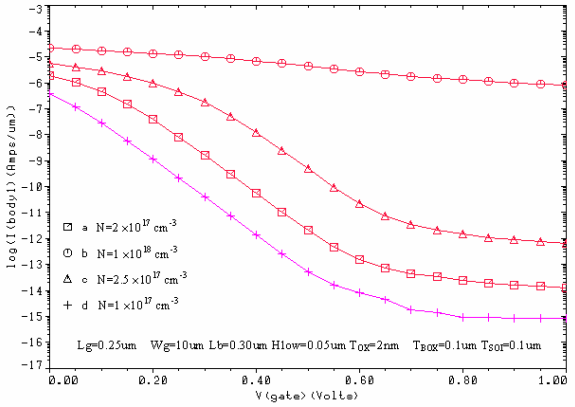

Fig. 11 $I_{body2\text{-}body1}$—V_G relationship with various p- area impurity concentrations

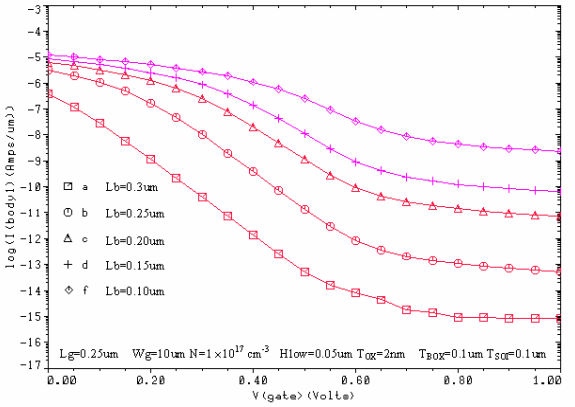

Fig. 12 $I_{body2\text{-}body1}$—V_G relationship with various equivalent p- area length

4.4 Improvement of p area beneath the gate

After steps above, the impurity concentration of p- area becomes comparable to that of p area, as shown in figure 13.The length of p area is 1 um, because the W/L of the NMOS is 1u/0.25u. Therefore, the total resistance between BODY1 and BODY2 decreases if the impurity concentration of p area increases. However, increasing the impurity concentration of p area affects the threshold voltage of NMOS/SOI, because this p area is the exact channel of NMOS. Thus, Ion implantation is used to create a buried channel to avoid this contradiction. Figure 14 is the channel impurity concentration curve after ion implantation. Figure 15 demonstrates that the threshold voltage of NMOS is normally between 0.1V and 0.2V, and figure 16 illustrates that the characteristics of the parasitic resistor are enhanced by ion implantation.

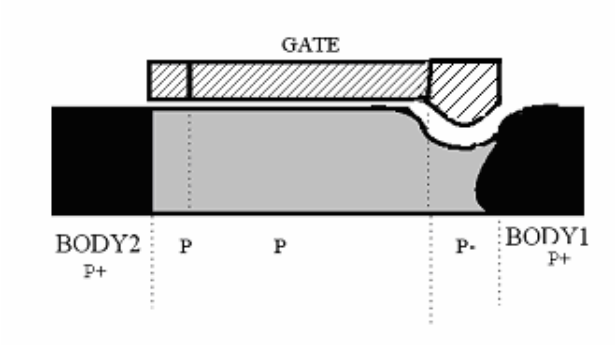

Fig. 13 The impurity concentration of p- area is comparable to that of p area

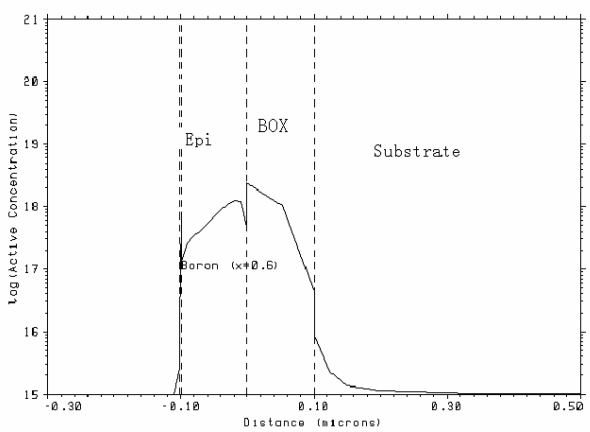

Fig. 14 P channel impurity distribution after ion implantation

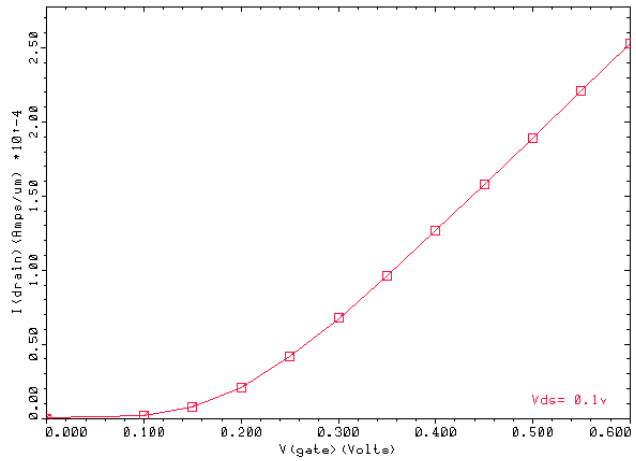

Fig. 15 I_{ds}—V_G relationship of NMOS after channel ion implantation

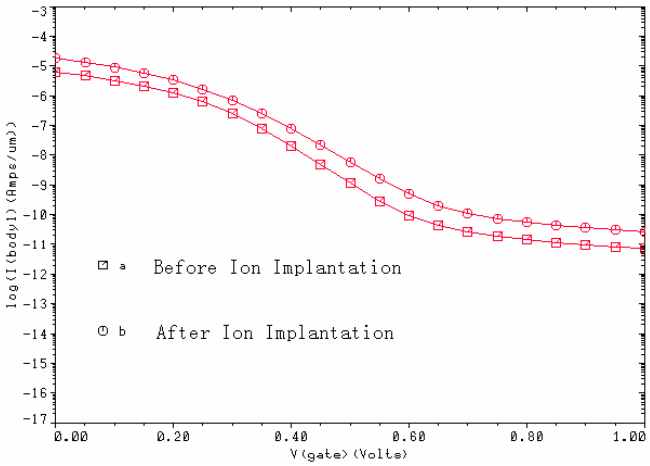

Fig. 16 Gate voltage dependence of resistor characteristics compare

5. Analyses of Total SRAM Cell

After kinds of improvements above, all the parameters of the SBB structure are fixed, transient analysis of the total SRAM cell is simulated using *MEDICI* according to schematic in figure 5.The transfer characteristics described in figure 17 shows that the 4T SRAM cell functions normally. In an attempt to compare with normal 6T SRAM cell, schematic like figure 18 is constructed using *Composer Schematic* in *Cadence ICFB* environment. 0.18 um technology is used, the supply voltage is 1.2V, the W/L of M1, M2, M3 and M4 are 1u/0.25u, the W/L of the two PMOS are 2u/0.25u. This schematic tests the transient response of SRAM when writing data into the cell. A pulse stimuli is add to pin Vin, the initial voltage of node Vout2 is 1.2V, 3 terminals' transient currents that have circle mark in figure 18 are to be plotted in order to calculate the cell's power dissipation.

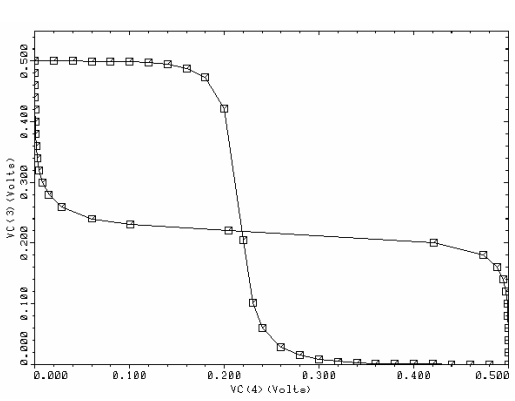

Fig. 17 Transfer curve of the 4T SRAM cell

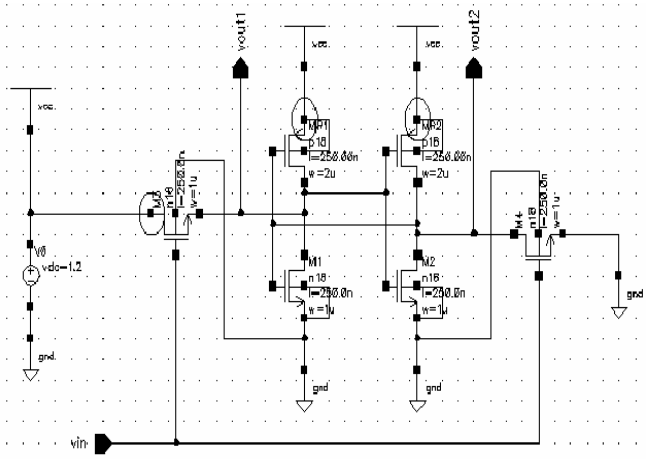

Fig.18 schematic of conventional 6T SRAM cell

As shown in figure 19, the writing delay of the conventional 6T SRAM is about 250 pico second. The total current is integrated in 1 nano second's simulation time, the result is 25 femto Amp*s. Thus the power dissipation is 30 uW at 1.2V supply voltage.

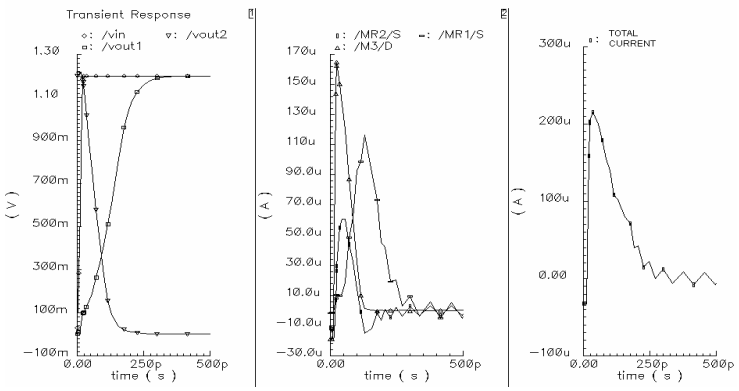

Figure 19 transient response of conventional 6T SRAM

Similar simulation on 4T SRAM with proposed structure produces results in figure 20. The writing delay is 500 pico second and its power dissipation is 3.3 uW.

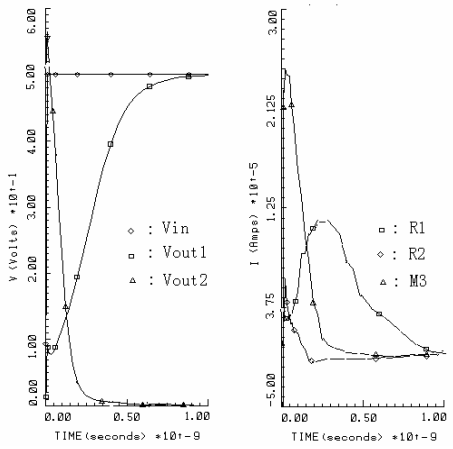

Fig. 20 Transient voltage and current of proposed 4T SRAM

The schematic in figure 21 simulates situation when reading data out of conventional 6T SRAM cell. Initial voltage conditions are marked in the schematic. The cell's output capacitances are simulated by M5 and M6 with their W/Ls equal to 2u/1u. The transfer delay is 200ps, and the power dissipation is 11.9uW. In contrast, based on

MEDICI simulation, the proposed 4T SRAM cell's transfer delay is 500ps, and its power dissipation is 1.7uW.

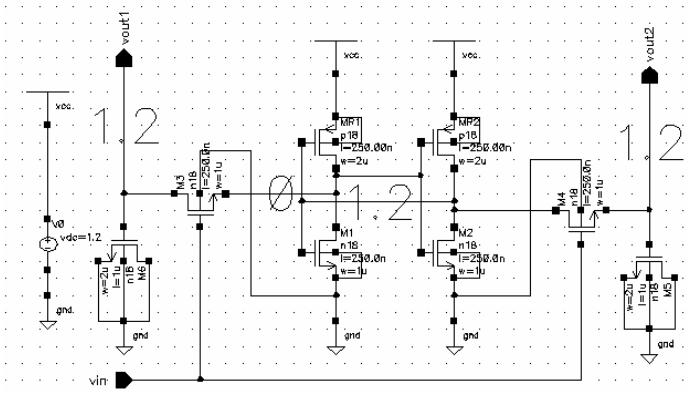

Fig. 21 Schematic of 6T SRAM cell in data reading state

Thus, whenever in state of writing or reading, the proposed 4T SRAM cell has its power dissipation 10 times less than conventional 6T SRAM cell, only at cost of doubling the transfer delay of 6T one.

6. Another SBB Structure Proposition

As shown in figure 22, this structure has no p- area, it uses the NMOS channel beneath the gate as the only part of the voltage controlled resistor. As described in figure 23, this structure's epitaxial layer is 0.07 um thick, the surface channel impurity concentration after ion implantation remains 10^{15} cm^{-3}, thus, according to function (1), the channel is fully depleted when 0.5V voltage is applied to the gate. Therefore, it is an FDSOI[16][17] device. Theoretically, as the gate voltage shifts from 0V to 0.5V, the resistor's resistance goes from zero to infinity. In practical situations, the resistor's performance is displayed in figure 24. And figure 25 shows that the NMOS's threshold voltage is about 0.14V.

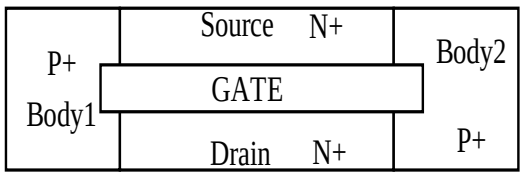

Fig. 22 Plan view of structure without p- area

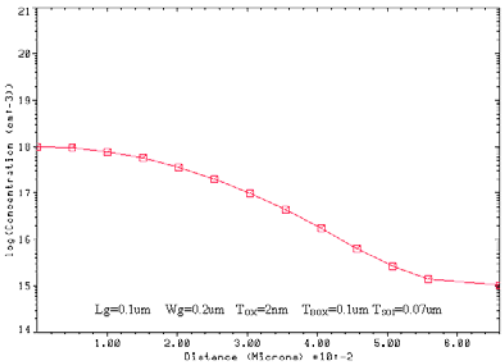

Fig. 23 Channel impurity distribution of structure without p- area

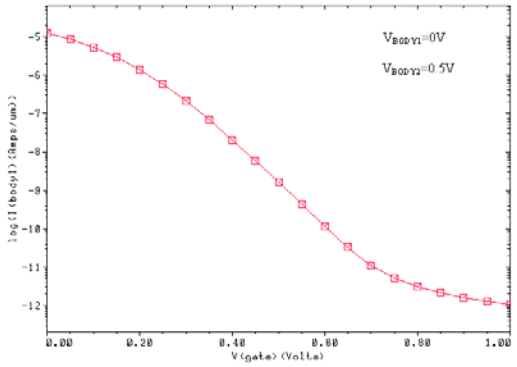

Fig. 24 Characteristics of resistor without p- area

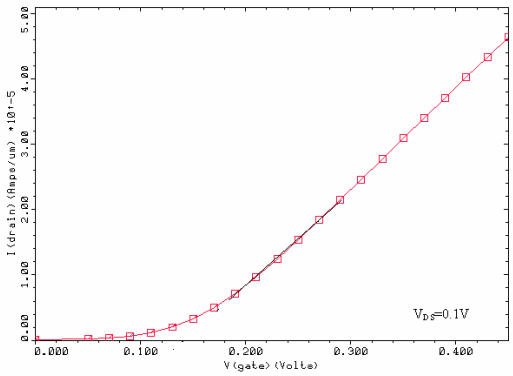

Fig. 25 Threshold voltage test of NMOS without p- area

7. Layout of the SRAM Cell

The layout of the 4T SRAM cell with H-gate SBB structure is demonstrated in figure 26. The p- area is not shown in the structure for reducing complexity. Actually it is located close to *GND* and beneath one terminal of H-shaped gate. The layout of the 4T SRAM cell based on SBB structure without p- area is simply replace the H-shaped gate structure shown in figure 24 and figure 27 (b) with the T-gate structure in figure 27 (a). Apparently, the T-gate SBB structure SRAM cell has less area than the H-gate one.

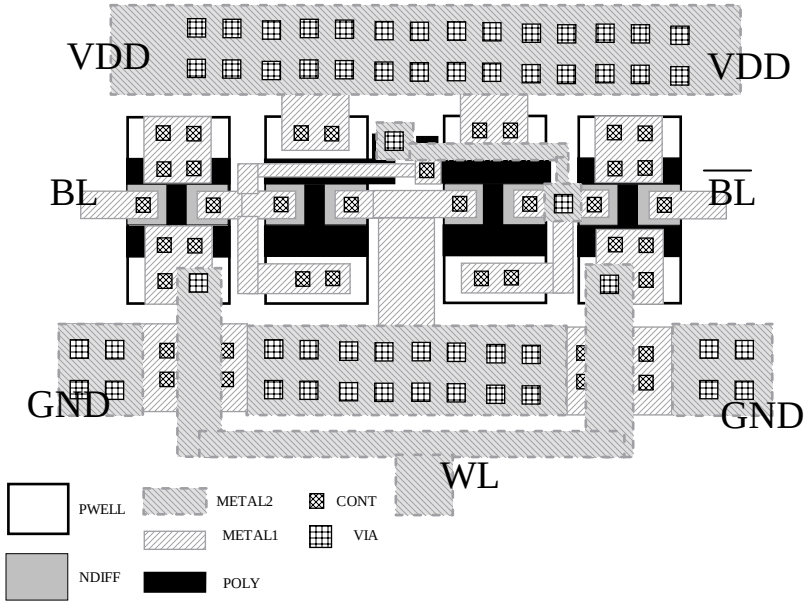

Fig. 26 Layout of the proposed 4T SRAM cell

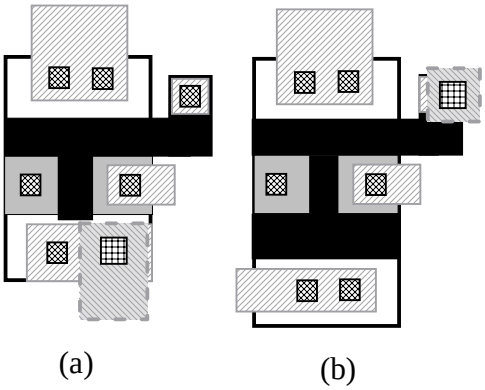

Fig. 27 T-gate structure (a) has less area than H-gate structure (b)

8. Conclusion

Stability analyses of basic SBB structure is proceeded to ensure that the parasitic PN junction will not affect the function of the SBB structure under 0.5V supply voltage.

The p- area of the gate-controlled resistor is the bottleneck of the device performance. Thus, adjustments of p- area are illustrated including impurity concentration adjustment, length alteration and thickness modification. The bottom of NMOS channel is also implanted with boron to enhance the resistor's performance. Finally, the resistor has 1000 on/off ratio with the shifting of gate voltage, and its on-state current is comparable to that of NMOS.

Transfer speed and power dissipation is analyzed by comparing the designed 4T SRAM cell with conventional 6T one. Although the transfer speed of the 4T cell is a bit slower, the power dissipation is vastly reduced.

Considering the extremely low power dissipation, the small area of the cell as well as the advantage of SOI, this design is prominent and prospective when 0.5V supply voltage is prevalently in use.

References

[1] J.B. Jacobs, et al., **"**Short channel effects and delay hysteresis for 0.25 μm SOI technology with minimal process changes from the bulk technology" ***IEEE Int. SOI Conference, 1998, pp. 111-112***

[2] Fransis P, et al., "SOI technology for high-temperature applications" ***Tech. Digest IEDM, Dec. 1992, pp. 353***

[3] Bruel M, "Silicon on Insulator material technology" ***Electronics Lett, Vol.31, No.14, 1995, pp.1201-1202***

[4] K. Noda, et al., " A loadless CMOS four-transistor SRAM cell in a 0.18-μm logic technology" ***Electron Devices, IEEE Transactions on Volume 48, Issue 12, Dec. 2001, pp. 2851-2855***

[5] Thomas, O et al., " Stability analysis of a 400 mV 4-transistor CMOS-SOI SRAM cell operated in subthreshold" *Electron Devices and Solid-State Circuits, IEEE Conference on 16-18 Dec. 2003 pp. 247-250*

[6] Amara, A. et al., " An SOI 4 transistors self-refresh ultra-low-voltage memory cell" *Circuits and Systems, 2003. ISCAS'03 Proceedings of the 2003 International Symposium on Volume 5, 25-28 May 2003 pp.V_401-V_404*

[7] Thomas, O. et al., " Ultra Low Voltage Design Considerations of SOI SRAM Memory Cells" *Circuits and Systems, 2005. ISCAS 2005. IEEE International Synposium on 23-26 May 2005 pp. 4094-4097*

[8] K. Osada, et al., "A 0.13-/spl mu/m, 0.78-/spl mu/m/sup 2/ low-power four-transistor SRAM cell with a vertically stacked poly-silicon MOS and a dual-word-voltage scheme" *VLSI Circuit, Digest of Technical Papers, 2004 Sympusium on 17-19 June 2004, pp.60-63*

[9] A. Kotabe, et al., " A low-power four-transistor SRAM cell with a stacked vertical poly-silicon PMOS and a dual-word-voltage scheme**"** *Solid-State Circuits IEEE Journal of Volume 40, Issue 4, April 2005, pp. 870-876*

[10] M. Terauchi, K. Terada, Proc. "`Self-body-biased' SOI MOSFET through `depletion isolation effect'" *IEEE International SOI Conference, 1999, pp.36-37*

[11] F. Assaderaghi, et al., **"**A dynamic threshold voltage MOSFET (DTMOS) for very low voltage operation**"** *Electron Device Letters, IEEE Volume 15, Issue 12, Dec. 1994 Page(s):510 - 512*

[12] Chun-Yen Chang, et al., "high-performance and high-reliability 80-nm gate-length DTMOS with indium super steep retrograde channel" ***Electron Devices, IEEE Transactions on Volume 47, Issue 12, Dec. 2000 pp.2379-2384***

[13] Bernstein K, et al., "SOI circuit design concepts" ***Norwell: Kluwer Academic Publishers, 2000:22***

[14] S. Funakoshi, et al., " Design guideline and performance prediction of `SBB' SOI MOSFETs" *IEEE International SOI Conference, Oct. 2000, pp. 52-53*

[15] M. Terauchi, "A novel 4T SRAM cell using 'self-body-biased' SOI MOSFET structure operating at 0.5 volt" *IEEE International SOI Conference, Oct. 2000, pp. 108-109*

[16] Chunshan Yin, et al., "Design guideline and performance prediction of `SBB' SOI MOSFETs" *Electron Devices Meeting, 2001. Proceedings. 2001 IEEE Hong Kong 30 June 2001 pp.89-92*

[17] Sang-Su Kim, "The drive currents improvement of FDSOI MOSFETs with undoped Si epitaxial channel and elevated source/drain structure" *SOI Conference, 2000 IEEE International 2-5 Oct. 2000, pp.74-75*