A Novel High Density, Low Voltage SRAM Cell with a Vertical NDR Device

Farid Nemati and James D. Plummer
Center for Integrated Systems, Stanford University, Stanford, CA 94305

Abstract

A novel $8F^2$ NDR-based cell for giga-scale SRAMs on silicon substrates is presented. The new SRAM cell uses a thin vertical PNPN structure with gate-assisted turn-off and turn-on mechanisms. Experimental measurements show standby cell currents lower than $10pA/\mu m^2$, switching speeds faster than 40ns, and operating voltages as low as 1.5V. An SRAM based on this new cell is comparable in cell area, standby current, architecture, speed, and fabrication process to a DRAM of the same capacity. To our knowledge, this cell has the lowest standby power consumption reported so far for an NDR-based SRAM cell either on silicon or on III/V substrates [1][2].

Introduction

The design of high density SRAMs has been limited by the large area of the conventional six-transistor and four-transistor cells. The number of elements per cell, and therefore the cell area, can be considerably reduced by using Negative Differential Resistance (NDR) devices. Unfortunately, most of the NDR devices introduced so far suffer from problems such as high standby power consumption, high operating voltages, low speeds, or complicated fabrication processes. In this work, a novel NDR-based SRAM cell is introduced. The new cell consists of only two elements, has an $8F^2$ footprint, can operate at high speeds and low voltages, has a good noise-margin, and is compatible in fabrication process with main-stream CMOS.

The New SRAM Cell Concept

PNPN devices can have excellent on/off current ratios and a low holding current in the on state. The problem with PNPN devices is their very slow turn-off due to the saturation of their junctions in the on state. Also, relatively high voltages are usually needed for the turn-on of a PNPN device. Our NDR device uses a surrounding gate around a thin vertical PNPN structure to solve these problems.

Fig. 1 shows the structure of the new cell. The vertical gated PNPN is defined on top of the source or drain of the planar pass transistor. The vertical gate serves as a second word-line (WL2) which is only used during the write operations. Fig. 2 shows the circuit diagram of this new two-element SRAM cell. Fig. 3 shows the equivalent circuit models of the cell. The PNPN can be modeled by its well-known two BJT equivalent. Fig. 4 shows the DC load-line diagrams of the cell based on the DC circuit model in Fig. 3a. At DC and low frequencies (Fig. 3a), the surrounding gate of the PNPN is modeled as a vertical MOSFET connecting the base of the PNP to the bit-line via the pass transistor. In the standby mode (Fig. 4a), the pass transistor is only partially on, providing the low standby current of the cell. The on-state standby current of the cell can be kept within a decade above the holding current of the NDR device, assuming a typical 50mV total on-chip variation in the threshold voltage of the pass transistor. In the read mode (Fig. 4b), the pass transistor is on and the bit-line is charged with a very large or very small current for logical "One" or logical "Zero" states, respectively. Because of the very large current that the PNPN can provide in its on state, the read operation is very fast. When WL2 is high, the forward break-over voltage of the PNPN decreases to very small values because the PNP transistor turns on (Fig. 4c).

At high frequencies, the equivalent circuit model of the cell can be simplified to a capacitive coupling between WL2 and the P region of the PNPN (Fig. 3b). Fig. 5 shows the waveforms of the word-lines and the bit-line for all the read and write operations. For the write "One", the rising edge of the pulse applied to WL2 forward-biases the NPN transistor by capacitive coupling and starts the regenerative process in the PNPN which turns the device on. For the write "Zero", BL is high and the falling edge of the pulse on WL2 pulls out all the minority charge of the middle junction of the PNPN via capacitive coupling. Therefore, the PNPN quickly turns off. These gate-assisted turn-on and turn-off mechanisms do not directly depend on the generation and recombination lifetimes of the minority carriers in the PNPN and therefore are fast and reliable. MEDICI device simulations of the cell show that the write operations can be carried out in about 30ns even when the carrier lifetimes are assumed to be greater than 100ns.

The cell structure is similar to a stacked-capacitor DRAM cell with the capacitor being replaced by the NDR device. The NDR device can be fabricated either before the planar device by etching silicon pillars and ion-implantation or after the planar device, e.g., by selective epitaxial growth techniques. The architecture of the cell array is essentially similar to DRAMs. Fig. 6 shows a cell array layout based on this new cell.

Experimental Results

The vertical NDR device was fabricated by etching silicon pillars and defining the P and N regions by ion-implantation and diffusion. An anisotropic poly etch was used to form the surrounding poly gate. Fig. 7 shows the cross-section of a fabricated 0.2μm thick device with the approximate location of the junctions.

Fig. 8 shows the measured DC characteristics of a typical NDR device. The holding current of the cell is less than 10pA for a 5μm by 0.2μm device. With Vref set to only 1V, the on/off current ratio for the read operation is more than 6 orders of magnitude, enabling high speed, low voltage operation. The forward break-over voltage of the PNPN vanishes as the gate voltage is increased to 1V, as predicted by the DC model of the cell.

Our transient measurements show that the device can be switched on and off within 40ns. At this speed, we are limited by the bandwidth of our test setup. Further work, to improve the bandwidth of our measurements, is currently underway so as to determine the ultimate switching speed of the device.

Summary

A novel $8F^2$ NDR-based SRAM cell is introduced. The operation of this new cell concept is verified by device simulations and experimental measurements. Small cell area, low voltage operation, acceptable standby power, good speed, and compatibility with main-stream CMOS make the new cell an ideal candidate for giga-scale SRAMs. The projected standby current of a 1Gbit SRAM in a 0.2μm technology, based on this new cell, is less than 10mA which is comparable to the standby current of a 1Gbit DRAM [3].

Acknowledgments

The authors wish to thank Dr. C.P. Auth and H.J. Cho for their suggestions and help during device fabrication. The funding of this project by DARPA (COSIN program) is gratefully acknowledged.

References

[1]- T.K. Carns et al, Elec. Dev. Letters, June 1995, p. 256
[2]- P.V. Wagt et al, IEDM tech. Dig., 1996, p. 425
[3]- K.N. Kim et al, VLSI Technology Tech. Dig., 1997, p. 9

0-7803-4700-6/98/$10.00 (c) 1998 IEEE

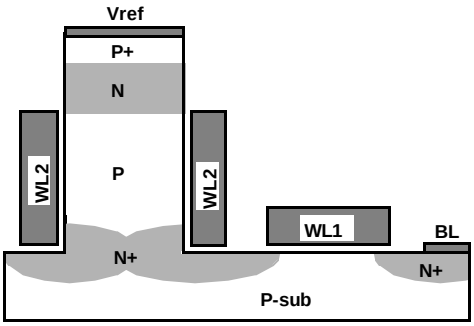

Fig. 1: The new SRAM cell structure. WL2 is a vertical surrounding gate.

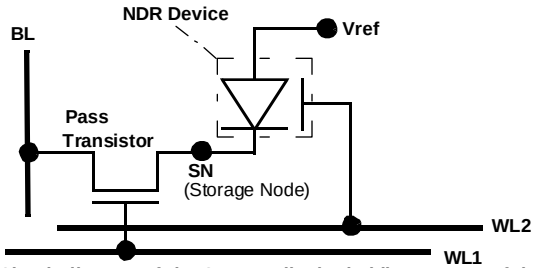

Fig. 2: Circuit diagram of the SRAM cell. The holding current of the NDR device, in the standby on state, is provided by the sub-threshold current of the pass transistor at V_{GS}=0.

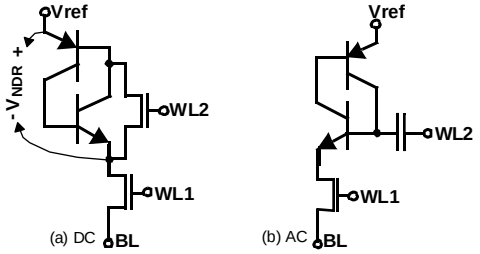

Fig. 3: DC and AC equivalent circuit models of the SRAM cell. The capacitive coupling between WL2 and the P region is used for the fast switching of the NDR device.

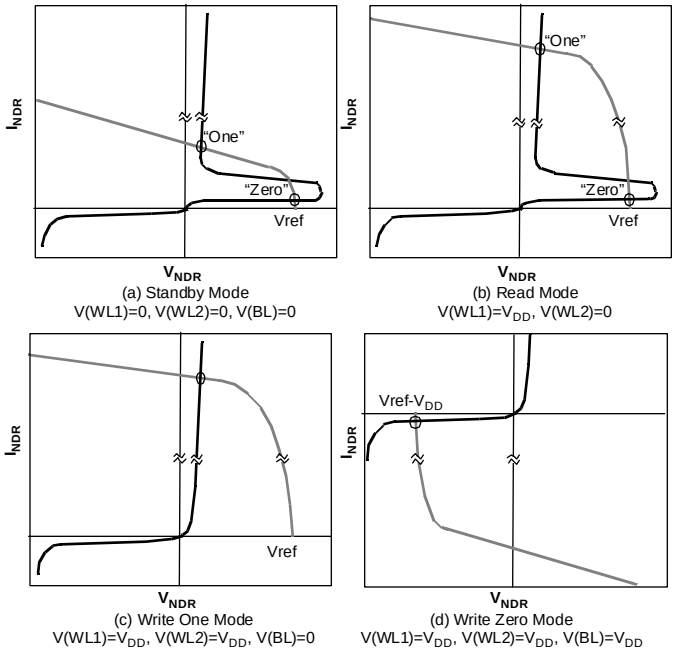

Fig. 4: DC Load-line diagrams of the SRAM cell in all the possible modes. Solid lines shows the NDR device and dashed lines show the pass transistor. The circles indicate the stable states of each mode.

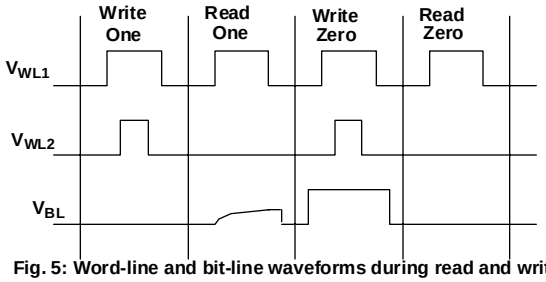

Fig. 5: Word-line and bit-line waveforms during read and write.

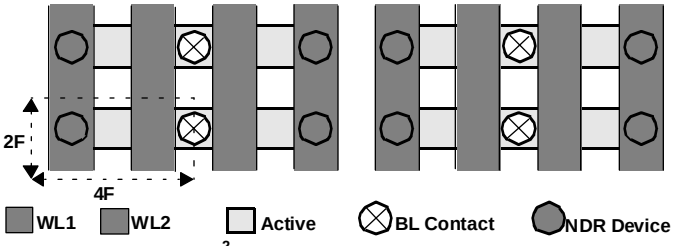

Fig. 6: Layout of the $8F^2$ SRAM cell in an open bit-line architecture. WL2 is not defined in the actual layout and is formed by poly spacer etch.

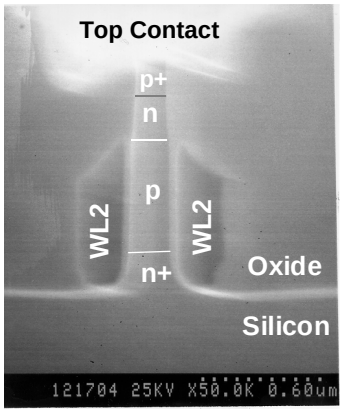

Fig. 7: Cross-sectional SEM image of a 0.2μm thick NDR device.

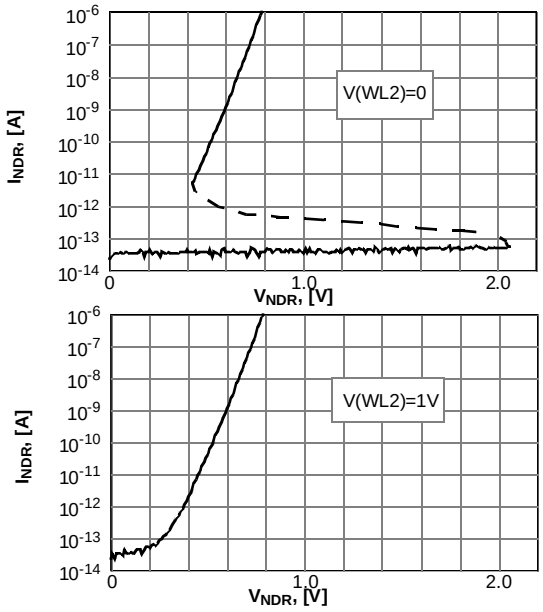

Fig. 8: Measured I-V characteristics of a typical NDR Device for various gate voltages. The holding current of the device in the standby on state is less than 10pA. The area of the device is 0.2μm X 5μm.