A Novel Four-Transistor SRAM Cell with Low Dynamic Power Consumption

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***Abstract*—**This paper presents a novel CMOS four-transistor SRAM cell for very high density and low power embedded SRAM applications as well as for stand-alone SRAM applications. This cell retains its data with leakage current and positive feedback without refresh cycle. The new cell size is 20% smaller than a conventional six-transistor cell using same design rules. Also proposed cell uses two word-lines and one pair bit-line. Read operation perform from one side of cell, and write operation perform from another side of cell, and swing voltage reduced on word-lines thus dynamic power during read/write operation reduced. The fabrication process is fully compatible with high-performance CMOS logic technologies, because there is no need to integrate a poly-Si resistor or a TFT load. HSPICE simulation in standard 0.25µm CMOS technology confirms all results obtained from this paper.

***Keywords*—**Positive feedback, leakage current, read operation, write operation, dynamic energy consumption.

I. Introduction

SRAMs are widely used for mobile applications as both on-chip and off-chip memories, because of their ease of use and low standby leakage [1], [2]. A six-transistor SRAM cell (6T SRAM cell) is conventionally used as the memory cell. However, the 6T SRAM cell produces a cell size an order of magnitude larger than that of a DRAM cell, which results in a low memory density. Therefore, conventional SRAMs that use the 6T SRAM cell have difficulty meeting the growing demand for a larger memory capacity in mobile applications.

In response to this requirement, our objective is to develop an SRAM cell with four transistors to reduce the cell area size. A thin-film transistor (TFT) load SRAM cell (TFT-load cell) [3], [4] and a four-transistor SRAM cell (4T SRAM cell) [5] can be used to shrink the cell size. However, the TFT used in the TFT-load cell requires a higher supply voltage to improve cell stability, and this does not allow a low-voltage operation of the cell [5]. On the other hand, the 4T SRAM cell [5] with stacked vertical PMOS requires three more additional photo masks and this increased manufactures cost [5]. Furthermore, TFT–load cell [3], [4] and 4T SRAM cell [5] uses differential voltage across its bit-lines during read/write operation. Therefore always there is change on bit-lines. Also this cell uses full swing voltage on word-line and these cause high dynamic energy consumption during read/write operation.

In this paper, we describe a novel four transistor SRAM cell. The novel cell size is 20% smaller than a conventional 6T cell using same design rules. Read operation performed form one side and write operation performed from other side of cell. Also swing voltages reduced on word-lines during read/write operation. Thus the dynamic energy consumption reduced during read and write operation.

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II. Cell Design Concept

Fig. 1 shows a circuit equivalent to a developed 4T SRAM cell using a supply voltage of 2.5V in 0.25µm CMOS technology.

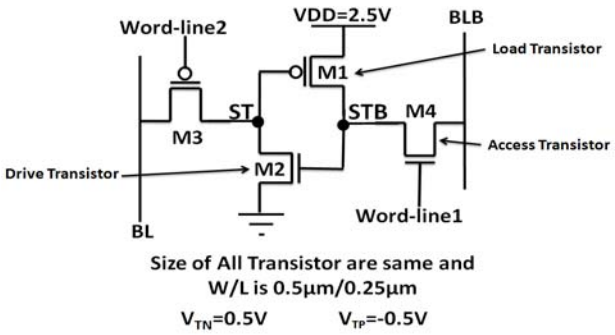

Fig. 1 New 4T SRAM cell in 0.25µm

When '0' stored in cell, load and driver transistor are ON and there is feedback between ST node and STB node, therefore ST node pulled to GND by drive transistor and STB node pulled to V_{DD} by load transistor. And when '1' stored in cell, load and driver transistor are OFF and for data retention without refresh cycle following condition must be satisfied.

$$I_{off-NMOS-access} \geq 3 \times (I_{DS-Load} - I_{G-Driver})$$

$$I_{off-PMOS-access} \geq 3 \times (I_{DS-Driver} - I_{G-Load})$$

For satisfying above condition when '1' stored in cell, we use leakage current of access transistor, especially sub-threshold current of access transistors. For this purpose during idle mode (when read and write operation don't performed on cell) of cell, BL and BLB maintained at V_{DD} and GND,

respectively and word-line1 and wordline2 maintained on V_{Idle1} and V_{Idle2}, respectively. Fig. 2 shows leakage current of cell for data retention when '1' stored in cell. Most of leakage current of access transistors is sub-threshold current since these transistors maintained in sub-threshold condition. Simulation result in standard 0.25µm technology shows if during idle mode of cell, BL and BLB maintained at V_{DD} and GND respectively, and V_{Idle1}=0.5V and V_{Idle2}=1.8V '1' stored in cell without refresh cycle and thus in idle mode above condition satisfied.

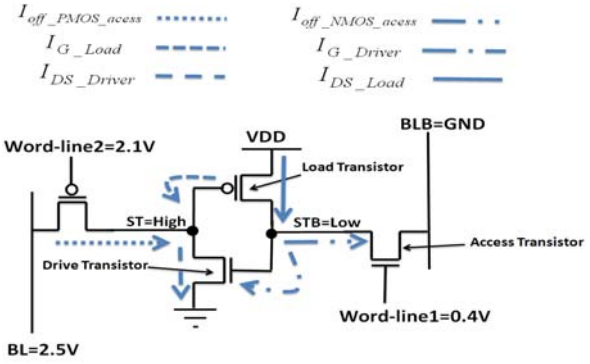

Fig. 2 Novel 4T SRAM cell in idle mode when '1' stored in cell

III. Write and Read Operation

When a write operation is issued the memory cell will go through the following steps.

1) -Bit-line driving: For a write, complement of data placed on BLB, and then word-line1 asserted to V_{DD}, but voltages on word-line2 and BL maintained at idle mode ($V_{word\text{-}line2}$=V_{Idle2} and V_{BL}=V_{DD}).

2) - Cell flipping: this step includes two states as follows.

(a) complement of data is zero: in this state, STB node pulled down to GND by NMOS access transistor, and therefore the drive transistor will be OFF, and ST node will be floated and then pulled up to voltage of BL (V_{DD}) by leakage current (most of this current is sub-threshold current) of PMOS access transistor, and thus load transistor will be OFF.

(b) complement of data is one: in this state, STB node pulled up to V_{DD}-V_{tn} by NMOS access transistor, and therefore the drive transistor will be ON , and ST node will be pulled down to GND, thus load transistor will be ON and STB node pulled up to V_{DD}.

3) - Idle mode: At the end of write operation, cell will go to idle mode and word-line1 and BLB asserted to V_{Idle1} and GND respectively.

When a read operation is issued the memory cell will go through the following steps.

1)-Bit-line Pre-charging: For a read, BL pre-charged to V_{DD}, and then floated. Since, in idle mode BL maintained at V_{DD}, this step didn't include any dynamic energy consumption.

2)-Word-line activation: in this step word-line2 asserted to GND and two states can be considered:

(a) Voltage of ST node is low: when, voltage of ST node is low, the voltage of BL pulled down to low voltage by PMOS access transistor. We refer to this voltage of BL as $V_{BL\text{-}Low}$.

(b) Voltage of ST node is height: when voltage of ST node is height, the voltage of BL and ST node equalized (we refer to voltage of BL in this state as $V_{BL\text{-}High}$). Since in this state, there is very small different between BL and ST node, dynamic energy consumption is very small.

3) -Sensing: After word-line2 deactivate the sense amplifier is turned on to read data on BL. Fig. 3 shows circuit schematic of sense amplifier that used for reading data from new cell.

4) - Idle mode: At the end of read operation, cell will go to idle mode and word-line2 and BL asserted to V_{Idle2} and V_{DD}, respectively.

Fig. 4 shows HSPICE simulated waveform for normal read/write operation of novel 4T SRAM cell in standard 0.25µm CMOS technology.

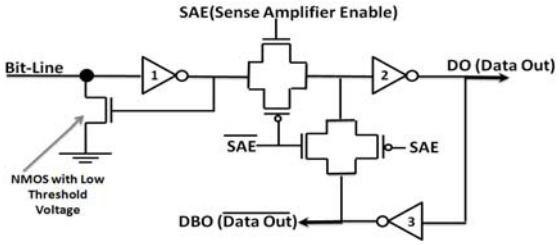

Fig. 3 Circuit schematic of sense amplifier

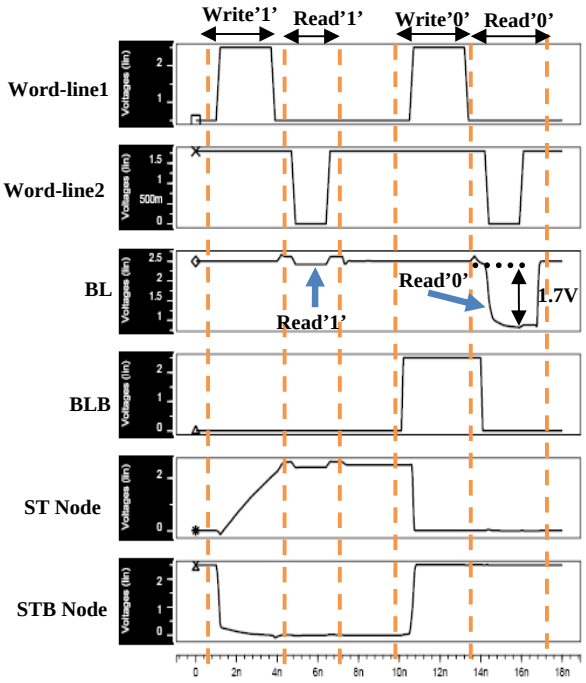

Fig. 4 Simulated waveform for read/write operation of novel 4T SRAM cell

IV. Cell Size

Fig. 5 shows possible layout of 4T SRAM cell in standard 0.25µm CMOS technology design rules. Also for comparison, in Fig. 5 shows layout of 6T SRAM cell and 4T SRAM cell in standard 0.25µm CMOS technology design rules. The 6T cell

has the conventional layout topology and is as compact as possible. The 6T SRAM cell requires 24.32μm^2 area in 0.25μm technology, whereas 4T SRAM cell requires 19.38μm^2 area in 0.25μm technology. These numbers do not take into account the potential area reduction obtained by sharing with neighboring cells. Therefore the new cell size is 20% smaller than a conventional six-transistor cell using same design rules.

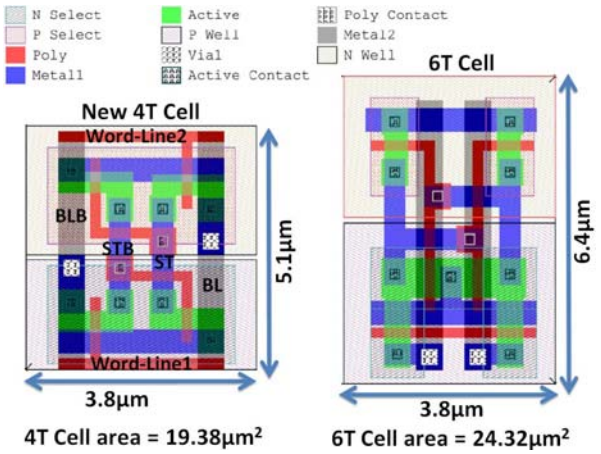

Fig. 5 Layout comparison of 4T SRAM cell and 6T SRAM cell

V. Dynamic Energy Consumption

In each cycle, a read or write operation performed on one cell in SRAMs. Therefore dynamic energy consumption in SRAMs consumed due to the charging and discharging capacitances during read and write operation, and thus during each cycle of SRAMs a certain amount of energy is drawn from the power supply and dissipated. The energy consumption of each cycle depended on type of operation (read or write). Furthermore, when the capacitor charged from GND to V_{DD} and then discharged to GND, amount of energy drawn from the power supply and dissipated, equals $C_L V_{DD}^2$ [6]. And stored energy on the capacitor C_L with voltage V_C equals $\frac{1}{2} C_L V_C^2$. Thus each time the capacitor C_L charged from V_C to V_{DD} and then discharged to V_C amount of energy drawn from the power supply and dissipated, obtained by following expression.

$$E_{Supply} = C_L(V_{DD}^2 - V_C^2) \quad (1)$$

In following dynamic energy consumption of 4T and 6T SRAM cell investigated analytically, also Table 1 lists the symbol and parameter that we use throughout our analytical modeling.

A. Dynamic Energy Consumption of Conventional 6T SRAM Cell

There are four premiere capacitances in 6T SRAM cell. These capacitances include bit-lines (BL and BLB) capacitance, word-line capacitance, ST capacitance and STB capacitance. Bit-line (BL and BLB) capacitance is mainly composed drain junction capacitance of access transistor of 6T SRAM cell. Next large capacitance in 6T SRAM cell is word-line capacitance and mainly composed of gate capacitance of access transistor of 6T SRAM cell. Next capacitances in 6T SRAM cell are ST capacitance and STB capacitance. These capacitances mainly composed gate capacitances and drain junction capacitance of PMOS load transistors and NOMS drive transistors of 6T SRAM cell. Table II lists expressions for estimation these capacitances. We ignored wiring and contact capacitances in these expressions.

TABLE I
Summary of Notations Used in the Analytical Model

SYMBOL	PARAMETER
$C_{BL\text{-}6T}$, $C_{BL\text{-}4T}$, $C_{BLB\text{-}4T}$	Bit-lines capacitances of 6T and 4T SRAM cell
$C_{WL\text{-}6T}$, $C_{WL1\text{-}4T}$, $C_{WL2\text{-}4T}$	Word-line capacitances of 6T and 4T SRAM cell
$C_{ST\text{-}6T}$, $C_{ST\text{-}4T}$	Storage node capacitances of 6T and 4T SRAM cell
$C_{STB\text{-}6T}$, $C_{STB\text{-}4T}$	ST node capacitances of 6T and 4T SRAM cell
$C_{J\text{-}AC\text{-}6T}$	Drain junction capacitance of access transistor of 6T SRAM cell
$C_{J\text{-}ACN\text{-}4T}$,$C_{J\text{-}ACP\text{-}4T}$	Drain junction capacitance of PMOS and NMOS access transistor of 4T SRAM cell
$W_{AC\text{-}6T}$	Channel width of access transistor of 6T SRAM cell
$W_{ACP\text{-}4T}$, $W_{ACN\text{-}4T}$	Channel width of PMOS and NOMS access transistor of 4T SRAM cell
$L_{AC\text{-}6T}$	Effective channel length of access transistor of 6T and 4T SRAM cell
$L_{ACP\text{-}4T}$, $L_{ACN\text{-}4T}$	Effective channel length of PMOS and NMOS access transistor of 6T SRAM cell
$C_{g\text{-}D\text{-}6T}$, $C_{g\text{-}D\text{-}4T}$	Gate capacitance NMOS drive transistor of 6T and 4T SRAM cell
$C_{g\text{-}L\text{-}6T}$, $C_{g\text{-}L\text{-}4T}$	Gate capacitance PMOS drive transistor of 6T and 4T SRAM cell
$C_{J\text{-}D\text{-}6T}$, $C_{J\text{-}D\text{-}4T}$	Drain junction capacitance of NMOS drive transistor of 6T and 4T SRAM cell,
$C_{J\text{-}L\text{-}6T}$, $C_{J\text{-}L\text{-}4T}$	Drain junction capacitance PMOS load transistor of 6T and 4T SRAM cell
$C_{g\text{-}P}$	Gate capacitance of PMOS transistor per unit area (1μm^2)
$C_{g\text{-}N}$	Gate capacitance of NMOS transistor per unit area (1μm^2)
$W_{L\text{-}6T}$, $W_{L\text{-}4T}$	Width channel of load transistor of 6T and 4T SRAM cell
$L_{L\text{-}6T}$, $L_{L\text{-}4T}$	Length channel of load transistor of 6T and 4T SRAM cell
$W_{D\text{-}6T}$, $W_{D\text{-}4T}$	Width channel of drive transistor of 6T and 4T SRAM cell
$L_{D\text{-}6T}$, $L_{D\text{-}4T}$	Length channel of drive transistor of 6T and 4T SRAM cell
$C_{J\text{-}N}$	Junction capacitance of NMOS transistor cell per unit area (1μm^2)
$C_{J\text{-}P}$	Junction capacitance of PMOS transistor cell per unit area (1μm^2)
$C_{J\text{-}P\text{-}SW}$	Side wall capacitance of PMOS transistor per unit length (1μm)
$C_{J\text{-}N\text{-}SW}$	Side wall capacitance of NMOS transistor per unit length (1μm)

Base on conventional write operation of 6T SRAM cell [7] whenever a write operation performed on 6T SRAM cell in worst case following changes occur on word-line, bit-line and ST node or STB node:

1-Word-line charged from GND to V_{DD} and then discharged to GND. Consequently amount of energy drawn from power supply and dissipated is $C_{WL\text{-}6T} V_{DD}^2$.

2-BL or BLB from V_{DD} discharged to GND and then charged to V_{DD}. Consequently amount of energy drawn from power supply and dissipated is $C_{BL\text{-}6T} V_{DD}^2$.

3)-ST node or STB node discharged from V_{DD} to GND and ST node or STB node charged from GND to V_{DD}.

Consequently amount of energy drawn from power supply and dissipated is $\frac{1}{2}\times C_{ST\text{-}6T}V_{DD}^{\ 2}+\frac{1}{2}\times C_{STB-6T}V_{DD}^{\ 2}$.

Therefore, when a write operation performed on 6T SRAM cell in worst case amount of energy is drawn from power supply and dissipated approximately obtained by following analytical expression.

$$E_{Write\text{-}6T}=C_{WL\text{-}6T}V_{DD}^{\ 2}+C_{BL\text{-}6T}V_{DD}^{\ 2}+\frac{1}{2}\times C_{ST-6T}V_{DD}^{\ 2}+\frac{1}{2}\times C_{STB-6T}V_{DD}^{\ 2} \quad (2)$$

Base on conventional read operation of 6T SRAM cell [7] when a read operation performed on 6T SRAM following changes occur on word-line and bit-lines and ST node or STB node.

1-Word-line charged from GND to V_{DD} and then discharged to GND. Consequently amount of energy drawn from power supply and dissipated is $C_{WL\text{-}6T}V_{DD}^{\ 2}$.

2-BL or BLB from V_{DD} discharged to $V_{Read\text{-}BL}$ and then charged to V_{DD}. Consequently amount of energy drawn from power supply and dissipated is $C_{BL-6T}(V_{DD}^{\ 2}-V_{Read\text{-}BL}^{\ 2})$.

Therefore, when a read operation performed on 6T SRAM cell amount of energy is drawn from power supply and dissipated approximately obtained by following analytical expression.

$$E_{Read\text{-}6T}=C_{WL\text{-}6T}V_{DD}^{\ 2}+C_{BL-6T}(V_{DD}^{\ 2}-V_{Read\text{-}BL}^{\ 2}) \quad (3)$$

If probability of read is P_{Read} in each cycle and probability of write is P_{Write} in each cycle, then energy consumption of each cycle obtained by following expression.

$$E_{Cycle\text{-}6T}=P_{Write}\times E_{Write\text{-}6T}+P_{Read}\times E_{Read\text{-}6T} \quad (4)$$

B. Dynamic Energy Consumption of Novel 4T-SRAM Cell

There are four premiere capacitances in 4T SRAM cell. These capacitances include BL and BLB capacitances, word-lines capacitances, ST capacitance and STB capacitance. BL and BLB capacitances are mainly composed drain junction capacitance of access transistor of 4T SRAM cell. Next large capacitance in 4T SRAM cell is word-lines capacitance and mainly composed of gate capacitance of access transistors of 4T SRAM cell. And finally next capacitances in 6T SRAM cell are ST capacitance and STB capacitance. These capacitances mainly composed drain junction capacitance of access transistors of 4T SRAM cell and gate capacitances and drain junction capacitance of PMOS load transistors and NOMS drive transistors. Table II lists expressions for estimation these capacitances. Also we ignored wiring and contact capacitance in these expressions.

Based on read and write operation described in section III, in worst case following changing occur on BLB, word-line1 and ST node and STB node when write operation is issued.

1-word-line1 charged from V_{Idle1} to V_{DD} and then discharged to V_{Idle1}. Consequently amount of energy drawn from power supply and dissipated is $C_{WL1\text{-}4T}(V_{DD}^{\ 2}-V_{Idle1}^{\ 2})$.

2-BLB from GND charged to V_{DD} and then charged to GND. Consequently amount of energy drawn from power supply and dissipated is $C_{BLB\text{-}4T}V_{DD}^{\ 2}$.

3- ST node discharged from V_{DD} to GND and STB node charged from GND to V_{DD}. Consequently amount of energy drawn from power supply and dissipated is $\frac{1}{2}\times C_{ST\text{-}4T}V_{DD}^{\ 2}+\frac{1}{2}\times C_{STB-4T}V_{DD}^{\ 2}$.

TABLE II
EXPRESSION FOR ESTIMATION CAPACITANCE IN 4T AND 6T SRAM CELL

Symbol	Expression
$C_{BL\text{-}6T}$	$C_{J-AC-6T}$
$C_{J\text{-}AC\text{-}6T}$	$W_{AC-6T}\,2.5\,L_{AC-6T}C_{J-N}+C_{J-SW-N}(5L_{AC-6T}+W_{AC-6T})$
$C_{WL\text{-}6T}$	$2\times(C_{g\text{-}AC\text{-}6T}\times W_{AC-6T}\times L_{AC-6T})$
$C_{ST\text{-}6T}$, $C_{STB\text{-}6T}$	$C_{g\text{-}L\text{-}6T}+C_{g\text{-}D\text{-}6T}+C_{J\text{-}L\text{-}6T}+C_{J\text{-}D\text{-}6T}+C_{J\text{-}AC\text{-}6T}$
$C_{J\text{-}L\text{-}6T}$	$W_{L-6T}\,2.5\,L_{L-6T}C_{J-N}+C_{J-SW-N}(5L_{L-6T}+W_{L-6T})$
$C_{J\text{-}D\text{-}6T}$	$W_{D-6T}\,2.5\,L_{D-6T}C_{J-N}+C_{J-SW-N}(5L_{D-6T}+W_{D-6T})$
$C_{g\text{-}L\text{-}6T}$	$C_{g\text{-}P}\times W_{L-6T}\times L_{L-6T}$
$C_{g\text{-}D\text{-}6T}$	$C_{g\text{-}N}\times W_{D-6T}\times L_{D-6T}$
$C_{BL\text{-}4T}$	$C_{J\text{-}APN\text{-}4T}$
$C_{BLB\text{-}4T}$	$C_{J\text{-}ACN\text{-}4T}$
$C_{J\text{-}CAN\text{-}4T}$	$W_{ACN-4T}\times 2.5\,L_{ACN-4T}\times C_{J-N}+C_{J-SW-N}(5L_{ACN-4T}+W_{ACN-4T})$
$C_{J\text{-}ACP\text{-}4T}$	$W_{ACP-4T}\times 2.5\,L_{ACP-4T}\times C_{J-N}+C_{J-SW-N}(5L_{ACP-4T}+W_{ACP-4T})$
$C_{WL1\text{-}4T}$	$C_{g-N}\times W_{ACN-4T}\times L_{ACN-4T}$
$C_{WL1\text{-}4T}$	$C_{g-N}\times W_{ACP-4T}\times L_{ACP-4T}$
$C_{ST\text{-}4T}$	$C_{g\text{-}L\text{-}4T}+C_{J\text{-}ACP\text{-}4T}+C_{J\text{-}D\text{-}4T}$
$C_{STB\text{-}4T}$	$C_{g\text{-}D\text{-}4T}+C_{J\text{-}ACN\text{-}4T}+C_{J\text{-}L\text{-}4T}$
$C_{g\text{-}L\text{-}4T}$	$C_{g-N}\times W_{L-4T}\times L_{L-4T}$
$C_{g\text{-}D\text{-}4T}$	$C_{g-N}\times W_{D-4T}\times L_{D-4T}$
$C_{J\text{-}D\text{-}4T}$	$W_{D-4T}\times 2.L_{D-4T}\times C_{J-N}+C_{J-SW-N}(4L_{D-4T}+W_{D-4T})$
$C_{J\text{-}L\text{-}4T}$	$W_{L-4T}\times 2..5\,L_{L-4T}\times C_{J-N}+C_{J-SW-N}\,4L_{L-4T}+W_{L-4T}$

Therefore, whenever a write operation performed on novel 4T SRAM cell in worst case amount of energy is drawn from power supply and dissipated approximately obtained by following analytical expression.

$$E_{Write\text{-}4T} = C_{WL1\text{-}4T} \times (V_{DD}^{\ 2} - V_{Idle1}) + C_{BLB-4T} V_{DD}^{\ 2} + \frac{1}{2} \times C_{ST\text{-}4T} V_{DD}^{\ 2} + \frac{1}{2} \times C_{STB-4T} V_{DD}^{\ 2} \quad (5)$$

Also when the read operation is issued in worst case following changing occur on BL and word-line2.

1-Word-line2 discharged from V_{Idle2} to GND and then charged to V_{Idle2}. Consequently amount of energy drawn from power supply and dissipated is $C_{WL2\text{-}4T} V_{Idle2}^{\ 2}$ ($V_{Idle2} < V_{DD}$).

2-BL from V_{DD} discharged to $V_{BL\text{-}Low}$ and then charged to V_{DD}. Consequently amount of energy drawn from power supply and dissipated is $C_{BL\text{-}4T}(V_{DD}^{\ 2} - V_{BL\text{-}Low}^{\ 2})$.

Therefore, whenever a read operation performed on novel 4T SRAM cell in worst case, amount of energy is drawn from power supply and dissipated approximately obtained by following analytical expression.

$$E_{Read\text{-}4T} = C_{WL2\text{-}4T} \times V_{Idle2} + C_{BL-4T}(V_{DD}^{\ 2} - V_{BL\text{-}Low}^{\ 2}) \quad (6)$$

If probability of read is P_{Read} in each cycle and probability of write is P_{Write} in each cycle, then energy consumption of each cycle obtained by following expression.

$$E_{Cycle\text{-}4T} = P_{Write} \times E_{Write\text{-}4T} + P_{Read} \times E_{Read\text{-}4T} \quad (7)$$

C. Dynamic Energy Consumption Comparison

Cell ratio is an important parameter of SRAM cells. This parameter defined as the ratio of the channel width of driver transistor of memory cell to channel width of access transistor of memory cell [8]. As cell ratio increased also the area of cell increased. Fig. 6 shows analytical worst case dynamic energy consumption of 4T SRAM cell and 6T SRAM cell as function of cell ratio of cell. As shown in Fig. 6 on average novel 4T SRAM cell has 65% smaller energy consumption in comparison with 6T SRAM cell with same cell ratio. Simulation result in standard 0.25µm technology shows as the cell ratio changes, on average novel 4T SRAM cell has 45% smaller dynamic energy consumption. This mismatching between simulation results and analytical results is due to ignoring wiring and contact capacitances.

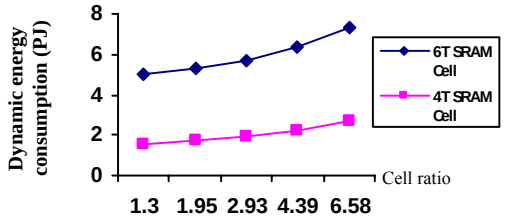

Fig. 6 Dynamic energy consumption of 6T and 4T SRAM cell

VI. Conclusion

With the aim of achieving a high-density SRAM, we developed a 4T SRAM cell. This cell retains its data with leakage current when there is not any positive feedback. Dynamic energy consumption of 6T SRAM cell and purposed 4T SRAM cell investigated analytically. Analytical results show, on average novel 4T SRAM has 65% smaller dynamic energy consumption. Also Simulation result in standard 0.25µm CMOS technology shows purposed 4T SRAM cell has correct operation during read/write operation and idle mode.

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