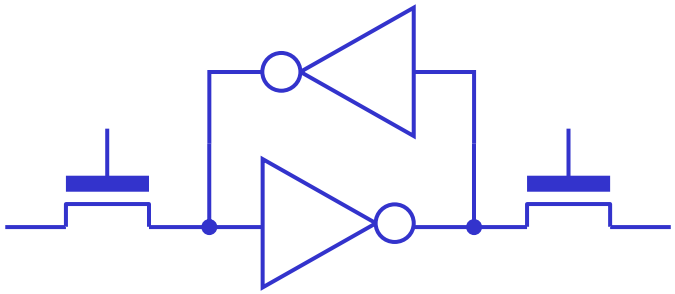


Review of 6T SRAM Cell

Ding-Ming Kwai
Intellectual Property Library Company
June 3, 2005

Why 6T SRAM Cell

- Embedded memory
  - Easy to implement in generic CMOS process
  - Easy to design as logic circuit
  - Easy to test by finite-state machine
- Compilable design
  - Fixed cell size to allow us dedicating in peripheral circuit design
  - Synchronous interface since 0.35μm generation simplifies the design
  - A larger number of instances required

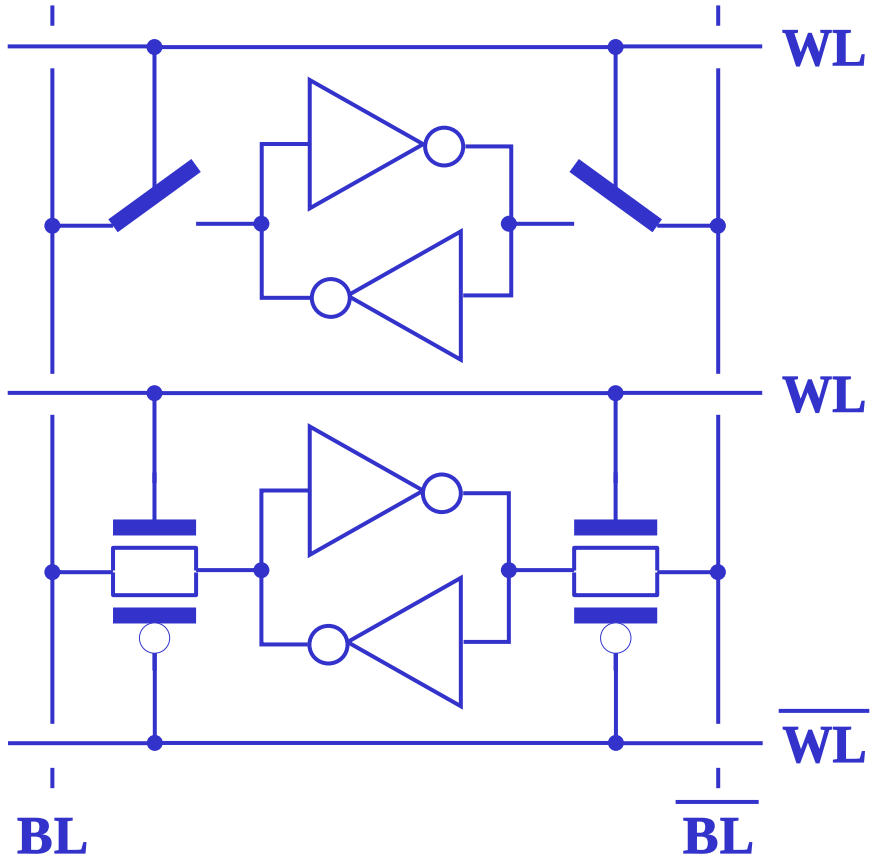
Outline

- **6T cell and its variants** – First we generalize and then we derive
- **Peripheral circuits** – Utilization is the key
- **Cell layout** – To be symmetric or to be asymmetric: that is the question
- **Performance indices** – To judge is human
- **Concluding remarks** – It does not end here

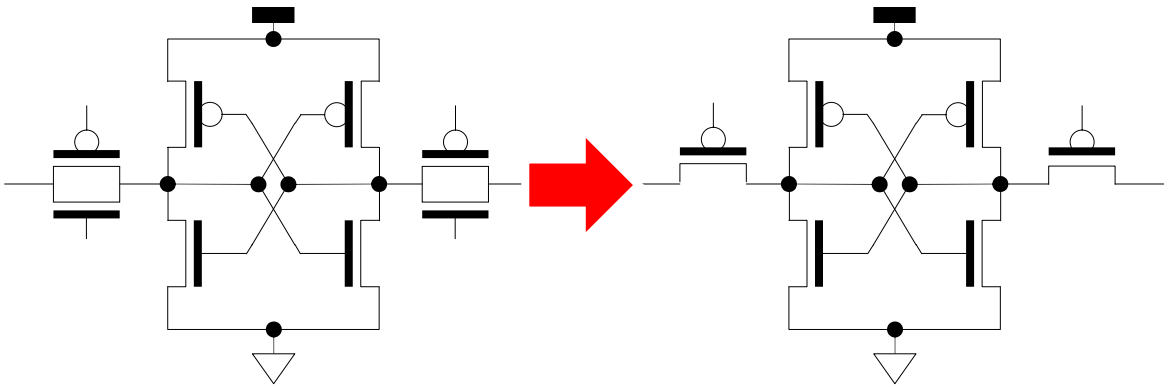
8T SRAM Cell

Making it completely complementary

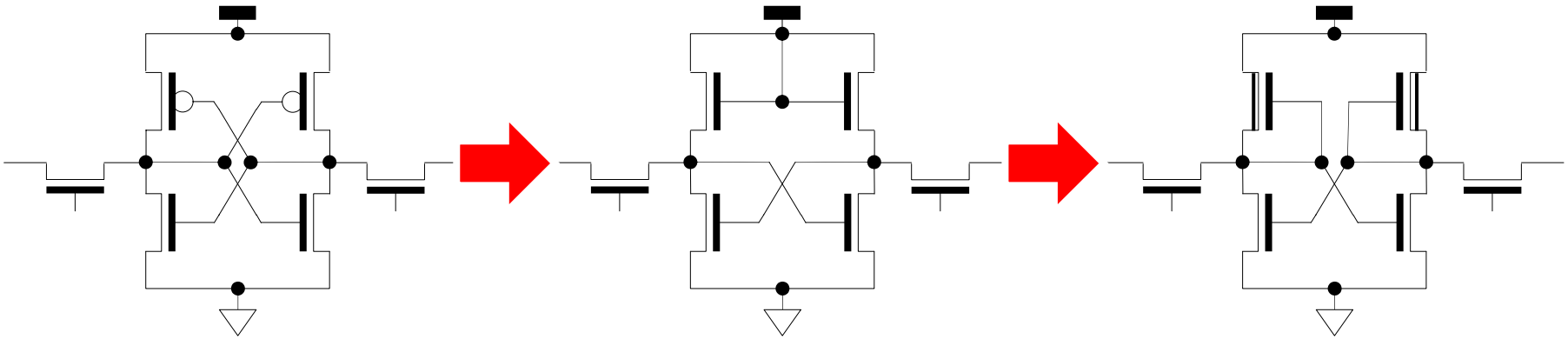
- Regenerative circuit for storing a single bit: two *equal-sized* inverters
- Access device to transfer the bit: two *equal-sized* transmission gates
  ⇨ pass transistors



What Have Been Invented



NEC, 1995

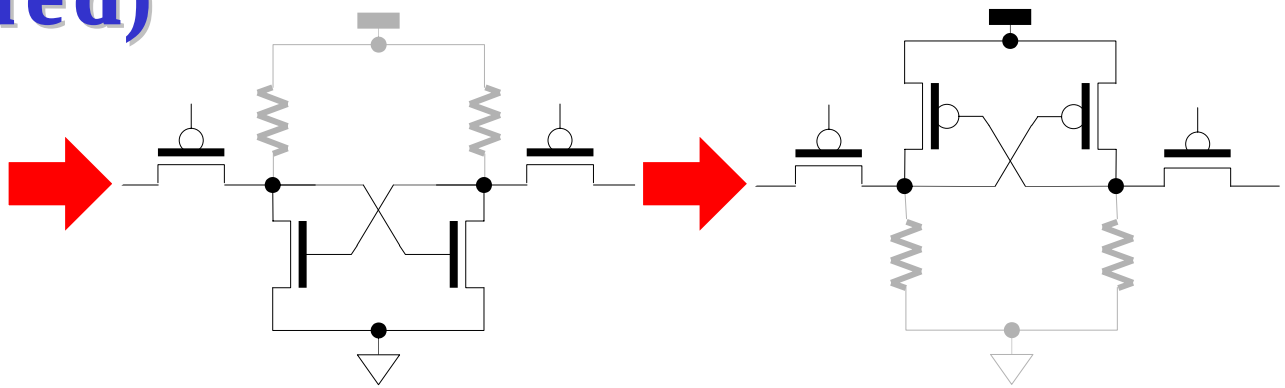


NEC, 1969

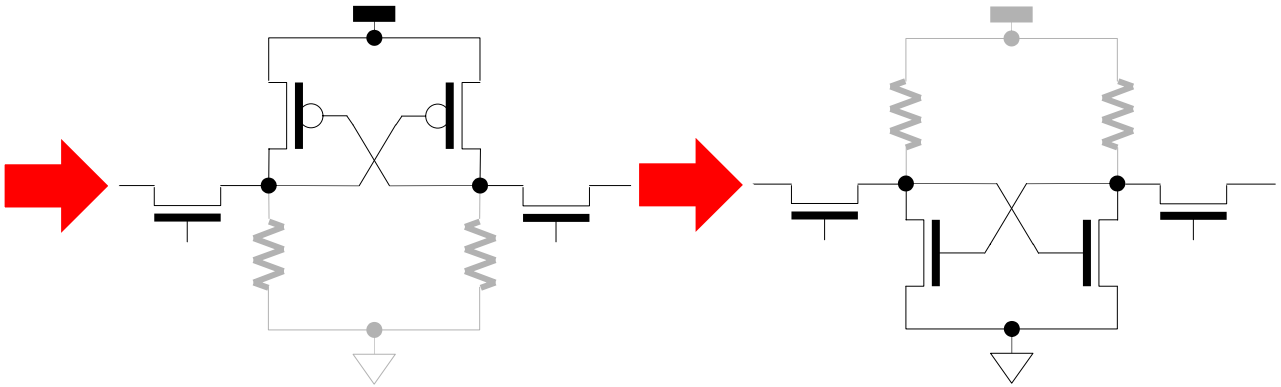
Intel, 1975

What Have Been Invented

(Continued)



NEC, 1998

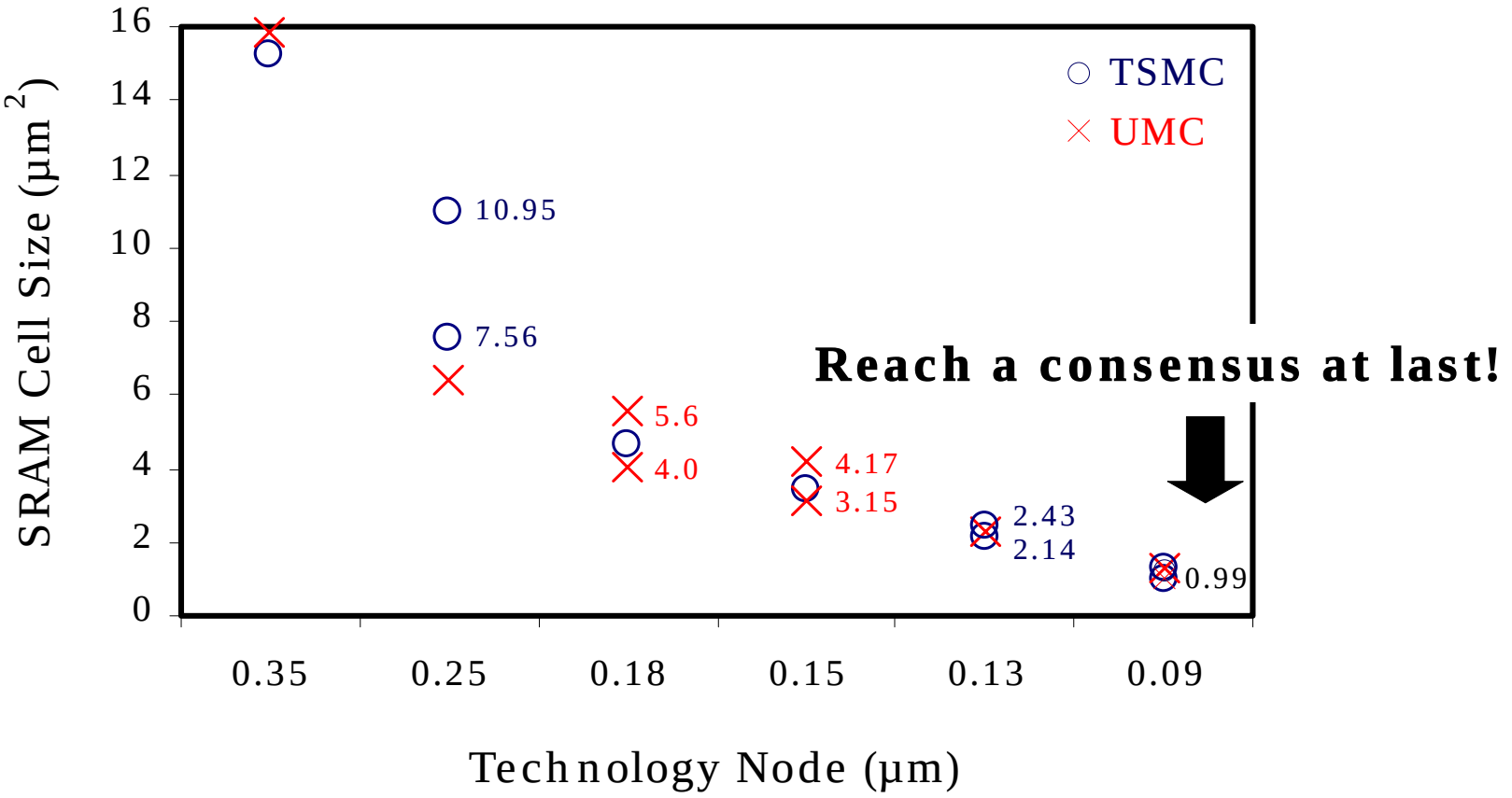


IBM, 1970
GE, 1985

IBM, 1976
MOSTEK, 1981

"The World's Smallest" Myth

Cell size as a competitive edge



C.-H. Hsiao and D.-M. Kwai, "Measurement and characterization of 6T SRAM cell," *Int. Workshop Memory Technology, Design, and Testing (MTDT)*, Taipei, Taiwan, Aug. 2005.

Tradeoffs to Be Made

- Small but slow ⇔ large but fast: area vs. speed (read current and write voltage)
- Small but hot ⇔ large but cold: area vs. leakage power (standby current)
- Small but unstable ⇔ large but stable: area vs. stability (static noise margin)
- Small but low-yield ⇔ large but high-yield: area vs. manufacturability
- Small but expensive ⇔ large but cheap: area vs. cost (masking and process steps)

Outline

- **6T cell and its variants** – First we generalize and then we derive
- **Peripheral circuits** – Utilization is the key
- **Cell layout** – To be symmetric or to be asymmetric: that is the question
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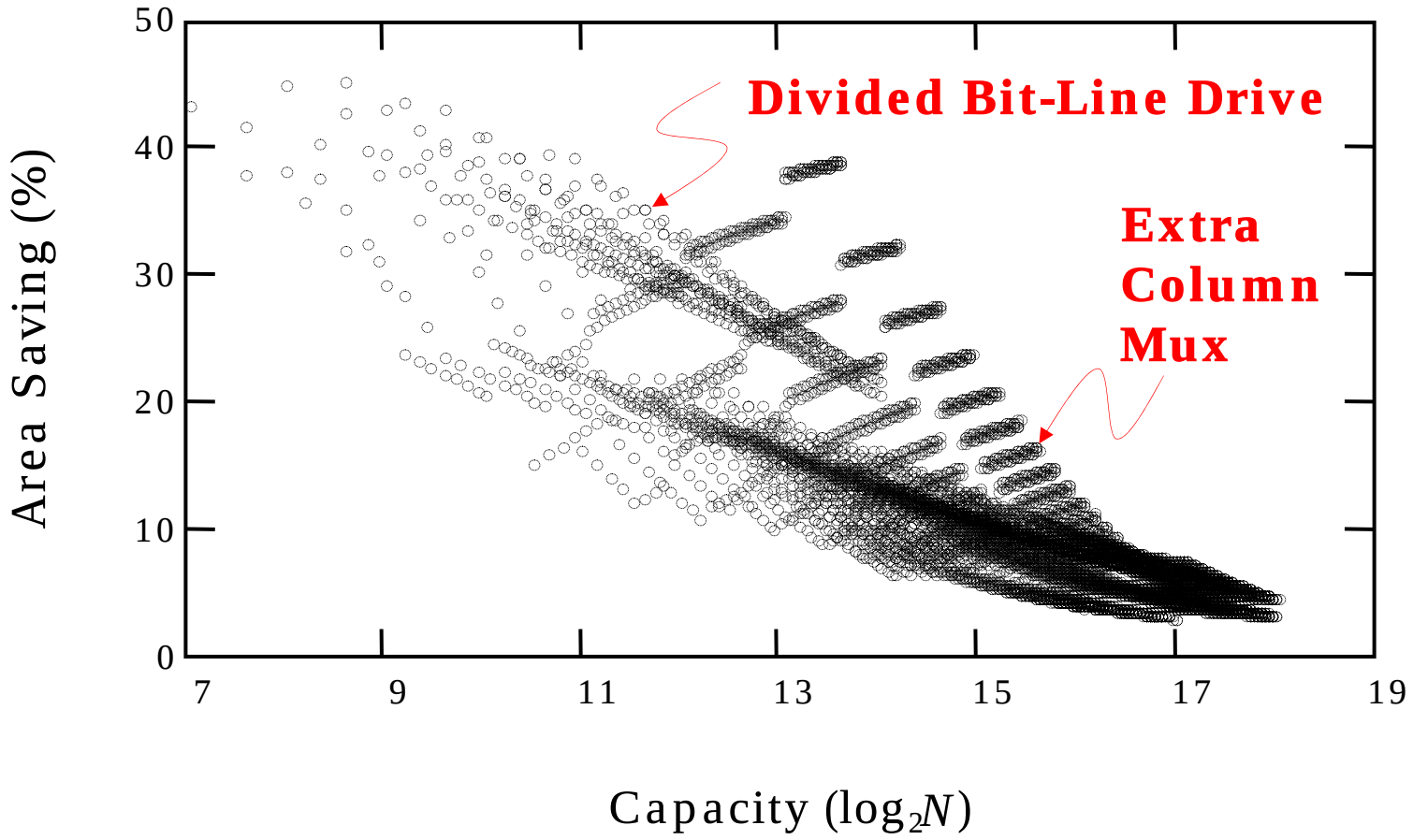
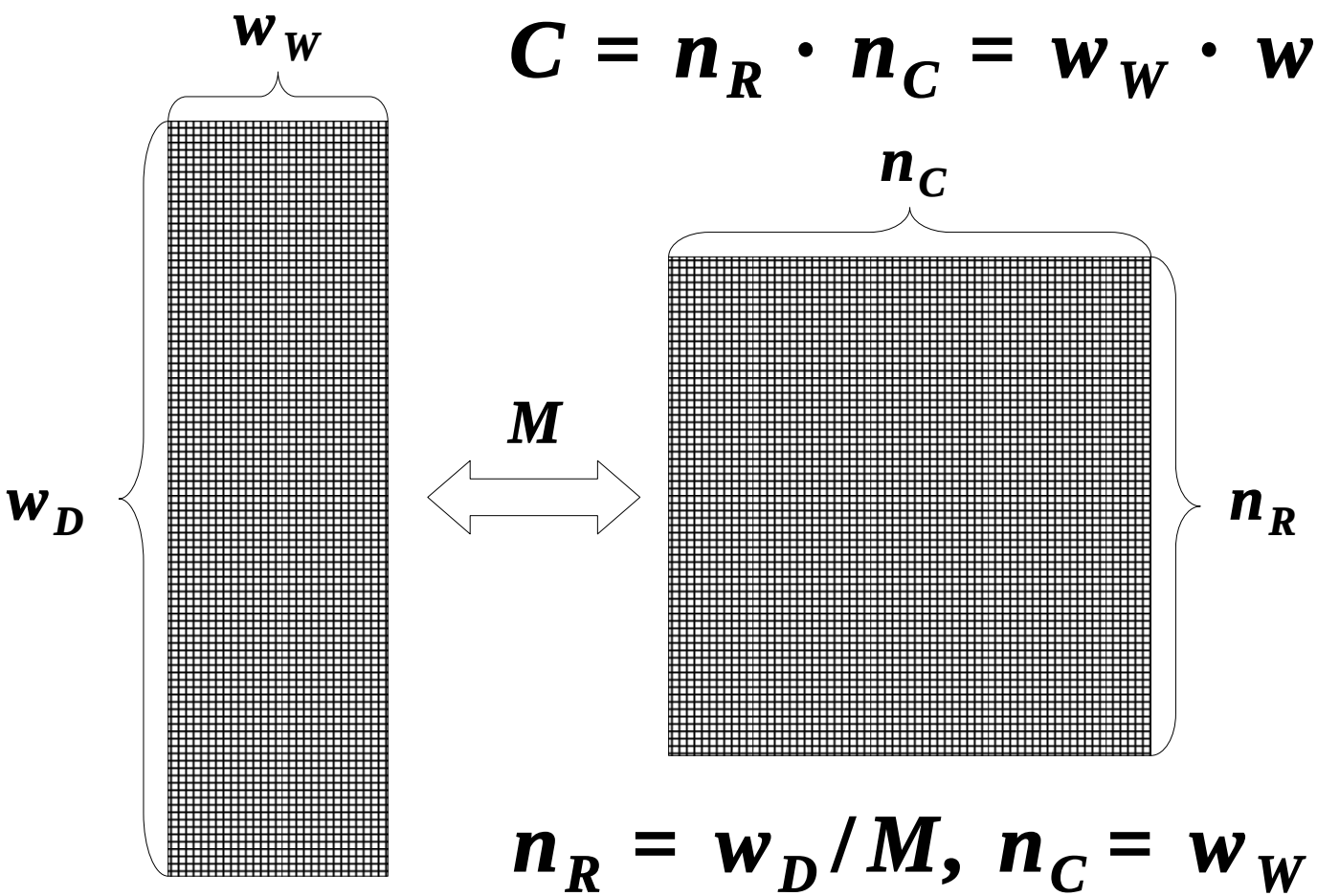
Utilization Is the Key

0.18μm single-port compiler generated instances with peripheral circuits minimized for layout area



What Is Column Mux and Why It Is Important

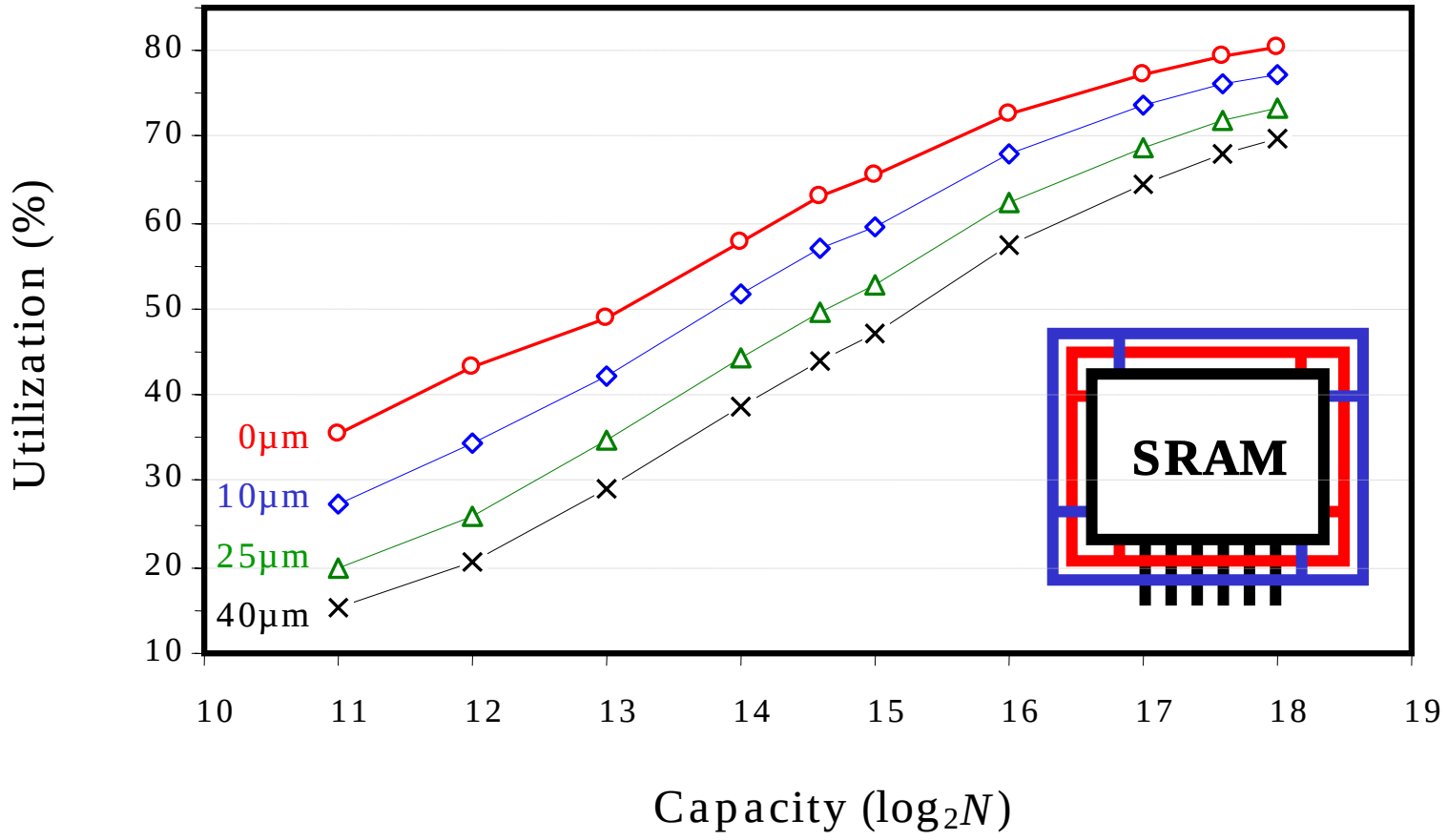
$$C = n_R \cdot n_C = w_W \cdot w_D$$



$$n_R = w_D / M,\ n_C = w_W \cdot M$$

P&R Can Easily Destroy It

0.18µm single-port compiler generated instances added with redundant power/ground rings



Outline

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- **Cell layout** – To be symmetric or to be asymmetric: that is the question
- **Performance indices** – To judge is human
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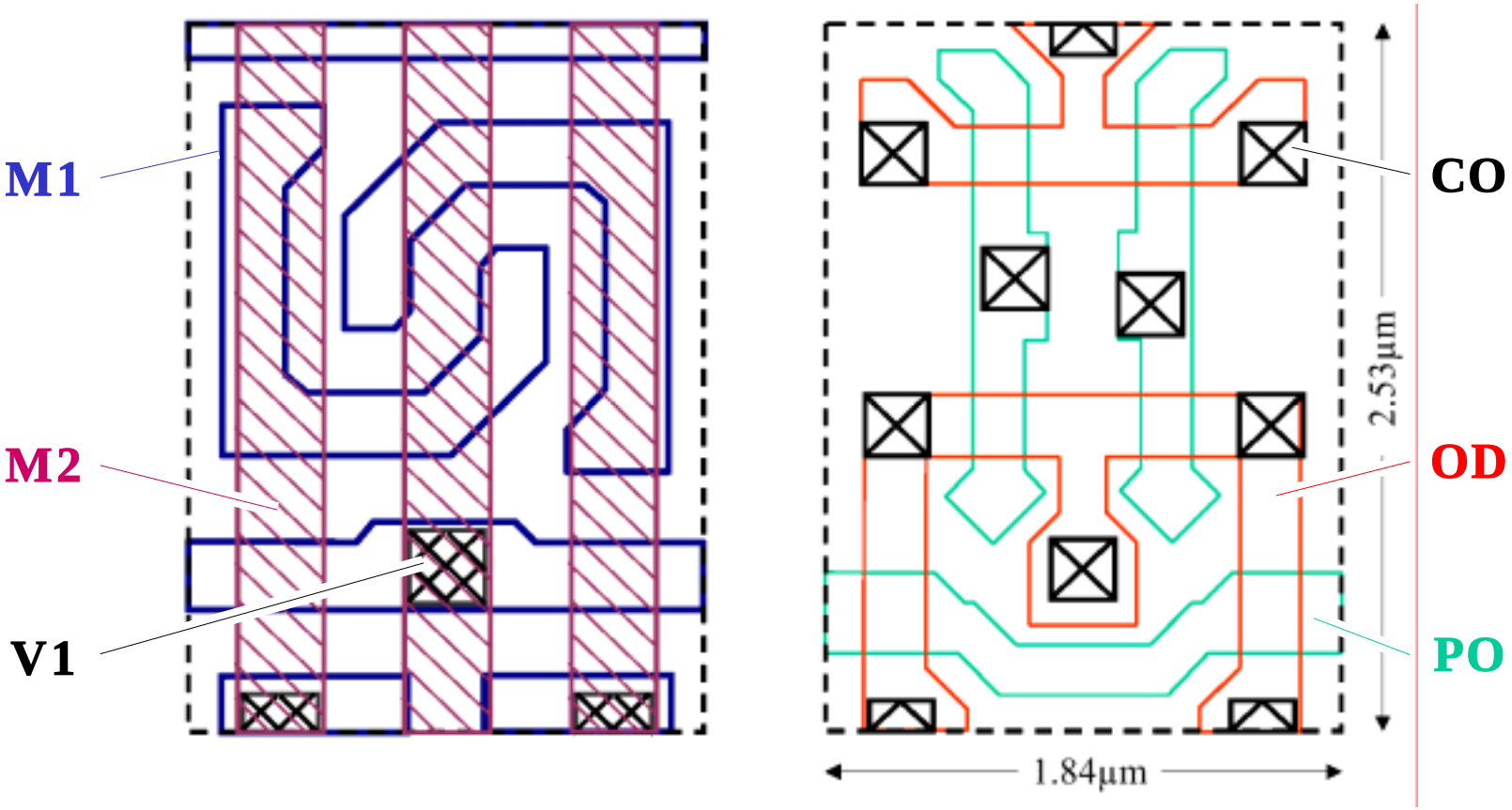
How They Are Drawn

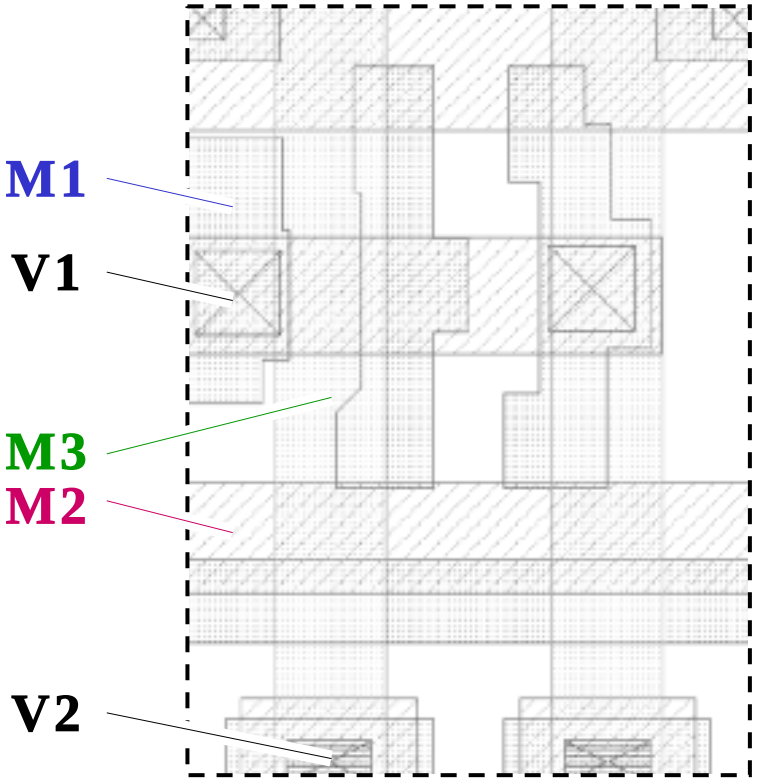
(TSMC 0.18µm Symmetric Example)

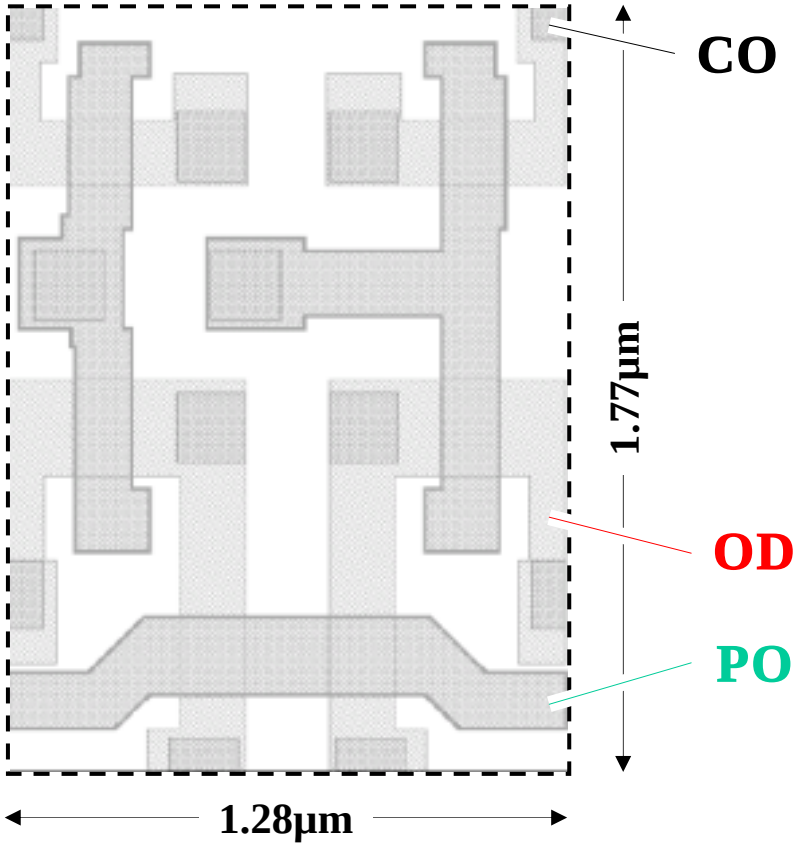


D.-M. Kwai *et al.*, "Detection of SRAM cell stability by lowering array supply voltage," *Proc. Asian Test Symp.*, Taipei, Taiwan, Dec. 2000, pp. 268-273.

How They Are Drawn

(TSMC 0.13µm Asymmetric Example)

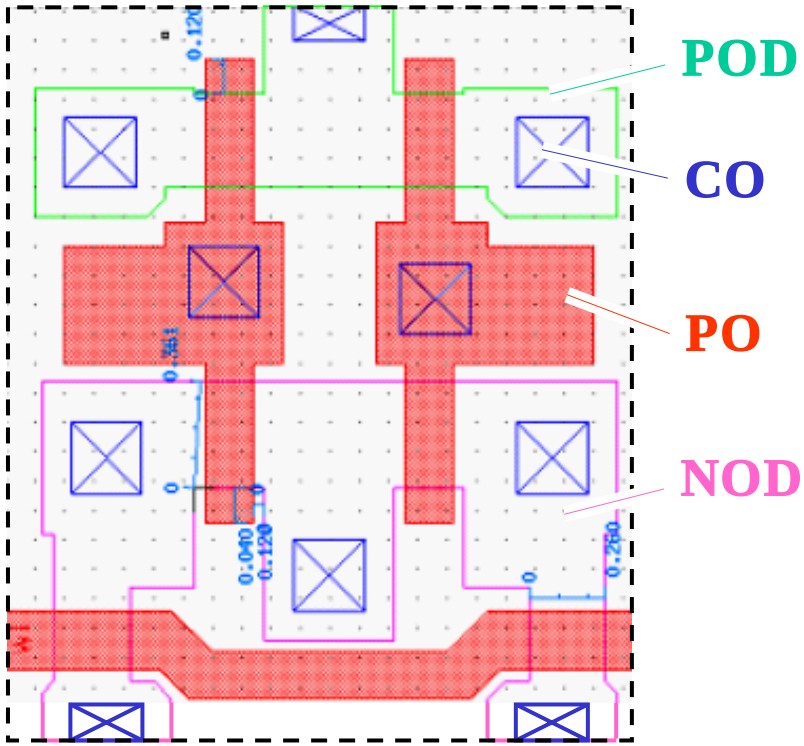




How They Are Drawn

(Intel 0.18µm Symmetric Example)

Asymmetry in cross-coupled inverters can degrade cell stability by **100X** [may be exaggerated]

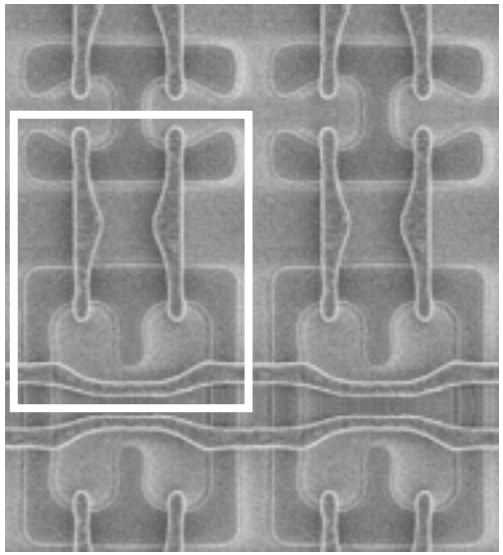


G. E. Sery, "Approaching the one billion transistor logic product: process and design challenges," *Proc SPIE*, vol. 4692, Design, Process Integration, and Characterization for Microelectronics, pp. 254-261, July 2002.

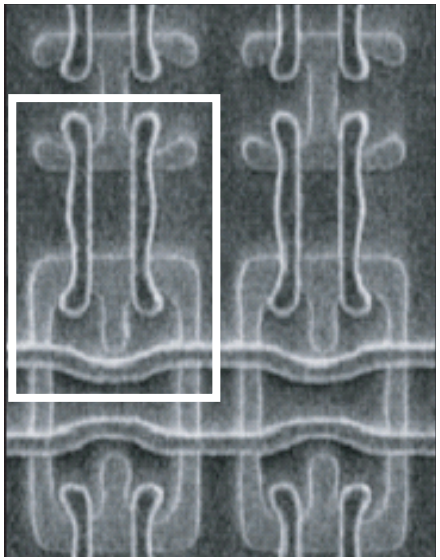
How They Are on Silicon

Symmetric and Asymmetric Examples

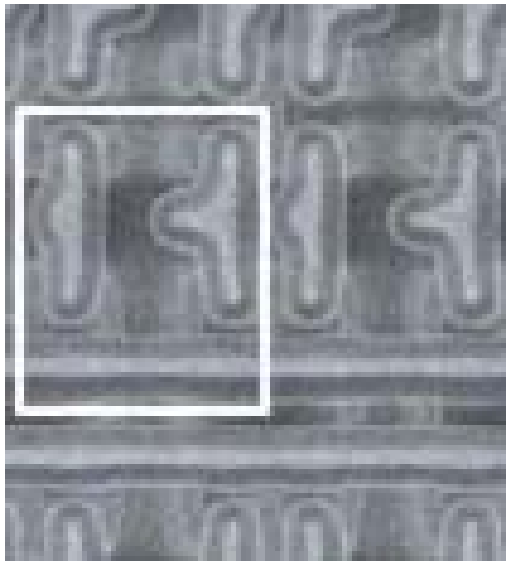
Poly and Diffusion for Devices



0.13µm
Intel 1.22 × 1.64 µm²



0.13µm
IBM 1.2 × 1.7 µm²



90nm
Fujitsu 0.9 × 1.1 µm²

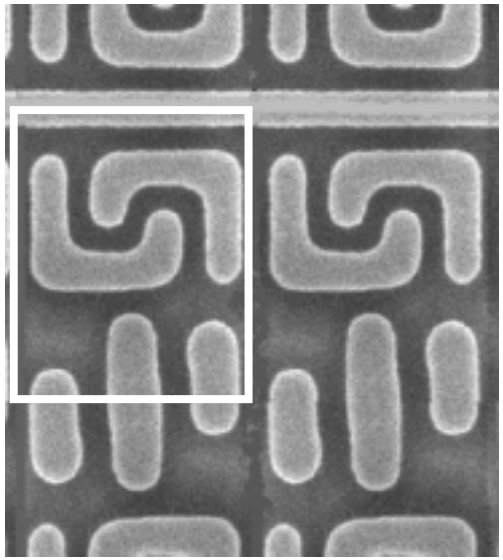
S. Thompson *et al.*, "130nm logic technology featuring 60nm transistors, low-k dielectrics, and Cu interconnects," *Intel Tech. J.*, vol. 6, iss. 2, pp. 5-12, May 2002.

S. S. Iyer *et al.*, "Embedded DRAM: technology platform for the Blue Gene/L chip," *IBM J. Research & Development*, vol. 49, no. 2/3, pp. 333-350, Mar./May 2005.

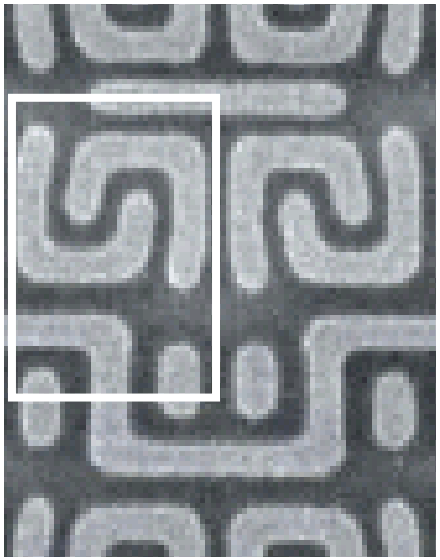
How They Are on Silicon

Symmetric and Asymmetric Examples

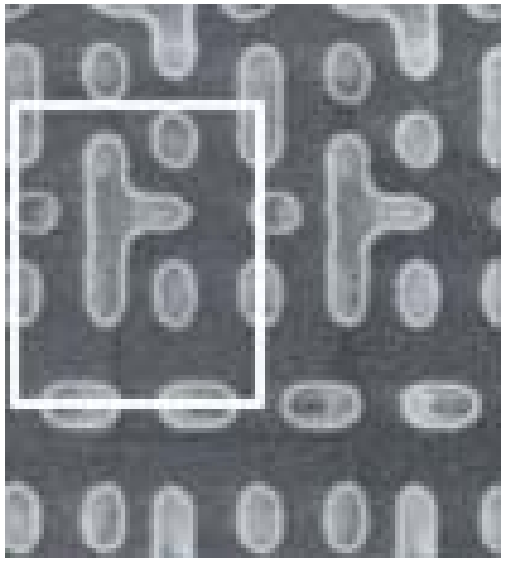
Metal-1 as Local Interconnect



0.13µm
Intel 1.22 × 1.64 µm²



0.13µm
IBM 1.2 × 1.7 µm²

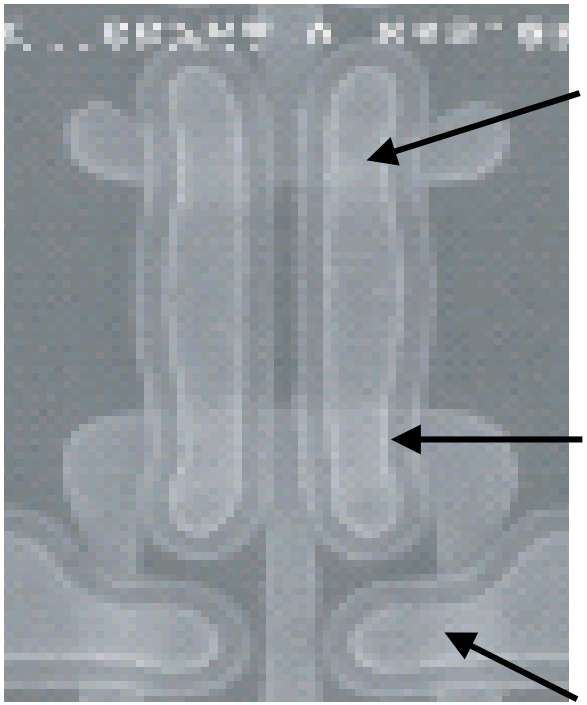


90nm
Fujitsu 0.9 × 1.1 µm²

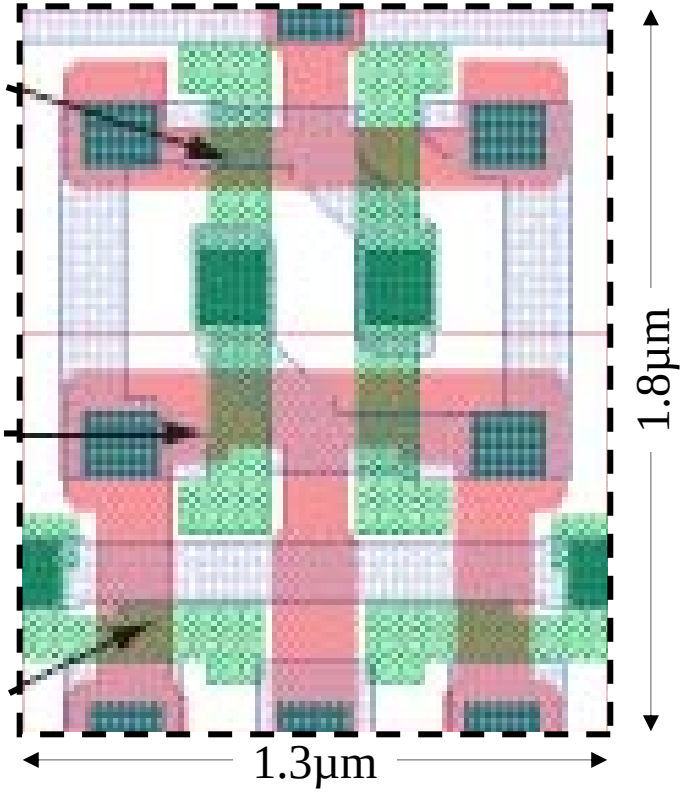
S. Nakai, T. Hosoda, and Y. Takao, "Integration of high-performance transistors, high-density SRAMs, and 10-level copper interconnects into a 90nm CMOS technology," *Fujitsu Sci. Tech. J.*, vol. 39, no. 1, pp. 23-31, June 2003.

How They Are Drawn

IBM 0.13µm Example for ULP SRAM



Split Word Line



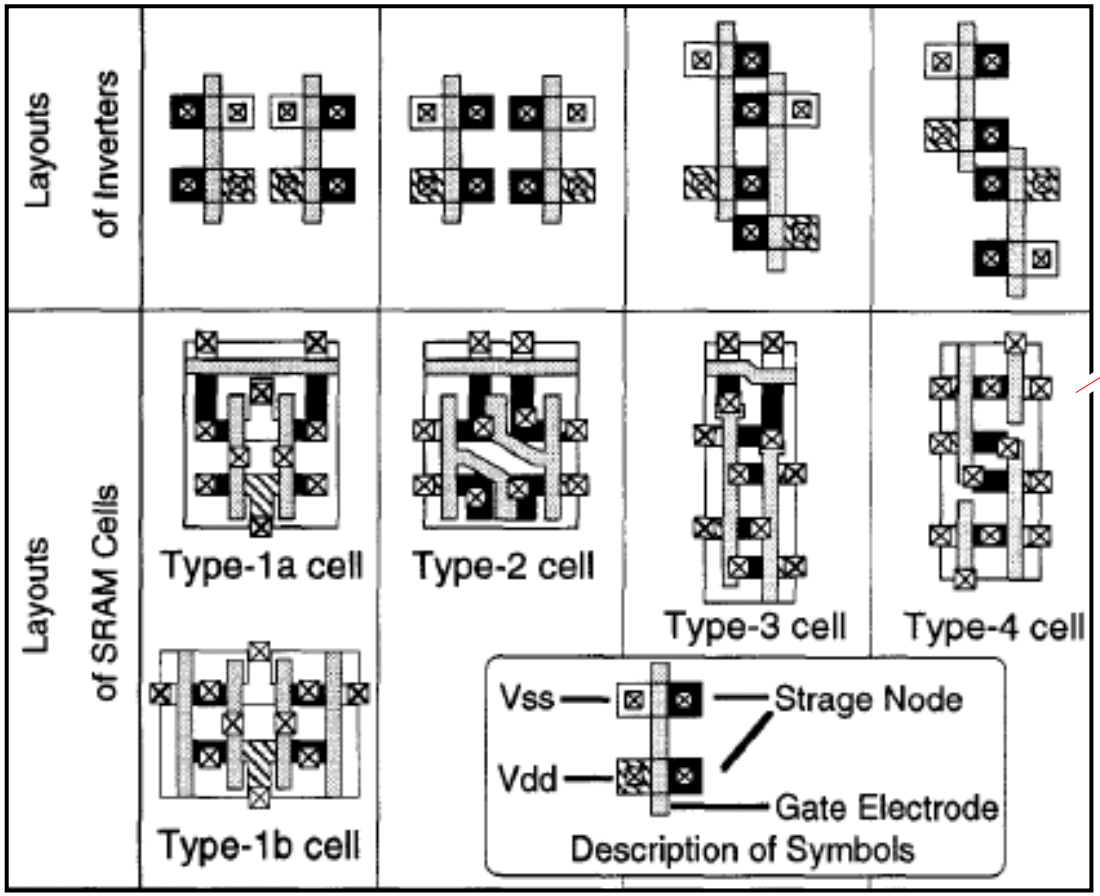
R. W. Mann, "Ultralow-power SRAM technology," *IBM J. Research & Development*, vol. 47, no. 5/6, pp. 553-566, Sep./Nov. 2003.

Disadvantages Related to Conventional Cell Layout

- Complicated irregular patterns involving corner rounding
  - ⇨ Simplified rectangular pattern
- Different orientation for access NMOS transistors
  - ⇨ Same orientation for all transistors
- Pushed spacing rules for metal routing
  - ⇨ Nominal spacing rules for metal routing

Variations by Inverter Layout

A Reveal Close to Success



It turns out to be very useful in 90nm and below process technologies

M. Ishida *et al.*, "A novel 6T-SRAM cell technology designed with rectangular patterns scalable beyond 0.18μm generation and desirable for ultra high speed operation," *Int. Electron Device Meeting Tech. Digest*, 1998, pp. 201-204.

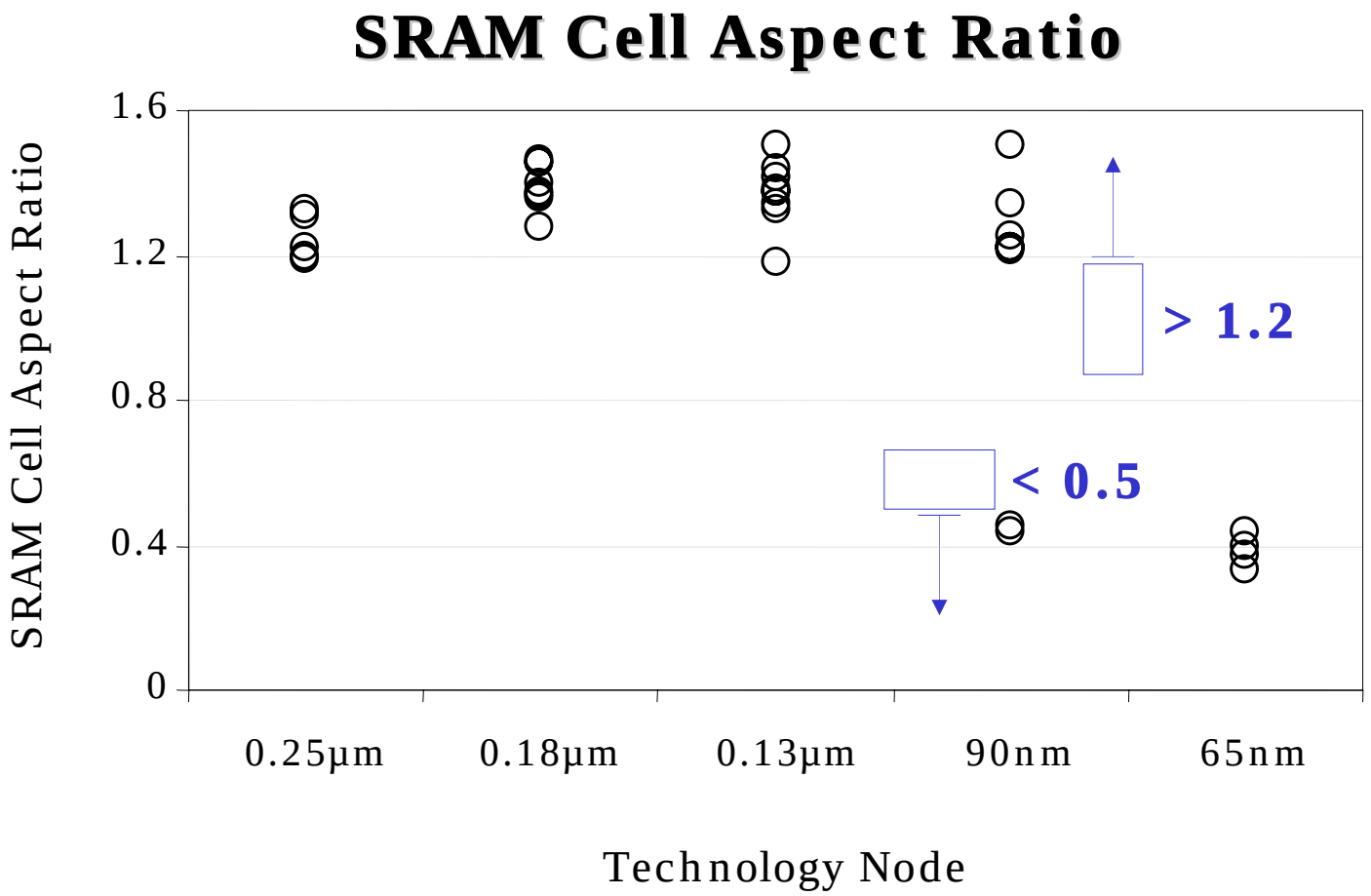
Can We Draw the Polygons in Another Way?

Metal-Layer Assignment for Routing

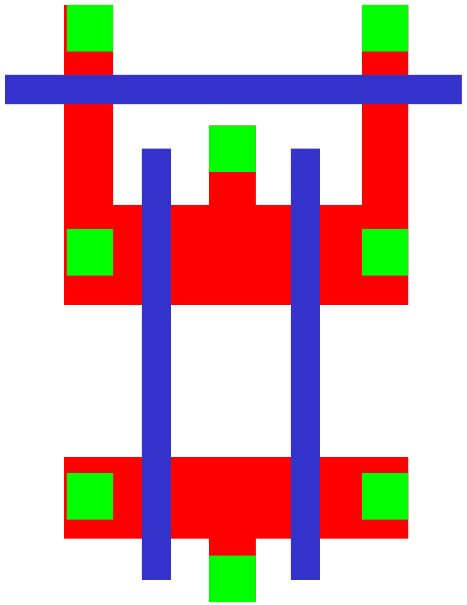
	Symmetric	Asymmetric	Symmetric
WL (H)	M3	M2	M2
BL (V)	M2	M3	M3
VSS (V)	M2	M3	M3

Vertical VSS lines parallel to bit lines are required in the memory array.

Can We Draw the Polygons in Another Way?



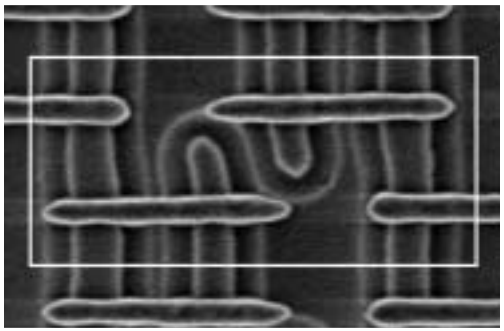
An Animation to Show Layout Changes to Rectangular Patterns



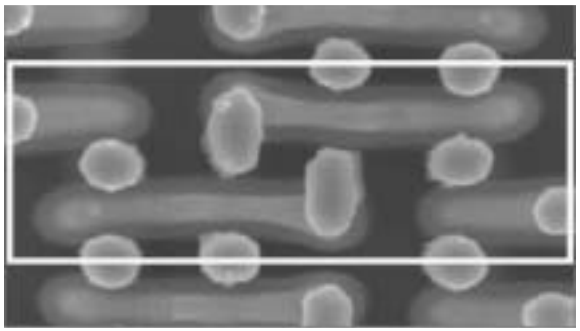
Original Symmetric Layout

Photo Demonstrations at 65nm Technology Node

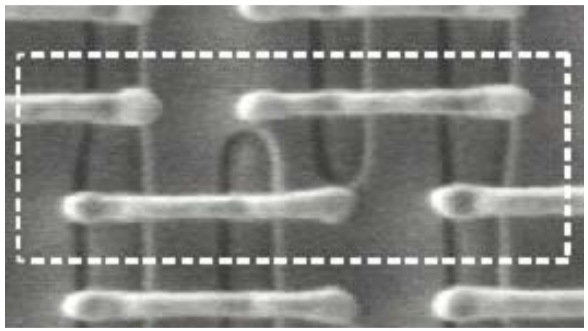
It seems that the layout style will pervade!



TI 0.46 × 1.06 μm²
0.49 μm²



IBM 0.41 × 1.25 μm²
0.51 μm²



Intel 0.46 × 1.24 μm²
0.57 μm²

A. Chatterjee *et al.*, "A 65nm CMOS technology for mobile and digital signal processing applications," *Int. Electron Device Meeting Tech. Digest*, San Francisco, CA, Dec. 2004.

P. Bai *et al.*, "A 65nm logic technology featuring 35nm gate lengths, enhanced channel strain, 8 Cu interconnect layers, low-k ILD and 0.57μm² SRAM cell," *Int. Electron Device Meeting Tech. Digest*, San Francisco, CA, Dec. 2004.

Z. Luo *et al.*, "High performance and low power transistors integrated in 65nm bulk CMOS technology," *Int. Electron Device Meeting Tech. Digest*, San Francisco, CA, Dec. 2004.

Disadvantages Related to Regular Pattern Cell Layout

- Longer and narrower wells
  - induce forward body bias
  - reduce static noise margin
  - require higher strapping frequency
  - lower array utilization
- More irredundant contacts and via holes
  - 10 contacts/cell ⇔ 8.5 contacts/cell
  - 3.5 via-1 holes/cell ⇔ 2 via-1 holes/cell
  - 2.5 via-2 holes/cell ⇔ 0 via-2 holes/cell

Outline

- **6T cell and its variants** – First we generalize and then we derive
- **Peripheral circuits** – Utilization is the key
- **Cell layout** – To be symmetric or to be asymmetric: that is the question
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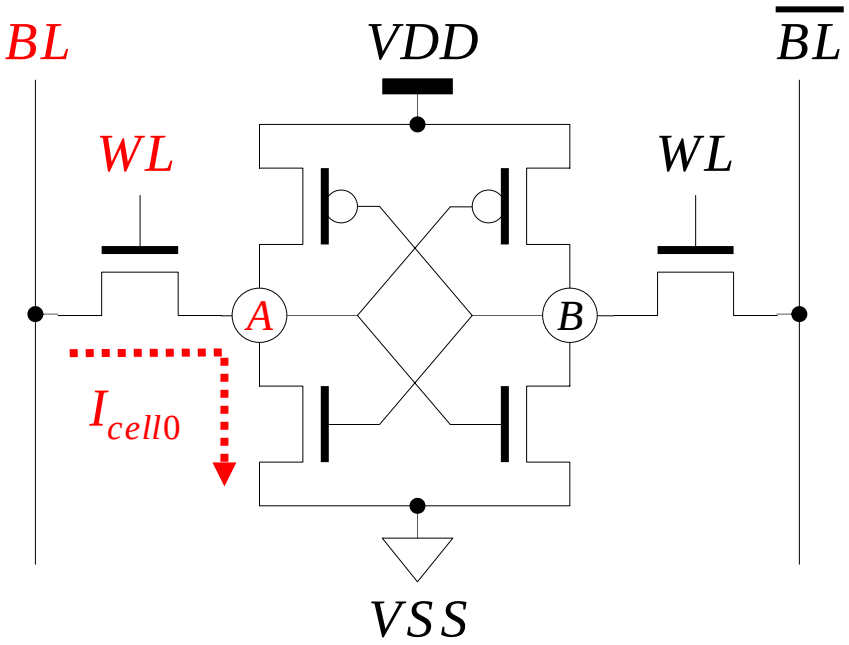
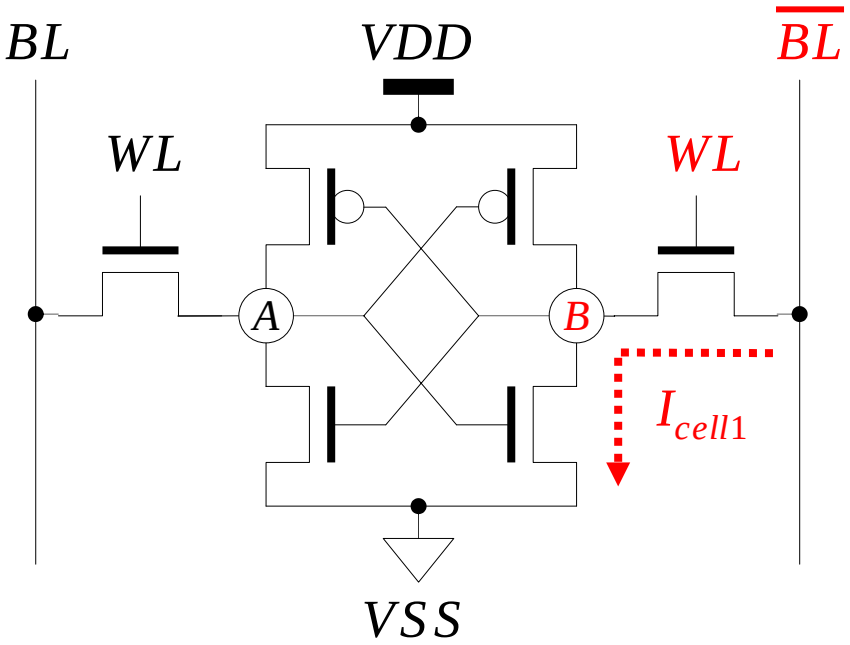
- **Concluding remarks** – It does not end here

Cell (Read) Current
Bit-Line Discharge Current

A = ‘0’ and B = ‘1’

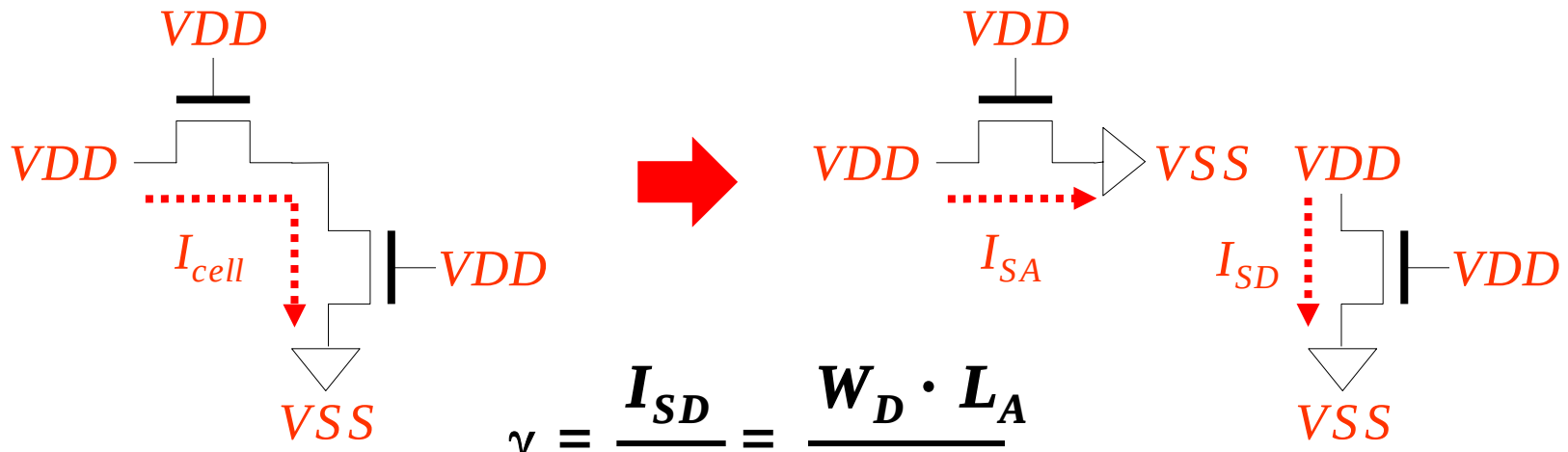


A = ‘1’ and B = ‘0’



$$\Delta V_{BL} = I_{cell} \cdot \Delta t / C_{BL}$$

Bounds on Cell Current where Cell Ratio γ comes in



$$\gamma = \frac{I_{SD}}{I_{SA}} = \frac{W_D \cdot L_A}{L_D \cdot W_A}$$

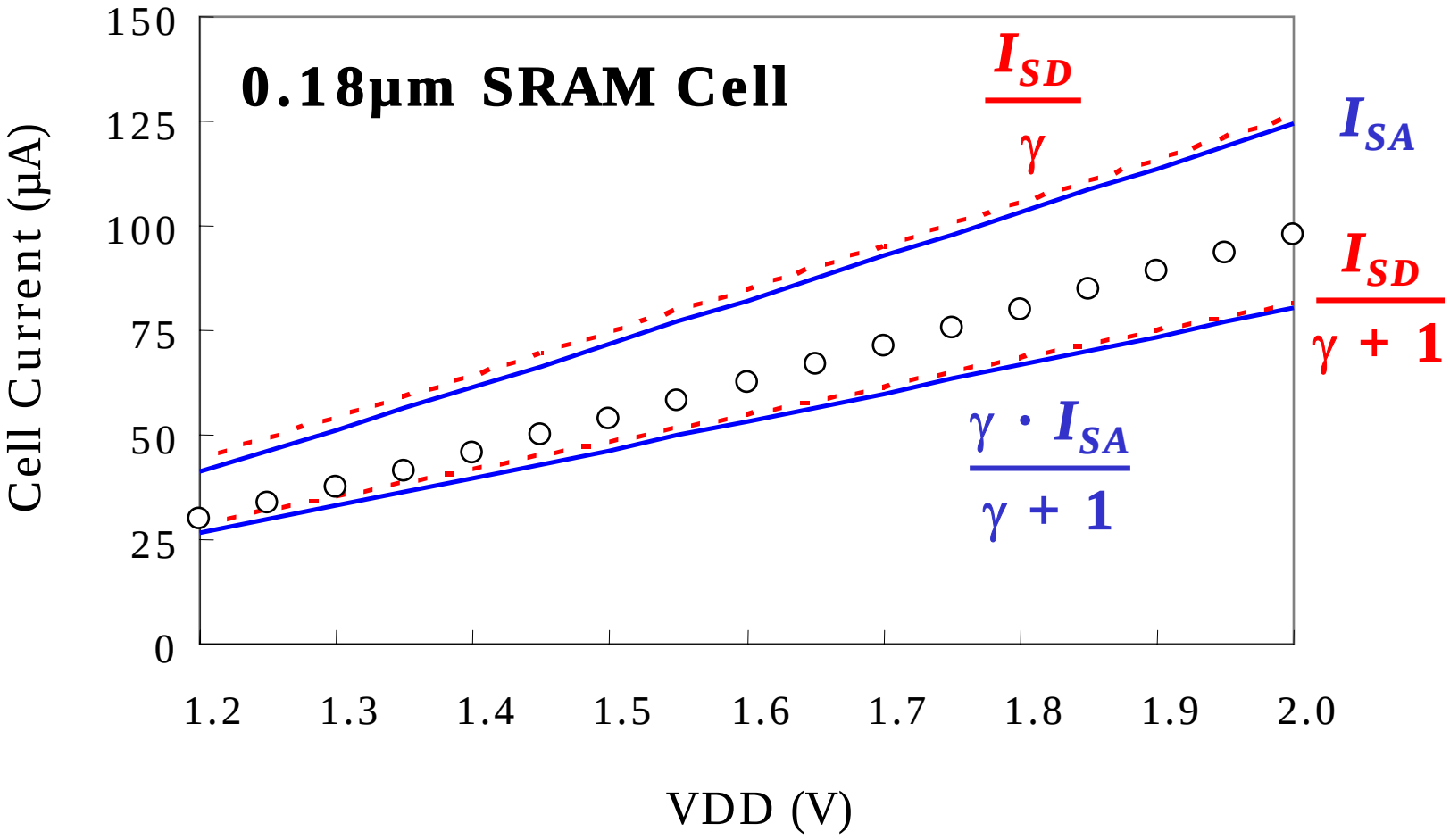
$$I_{cell} < I_{SA}$$

$$I_{cell} < \frac{I_{SD}}{\gamma}$$

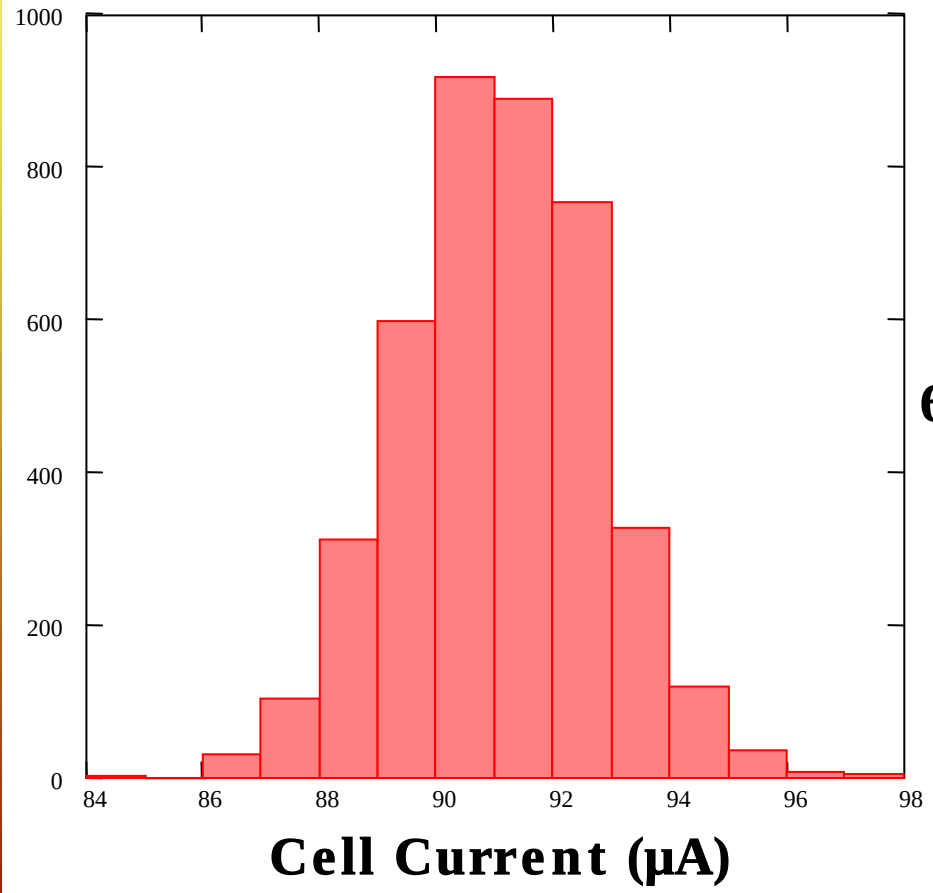
$$I_{cell} > \frac{I_{SA} \cdot I_{SD}}{I_{SA} + I_{SD}} = \frac{\gamma \cdot I_{SA}}{\gamma + 1}$$

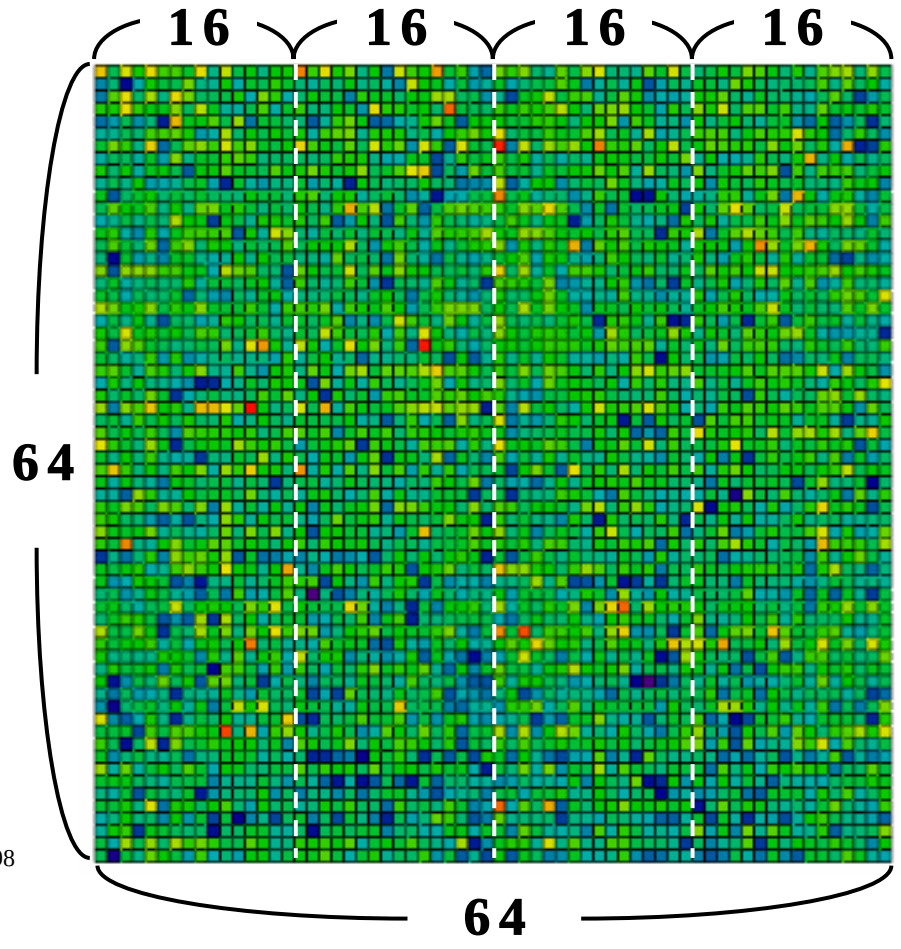
$$I_{cell} > \frac{I_{SD}}{\gamma + 1}$$

Saturation Current Monitor Is Not Good Enough

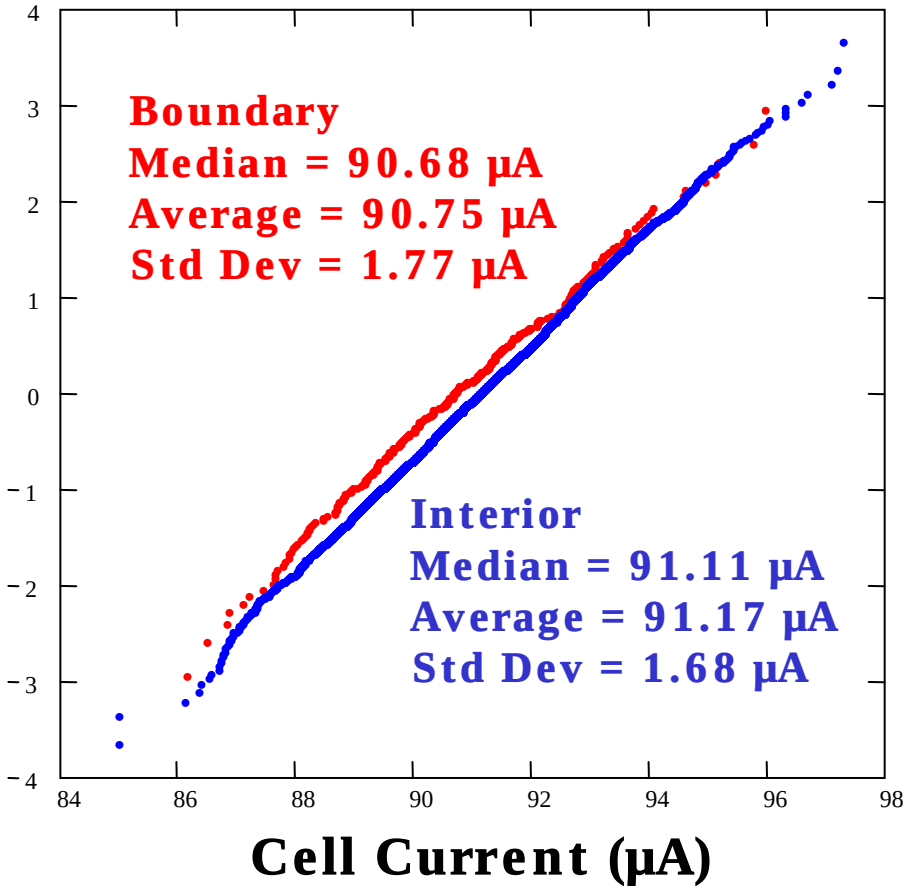


On-Chip Measurement of Cell Current





Location Dependence of Cell Current

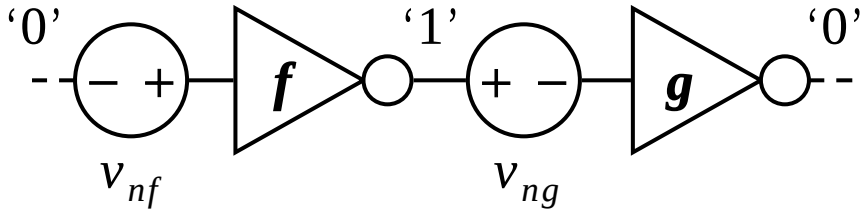


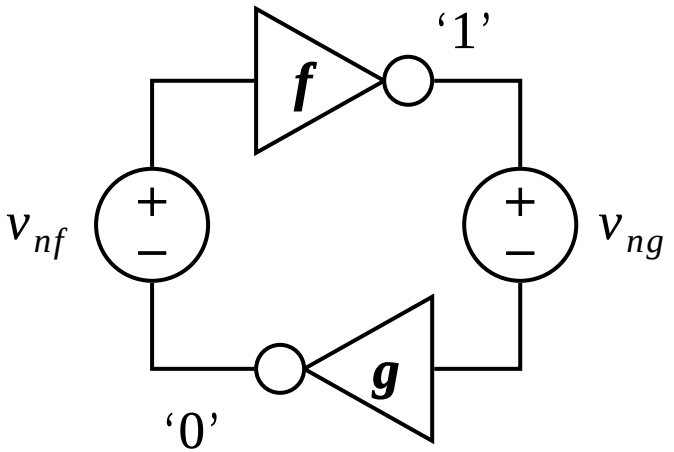
- Cells are divided into two groups by their discharge paths (half cells) being next to a strap of a sub-array or not
- Boundary cells tend to have a smaller mean and a larger standard deviation

Static Noise Margin (SNM)

Every cell has to demonstrate

- Static noise is the DC disturbance present in logic gates
- The worst case occurs when the static noise is adversely present in **all** logic gates in **the same way**
- It is the most important parameter of an SRAM cell

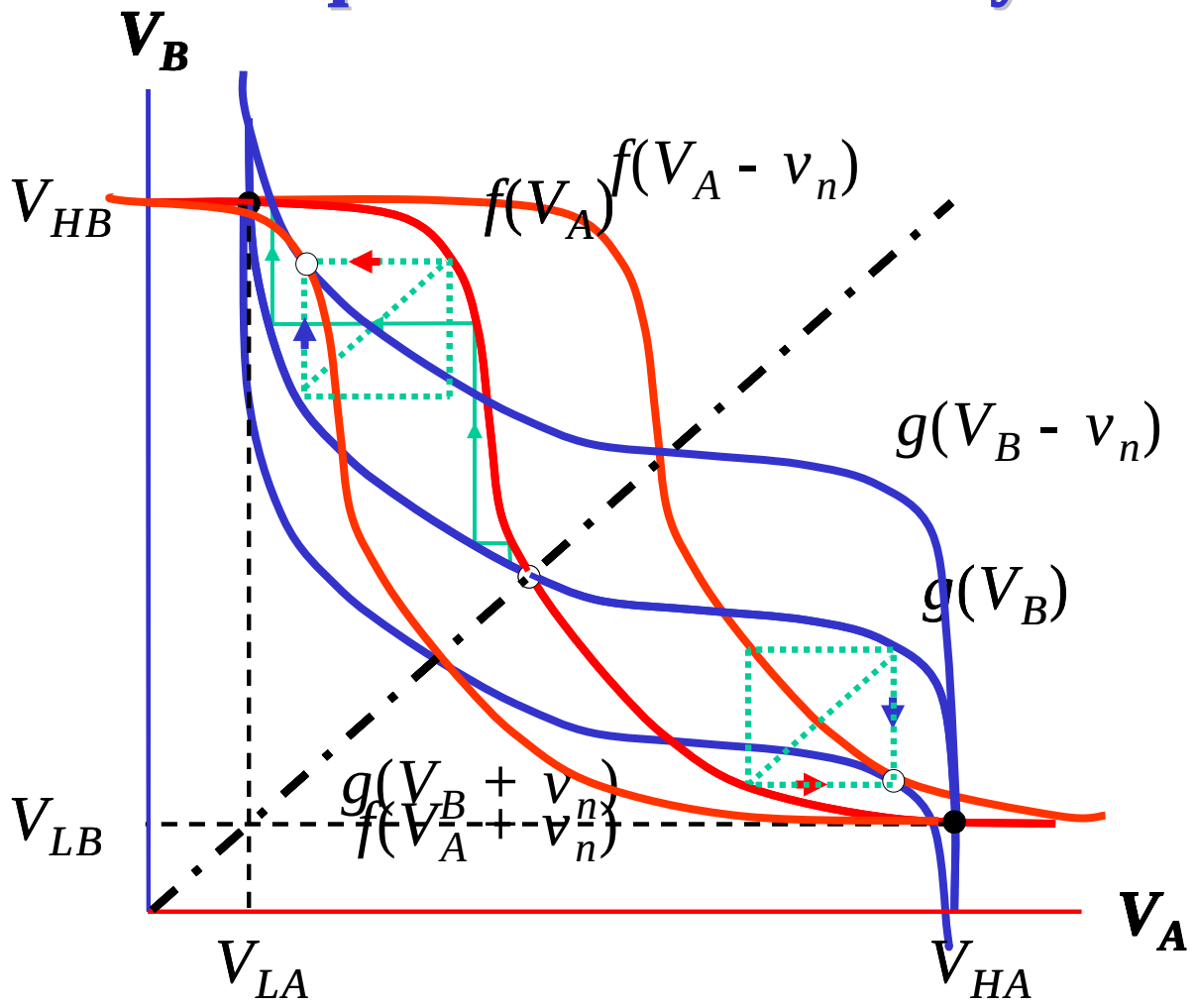




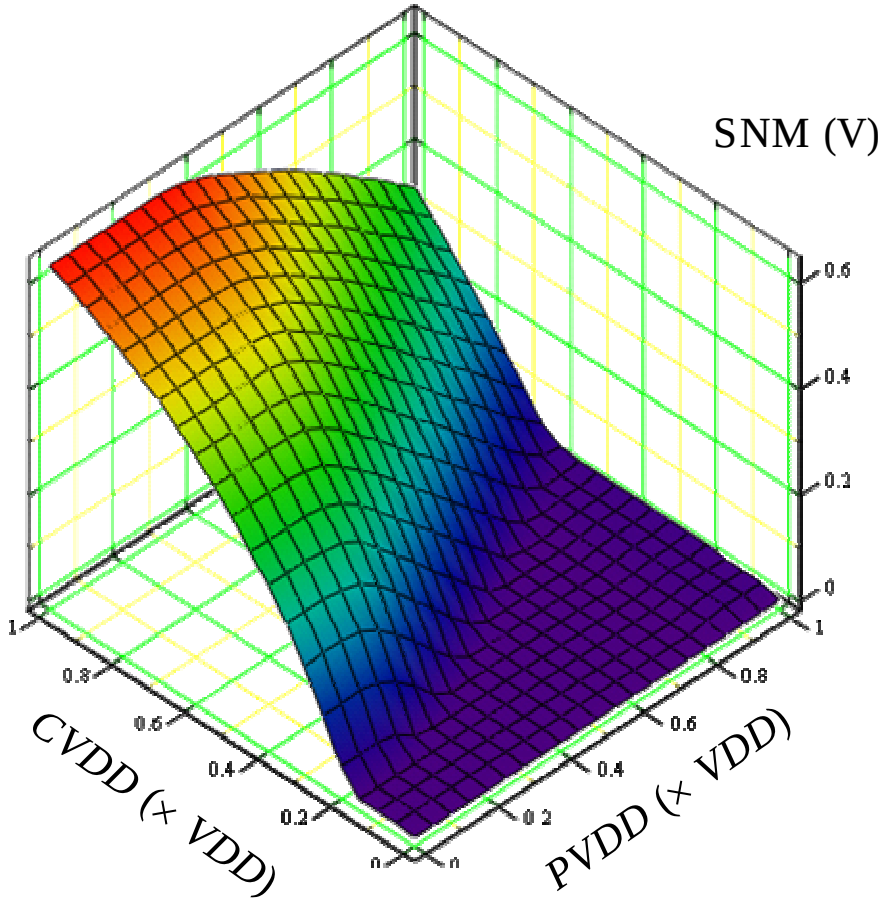
E. Seevinck, F. J. List, and J. Lohstroh "Static noise margin analysis of MOS SRAM cells," *IEEE J. Solid-State Circuits*, vol. SC-22, no. 5, pp. 748-754, Oct. 1987.

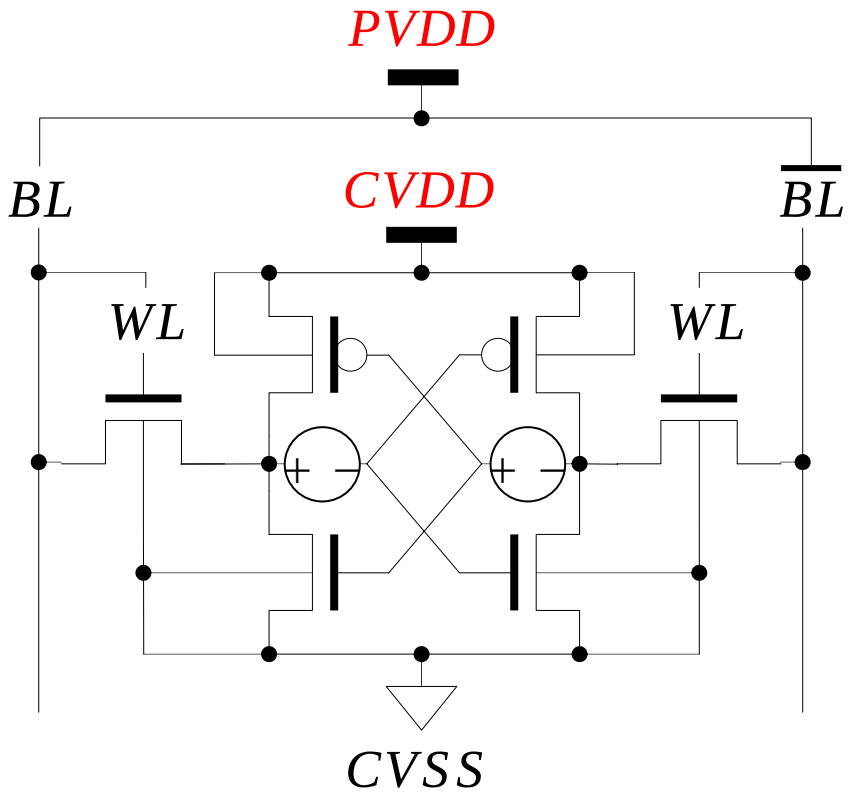
Shift of Meta-stable Point

Maximum Squares in Butterfly Curves



Static Noise Margin
as a Function of Supply Voltages

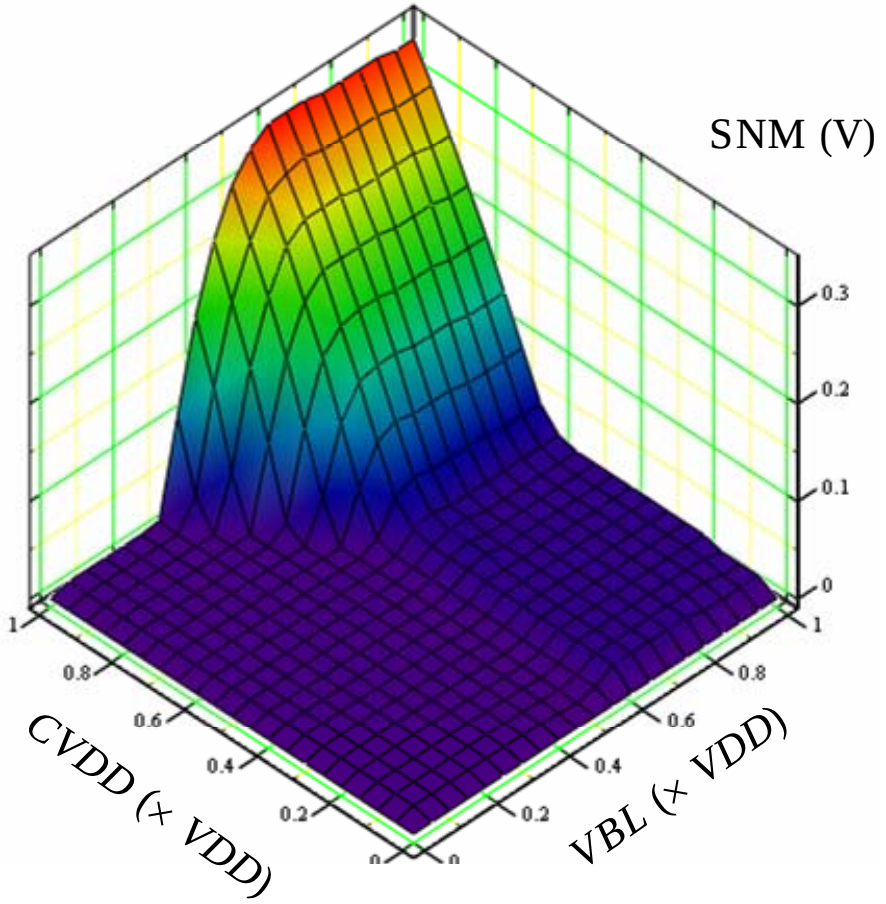


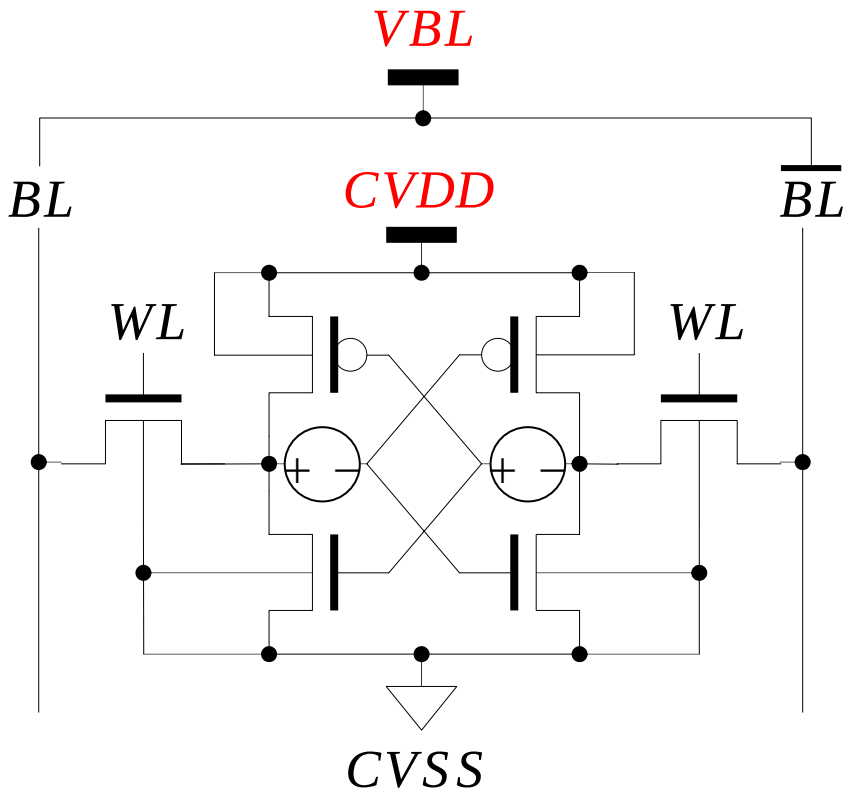


$$WL = BL = \overline{BL} = PVDD$$

D.-M. Kwai *et al.*, "Detection of SRAM cell stability by lowering array supply voltage," *Proc. Asian Test Symp.*, Taipei, Taiwan, Dec. 2000, pp. 268-273.

Static Noise Margin
as a Function of Precharge Voltages

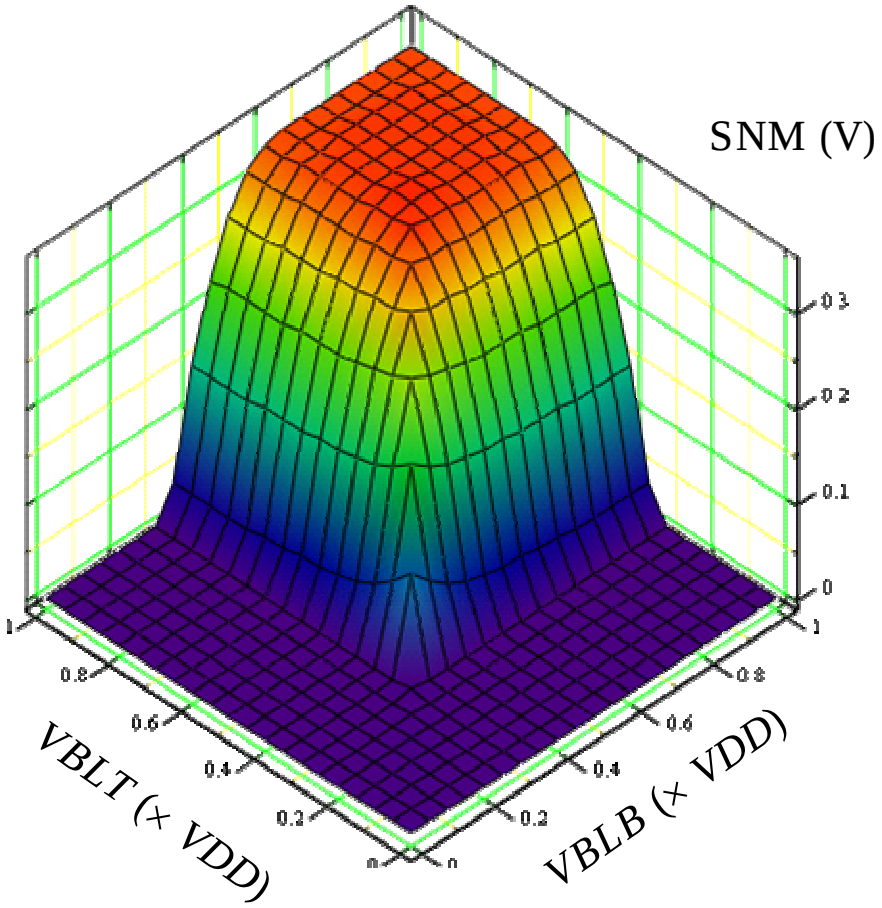


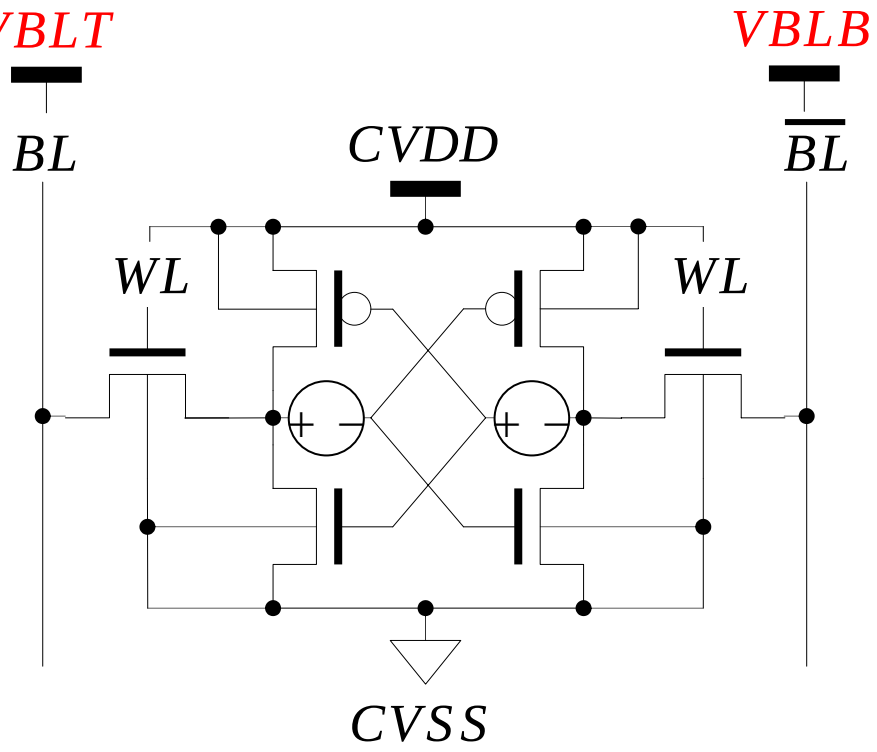


WL = VDD, BL = $\overline{BL}$

K. W. Mai *et al.*, "Low-power SRAM design using half-swing pulse-mode techniques," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1659-1671, Nov. 1998

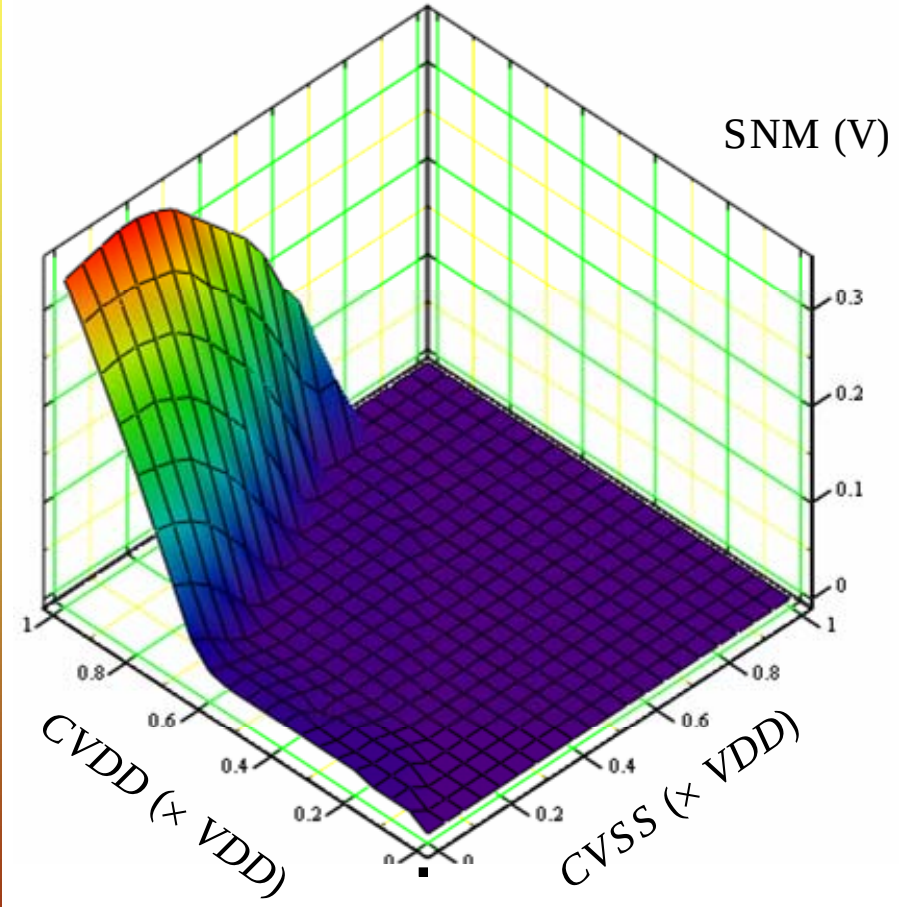
Static Noise Margin
as a Function of Bit-Line Voltages

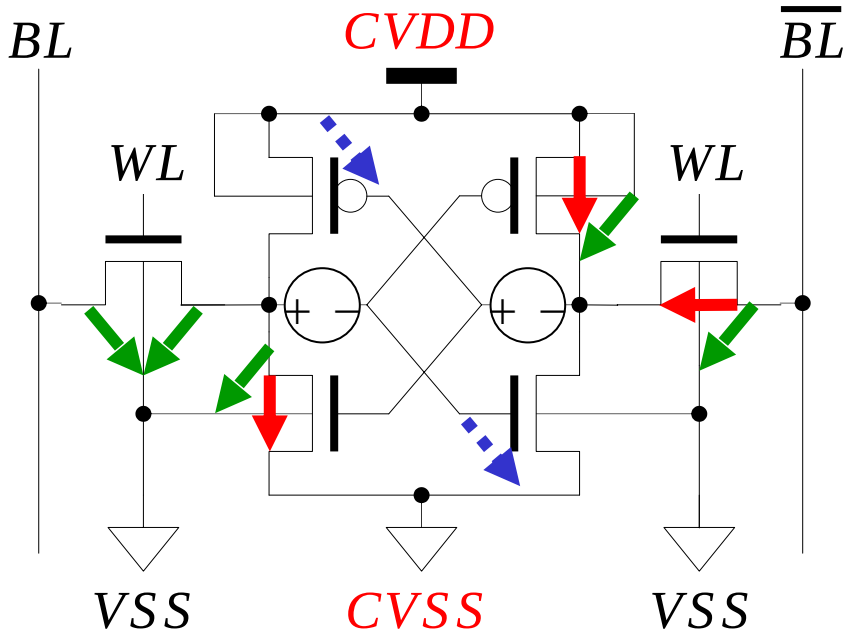




WL = CVDD = VDD

Static Noise Margin
as a Function of Source Voltages





WL = VSS, BL = $\overline{BL}$ = VDD

K. Osada *et al.*, "16.7-fA/cell tunnel-leakage-suppressed 16-Mb SRAM for handling cosmic-ray induced multierrors," *IEEE J. Solid-State Circuits*, vol. 38, no. 11, pp. 1952-1957, Nov. 2003.

Outline

- **6T cell and its variants** – First we generalize and then we derive
- **Peripheral circuits** – Utilization is the key
- **Cell layout** – To be symmetric or to be asymmetric: that is the question
- **Performance indices** – To judge is human
- **Concluding remarks** – It does not end here

What Revive 6T SRAM Cell

- Panel display driver/controller
  - Large wafer quantity that foundries cannot refuse
  - Shrinking pad pitch that cell size becomes an issue
  - Lag behind the most advanced process at least three generations
  - Power, either static or dynamic, is the concern

Challenges in the Future

- To many simulation works, too few measurement results
- Not only to show it functional, but also to prove it manufacturable
- To invent a new cell is costly, it will be a pity to serve only one purpose
- There are still some things we do not know well (e.g., substrate noise)

M.-F. Chang, K.-A. Wen and D.-M. Kwai, "Supply and substrate noise tolerance using dynamic tracking clusters in configurable memory designs," *Proc. IEEE Int'l Symp. Quality Electronic Design*, pp. 225-230 Mar. 2004.