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HIGH DENSITY FOUR-TRANSISTOR SRAM CELL WITH LOW POWER CONSUMPTION

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Abstract-This paper presents a CMOS four-transistor SRAM cell for very high density and low power embedded SRAM applications as well as for stand-alone SRAM applications. The new cell size is 35.45% smaller than a conventional six-transistor cell using same design rules. Also proposed cell uses two word-lines and one pair bit-line. Read operation perform from one side of cell, and write operation perform from another side of cell, and swing voltage reduced on word-lines thus power during read/write operation reduced. Cadence Virtuoso simulation in standard 45nm CMOS technology confirms all results obtained from this paper.

Keywords: SRAM, read operation, write operation, power consumption.

INTRODUCTION: SRAMs are widely used for mobile applications as both on chip and off-chip memories, because of their ease of use and low standby leakage [1], [2]. A six-transistor SRAM cell (6T SRAM cell) is conventionally used as the memory cell. However, the 6T SRAM cell produces a cell size an order of magnitude larger than that of a DRAM cell, which results in a low memory density. Therefore, conventional SRAMs that use the 6T SRAM cell have difficulty meeting the growing demand for a larger memory capacity in mobile applications.

In response to this requirement, our objective is to develop an SRAM cell with four transistors to reduce the cell area size. In this paper, we describe a four transistor SRAM cell. The cell size is 35.45% smaller than a conventional 6T cell using same design rules. Read operation performed from one side and write operation performed from other side of cell. Also swing voltages reduced on word-lines during read/write operation. Thus the dynamic energy consumption reduced during read and write operation.

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1. CELL DESIGN CONCEPT

Fig. 1 shows a circuit equivalent to a developed 4T SRAM cell using supply voltage of 1.1V in 45nm CMOS technology.

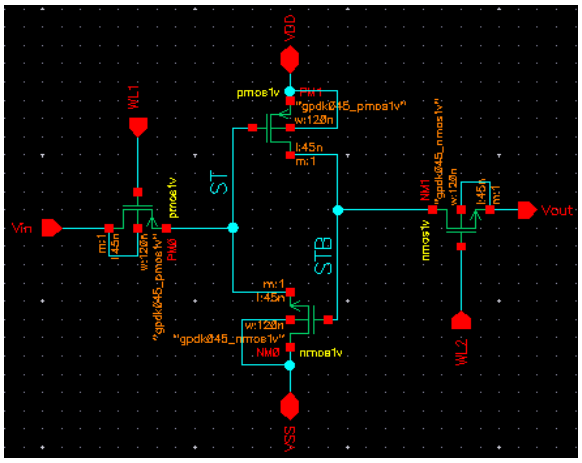

Fig. 1 New 4T SRAM cell in 45nm technology

When '0' stored in cell, load and driver transistor are ON and there is feedback between ST node and STB node, therefore ST node pulled to GND by drive transistor and STB node pulled to VDD by load transistor. And when '1' stored in cell, load and driver transistor are OFF and for data retention without refresh cycle following condition must be satisfied.

$$I_{off\text{-}NMOS\text{-}access} \geq 3 \times (I_{DS\text{-}Load} - I_{G\text{-}Driver})$$

$$I_{off\text{-}PMOS\text{-}access} \geq 3 \times (I_{DS\text{-}Driver} - I_{G\text{-}Load})$$

For satisfying above condition when '1' stored in cell, we use leakage current of access transistor, especially sub threshold current of access transistors. For this purpose during idle mode (when read and write operation don't performed on cell) of cell, BL and BLB maintained at V_{DD} and GND, respectively and word-line1 and wordline2 maintained on V_{Idle1} and V_{Idle2}, respectively. Fig. 2 shows leakage current of cell for data retention when '1' stored in cell. Most of leakage current of access transistors is sub-threshold current since these transistors maintained in sub-threshold condition. Simulation result in standard 45nm technology shows if during idle mode of cell, BL and BLB maintained at V_{DD} and GND respectively, and V_{Idle1}=0.5V and V_{Idle2}=1.1V '1' stored in cell without refresh cycle and thus in idle mode above condition satisfied

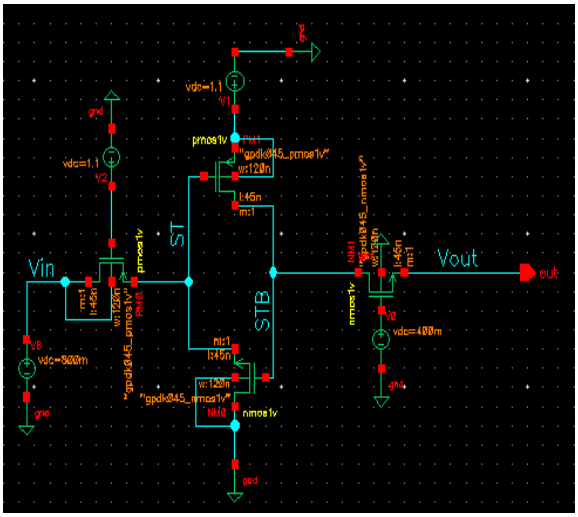

Fig. 2 4T SRAM cell in idle mode when '1' stored in cell

Output waveform of the 4T memory cell design is shown in the figure no.3.

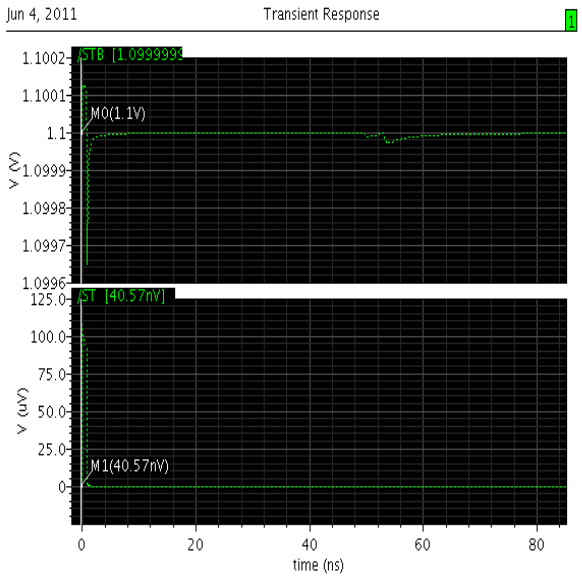

Fig.3 Output waveform of the 4T memory cell design.

The conventional 6T SRAM memory cell is composed of two cross-coupled CMOS inverters with two pass transistors connected to complementary bit-lines [7]. Fig. 4 shows this well known architecture, where the access transistors AXR and AXL are connected to the word-line (WL) to perform the access write and read operations thought the column bit-lines (BL and BLB). All transistors have minimum length (Lmin), while their width is a design parameter. The value of WP defines all PMOS transistors width and WN defines the NMOS driver transistors width, while WAX the width of the access transistors.

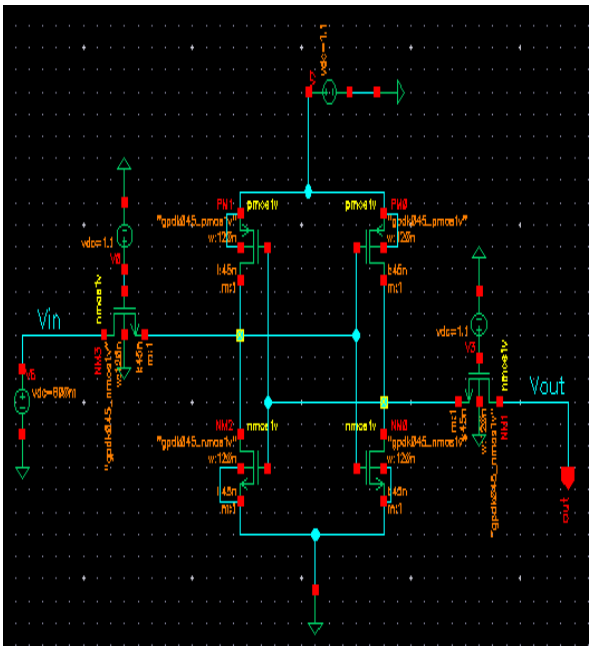

Fig. 4 6T SRAM cell in idle mode when '1' stored in cell

2. WRITE AND READ OPERATION

When a write operation is issued the memory cell will go through the following steps.

1) Bit-line driving: For a write, complement of data placed on BLB, and then word-line1 asserted to V_{DD}, but voltages on word-line2 and BL maintained at idle mode ($V_{word\text{-}line2}=V_{Idle2}$ and $V_{BL}=V_{DD}$).
2) Cell flipping: this step includes two states as follows.
   (a) complement of data is zero: in this state, STB node pulled down to GND by NMOS access transistor, and therefore the drive transistor will be OFF, and ST node will be floated and then pulled p to voltage of BL (V_{DD}) by leakage current (most of this current is sub-threshold current) of

PMOS access transistor, and thus load transistor will be OFF.

(b) complement of data is one: in this state, STB node pulled up to V_{DD}-V_{tn} by NMOS access transistor, and therefore the drive transistor will be ON , and ST node will be pulled down to GND, thus load transistor will be ON and STB node pulled up to V_{DD}.

3) Idle mode: At the end of write operation, cell will go to idle mode and word-line1 and BLB asserted to VIdle1 and GND respectively. When a read operation is issued the memory cell will go through the following steps.

(a) Bit-line Pre-charging: For a read, BL pre-charged to V_{DD}, and then floated. Since, in idle mode BL maintained at V_{DD}, this step didn't include any dynamic energy consumption.

(b)Word-line activation: in this step word-line2 asserted to GND and two states can be considered:

(1) Voltage of ST node is low: when, voltage of ST node is low, the voltage of BL pulled down to low voltage by PMOS access transistor. We refer to this voltage of BL as $V_{BL\text{-}Low}$.

(2) Voltage of ST node is high: when voltage of ST node is high, the voltage of BL and ST node equalized (we refer to voltage of BL in this state as V_{BL}-High). Since in this state, there is very small different between BL and ST node, power consumption is very small.

4) Sensing: After word-line2 deactivate the sense amplifier is turned on to read data on BL. Fig. 5 shows circuit schematic of sense amplifier that used for reading data from new cell.

5) Idle mode: At the end of read operation, cell will go to idle mode and word-line2 and BL asserted to V_{Idle2} and V_{DD}, respectively.

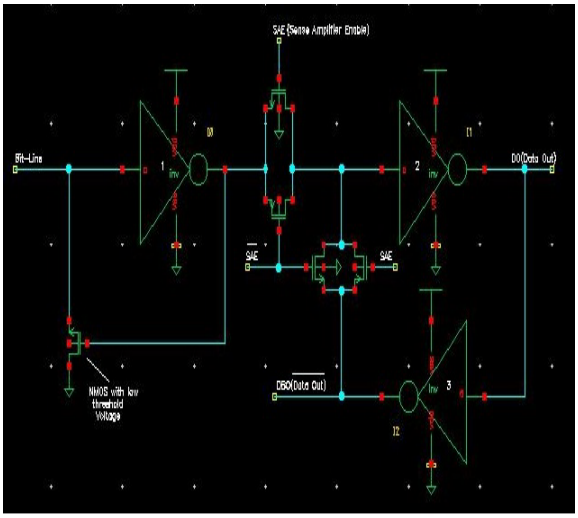

Fig. 5 Circuit schematic of Sense amplifier

3. CELL SIZE

Fig. 6 shows possible layout of 6T SRAM cell in standard 45nm CMOS technology design rules.

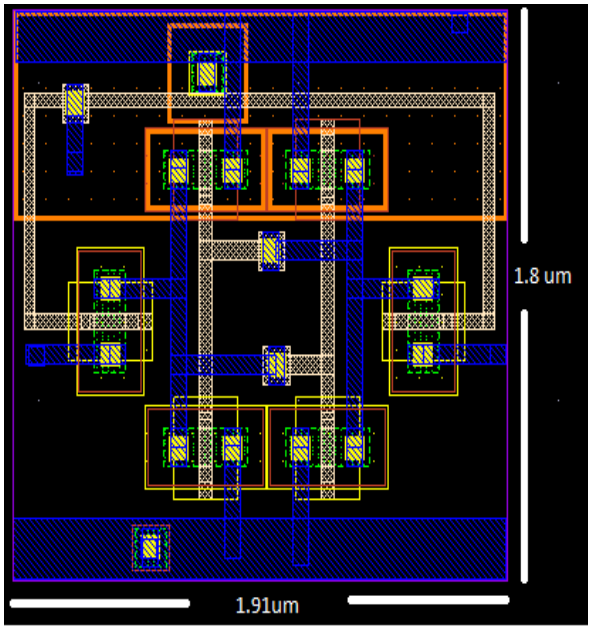

Fig. 6 layout of 6T SRAM cell

Also for comparison, in Fig. 7 shows layout of 4T SRAM cell and 6T SRAM cell in standard 45nm CMOS technology design rules. The 6T cell has the conventional layout topology and is as compact as possible. The 6T SRAM cell requires 3.438 um^2 area in 45nm technology, whereas 4T SRAM cell requires 2.2192um^2 area in 45nm technology. These numbers do not take into account the potential area reduction obtained by sharing with neighboring cells. Therefore the new cell size is 35.45% smaller than a conventional six-transistor cell using same design rules.

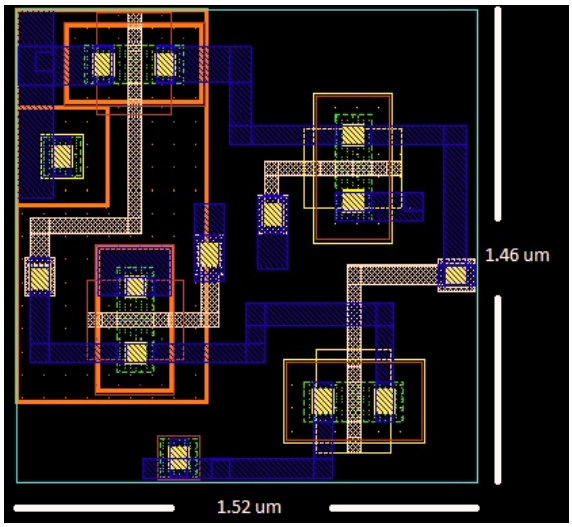

Fig. 7 layout of 4T SRAM cell

4. POWER CONSUMPTION

In each cycle, a read or write operation performed on one cell in SRAMs. Therefore dynamic energy consumption in SRAMs consumed due to the charging and discharging capacitances during read and write operation, and thus during each cycle of SRAMs a certain amount of energy is drawn from the power supply and dissipated. The power consumption of each cycle depended on type of operation (read or write). Furthermore, when the capacitor charged from GND to VDD and then discharged to GND, amount of energy drawn from the power supply and dissipated, equals $C_L V_{DD}^{\ 2}$. And stored energy on the capacitor C_L with voltage V_C equals ½ $C_L V_C^2$. Thus each time the capacitor C_L charged from V_C to V_{DD} and then discharged to V_C amount of power drawn from the power supply and dissipated, obtained by following expression.

$$P_{av} = [(1/T) \int_0^T I\, dt] \times V \qquad [1]$$

In following power consumption of 4T and 6T SRAM cell investigated practically.

A. Power Consumption of 6T Conventional SRAM Cell

There are four premiere capacitances in 6T SRAM cell. These capacitances include bit-lines (BL and BLB) capacitance, word-line capacitance, ST capacitance and STB capacitance. Bit-line (BL and BLB) capacitance is mainly composed drain junction capacitance of access transistor of 6T SRAM cell. Next large capacitance in 6T SRAM cell is word line capacitance and mainly composed of gate capacitance of access transistor of 6T SRAM cell. Next capacitances in 6T SRAM cell are ST capacitance and STB capacitance. These capacitances mainly composed gate capacitances and drain junction capacitance of PMOS load transistors and NMOS drive transistors of 6T SRAM cell.

Average power deliver by the circuit initially on the side of the V_{in} is

$$P_{av\text{-}6T\text{-}Vin} = [(1/T)\,{}_0\textstyle\int^T I\,dt] \times V_{in} \qquad [2]$$

Here $P_{av\text{-}6T\text{-}vin}$ = average power of 6T from Vin supply

$P_{av\text{-}6T\text{-}Vin} = 5.682 \times 10^{-10}$ w

Average power on the output of the circuit is

$$P_{av\text{-}6T\text{-}Vout} = [(1/T)\,{}_0\textstyle\int^T I\,dt] \times V_{out} \qquad [3]$$

$P_{av\text{-}6T\text{-}Vout} = 7.01 \times 10^{-29}$ w

Power consumed by the 6T memory cell is

$P_{consumed\text{-}6T} = P_{av\text{-}6T\text{-}Vin} - P_{av\text{-}6T\text{-}Vout} = 5.682 \times 10^{-10}$ w $= 0.5682$nw

B. Power Consumption of 4T-SRAM Cell

There are four premiere capacitances in 4T SRAM cell. These capacitances include BL and BLB capacitances, word lines capacitances, ST capacitance and STB capacitance. BL and BLB capacitances are mainly composed drain junction capacitance of access transistor of 4T SRAM cell. Next large capacitance in 4T SRAM cell is word-lines capacitance and mainly composed of gate capacitance of access transistors of 4T SRAM cell. And finally next capacitances in 6T SRAM cell are ST capacitance and STB capacitance. These capacitances mainly composed drain junction capacitance of access transistors of 4T SRAM cell and gate capacitances and drain junction capacitance of PMOS load transistors and NOMS drive transistors.

Average power deliver by the circuit initially on the side of the V_{in} is

$$P_{av\text{-}4T\text{-}Vin} = [(1/T)\,{}_0\textstyle\int^T I\,dt] \times V_{in} \qquad [4]$$

Here $P_{av\text{-}4T\text{-}vin}$ = average power of 4T from V_{in} supply

$P_{av\text{-}4T\text{-}Vin} = 5.483 \times 10^{-13}$ w

Average power on the output of the circuit is

$$P_{av\text{-}4T\text{-}Vout} = [(1/T)\,{}_0\textstyle\int^T I\,dt] \times V_{out} \qquad [5]$$

$P_{av\text{-}4T\text{-}Vout} = 3.928 \times 10^{-19}$ w

Power consumed by the 4T memory cell is

$P_{consumed\text{-}4T} = P_{av\text{-}4T\text{-}Vin} - P_{av\text{-}4T\text{-}Vout} = 5.482\times10^{-13}$ w = 0.5482pw

C. Waveforms of 6T & 4T for power consumption

This waveform shows the 6T memory power on the initial side of the circuit.

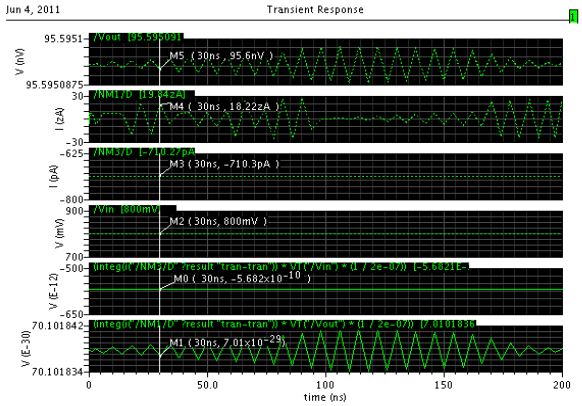

Fig. 8 Power consumption waveform of 6T

Which is connected to the V_{in} having supply of 1.1V and this waveform is shown in the circuit which is constant throughout the all values of the time constant.

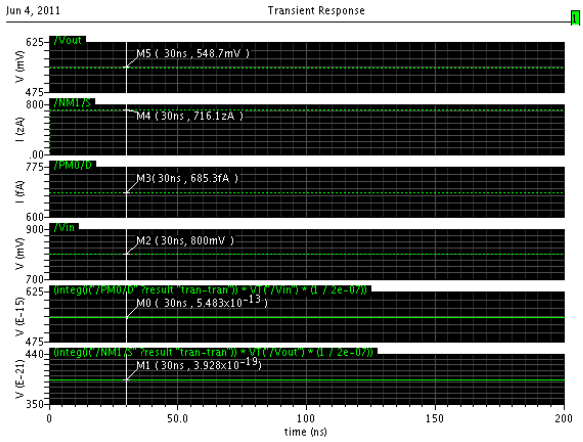

Fig. 9 Power consumption waveform of 4T

Because average power will be the same at all the values of the time constant. At the end side of the circuit the average power will shown in the circuit. As per the 6T memory cell the same process done for the 4T memory cell and the graph is shown as fig .9.

D. Power Consumption Comparison

Cell ratio is an important parameter of SRAM cells. This parameter defined as the ratio of the channel width of driver transistor of memory cell to channel width of access transistor of memory cell

SI. No.	SRAM cell	Avg. power on Vin	Avg. power on Vout	Power consumed
1	6T	5.682×10^{-10}w	7.01×10^{-29}w	0.5682nw
2	4T	5.483×10^{-13}w	3.928×10^{-19}w	0.5482pw

[6]. As cell ratio increased also the area of cell increased.

CONCLUSION

With the aim of achieving a high-density SRAM, we developed a 4T SRAM cell. This cell takes 35.45% less cell area with respect to conventional 6T memory cell and consumes less power with respect to 6T conventional memory cell. Read operation perform from one side of cell, and write operation perform from another side of cell, and swing voltage reduced on word-lines thus power during read/write operation reduced.

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