A 1-GHz Logic Circuit Family with Sense Amplifiers

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***Abstract*—This paper describes a newly developed logic circuit family based on dual-rail bit lines and sense amplifiers that is used extensively in a 1.0-GHz, single-issue, 64-bit PowerPC integer processor, gigahertz unit test site (guTS). The family consists of an incrementor, a count-leading-zero, a rotator, and a read-only memory. Each macro consists of a leaf-cell array, dual-rail bit lines, a row of sense amplifiers, a control block, and peripheral circuits. A common read-out scheme sensing the differential voltage of dual-rail bit lines is used. The hardware was fabricated in a 0.25-μm drawn channel length, six-metal-layer (Al) CMOS technology (1.8-V nominal V_{DD}). Wafer testing was performed using a probe card. The macros were tested cycle by cycle by scanning the input data to the read/write address latches and data latches, and scanning the result out from the output receiving latches. Functional testing was performed on guTS macros at frequencies up to 1.0 GHz at 25°C with nominal V_{DD} (1.1 GHz for the ROM).**

***Index Terms*—CMOS integrated circuits, count-leading zeros, high-speed integrated circuits, incrementor, logic circuits, microprocessors, ROM, rotator, sense amplifiers.**

I. Introduction

THIS paper describes a newly developed logic circuit family based on dual-rail bit lines and sense amplifiers. A sense amplifier, which is commonly used in memory-type circuits, detects the small voltage difference between a bit line and a bit-line bar and amplifies it to a rail-to-rail signal. Our approach to developing logic circuits for our high-frequency research microprocessor, called the gigahertz unit test site (guTS) [1], [2], is to leverage the speed advantage of sense-amplifier-based circuits [3]. A conventional receiver, such as an inverter, generally needs to accept a rail-to-rail signal. This results in a longer latency for read-out for conventional circuits than for sense-amplifier-based circuits if a bit-line potential changes slowly or only partially. The resulting circuits are well structured, consisting of a leaf-cell array, dual-rail bit lines, a row of sense amplifiers, a control block, and peripheral circuits such as decoders and word-line drivers. Our approach has several advantages over a conventional approach. One advantage is its speed, especially for performing a large ANDing function. Another is the ease of making accurate area and speed estimations due to the well-structured circuit nature. A third is resource sharing across macros due to the modular nature of the circuits.

We applied this read-out scheme of sensing dual-rail bit lines to several functional units in the guTS processor. The circuit family includes an incrementor (INC), a count-leading zero (CLZ), a rotator (ROT), and a read-only memory (ROM). The register file in the guTS processor also uses a similar read-out scheme [4].

In the remainder of the paper, we describe the overall characteristics of the circuit family, including a detailed discussion of the read-out scheme and the design of each functional unit. The circuits have been fabricated in a 0.25-μm drawn channel length, six-metal-layer (Al) CMOS technology (1.8-V nominal V_{DD}). We present test results for these macros before concluding the paper.

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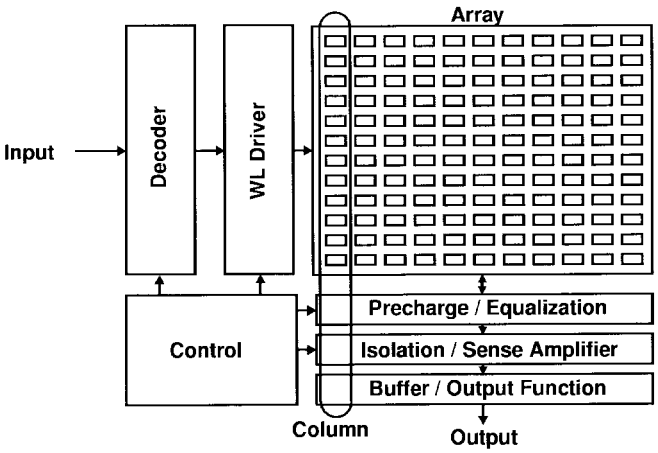

Fig. 1. Basic block diagram of the circuit family.

II. Circuit Design

A. Common Characteristics

Fig. 1 illustrates the basic block diagram of the circuit family. All the circuits have a structure similar to Fig. 1, although the decoder may or may not be present, depending on the function. All the circuits implement 64-bit functions. Therefore, there are 64 columns. One column consists of a stack of array cells, a precharge and equalization cell, an isolation and sense-amplifier cell, and an output buffer/output function gate cell. The bit pitch of each block is matched in both directions. The leaf cell in the array determines the bit pitch.

Fig. 2 illustrates the basic read-out scheme of this circuit family. The PC signal precharges and equalizes the bit lines. The WL_0 to WL_n signals are the word-line signals. The RWL signal is the reference word-line signal. The ISO signal isolates the sense amplifier from the bit lines. The SET signal activates the sense amplifier. The symbol VG stands for the virtual

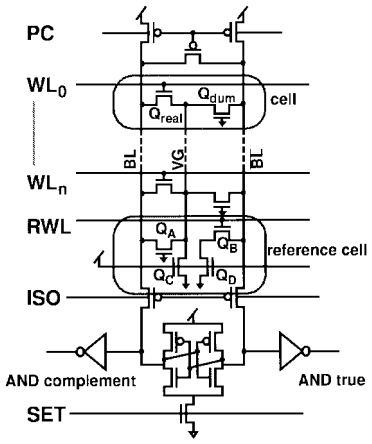

Fig. 2. Common read-out scheme.

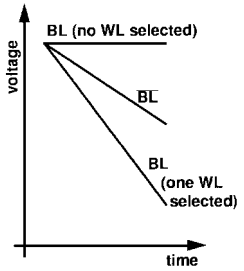

Fig. 3. Simplified transient relationship between BL and $\overline{\text{BL}}$.

ground. The bit-line (BL) and bit-line bar ($\overline{\text{BL}}$) wires are precharged high and equalized. When a word-line is activated, the real device (Q_{real}) in some cell pulls BL down; otherwise, BL stays high. The purpose of the dummy device (Q_{dum}) and Q_A is to load-balance BL and $\overline{\text{BL}}$. The $\overline{\text{BL}}$ wire is always pulled down by transistors Q_B and Q_D in the reference cell. The transistor Q_B is activated by the RWL signal every cycle. Fig. 3 illustrates the simplified transient relationship between BL and $\overline{\text{BL}}$. The device sizes of Q_A, Q_B, Q_C, and Q_D are designed such that when only one word-line is activated, the speed of BL falling is twice the speed of $\overline{\text{BL}}$ falling.

There are three word-line activation patterns.

Case 1) Only the reference word-line is activated; thus, BL stays high and $\overline{\text{BL}}$ falls.

Case 2) The reference word-line and only one word-line along the column are activated; thus, BL is pulled down by only one device.

Case 3) The reference word-line and multiple word-lines are activated; thus, BL is pulled down by several devices in parallel.

For Cases 1) and 2), the voltage difference between BL and $\overline{\text{BL}}$ increases at the rate described above and illustrated in Fig. 3. The SET signal must arrive after the developed voltage difference becomes larger than the designed sense voltage of 150 mV (300 mV for the ROM) and after the ISO signal isolates the sense amplifier from the bit lines. Since the differential voltages for these two cases are identical in magnitude, the SET signal can arrive at the earliest timing for both cases. For the case of multiple active word-lines, BL discharges very quickly, producing a differential voltage well in excess of 150 mV when the sense amplifier sets.

For the multiple word-line case [Case 3)], BL would discharge to ground if the source of the transistor (Q_{real}) were grounded. As a result, it would take a long time to precharge BL. This motivates the use of a virtual ground (VG) and the transistor Q_C. Parallel real devices in the multiple selected cells and Q_C form a voltage divider so that BL never reaches GND even if all word-lines turn on. Therefore, a relatively small PMOS device can precharge the bit-lines completely. The small precharge device results in a small bit-line load, which enables BL to fall faster. Overall, this helps to raise the operating frequency of the circuits. The VG reference voltage and Q_C are used in the INC and the CLZ.

The input signal requirements differ slightly among the circuits, as will be described in more detail in the following sections. The internal control signals and the sense-amplifier set signals are generated from either the global clock or incoming data. The ROM macro uses the incoming data. The INC, CLZ, and ROT macros use the global clock, delayed with a chain of inverters. The ROM's approach is described in detail in the corresponding section. For both cases, extensive simulations have been performed using simulation corner parameters to ensure good tracking between the control signal path and the data signal path. The netlists used in the simulations include wire models with the length, width, and separation from adjacent lines. These values are estimated initially, then updated according to the dimensions of layouts. Some of the simulation corner parameters are listed in Table I. The reset signal of the final dynamic output gate is generated from the global clock to ensure that output pulses are stretched, i.e., output signals are not reset until a fixed time after the start of the next processor cycle. This guarantees that the hold-time requirement of the receiving latches is met and allows the processor to also operate correctly at low frequencies.

B. Advantages

Many functions require ANDing of a large number of signals. Implementing large, yet fast ANDing is always challenging, especially in static CMOS. Our approach allows a large AND function to be implemented in one dynamic stage. Since an AND result can be obtained by performing a NOR of complement signals, each column in Fig. 1 becomes a large AND gate if the word-line signals are complementary. This approach has a substantial speed advantage over using cascaded static gates for wide AND functions.

Second, this proposed approach is fast. Comparison of delays between the proposed implementations and traditional implementations for the INC and ROT functions are made in Table II. Our approach has a speed improvement of roughly 35% over the traditional, static approach and 15% over the traditional dynamic approach. The delay numbers for the traditional implementations are based on macros used in a current IBM product microprocessor [5]. These numbers are projected to the same technology as our implementation with the assumption of the same output load.

TABLE I
SIMULATION CORNER PARAMETERS

Parameter	best	typical	worst	strongNweakP	strongPweakN
V_{DD}	2.16	1.62	1.44	1.40	1.40
Temperature	10 °C	85 °C	105 °C	85 °C	85 °C
Nominal Random Number	0.0548	0.5	0.9452	0.84	0.84

TABLE II
MACRO SPECIFICATION COMPARISON BETWEEN OUR IMPLEMENTATION AND TRADITIONAL STATIC IMPLEMENTATION

Macro	Implementation	Delay	Physical dimension	Area
INC	Our implementation	670 ps	290 μm X 129 μm	37,410 μm^2
	Traditional static implementation	1024 ps*	1166 μm X 27 μm**	31,482 μm^2 **
ROT	Our implementation	640 ps	285 μm X 217 μm	61,845 μm^2
	Traditional dynamic implementation	755 ps*	1296 μm X 160 μm**	207,360 μm^2 **

Two advantages result from the array-based nature of the circuit family. First, the regularity provides predictable delay among the various macros in the circuit family as well as inside each individual circuit. In addition, the area required to implement a function is highly predictable, especially compared to random-logic approaches. Since all the circuit family members have similar structures and dimensions, the latencies among the members are also relatively uniform. Inside the circuits, the latency of the final output is determined by the timing of the sense-amplifier set signal, not by the load on the bit lines directly. Therefore even if bit lines in some of the columns are more lightly loaded than others, the final output in all the bits appears at almost the same time. The output skew between the least significant bit (LSB) and most significant bit (MSB) is due to only the propagation delay of the sense-amplifier set signal to all 64 sense amplifiers.

A fifth advantage of this approach is that many of the elemental circuit blocks can be shared among the functions of interest. For example, the precharge/equalization cells and the isolation/sense amplifier cells are used in all the members, while the decoder block is used in both the ROM and the ROT. All the circuit blocks are optimized and laid out manually; thus, the area penalty due to sharing blocks is minimal. The comparison of physical dimensions and areas between these implementations and traditional implementations is made in Table II. Our approach has roughly an 18% area disadvantage compared to the traditional static approach, and a 70% advantage over the traditional dynamic approach. As above, the dimensions of the traditional implementation are those of macros used in a current IBM product microprocessor.

Noise can be a serious problem in high-frequency dynamic circuits. Our approach is robust with respect to noise, especially common-mode noise, due to the dual-rail bit lines. Five circuit macros in the proposed family (three ROM's, the INC, and the CLZ) have been used in the guTS processor (Fig. 4), which provides a relatively noisy environment for testing these circuits. The testing results of the guTS processor show that all the circuits operate correctly, demonstrating the high noise immunity of this read-out scheme.

In the following sections, each major member of the circuit family is described.

III. IMPLEMENTATION OF CIRCUIT FAMILY MEMBERS

A. ROM Plus AND Gate

Fig. 5 shows the ROM block diagram. The circuit consists of two major blocks: a ROM block and an AND-gate block. The sense-amplifier outputs (ROM outputs) are ANDed with external signals. The ROM receives 6-bit true and complement pulse signals as the ROM address. The final outputs are stretched into the next clock cycle. The size of the ROM is 64 bits $\times$ 64 entries. The leaf-cell array consists of two cell types, namely, "1" cells and "0" cells, and is personalized according to the required function. There are two devices in a cell. One is connected to $V_{\rm DD}$ and the other to GND. For example, in the "1" cell, the BL side transistor (Q_t) is connected to GND and the $\overline{\rm BL}$ side transistor (Q_c) to $V_{\rm DD}$. In addition to balancing the BL and $\overline{\rm BL}$ capacitances, the device connected to $V_{\rm DD}$ (Q_c in the "1" cell and Q_t in the "0" cell) prevents false results caused by leakage. It also helps speed up sense-voltage development. The cell is designed physically such that the connections to power and the bit lines are shared by neighboring cells. Since the bit lines are fully differential and because only one word-line is activated at any time, VG is not needed in the ROM.

The address signal is decoded into one of 64 entries. A combination of a NOR and a NAND decoder is used. The result from the NAND decoder enables one of four blocks. Each block consists of 16 entries, one of which is enabled by the NOR decoder. All the internal control signals except the reset signal of the last stage AND gate are generated from the ROM address signals [6], [7]. The dynamic latch feeding the ROM generates the complementary pulsed input signals. Input pulse widths are 50% of cycle time plus approximately 150 ps. The true and complement input signals are ORed to detect their arrival and the start of a ROM cycle. This start signal triggers the generation of all subsequent control signals. The entire ROM macro is in the standby mode before the input signals arrive,

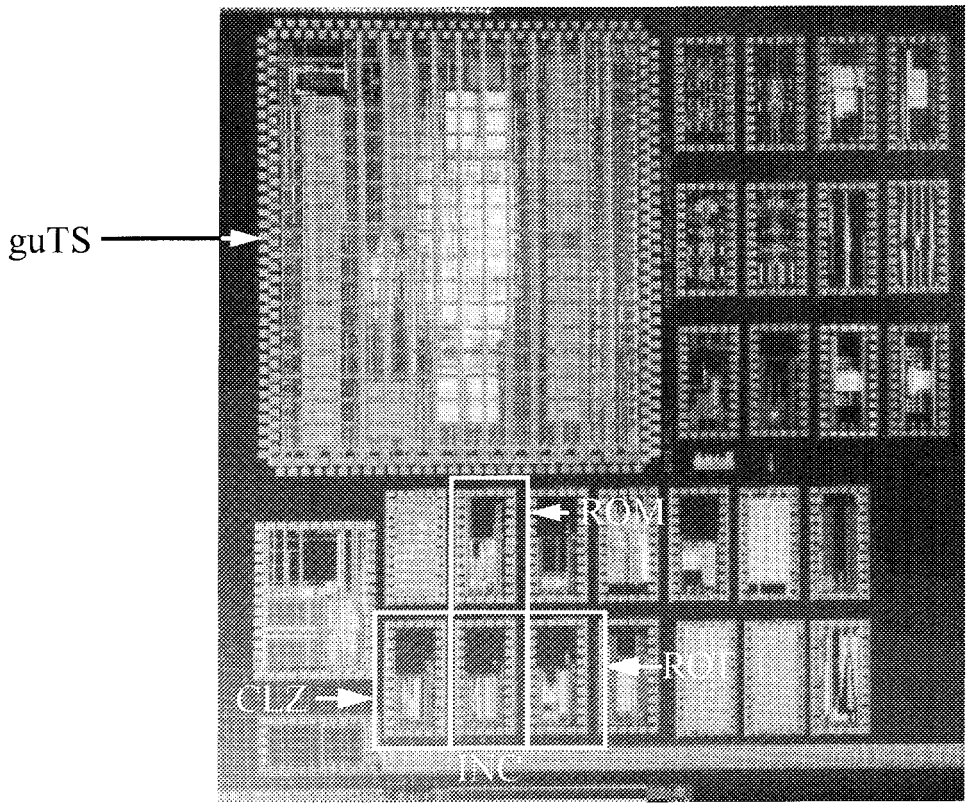

Fig. 4. Microphotograph of guTS processor and stand-alone macro test sites.

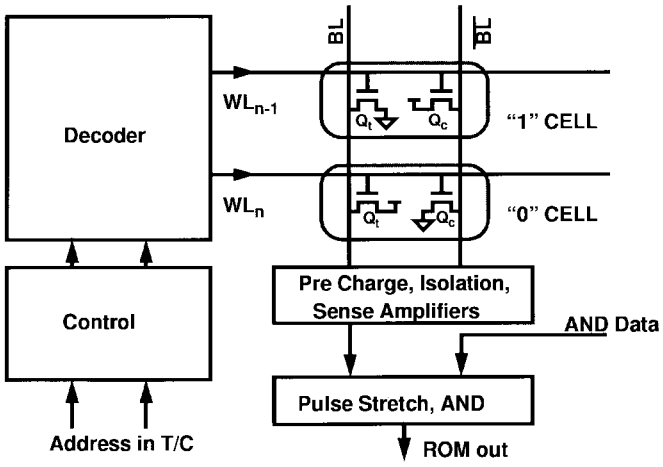

Fig. 5. ROM block diagram.

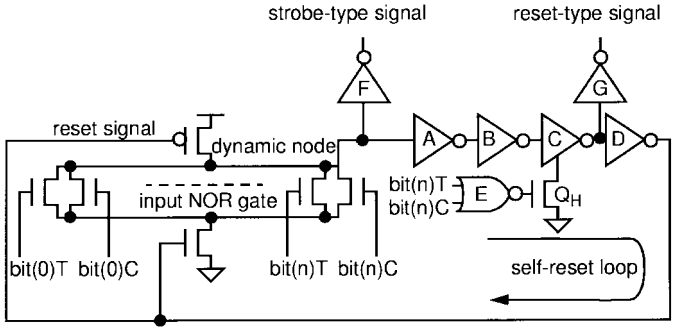

Fig. 6. Simplified view of ROM control block.

which leads to lower power consumption. The ROM employs self-resetting techniques. This reduces the global clock net load because most timing is internally generated rather than directly driven by clocks. Fig. 6 illustrates the simplified control-signal generation scheme. The reset signal is initially high, and the dynamic node is also precharged high (standby mode). When the input data, bits $(0 \cdots n)T/C$, arrive at the input NOR gate, the dynamic node is discharged. Then the inverters A and F start to switch. The output of inverter F is a strobe signal. Several signals in the ROM, such as the SET signal, are strobe signals. The output of inverter A propagates through the self-reset loop and inverter G. The output of the inverter G becomes low after a fixed delay from the arrival of the input signals.

This signal can be used for resetting some dynamic gates. For example, the reset signals of the NOR gate and the NAND gate in the decoder are of this type. The signal that propagates through the self-reset loop resets the input NOR gate. This shuts off the strobe-type signal. Also, this makes the output of the inverter B change to high. However, as long as either bit$(n)T$ or bit$(n)C$ stays high, the output of the static NOR gate turns off the device Q_H so that the low-to-high transition at the output of inverter B does not propagate further. In this way, the static NOR gate E prevents generation of multiple control signals. When some of the input signals arrive late, the strength of the pulldown network in the input NOR gate is weakened. As a result, the subsequent inverters switch slower than normally expected. In this way, this circuit can accommodate a certain range of skew among the input signals.

TABLE III
MACRO CHARACTERISTICS COMPARISON

Macro Name	ROM	INC	CLZ	ROT
Physical Dimension	450 μm x 171 μm	290 μm x 129 μm	295 μm x 130 μm	285 μm x 217 μm
Number of Transistors	10.5 K	6.4 K	6.5 K	10.7 K
Design Input Capacitance	200 fF	30 fF	30 fF	180 fF
Design Output Load	400 fF	100 fF	100 fF	200 fF
EST. Power (@ 1GHz)	57 mW	75 mW	45 mW	80 mW
Simulation Delay	600 ps	670 ps	875 ps	640 ps
Measured Delay	550 ps	640 ps	750 ps	NA

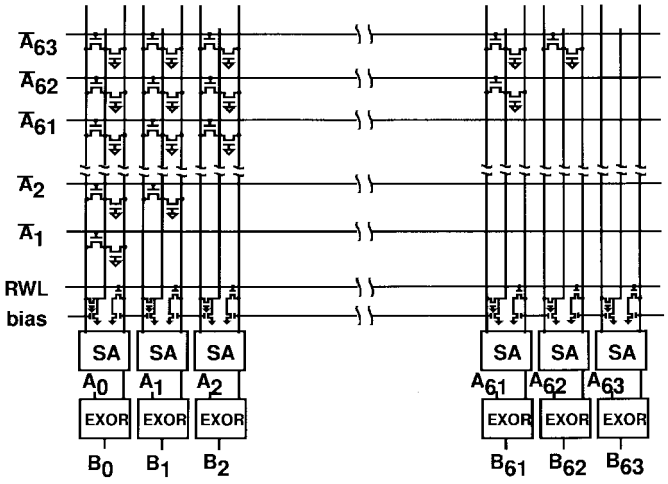

Fig. 7. INC block diagram.

The characteristics of the ROM are summarized in Table III.

B. Incrementor

The INC takes a 64-bit data entry, A_0 to A_{63}, and increments it by one. The INC is designed for static signals for true inputs and either pulse or static signals for complement inputs. All the internal control signals are generated from the global clock. Taking advantage of the large ANDing capability, the required bit-wise function B_i (1) can be realized by first ANDing all the bits from the LSB (A_{63}) to the adjacent bit on the LSB side (A_{i+1}) and then EXORing the result with A_i

$$B_i = A_i \oplus (A_{i+1}A_{i+2}A_{i+3}\cdots A_{62}A_{63}). \tag{1}$$

The intermediate results—that is, the ANDing of A_{i+1} through A_{63}—are computed in the array and sense amplifiers by NORing the complement signals. Fig. 7 illustrates the INC. A static EXOR gate is used at the outputs where the sense-amplifier pulse output is converted into a static signal. The characteristics of the INC are summarized in Table III.

C. Count Leading Zero

The CLZ receives a 64-bit data value and detects the first nonzero bit to generate intermediate results, which are then encoded into a 7-bit output. Fig. 8 shows the relationship between the input data (A) and the intermediate result (X)

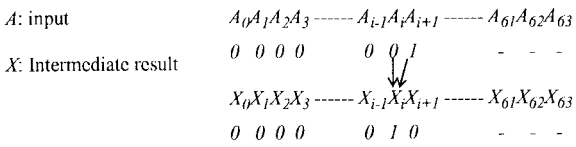

Fig. 8. Relationship between the input data (A) and the intermediate result (X).

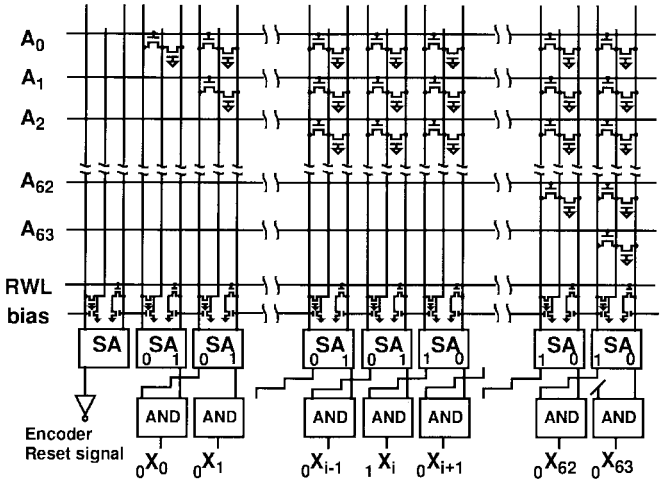

Fig. 9. CLZ block diagram.

pictorially. The CLZ accepts either pulse or static signals as inputs. All the internal control signals except the reset signal for the encoder are generated from the global clock signal. The encoder reset signal is generated through a dummy column. Equation (2) shows how the detection of the first nonzero bit is performed, utilizing the large ANDing capability. Equation (2) is rewritten as (3) to represent the actual implementation

$$X_i = \left(\overline{A}_0\overline{A}\cdots\overline{A}_{i-1}\overline{A}_i)(\overline{\overline{A}_0\overline{A}_1\cdots\overline{A}_i\overline{A}_{i+1}}\right) \tag{2}$$

$$X_i = \left(\overline{A_0 + A_1 + \cdots + A_{i-1} + A_i}\right) \cdot (A_0 + A_1 + \cdots + A_i + A_{i+1}). \tag{3}$$

Fig. 9 illustrates the CLZ. A sense amplifier generates both true and complement results simultaneously. Therefore, the NOR and OR results in (3) are available from the ith column and the $i+1$th column, respectively. This is another advantage

TABLE IV
TECHNOLOGY SUMMARY AND TESTING CONDITION

Item	Value
Technology	IBM CMOS 6X, L_{drawn} = 0.25 μm, L_{eff} = 0.15 μm, T_{OX} = 4.0 nm V_{DD} = 1.8 V, 6 Level Al wiring + 1 local interconnection
Design Conditions	Typical, V_{DD} = 1.62 V, Temp = 85 °C
Test Conditions	V_{DD} = 1.80 V @ Pad, Temp = Room Temp

of this read-out scheme. A static AND gate is used to obtain the intermediate results X, which are then encoded. The encoded results—that is, the final outputs—are the binary representation of the number of leading zeros. When the number of leading zeros ranges from zero to 63, the intermediate results are encoded into six bits (bits 1–6). Bit 0, the MSB, is always zero except for when the number of leading zeros is 64—in other words, the input data bits are all zeros. This is the only case in which the intermediate result X_{63} becomes one, which sets the MSB in the final output. The characteristics of the CLZ are summarized in Table III.

D. Rotator

The ROT receives a 64-bit input data value and 6-bit rotate amount. The input data bits are rotated by the rotate amount (0–63). The input data signals in the present implementation need to be static. The rotate-amount signal can be either pulse or static, and is decoded into one of 64 selections. Again, all the internal control signals are generated from the global clock signal. Equation (4) shows the implementation of the ROT and illustrates the case of rotation by one

A: Input Data, B: Output, R: Rotate amount

$$
\begin{aligned}
B_0 &= R_0A_0 + R_1A_1 + \cdots + R_{62}A_{62} + R_{63}A_{63} \\
B_1 &= R_0A1\underline{+R_1A_2 + \cdots + R_{62}A_{63} + R_{63}A_0} \\
B_2 &= R_0A_2 + R_1A_3 + \cdots + R_{62}A_0 + R_{63}A_1 \\
&\vdots \\
B_i &= R_0A_i + R_1A_{i+1} + \cdots + R_{62}A_{i-2} + R_{63}A_{i-1} \\
&\vdots \\
B_{62} &= R_0A_{62} + R_1A_{63} + \cdots + R_{62}A_{60} + R_{63}A_{61} \\
B_{63} &= R_0A_{63} + R_1A_0 + \cdots + R_{62}A_{61} + R_{63}A_{62}. \qquad (4)
\end{aligned}
$$

Only the column of the rotation by one, the R_1 column, should be selected. In other words, R_1 is a word-line signal. The sense-amplifier outputs become the required outputs (B). The input data (A) are distributed diagonally, as shown in (4). Fig. 10 illustrates the actual implementation of the ROT. The characteristics of the ROT are summarized in Table III.

IV. TEST RESULTS

All testing of these macros was done using a wafer probe card. The macros inside the guTS processor were tested cycle by cycle by scanning the input data into the read/write address latches and data latches and scanning the results out from the output-receiving latches. Scanning is done at the same frequency as functional operation [8]. All the circuits were implemented and fabricated in IBM CMOS 6X technology. The technology characteristics and the testing conditions are summarized in Table IV. The ROM, INC, and CLZ are functional units in the guTS processor. In addition, stand-alone versions of all four members of the circuit family were fabricated for testing purposes. Functional testing was performed on guTS at frequencies up to 1.0 GHz at 25°C with 1.8-V nominal V_{DD} (1.1 GHz for ROM). The test results of the guTS processor show that all the circuits operate

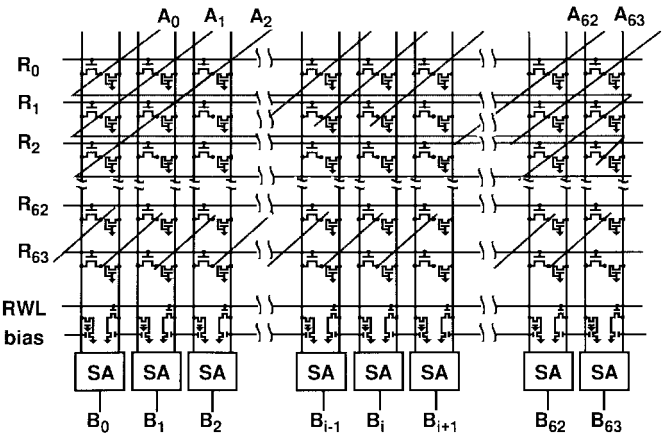

Fig. 10. ROT block diagram.

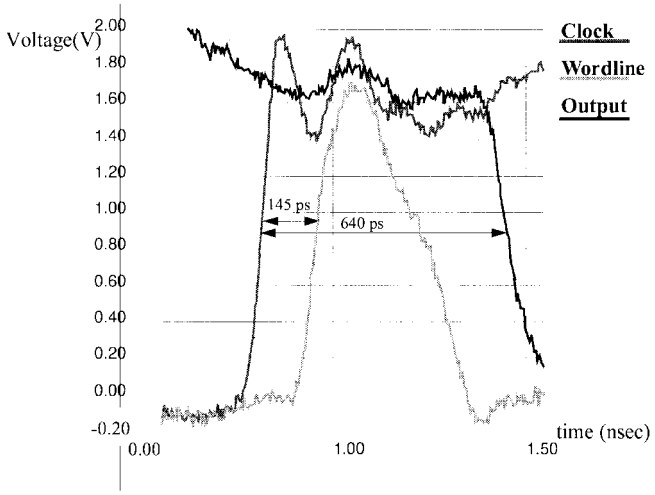

Fig. 11. INC picoprobe measurement.

correctly. The stand-alone versions of the macros were tested at low frequency (10 MHz) due to limitations of the testing equipment. Several macros' propagation delays were measured using a picoprobe. Fig. 11 shows the picoprobe measurement of the INC stand-alone macro. The delay from the clock signal to the word-line signal is 145 ps; the delay from the clock to the output is 640 ps. The delay measurements of the INC and CLZ in Table III were performed at 10 MHz using the stand-alone versions, while the measurements of the ROM were performed at 710 MHz in the guTS processor.

V. Conclusion

A logic circuit family based on dual-rail bit lines and sense amplifiers has been developed. By taking advantage of the fast read-out capabilities of sense amplifiers, high-frequency operation with good noise immunity has been achieved. The logic circuits are implemented in a well-structured array fashion, which enables accurate area and performance predictability. The circuit family includes a read-only memory, an incrementor, a count-leading zero, and a rotator. The circuits have been validated through hardware fabricated in a 0.25-μm drawn channel length CMOS technology. Functional testing at frequencies up to 1.0 GHz show that all the circuits operate correctly.

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