**ABSTRACT**

Memory refers to the physical devices used to store program or data on a temporary or permanent basis for use in a [computer](http://en.wikipedia.org/wiki/Computer) or other [digital](http://en.wikipedia.org/wiki/Digital) [electronic](http://en.wikipedia.org/wiki/Electronics) device. Semiconductor memory is an electronic [data storage device](http://en.wikipedia.org/wiki/Data_storage_device), often used as [computer memory](http://en.wikipedia.org/wiki/Computer_memory), implemented on a [semiconductor](http://en.wikipedia.org/wiki/Semiconductor)-based [integrated circuit](http://en.wikipedia.org/wiki/Integrated_circuit). It forms an integral part of many computer and data processing integrated circuits. On chip caches can effectively reduce the speed gap between the processor and main memory. Almost all microprocessors employ them to boost system performance.

The cost and performance of an embedded system heavily depends on the kind of memory devices it utilizes. Due to high demands on portable products power consumption is a major concern in VLSI chip and microprocessor designs. Low power consumption is highly desirable in battery powered embedded systems. Such systems generally employ memory devices which can operate at low and ultra-low voltage levels. Hence embedded caches need to operate at a faster rate and also consume less power.

Conventionally, cache memories are implemented using 6T SRAM cells. This project aims to implement cache memory using 4T SRAM cells which consume less area compared to that of 6T SRAM cells. Access time of 4T SRAM cache is greater than that of 6T SRAM cache. The performance of 4T cache is improved by implementing divided bit-line technique to reduce delay and power consumption.

Further, Microwind tool is used for creating layouts of both 6T and 4T cache memories of size 8x16. Simulation results are compared for both cases in terms of area, power and access delay. To reduce the delay, “Divided bit-line technique” is applied on a column of 128 cells and from the simulation results it is shown that access delay is reduced.