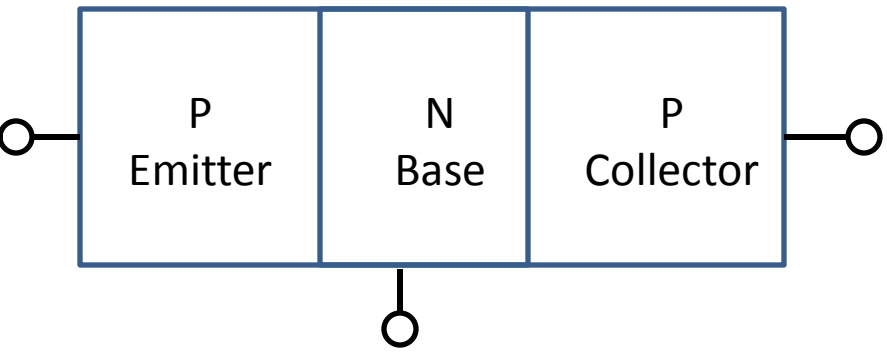
BJT and BJT Digital Circuits

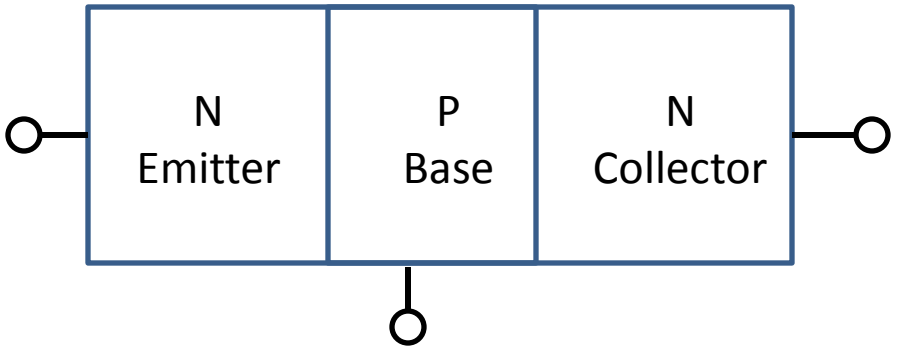
EE 101

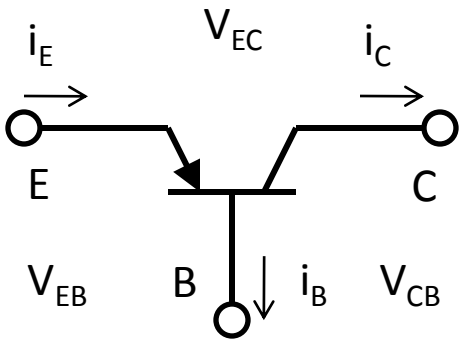
S. Lodha

Reference material: L. Bobrow's Book

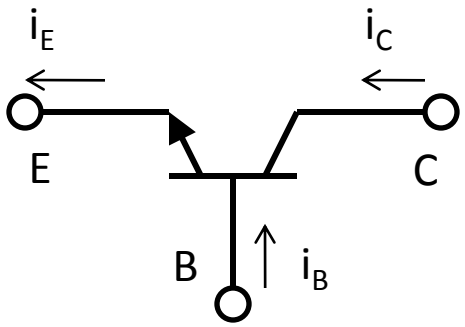
PNP and NPN







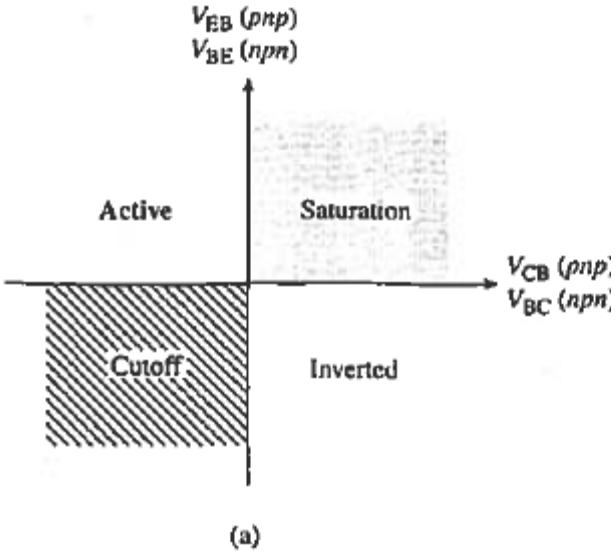
PNP



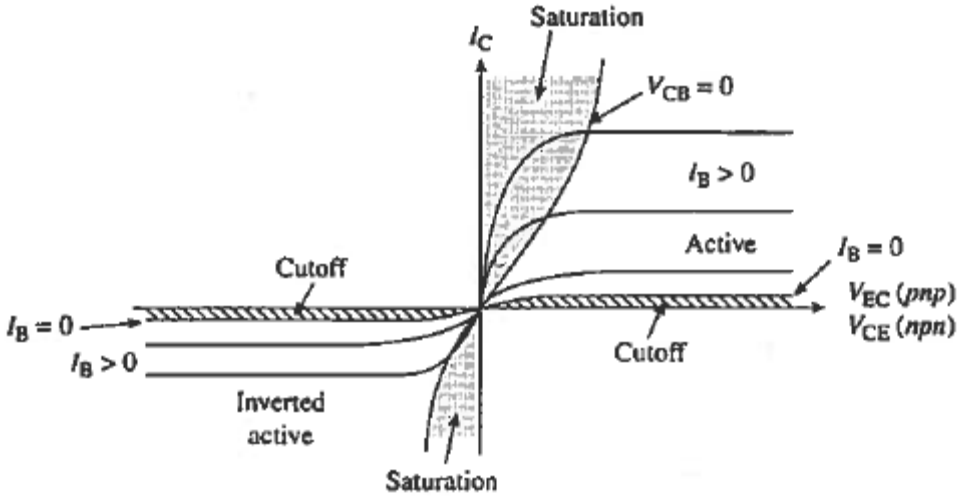
NPN

- $i_E=i_B+i_C$
- Terminal voltages also follow KVL

Biasing Modes

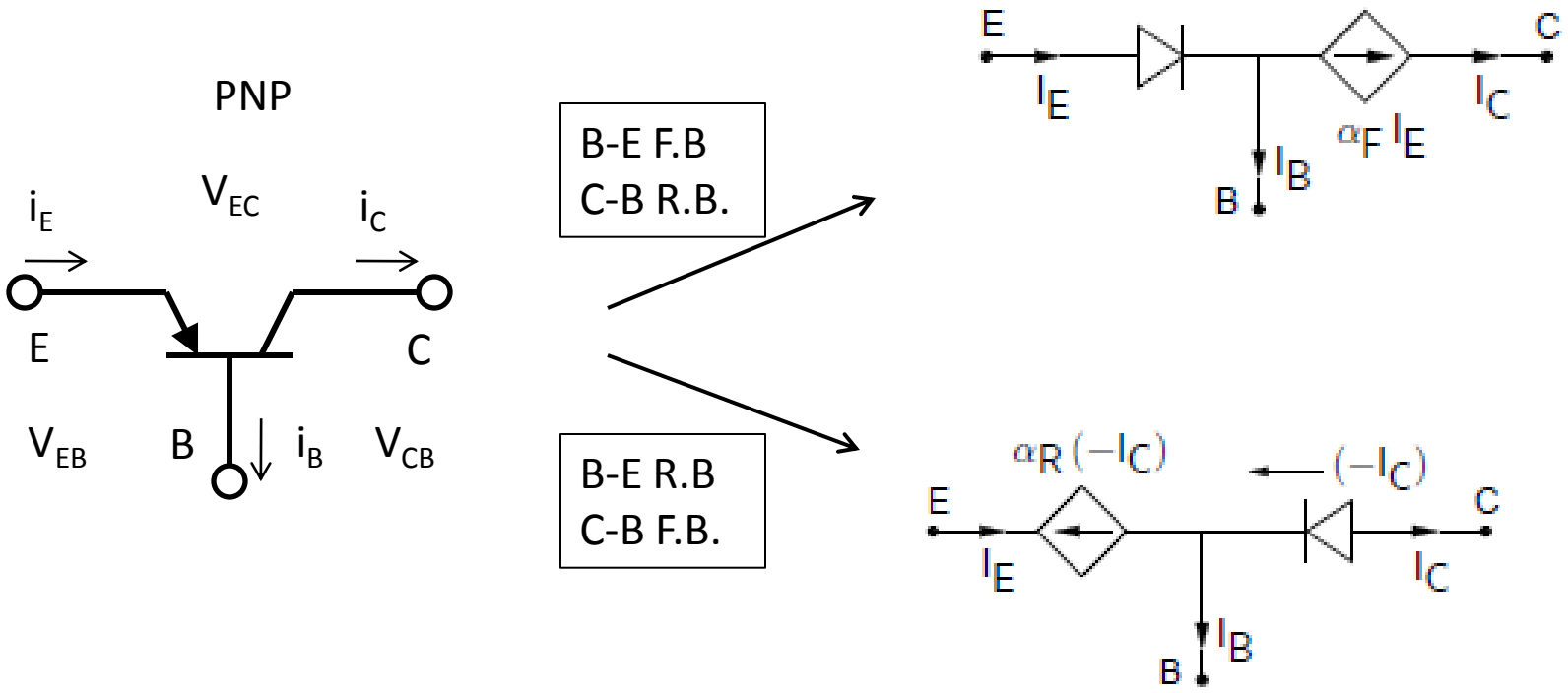


Biasing Mode	Biasing Polarity E–B Junction	Biasing Polarity C–B Junction
Saturation	Forward	Forward
Active	**Forward**	**Reverse**
Inverted	Reverse	Forward
Cutoff	Reverse	Reverse



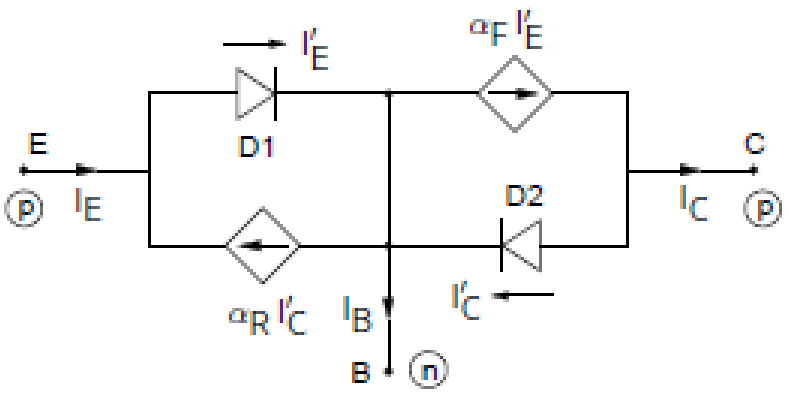
- Amplifier in active mode
  - Analog circuits
- Switch in cut-off and saturation regimes
  - Digital circuits

Biasing modes



- Emitter and collector roles are reversed in reverse-active mode
- Forward and reverse α → α_F (>0.98) and α_R (<0.5) are quite different
  - Structure is not symmetric → P+ / N / P- or N+ / P / N-
- Consequently β_F and β_R are very different too

Ebers-Moll (DC) Model



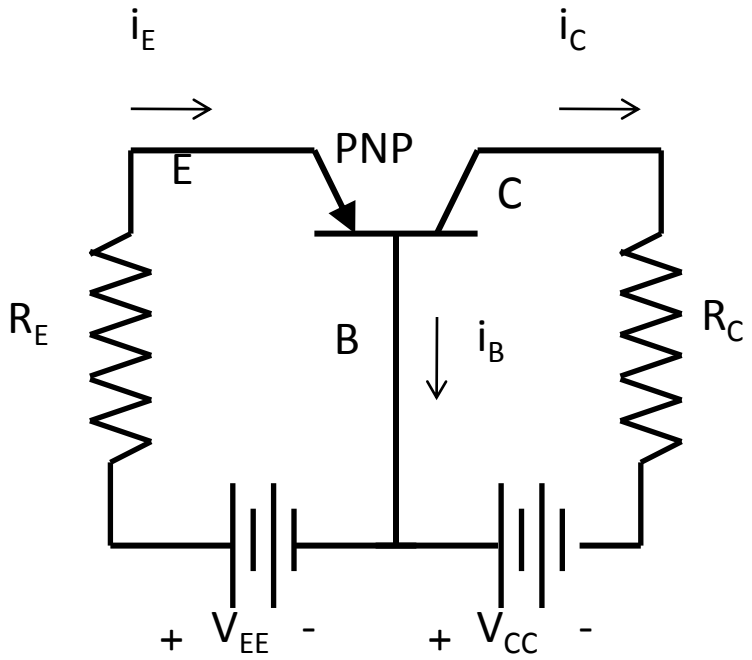
$$I'_E = I_{ES}\left[\exp\left(\frac{V_{EB}}{V_T}\right) - 1\right], \quad I'_C = I_{CS}\left[\exp\left(\frac{V_{CB}}{V_T}\right) - 1\right]$$

$$I_C = \alpha_F I_{ES}\left[e^{\left(\frac{V_{EB}}{V_T}\right)} - 1\right] - I_{CS}\left[e^{\left(\frac{V_{CB}}{V_T}\right)} - 1\right]$$

$$I_E = I_{ES}\left[e^{\left(\frac{V_{EB}}{V_T}\right)} - 1\right] - \alpha_R I_{CS}\left[e^{\left(\frac{V_{CB}}{V_T}\right)} - 1\right]$$

- Similar model for npn
- In saturation, for example, even though D_2 is F.B., $\alpha_F I_E' >> I_C'$ (emitter is heavily doped) and the collector current flows out of collector terminal

Common base PNP in active mode



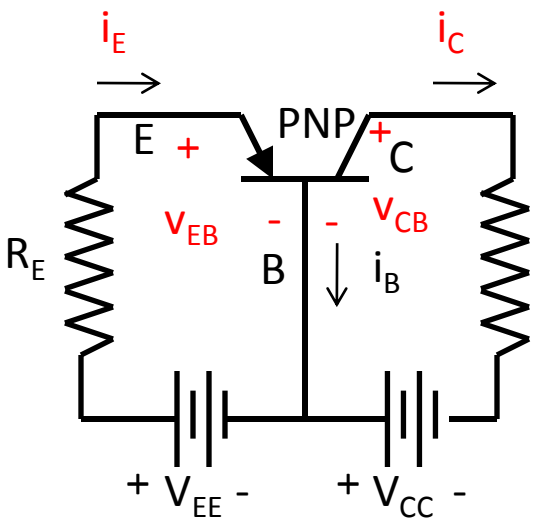
$$i_E = i_{EP} + i_{EN} \approx i_{EP}$$

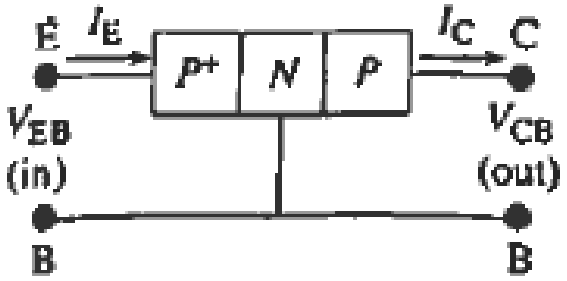
$$i_C = \alpha i_{EP} + I_{CO} \approx \alpha i_E + I_{CO}$$

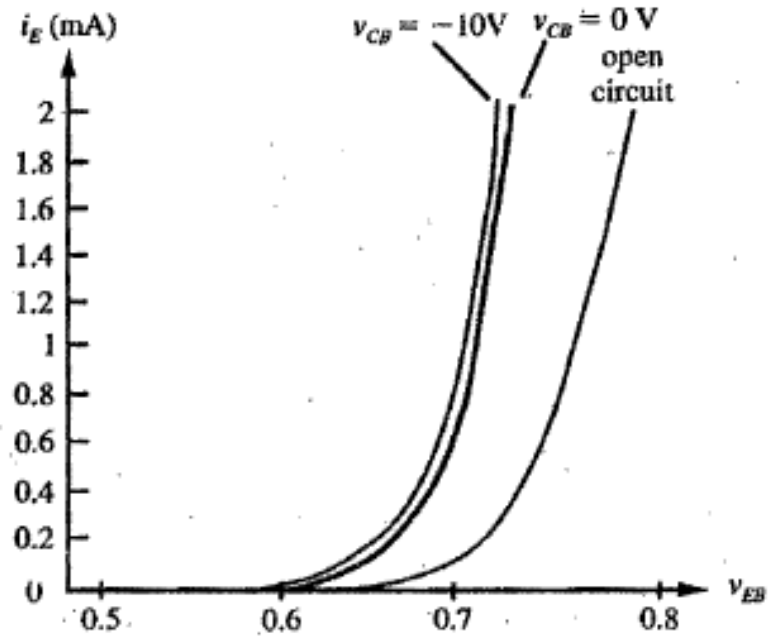
$$\alpha = \frac{i_C - I_{CO}}{i_E} \approx \frac{i_C}{i_E}$$

- Emitter current is mainly due to hole diffusion
- Collector current is due to holes that make it + reverse current
- Ratio of emitter/collector is the “large signal current gain” α
- α is typically 0.95-0.99

Input Characteristics (Common base pnp)

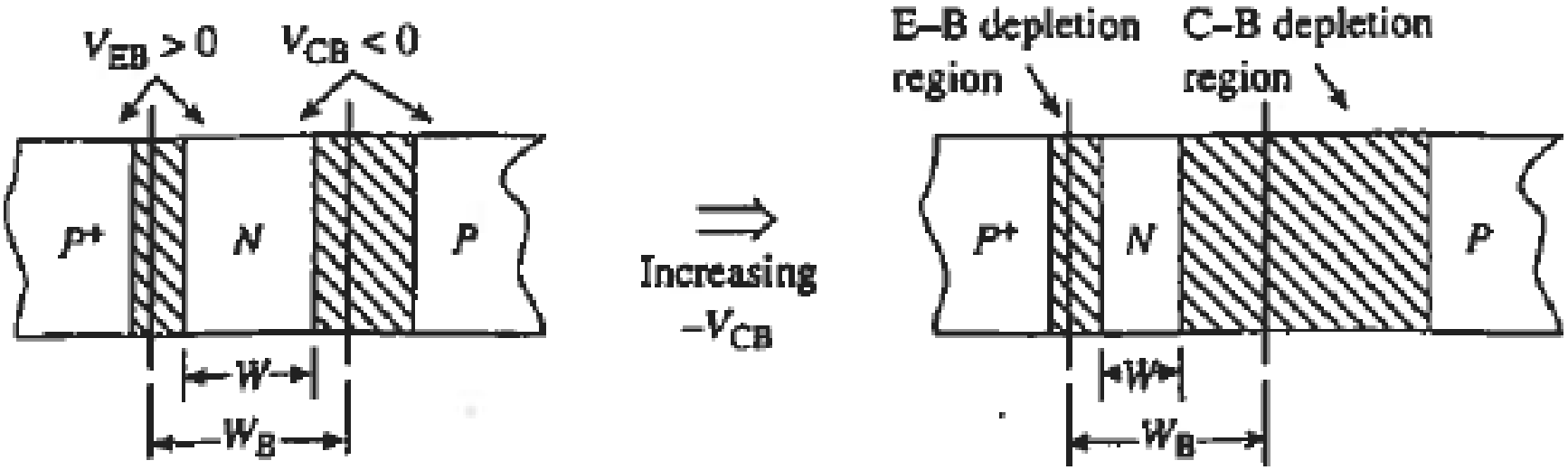






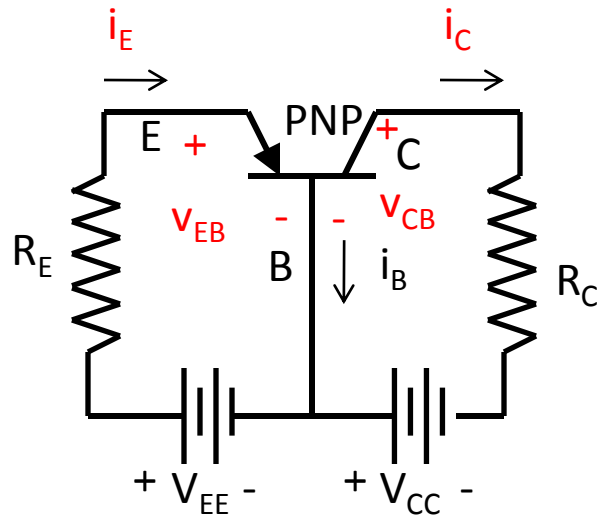
- Input characteristics i_E vs v_{EB} (varying v_{CB})
- As v_{CB} increases, base W decreases, dp/dx increases, i_E and i_C increase for the same v_{EB}
- This effect is also called “base width modulation”

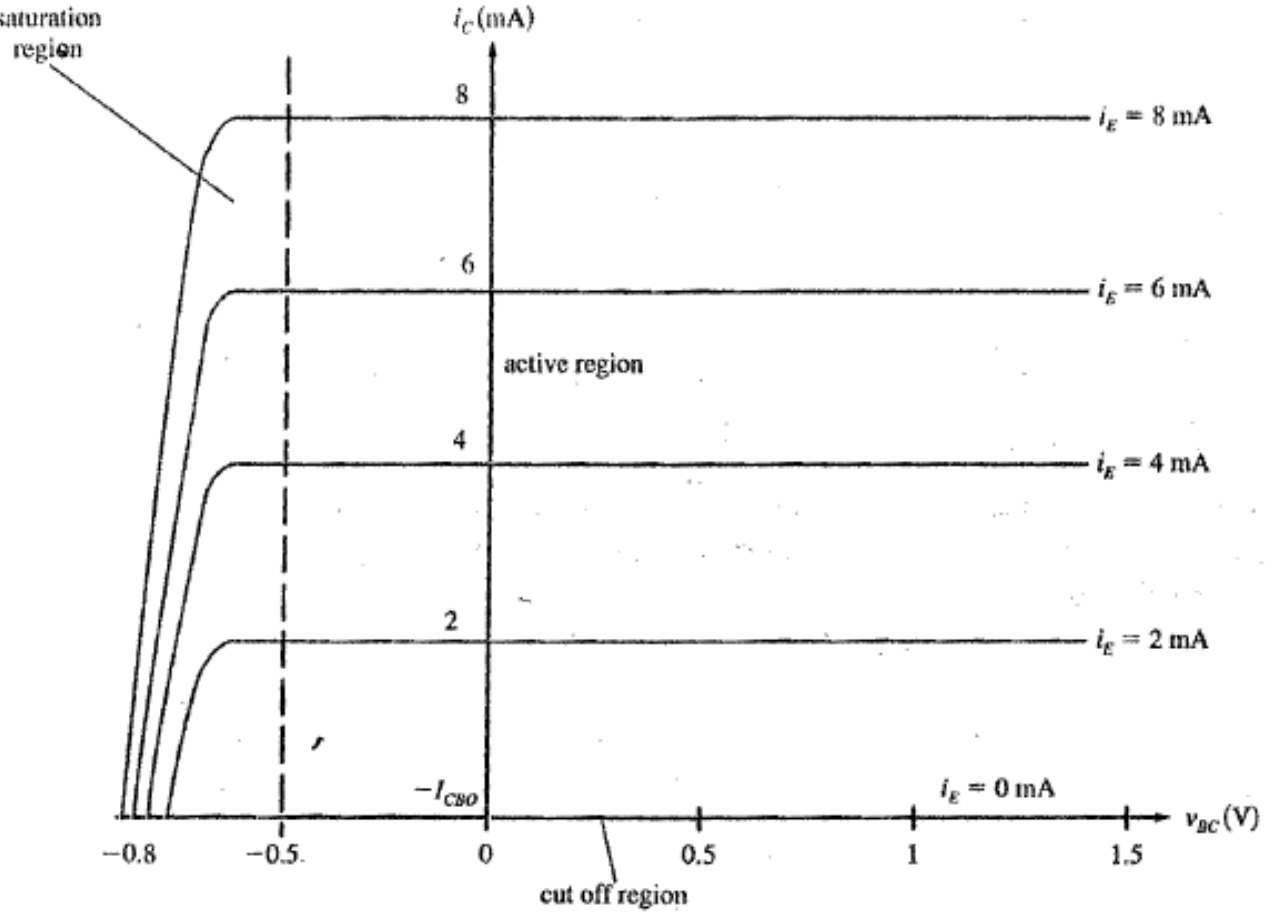
Base width modulation



- Intuitively, as v_{CB} increases (reverse bias)
  - i_E increases (dp/dx increases)
  - i_B decreases (recombination in base decreases)
  - α increases (less recombination in base)
- Also called the "Early effect" → after J. Early

Output Characteristics (Common base pnp)



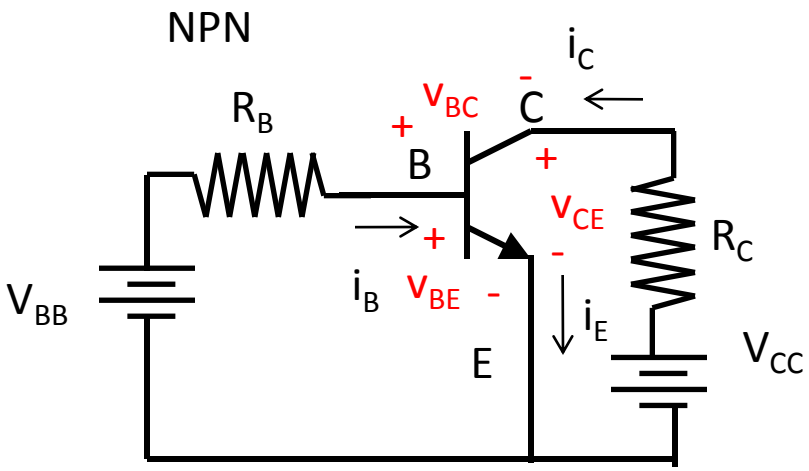


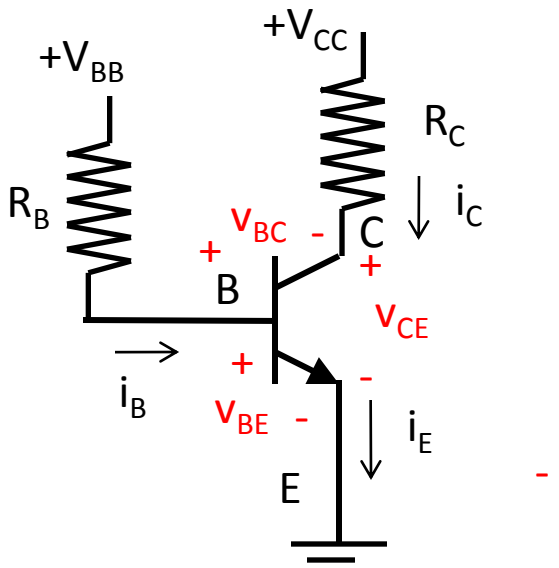
- Output characteristics i_c vs v_{BC} (varying i_E)
- i_E=0, I_{CBO}→ CB current with emitter open, typically nA (~0)

<u>Different biasing regions</u>

- Right of dashed line: i_E>0 (FB), v_{BC}>-0.5 (Vγ) (RB)→ Active region
- For i_E>0, -0.8<v_{BC}<-0.5, both FB → saturation
- On or below i_E=0 → cutoff

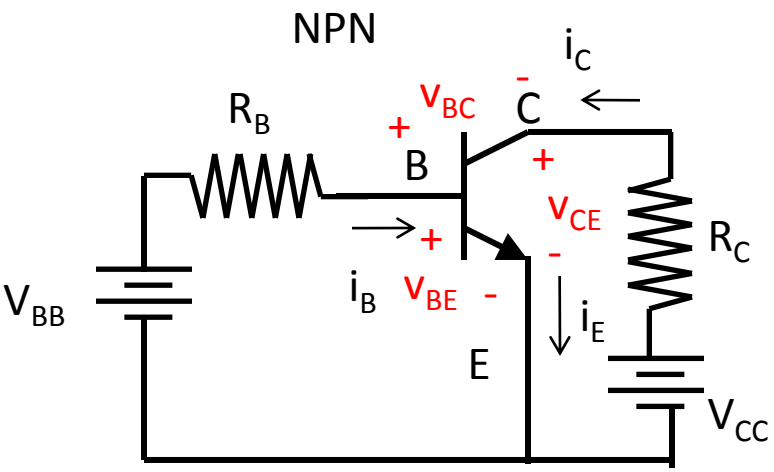
Common emitter npn





- Active region: Large V_{BB} → v_{BE}>0 → BE jn F. B.
- For CB R.B.: $v_{BC}=v_{BE}-v_{CE}<V_\gamma$ (V_γ cut-in voltage=0.5 V)
  - Therefore, $v_{CE}>v_{BE}-V_\gamma$ =0.7-0.5=0.2 V
- v_{CE}>0.2 V ensures reverse bias CB junction

Common emitter npn



$$i_C = \alpha i_E + I_{CO} = (i_B + i_C)\alpha + I_{CO}$$

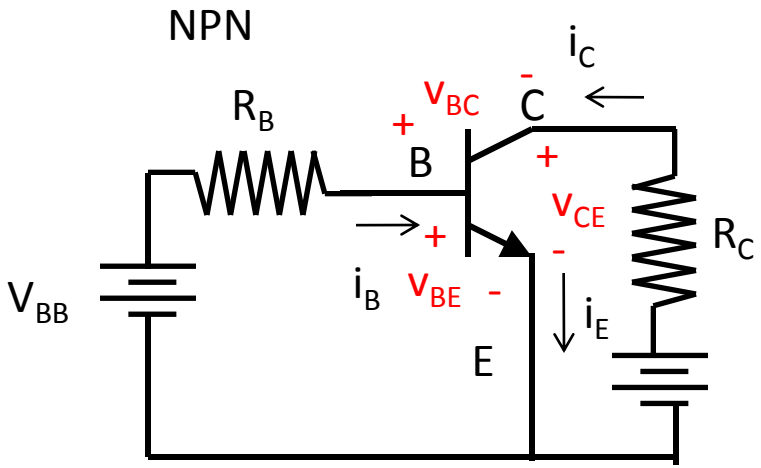
$$i_C = \frac{\alpha}{1-\alpha} i_B + \frac{1}{1-\alpha} I_{CO} = \beta i_B + (1+\beta) I_{CO}$$

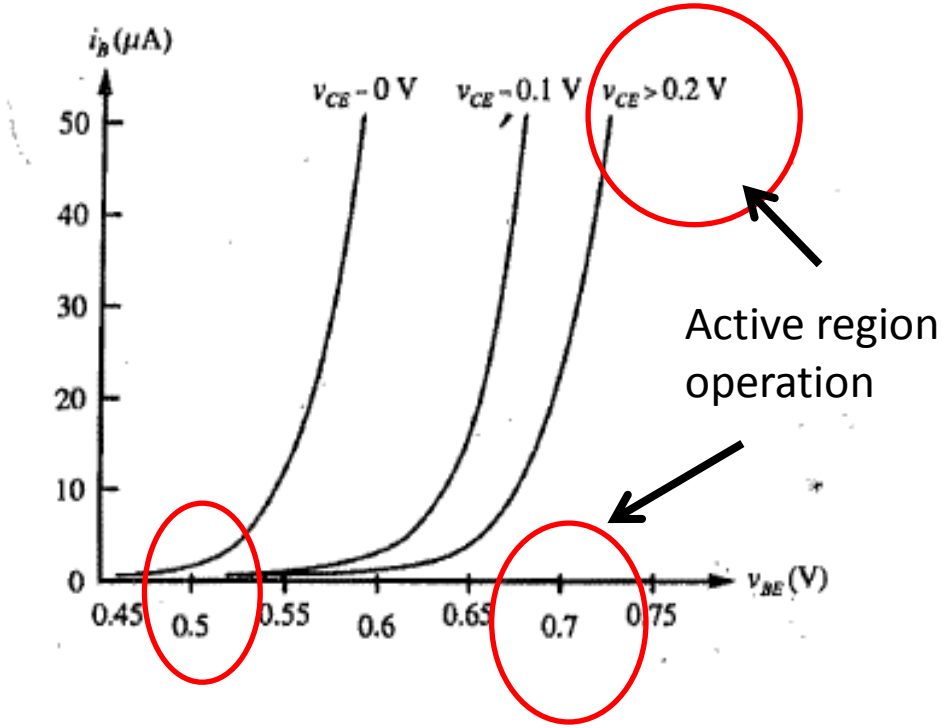
$$\beta = \frac{\alpha}{1-\alpha} \approx \frac{i_C}{i_B}$$

α=0.98 → β=49
α=0.99 → β=99
1% change → 100% change

- β is the large signal common emitter gain, much larger than α

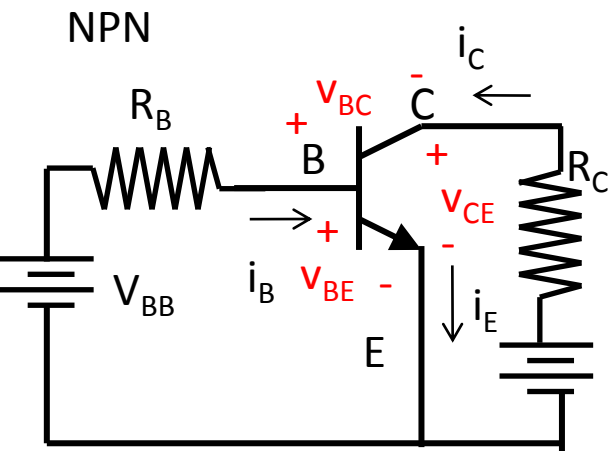
Input Characteristics (C.E. npn)

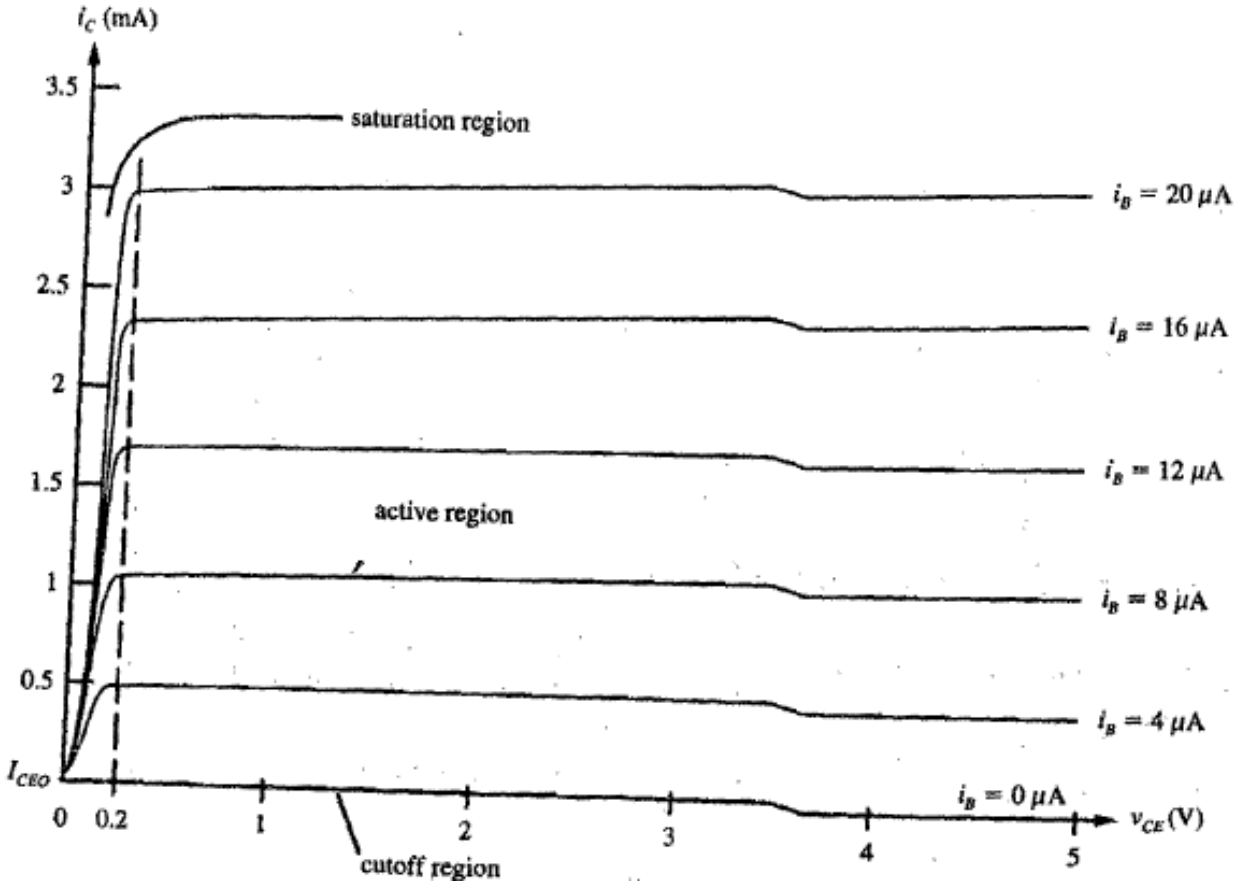




- As v_{CE} increases → v_{CB} ($v_{CB}=v_{CE}-v_{BE}$) increases → W_B decreases → i_B decreases (less recombination)
  - Therefore for same v_{BE} you get less i_B

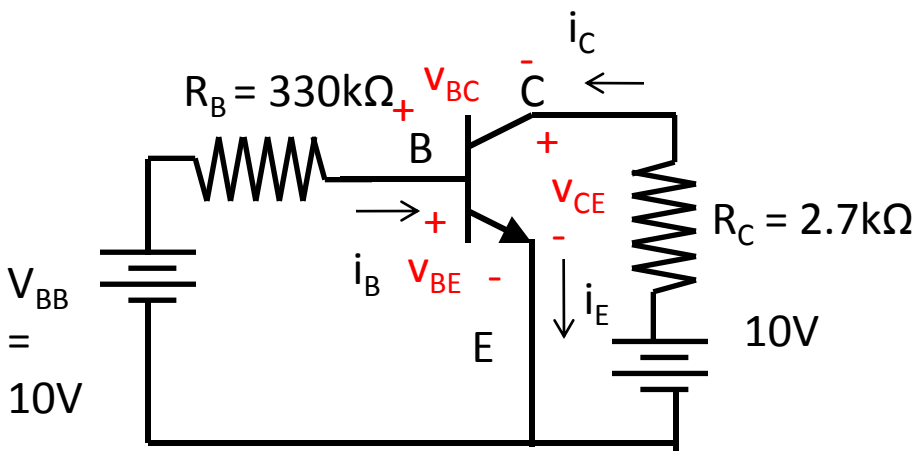
Output Characteristics (C.E. npn)

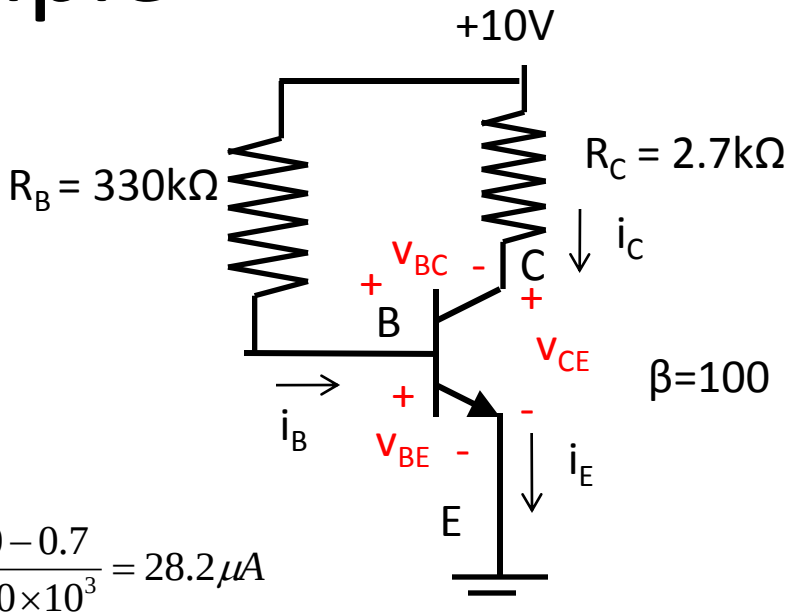




- Active region: $i_B>0$, $v_{CE}>0.2$ V
- Saturation: $i_B>0$, $v_{CE}<0.2$ V
- Cutoff: $i_B\leq 0$. $I_{CEO} \rightarrow i_C\ (=i_E)$ when base is open ($i_B=0$)

Example





Assuming active operation
v_{BE}=0.7 V, i_C=100i_B

$$i_B = \frac{10 - v_{BE}}{330 \times 10^3} = \frac{10 - 0.7}{330 \times 10^3} = 28.2\mu A$$

$$i_C = \beta i_B = 100(2.82 \times 10^{-5}) = 2.82mA$$

i_B>0 indicates that BE junction is forward-biased,
for CB junction

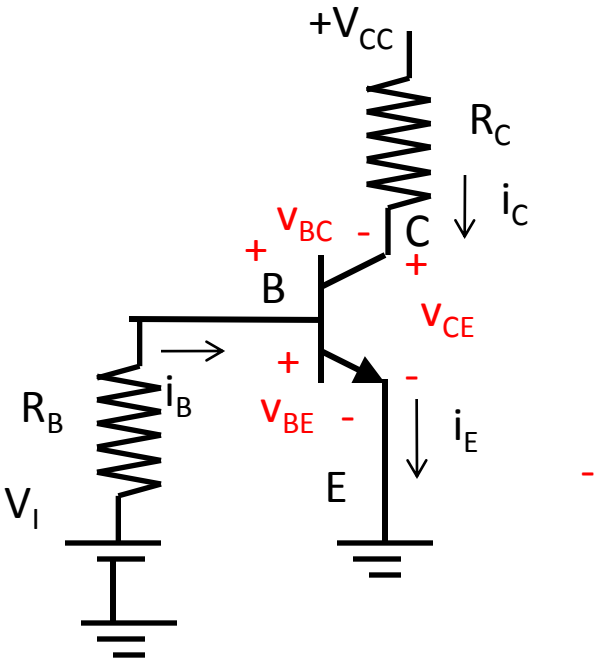
$$v_{CE} = 10 - (2.7 \times 10^3) i_C = 2.39\ \text{V}$$

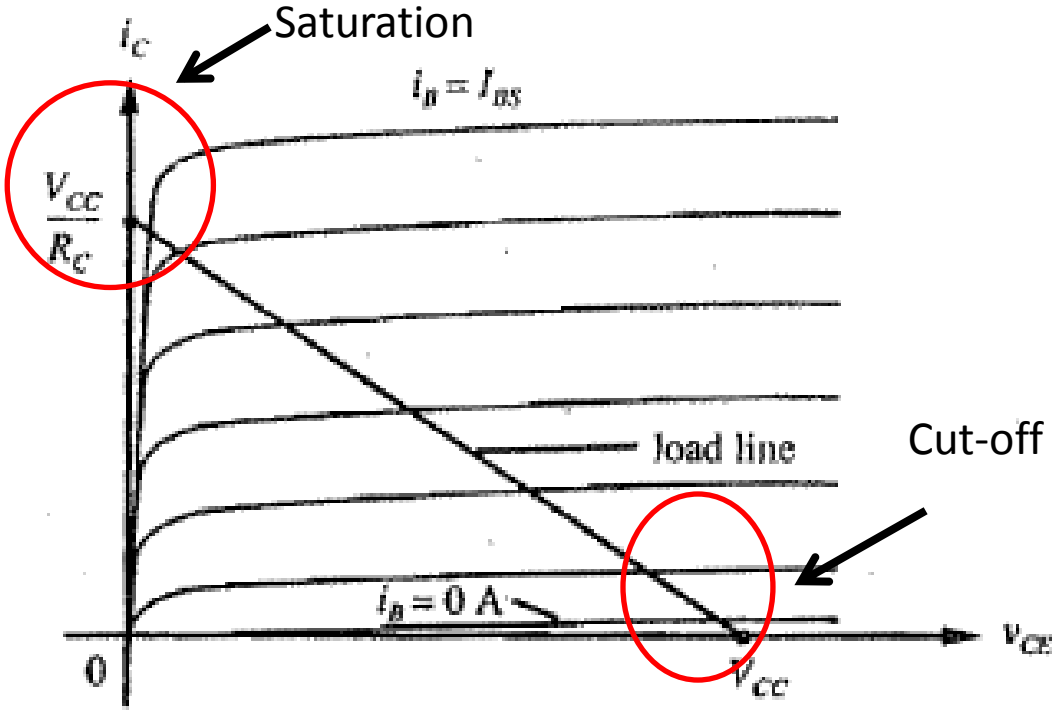
$$v_{BC} = v_{BE} - v_{CE} = 0.7 - 2.39 = -1.69\ \text{V} < V_\gamma = 0.5\ \text{V}$$

Hence the transistor is indeed operating in the active region.

Cut-off and saturation

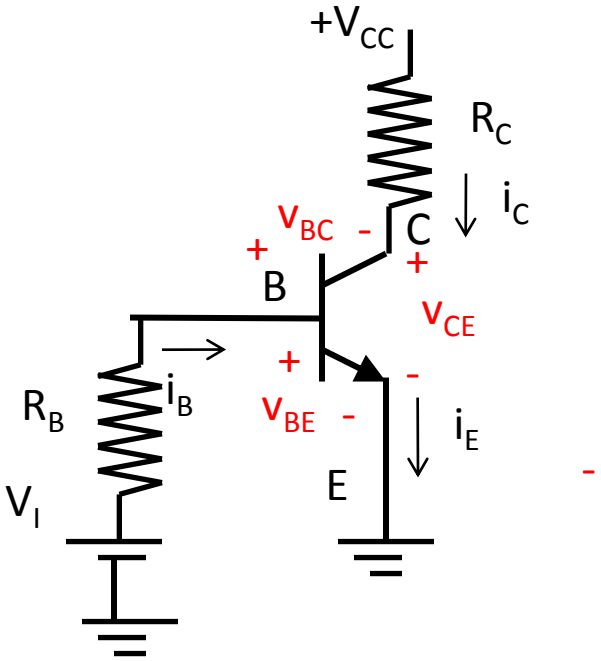
$$i_C = \frac{V_{CC} - v_{CE}}{R_C} = -\frac{1}{R_C} v_{CE} + \frac{V_{CC}}{R_C}$$

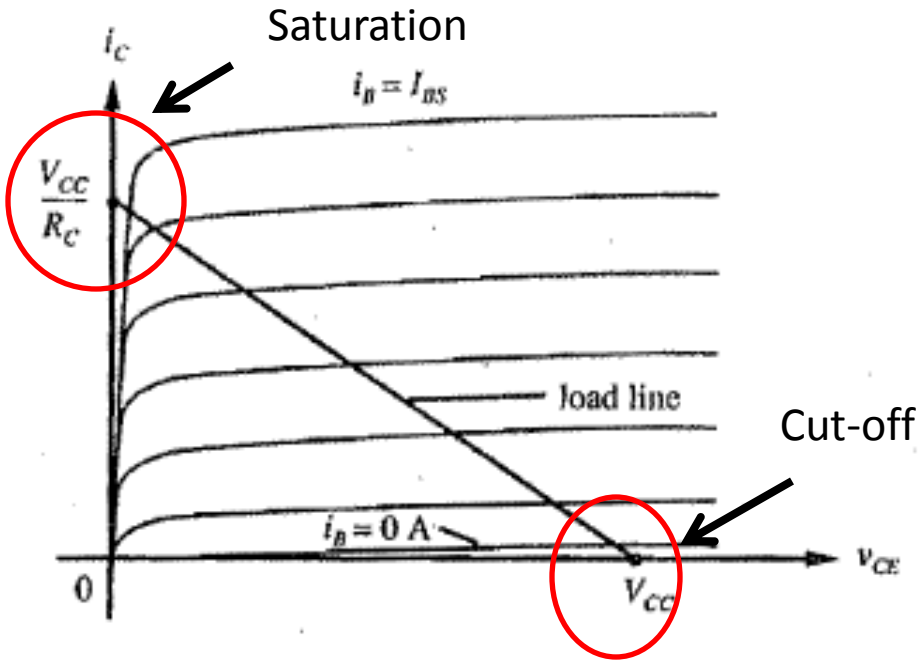




- Cut-off
  - $i_B=0 \rightarrow v_{BE}<0.5\ V \rightarrow$ R.B.
  - $i_C=i_E=0$, $v_{CE}=V_{CC}$, $v_{BC}=v_{BE}-v_{CE}<0.5-V_{CC} \rightarrow$ R.B.
- Saturation
  - $i_B>I_{BS}$, $i_C(sat) = V_{CC}-v_{CE}(sat)/R_C \sim V_{CC}/R_C \rightarrow$ collector current is saturated
  - $v_{CE}=v_{CE}(sat) \sim 0.2\ V$, $v_{BE}(sat) \sim 0.8\ V$
  - $v_{BC}=v_{BE}(sat)-v_{CE}(sat)=0.8-0.2=0.6V > 0.5V\ (V_\gamma) \rightarrow$ BC is forward biased

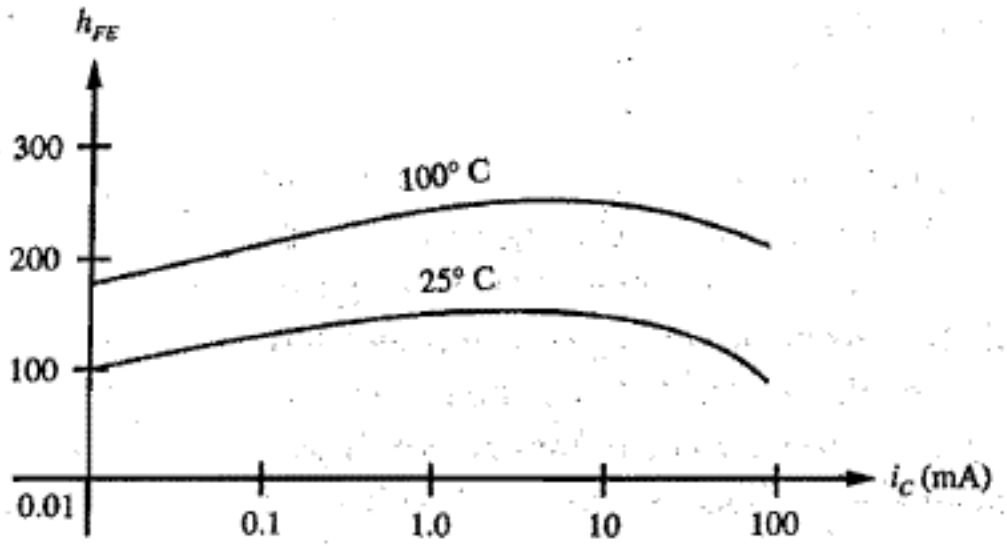
Cut-off and saturation





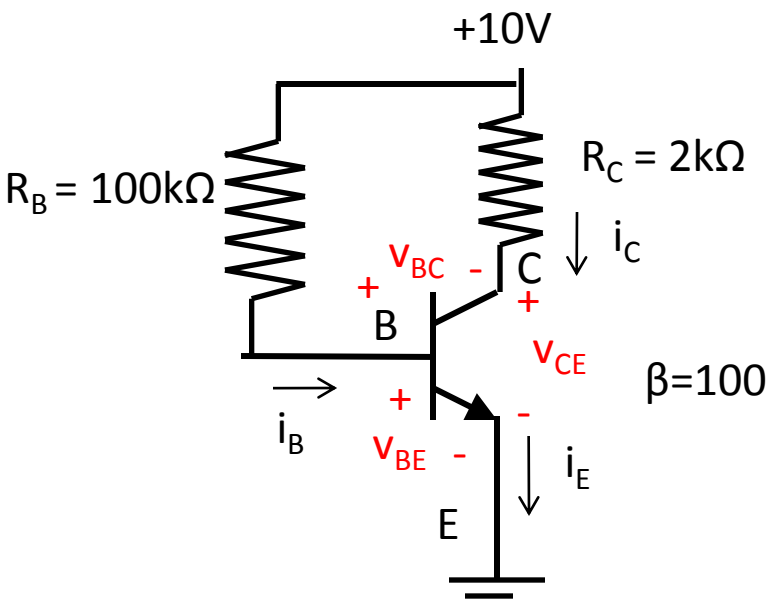
- ON (SAT), v_{CE}=0.2V, i_C=V_{CC}/R_C → short circuit
- OFF (CUTOFF), v_{CE}=V_{CC}, i_C=0 → open circuit
- Transistor behaves as a switch

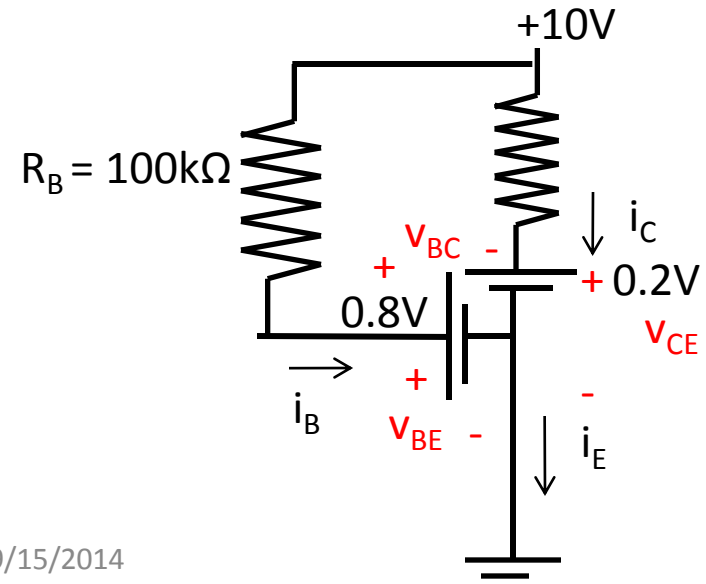
Common emitter dc gain



- $h_{FE}=i_C/i_B \sim \beta$
- For all practical purposes we will assume h_{FE} is constant

Example





Assuming active operation

v_{BE}=0.7 V, i_C=100i_B

$$i_B = \frac{10 - v_{BE}}{100 \times 10^3} = \frac{10 - 0.7}{100 \times 10^3} = 93\mu A$$

$$i_C = \beta i_B = 100(9.3 \times 10^{-5}) = 9.3mA$$

$$v_{CE} = -(2 \times 10^3) i_C + 10 = -8.6V < 0.2V$$

$$v_{BC} = v_{BE} - v_{CE} = 0.7 + 8.6 = 9.3 > V_\gamma = 0.5V$$

Therefore not in active mode

Assume saturation,

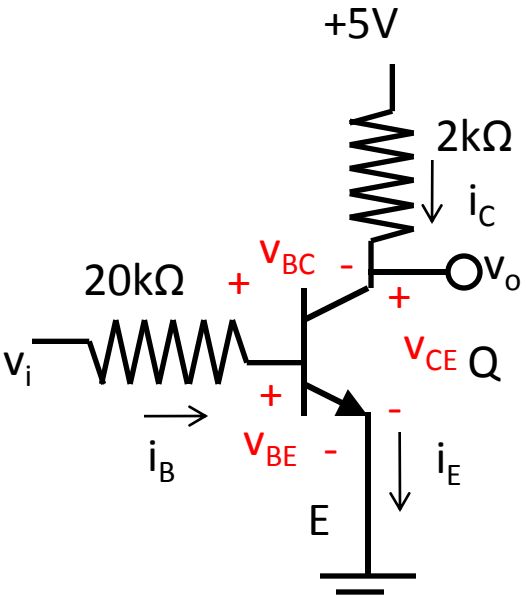
$$i_B = \frac{10 - v_{BE(sat)}}{100 \times 10^3} = \frac{10 - 0.8}{100 \times 10^3} = 92\mu A$$

$$i_C = \frac{10 - v_{CE(sat)}}{2 \times 10^3} = \frac{10 - 0.2}{2 \times 10^3} = 4.9mA$$

In saturation, $i_B \geq \frac{i_C}{h_{FE}} = \frac{4.9 \times 10^{-3}}{100} = 49\mu A$

Hence assumption of saturation is correct.

Example: BJT Inverter



low voltage=0.2 V (logic '0')
high voltage=5.0 V (logic '1')

For v_i=0.2 V, assume Q is OFF (cutoff)
i_B=0, v_{BE}=v_i=0.2 V < 0.5 V, indeed Q is off → i_c=0 and v_o=5 V (logic '1')

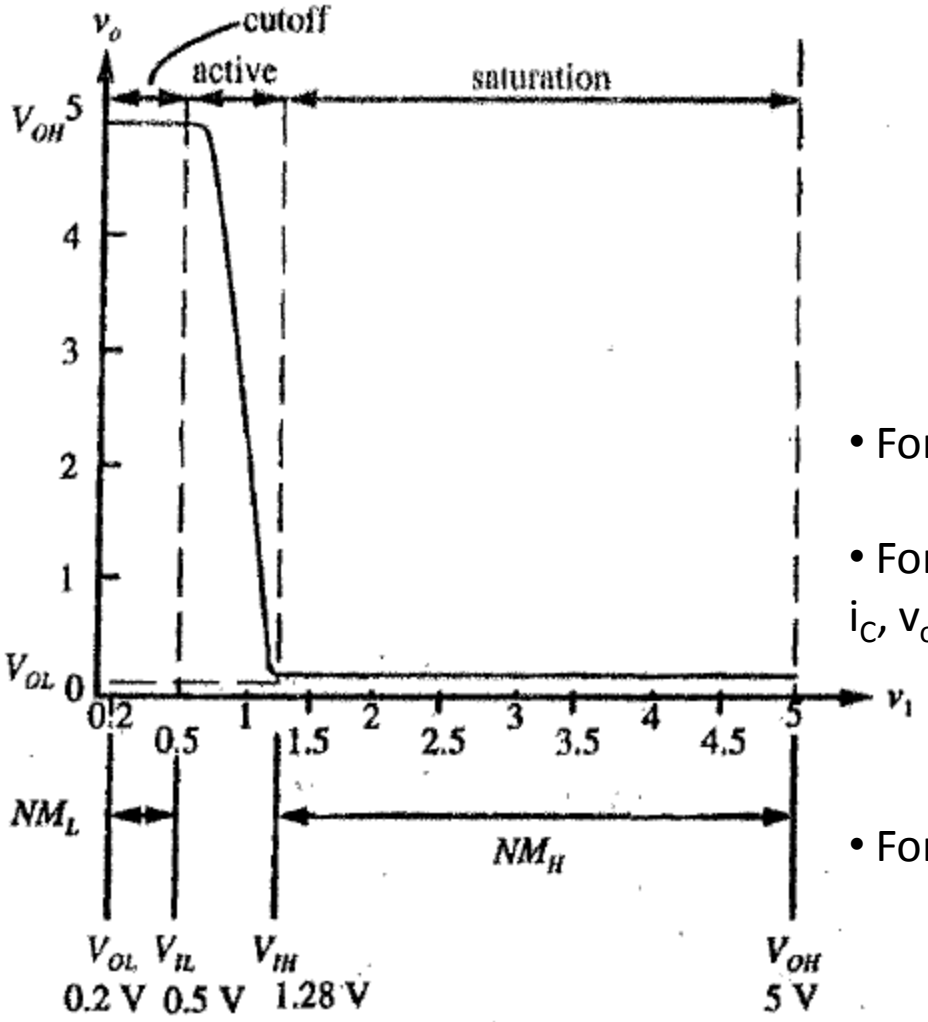
For v_i=5 V, assume Q is ON (saturation)
i_B=0.21 mA, i_c=2.4 mA and v_i=5 V (logic '1')

$$i_B \geq \frac{i_C}{h_{FE}} = \frac{2.4\times10^{-3}}{100} = 24\mu A$$

Hence Q is indeed ON, and v_o=0.2 V (logic '0')

Hence this circuit acts as an "inverter", $v_o = \overline{v}_{in}$

Transfer characteristic (v_o vs v_{in})



V_{OH} → Output Voltage high = 5 V

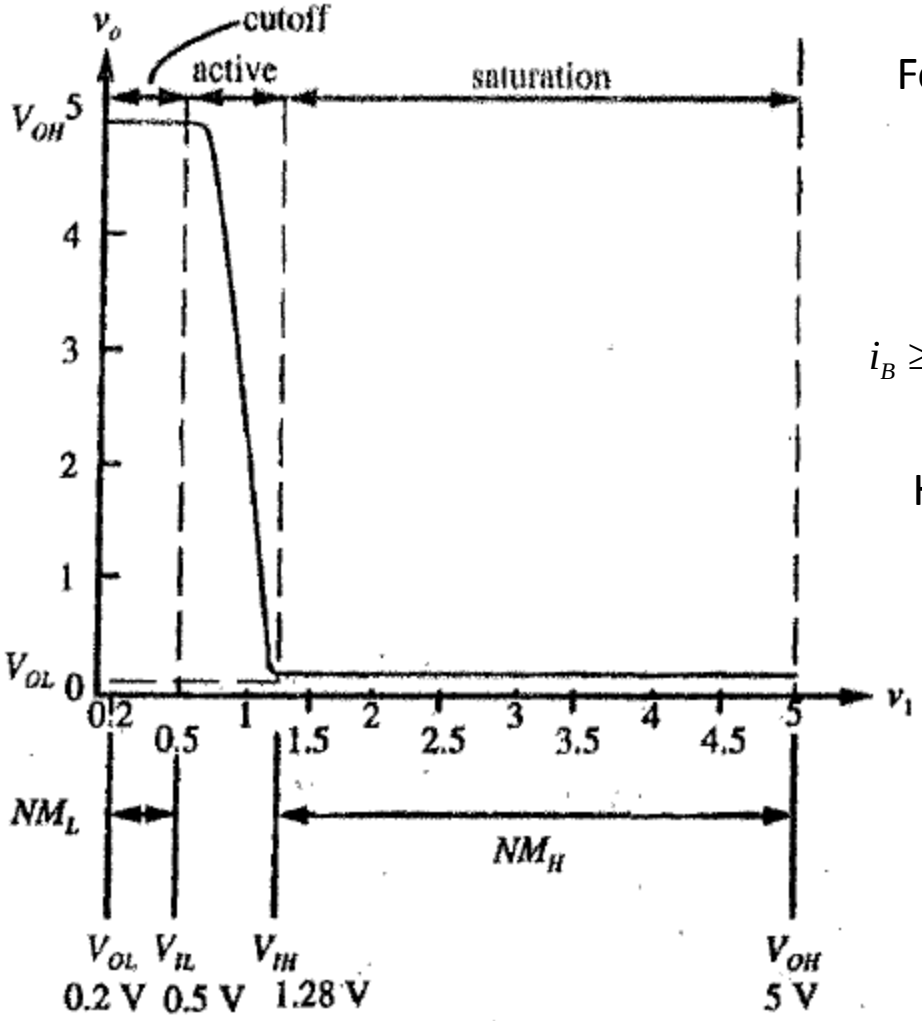
V_{OL} → Output Voltage low = 0.2 V

$$v_o = v_{CE} = 5 - (2 \times 10^3) i_C$$

$$v_{BC} = v_{BE} - v_{CE}$$

- For $0.2 < v_i < 0.5$V, Q off
- For $v_i > 0.5$ V, Q enters active region for small i_B and i_C, v_o is ~5 V
  → 0.5 V = V_{IL} (largest input voltage that still results in the same output as low input voltage)
- For increasing v_i, Q enters saturation and v_o=0.2 V
  → V_{IH}= minimum input voltage that results in the same output as high input voltage

Finding V_{IH} and Noise Margins



For V_{IH}, and Q to be ON

$$i_B = \frac{v_i - 0.8}{20\times10^3}, i_C = \frac{5-0.2}{2\times10^3} = 2.4mA$$

$$i_B \geq \frac{i_C}{h_{FE}} \Rightarrow \frac{v_i - 0.8}{20\times10^3} \geq \frac{2.4\times10^{-3}}{100} \Rightarrow v_i \geq 1.28V$$

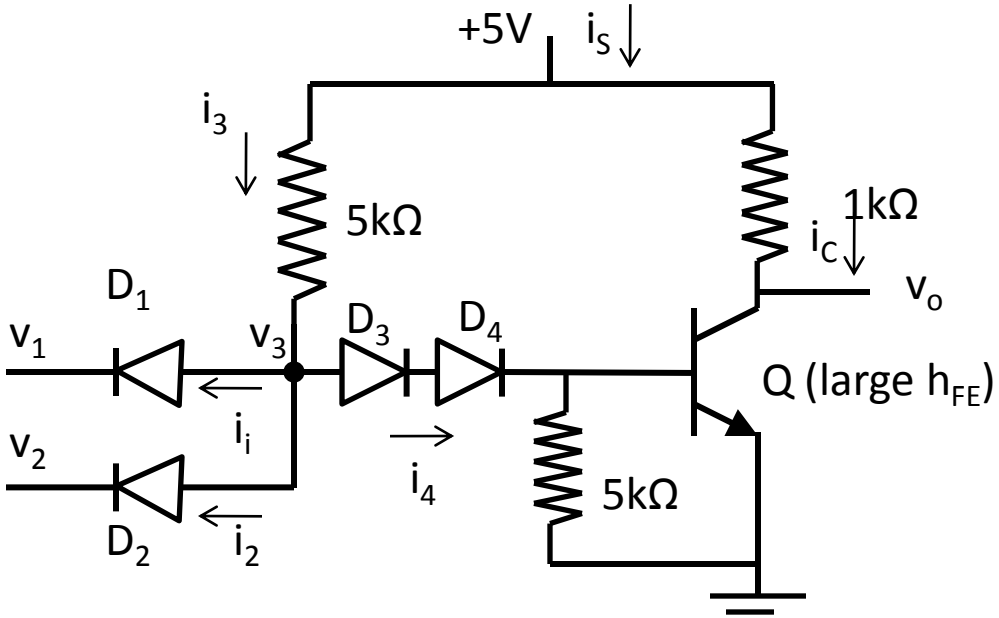
Hence, V_{IH}=1.28 V

NOISE MARGINS

- minimum noise (unwanted) voltage at the input of a digital logic gate that causes output to deviate is called the noise margin of the gate

- NM_L → minimum voltage noise that can produce an output other than that from a low input= V_{IL}-V_{OL}
- NM_H → minimum voltage noise that can produce an output other than that from a high input = V_{OH}-V_{IH}

Diode-Transistor Logic (DTL)



v_1	v_2	v_o (NAND)
0	0	1
0	1	1
1	0	1
1	1	0

Case 1 (v_1=v_2=0.2 V)

Assume D_1 and D_2 are F.B.

→v_3=0.7+0.2=0.9V,

Assume D_3 and D_4 are off.

$$i_2 + i_1 = i_3 = \frac{5-(0.9)}{5\times10^3} = 0.82mA, i_2 = i_3 = 0.41m$$

i_B=i_4=0, v_{BE}=0V, v_3-v_{BE}=0.9<0.7+0.7 =1.4V

Hence D_3 and D_4 are indeed off.

Q is off and v_o is 5V.

Case 2/3 (**v_1=0.2V, v_2=5 V**/ v_1=5V, v_2=0.2 V)

Assume D_1 is on, D_2 is off →v_3=0.7+0.2=0.9V,

v_3-v_2=0.9-5=-4.1<0.7 V → D_2 is off

Assume D_3 and D_4 are off.

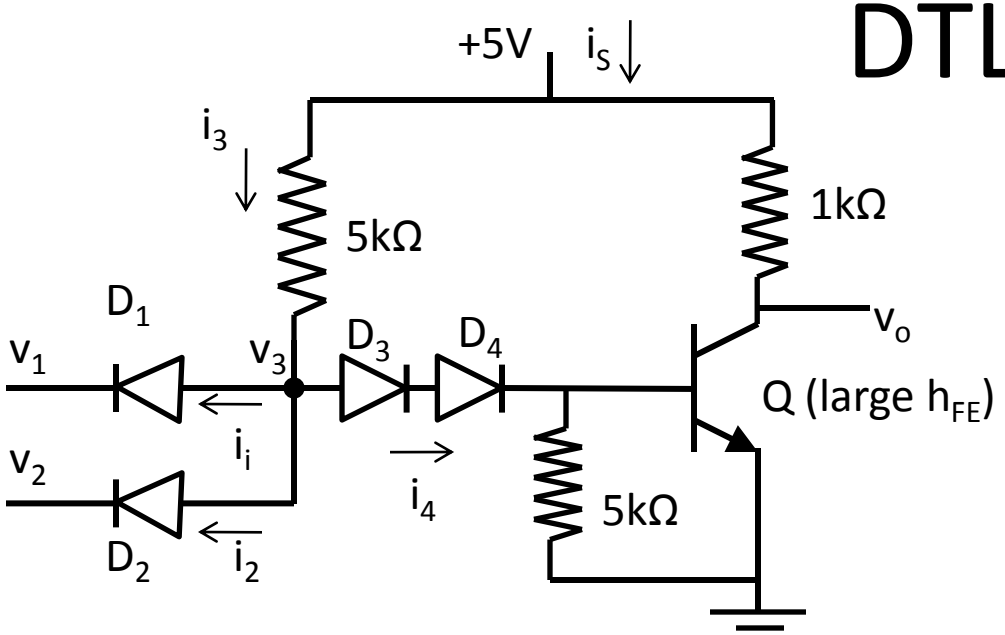
$$i_1 = i_3 = \frac{5-(0.9)}{5\times10^3} = 0.82mA > 0$$

i_B=i_4=0, v_{BE}=0V, v_3-v_{BE}=0.9<0.7+0.7 =1.4V

Hence D_3 and D_4 are indeed off.

Q is off and v_o is 5V.

DTL



v_1	v_2	v_o (NAND)
0	0	1
0	1	1
1	0	1
1	1	0

Case 4 (v_1=v_2=5 V)

Assume D_1 and D_2 are off → i_1=i_2=0.

Assume D_3, D_4, Q are on.

v_3=0.7+0.7+0.8=2.2V

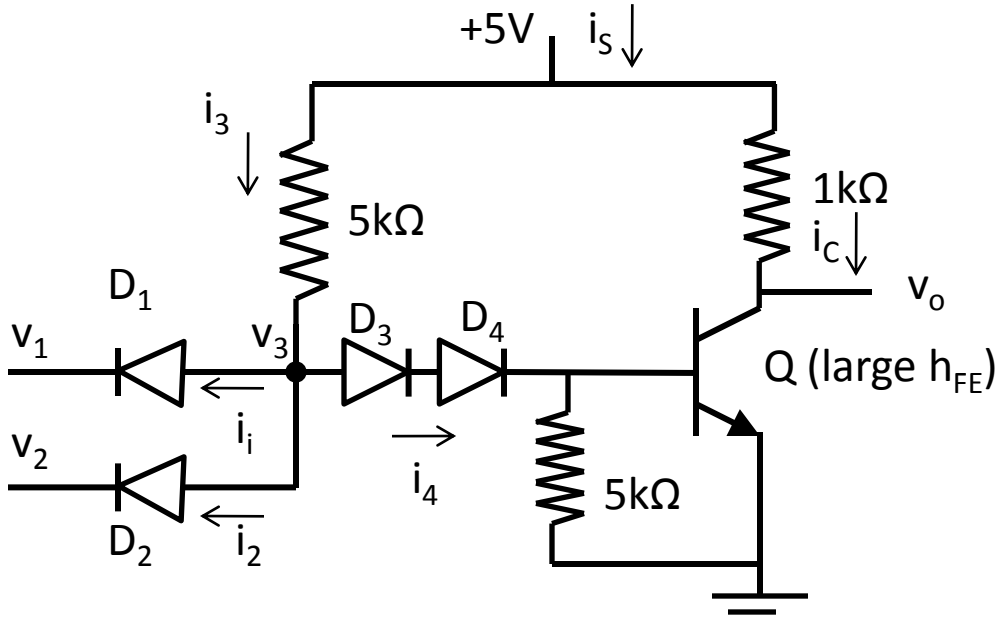
5-v_3=-2.8 V → D_1 and D_2 are off

$$i_4 = i_3 = \frac{5-2.2}{5\times10^3} = 0.56mA > 0$$

$$i_B = i_4 - \frac{0.8}{5\times10^3} = 0.4mA, i_C = \frac{5-0.2}{1\times10^3} = 4.8mA$$

$$h_{FE} \geq \frac{i_C}{i_B} = \frac{4.8}{0.4} = 12$$ → Q is on, v_o=0.2V

DTL: Power Dissipation



v_1	v_2	v_o (NAND)	
0	0	1	Q is off
0	1	1	
1	0	1	
1	1	0	Q is on

Case 1/2/3 (v_1=0.2V, v_2=5 V/ v_1=5V, v_2=0.2 V/ v_1=v_2=0.2 V)

Only i_3 is flowing, hence power consumed

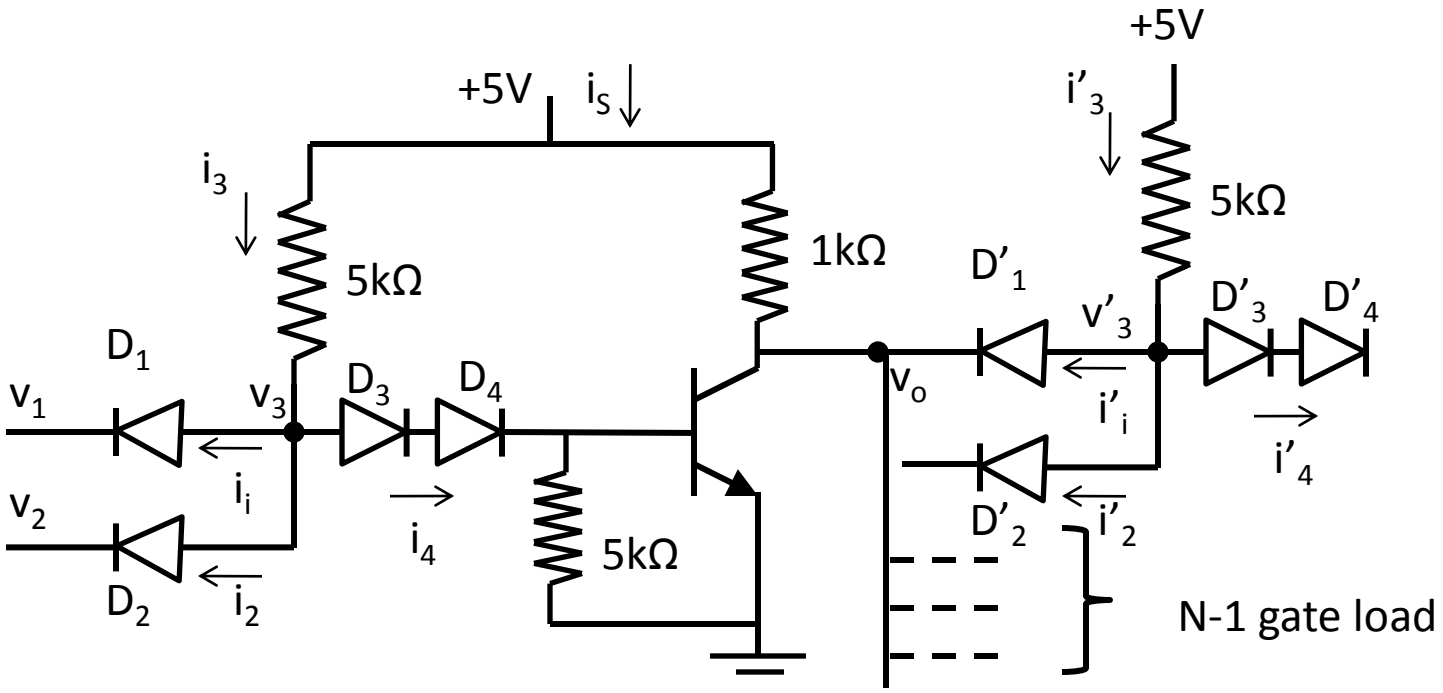
$P_1=5i_s=5i_3=5(0.82x10^{-3})=4.1mW$

Case 4 (v_1=5V, v_2=5, v_o=0.2 V)

$P_0=5(i_3+ic)=5(0.56x10^{-3}+4.8x10^{-3})=26.8mW$

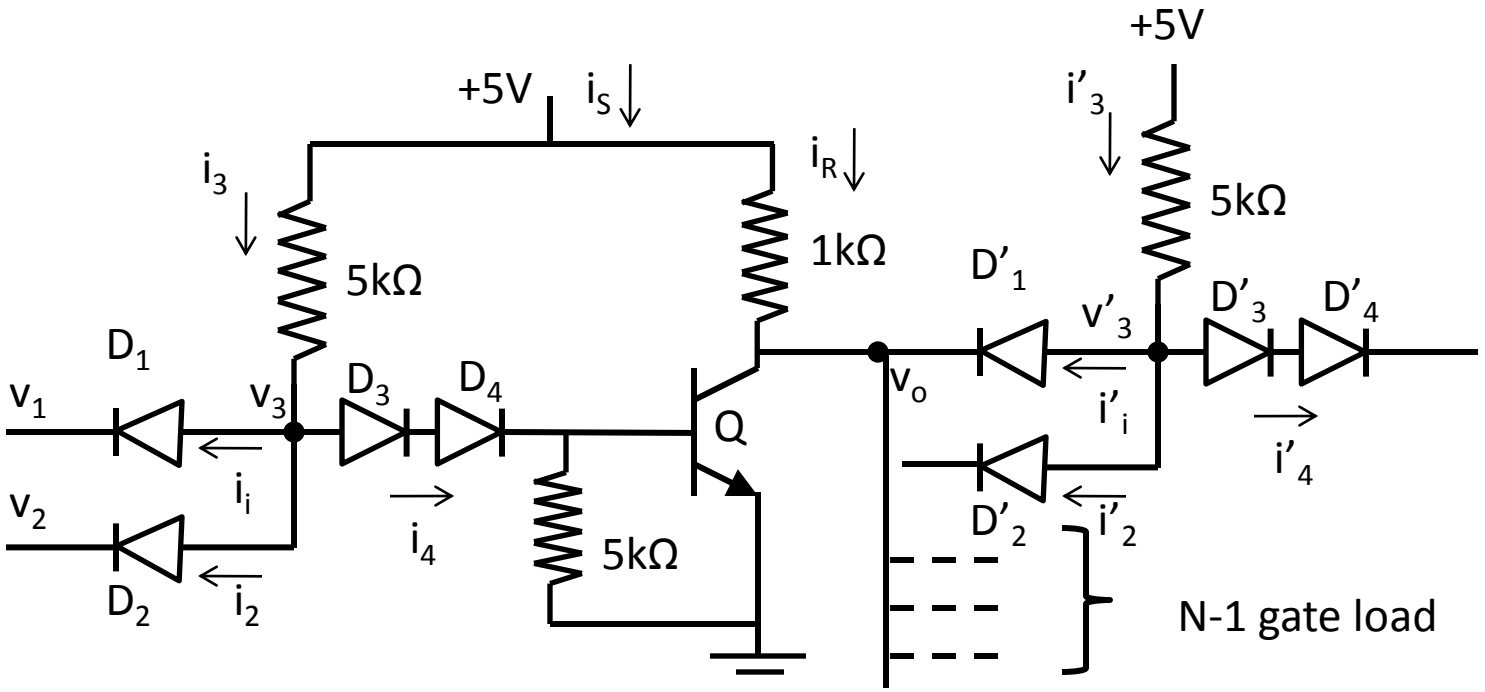
Average power (assuming the gate spends equal time in the 1 and 0 states) = $(P_0+P_1)/2$=15.45 mW

DTL: Fan-out



- Fan-out= number of gates connected to the output of the logic gate

DTL Fan-out

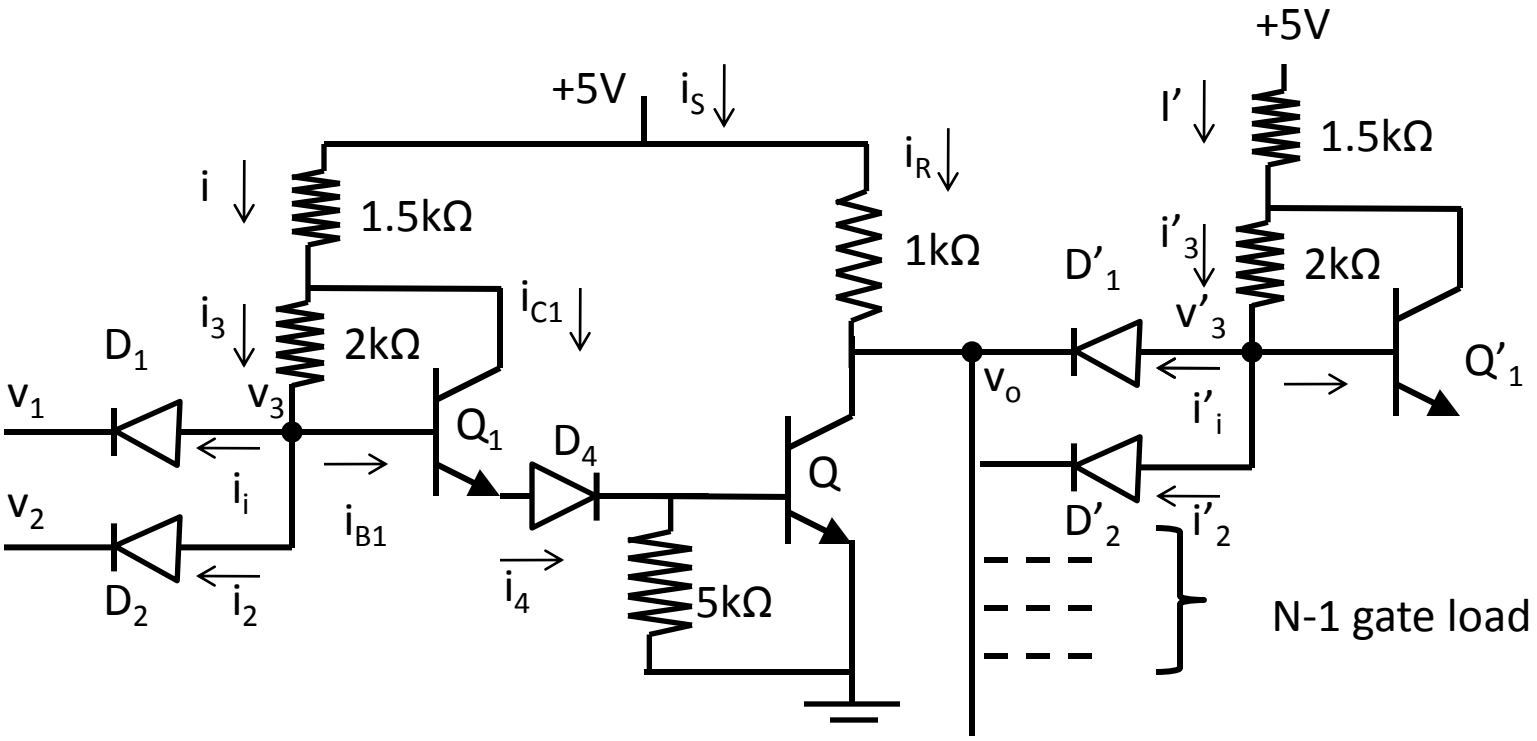


For v_o=5V, D'_1 will be off, and similarly input diodes of other N-1 gates will be off.

For v_o=0.2V, D'_1 will be on with i'_3 ➔ $i_C = i_R + Ni_1^{'} = \frac{5-0.2}{1\times10^3} + N(0.82\times10^{-3}) = 4.8\times10^{-3} + N(0.82\times10^{-3})$

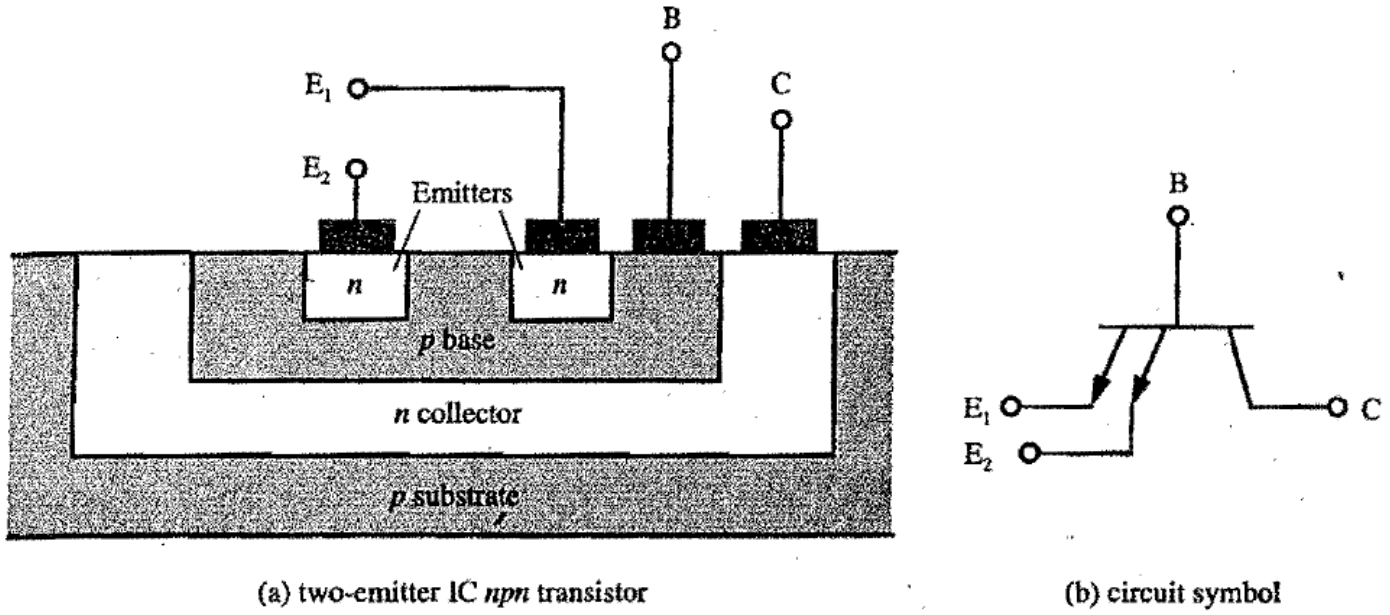
For Q to be on $h_{FE} i_B \geq i_C \Rightarrow 40(0.4\times10^{-3}) \geq 4.8\times10^{-3} + N(0.82\times10^{-3}) \Rightarrow \boxed{N \leq 13.7}$

DTL: Fan-out



- Replacing D_3 by Q_1 can increase fan-out
  - Solve as HW and find out maximum N
  - Why?

TTL: Transistor-Transistor Logic

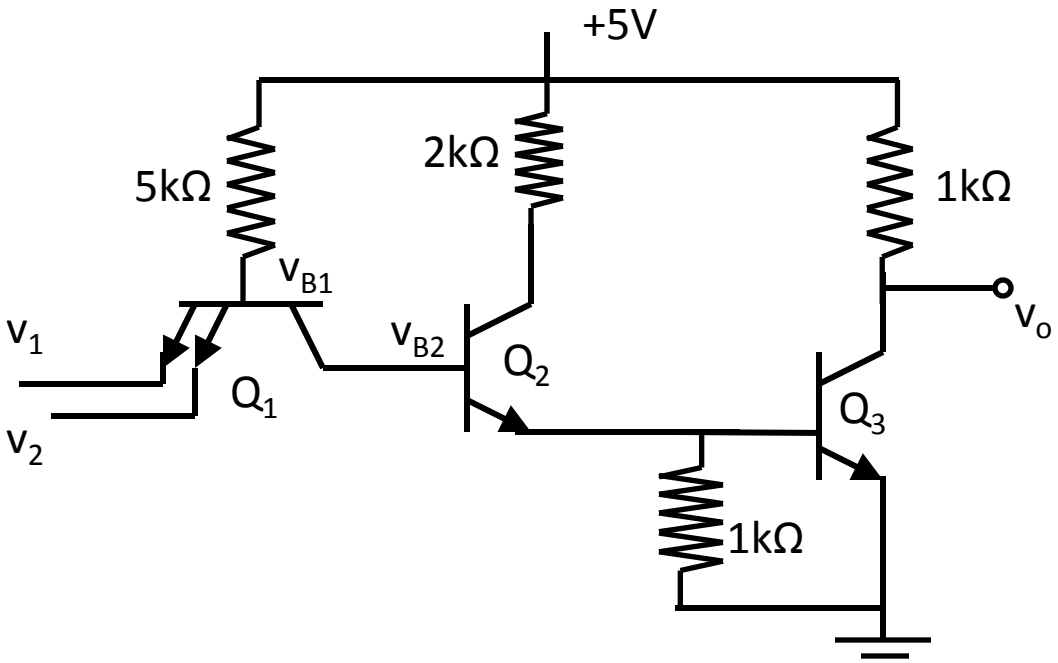


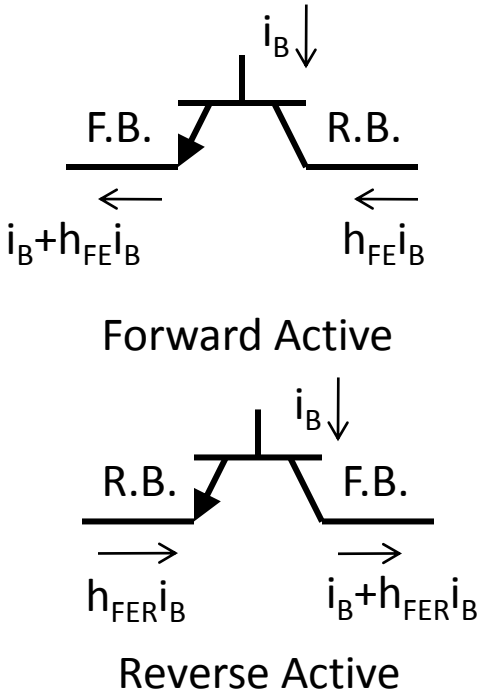
(a) two-emitter IC *npn* transistor

(b) circuit symbol

- Multi-emitter BJT: Faster than DTL

TTL NAND Gate





<u>Case1/2/3 (v_1=0.2V, v_2=5 V/ v_1=5V, v_2=0.2 V/ v_1=v_2=0.2 V)</u>

Q_1 active → v_{B1}=0.9V → i_{B1}=0.82mA

Q_1 saturation → v_{B1}=1.0V → i_{B1}=0.8mA

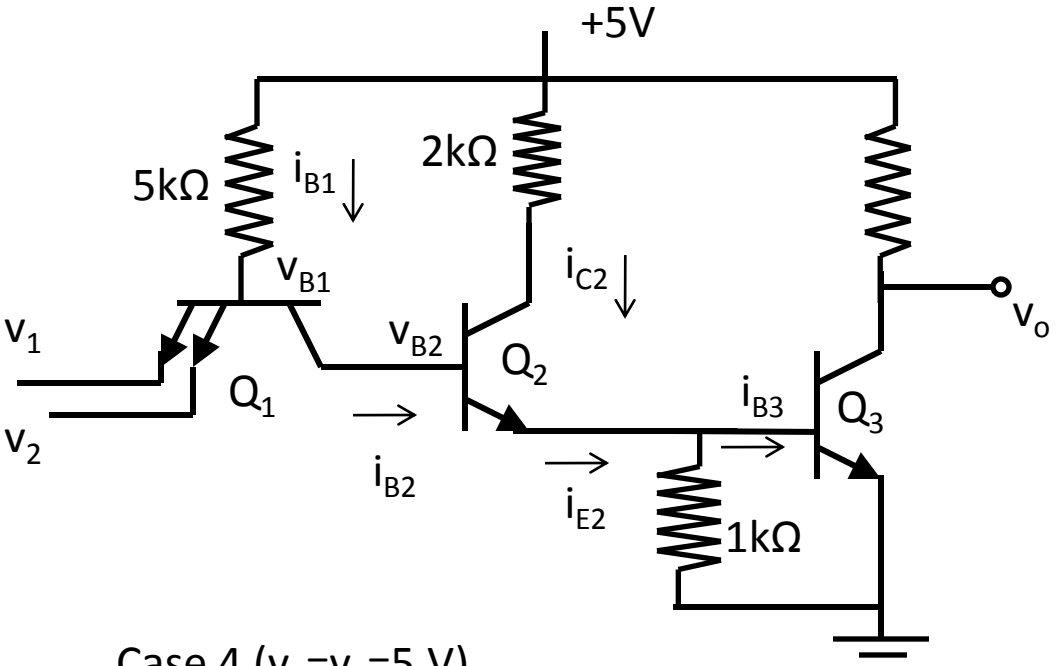
Assume Q_2 and Q_3 off.

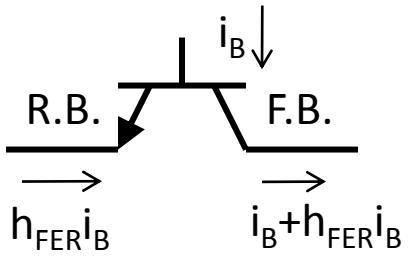
I_{CO2}=-i_{B2}=i_{C1} → nA

$$h_{FE1} \geq \frac{i_{C1}}{i_{B1}} \Rightarrow v_{B2} = v_{CE1} + v_1 = 0.2 + 0.2 = 0.4V$$

Hence Q_2 and Q_3 are off and v_o=5V

TTL NAND Gate





Reverse Active

<u>Case 4 (v_1=v_2=5 V)</u>

Q_1 → B.E. is R.B. and B.C. is forward-biased → reverse active mode!

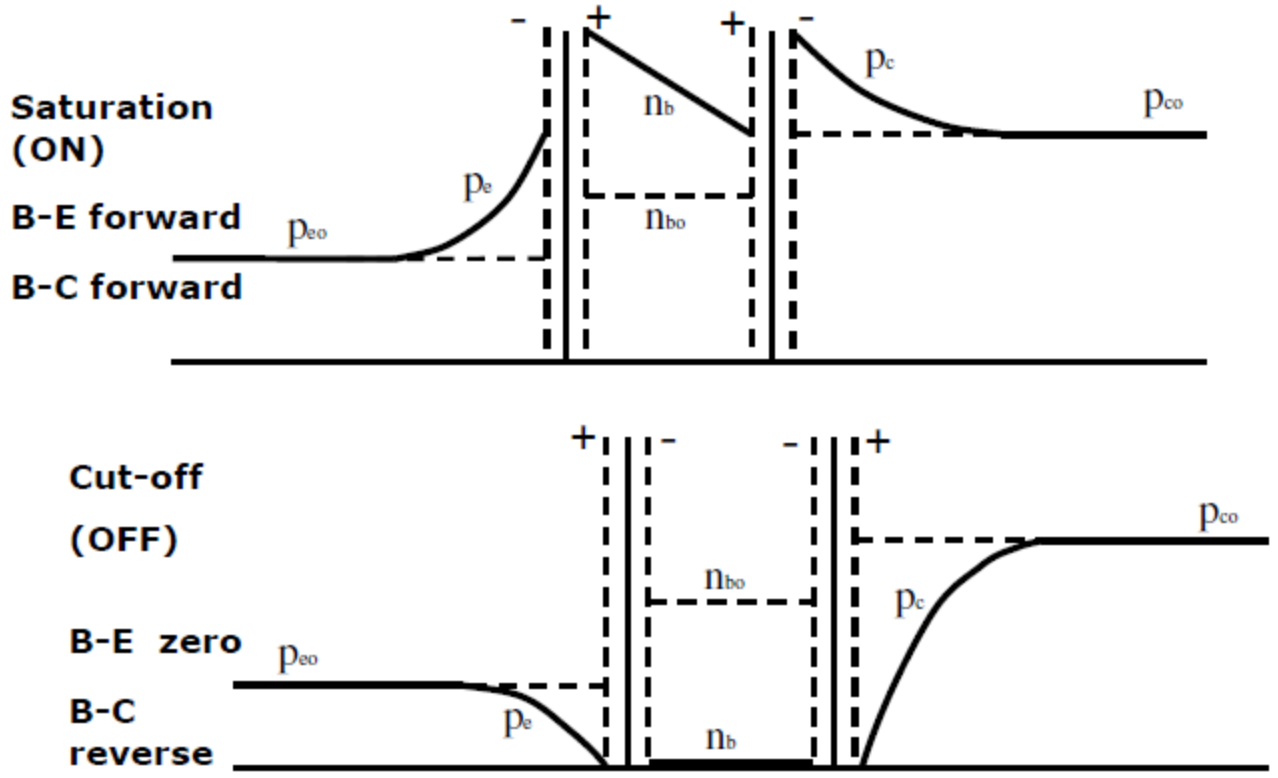
$i_{B2}=i_{B1}+h_{FER}i_{B1}$ turns Q_2 and Q_3 on. $v_{B1}=v_{BC1}+v_{BE1}+v_{BE2}=0.7+0.8+0.8=2.3$ V, $i_{B1}=0.54$mA

$i_{C2}=5-(0.2+0.8)/2000=2$mA, For Q_2 to be on, $h_{FE2} \geq \frac{i_{C2}}{i_{B2}} \Rightarrow h_{FE2} \geq \frac{2\times10^{-3}}{(1+h_{FER})0.54\times10^{-3}} = \frac{3.7}{1+h_{FER}}$

$i_{B3}=i_{B2}+i_{C2}-(0.8/1000)=(0.54+2-0.8)\text{x}10^{-3}=1.74$mA, $i_{C3}=(5-0.2)/1000=4.8$mA,

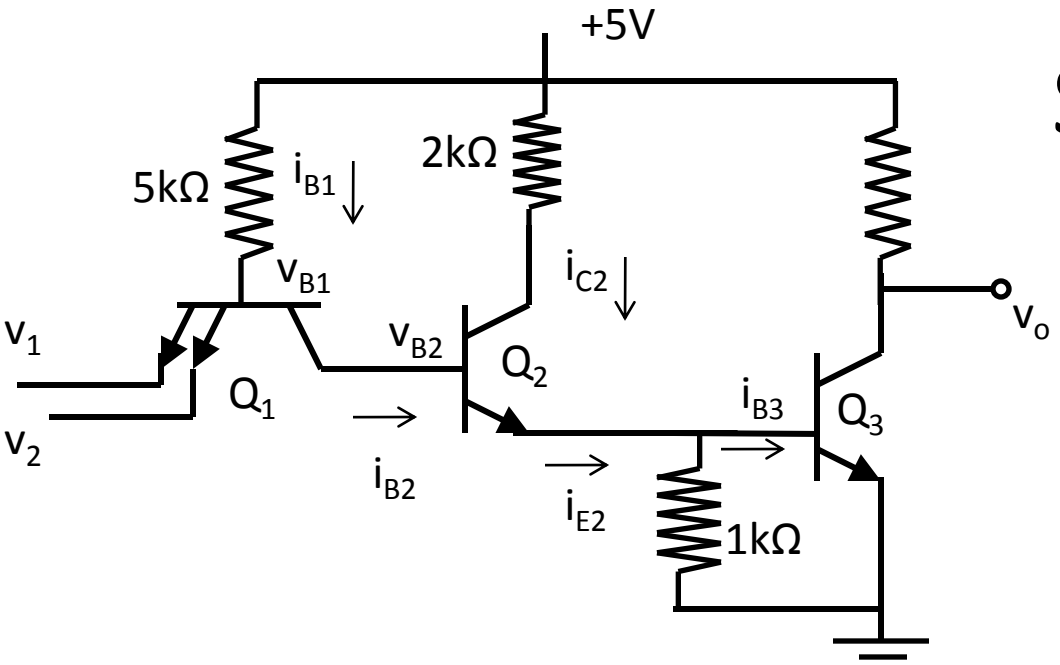
$h_{FE3} \geq \frac{i_{C3}}{i_{B3}} \Rightarrow h_{FE3} \geq \frac{4.8\times10^{-3}}{1.74\times10^{-3}} = 2.76$ Hence, Q_3 is also on and v_o=0.2V.

What determines switching speed?



- ON (SAT) → OFF (CUT OFF) requires time to remove excess minority carriers in the base

Switching speed in TTL circuits



$v_1=v_2=5V \rightarrow Q_1$ is reverse active, Q_2 and Q_3 are ON
$v_{B2}=v_{BE2}+v_{BE3}=0.8+0.8=1.6$ V

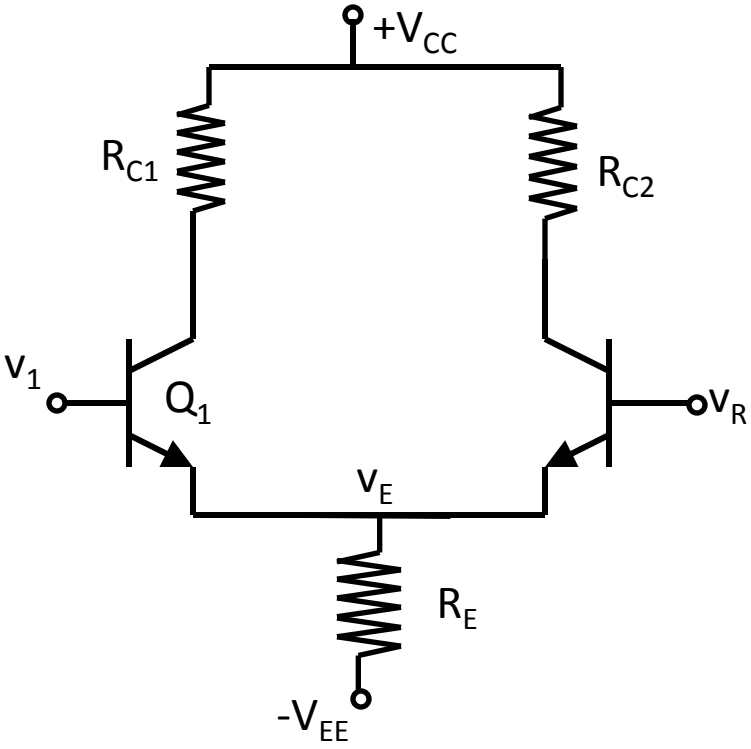
Say v_1 switches to 0.2 V

$v_{B1}=0.9$ V
$v_{B1}-v_{B2}=0.9-1.6=-0.7$ V → R.B.
Hence Q_1 is in active mode

$i_{C1}=h_{FE1}i_{B1}=0.82mA \times 50 = -41mA = i_{B2}$

A large base current quickly removes stored charge from Q_2 and Q_3. Subsequently Q_1 turns ON and Q_2 and Q_3 turn off.

Emitter-Coupled Logic (ECL)- "Non-saturating logic"



If $-V_{EE}+0.7<v_1<V_{CC}+0.5$ V → Q_1 is active

Also, $v_1>v_R+0.2$ V → $v_R-v_1<-0.2$V

Then,

$v_{BE2}=v_R-v_E=v_R-(v_1-0.7)$

$=0.7+v_R-v_1<0.7-0.2=0.5$V → Q_2 is cutoff

- Fastest logic→ no saturation, only cut-off and active mode
- See example 7.18 in Bobrow's book for an ECL NOR/OR gate