Karna Pardheev Sai
Fourth Year Undergraduate
Dual major in Chemical and Computer Science

Email:
Karna Pardheev Sai
LinkedIn | Github
+91 9381684976

Education

Degree	Institution	CPI/%	Year
B.Tech	IIT Gandhinagar	7.5	2021 - Present
Class XII	Star Junior College, Andhra Pradesh	9.79	2019-2020
Class X	St.Vincent pallotti school, Pedana,A.P	10.0	2017-2018

Internships

- **Invention Factory 2023** **[Jun – July 2023]**
  - Provisional patent application number: **202311054752**. (filed on 11-Aug-23)
  - Developed a safety solution to prevent hands from getting caught between rollers by designing gloves embedded with 5mm neodymium magnets at the fingertips, triggering a detection mechanism to halt gears when a threshold is exceeded.
  - Future development can incorporate RFID technology to enhance safety and operational efficiency.
  - Applied for Indian provisional patent (Patent pending).

Projects

- **Ball On The Plate Project** **[March 2023]**
  - Developed a system to control and maintain the position of a ball at the centre of a plate.
  - Utilized OpenCV for real-time detection of the ball's position.
  - Calculated coordinates of the ball relative to the plate's centre.
  - Tools and Technologies: Arduino, OpenCV-Python.
- **Phone Directory Database & Web Application** **[Jan-Apr 2024]**
  - Developed a phone directory web application for the IITGN community as a team of 10.
  - Designed the front-end interface with HTML and CSS to ensure a user-friendly experience.
  - Created and managed a SQL database using MySQL Workbench to store directory information efficiently. Implemented features for seamless dynamic access and updates, enhancing communication and connectivity.
  - Tools and technologies: HTML and CSS, python, Flask framework.
- **Three-Stage Pipelined Mips Processor** **[Aug-Nov 2024]**
  - **Designed and Implemented a 3-Stage Pipeline MIPS Processor**: Developed a modular MIPS processor with **Instruction Fetch**, **Execution**, and **Write-back** stages, integrating pipeline registers and hazard detection for improved efficiency.
  - **Implemented Forwarding and Hazard Detection Units**: Ensured accurate instruction execution by resolving data hazards through forwarding techniques and hazard detection logic, enabling smooth pipeline operation.
  - **Developed and Simulated in Verilog**: Utilized Verilog for modular design, including components such as the **register file**, **pipeline stages**, and **control units**, and validated functionality using testbenches in tools like Vivado.

Positions of Responsibility

- **Member of Tinkerer's Lab IITGN.**

Helped in making the mechanical mirror by Tinkerer's lab, designed the basic structure for me and my teammate, and it was modified by the senior team.

Skill Summary

- **Languages:** Python, C, C++, SQL, git, GitHub, OpenSource Contributor
- **Tools:** Autodesk Inventor Professional, Ansys, Arduino, MATLAB, Simulink, ASPEN V14.
- Created the PULL REQUEST for Matplotlib open source and Lfortran Compilers (Matplotlib and Lfortran)

Extra-curricular Activities

- **INTER IIT AQUATICS TEAM** **[October 2023]**

Played as a key defender in our water polo team. Contributed to team strategy and defence, enhanced skills in coordination, teamwork, and goal-oriented enthusiasm.

- **Robotic arm** **[December 2022]**

The end effector can touch the given coordinates. This robotic arm has 3 degrees of freedom. 1 rotational and 2 linear.