A Project Report

On

IMPLEMENTATION OF ALARM CLOCK ON FPGA

BY

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ABSTRACT

The development of digital system design as a result of the spectacular advancements in digital technology over the years has continued to be a major source of relief and comfort for humanity in many ways. Many applications in electronics and other fields of technology today use digital approaches to carry out tasks that were formerly handled by analog methods. Due to their better precision and accuracy, ability to store billions of bits of data in a relatively little amount of space, and immunity to spurious voltage fluctuations, digital systems are more versatile and superior than analog technologies. A component of the research is the creation of FPGA boards. Reprogrammable integrated circuits with a collection of programmable logic blocks are known as field-programmable gate arrays (FPGAs). The adoption of FPGA chips is fuelled by their parallelism, hardware-timed speed, and flexibility. The main scope of this project is to implement an FPGA-based alarm clock using Verilog HDL. The alarm clock would output a real-time clock with a 24-hour format and provide an alarm feature. The CLK input to the alarm clock would have a frequency of 10 Hz, which means the clock time would be incremented by 1 second after ten cycles of CLK. At first, the clock time must be set through appropriate input pins. The same input pins can also be used to set the alarm time by changing the values of select pins. A reset pin can be used to reset the clock time and change the alarm time to 00:00:00. If the alarm is on, the output will be high when the clock time equals the alarm time. The alarm output pin could be connected to a buzzer to realize the functioning of an alarm. The alarm could be turned off by setting the stop pin to high. The time will also be displayed on PMOD OLED.

Keywords: Alarm clock, Analog Technologies, FPGA, PMOD OLED, Verilog HDL.

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INTRODUCTION

XILINX VIRTEX FPGA:

Configurable logic blocks (CLBs) are a Xilinx Virtex FPGA's primary source of logic resources. A CLB has two slices per unit. Four of these carry-chain cascaded elements make up each slice. As a result, each slice has four LUTs with six inputs. Two 5-input combinational logic functions and one 6-input combinational logic function can both be implemented with a single LUT.

The customizable logic block (CLB) matrix at the Centre of field programmable gate arrays (FPGAs), a semiconductor device, is coupled by programmable interconnects. After production, FPGAs can be reprogrammed to meet specific application or feature needs. FPGAs are distinguished from Application Specific Integrated Circuits (ASICs), which are made especially for design tasks, by this property. Although one-time programmable (OTP) FPGAs are available, SRAM-based FPGAs, which can be updated as the design changes, are more common.

FPGAs are a perfect fit for many different markets because of their programmable nature. As the global leader, Xilinx offers complete solutions for markets and applications that include configurable, ready-to-use IP cores, FPGA devices, and cutting-edge software.

ZEDBOARD:

For designers interested in exploring designs employing the AMD Xilinx Zynq-7000 All Programmable SoC, ZedBoard is a complete development kit. The board has all the required interfaces and auxiliary features to accommodate a variety of applications.

The board's expandability characteristics make it perfect for proof-of-concept development and rapid prototyping.

A light-emitting diode (LED) with an organic compound film as the emissive electroluminescent layer generates light in response to an electric current is referred to as an organic light-emitting diode (OLED or organic LED), also known as an organic electroluminescent (organic EL) diode. This organic layer is sandwiched between two electrodes, usually with at least one transparent electrode. OLEDs are utilized to make digital displays in gadgets like televisions, computer monitors, and portable gaming systems like smartphones. The creation of white OLED components for use in solid-state lighting systems is a significant field of research. In this project we are using the inbuilt OLED of Zedboard.

OBJECTIVE:

To create a fully synthesizable alarm clock which can be implemented on Xilinx zync – 7000 Zedboard. This clock also includes date, month, year.

The alarm clock must be able to perform the following functions:

1. Clock Generation
2. Setting the clock to a particular value
3. Set the alarm to a specific time
4. Enabling or disabling the alarm
5. Turning off the alarm

SOFTWARE COMPONENTS:

XILINX VIVADO IDE

HARDWARE COMPONENTS:

1. Xilinx zync – 7000 Zedboard with at least 8 LEDS AND 8 Switches for output and input respectively.
2. Buzzer for alarm (Optional)

RELATED WORK

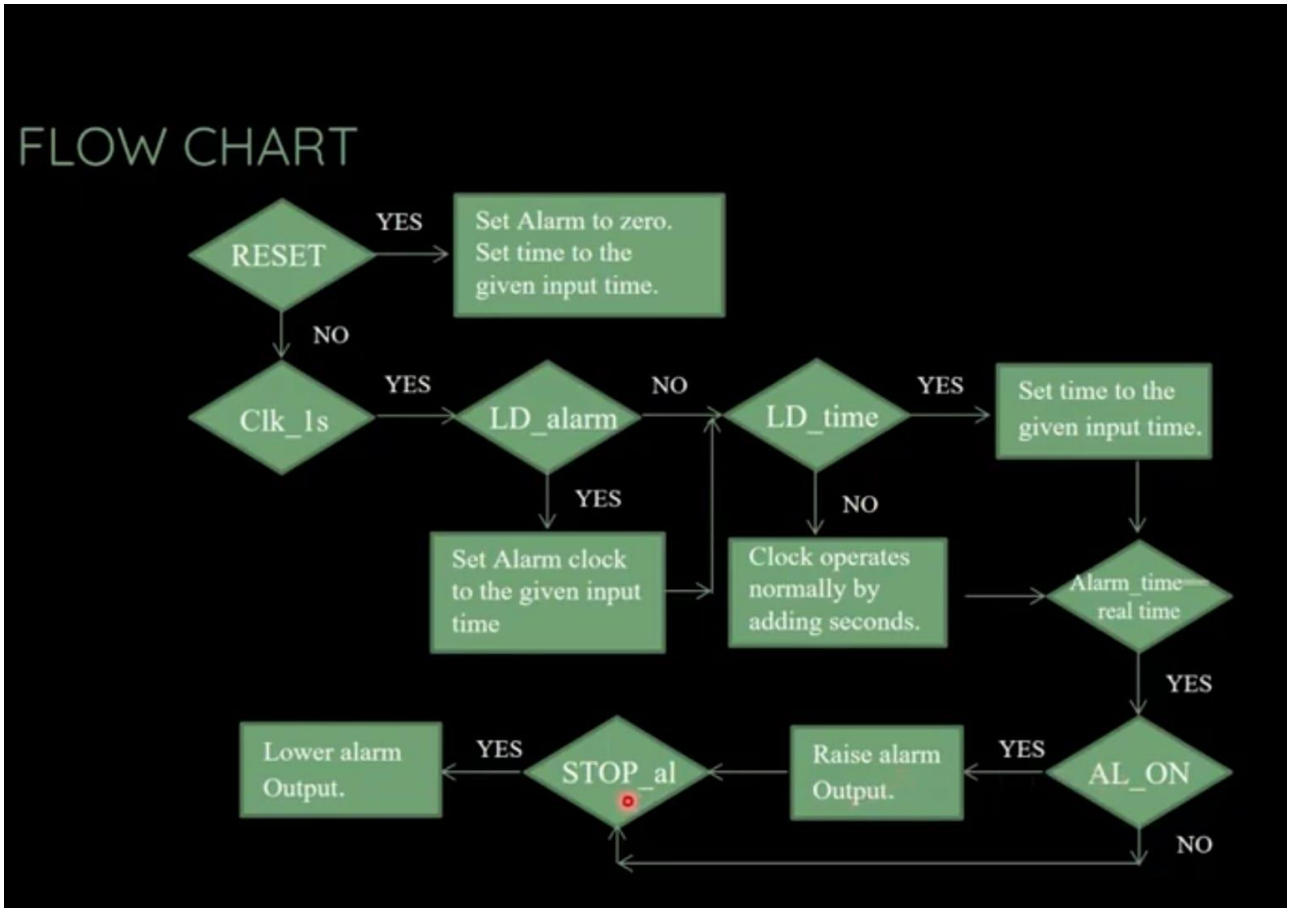
1. Zefan Ge, Yizhun Peng, Yuhan Zhang, Shiqian Zhang and Zhou Yang. *Design of Intelligent Digital Clock Based on FPGA*

This paper takes ALTERA EP4CE6E22C8N as the control center, and designs a multifunctional digital clock system based on FPGA, which consists of clock module, timing module, power module, keyboard control module, data decoding module and digital tube display module HDL designs text input for the system logic description language. In the QUARTUSII tool software environment, based on the top-down design idea of FPGA, hierarchical modeling of digital clock circuit is completed by text file input, and the digital clock based on FPGA is constructed jointly by each basic module. After the program is compiled and simulated, download it on the core board to review. This system can realize the function of displaying time in hour, minutes and seconds in turn, calibrating with keys, timing on the hour and alarm clock.

2. Jason Fong and Fernando Mattos. *Digital Alarm Clock*

Digital alarm clocks typically use 7-segment LED's as its display, and a count-up scheme for changing the clock time and alarm times. With the availability of a twelve key keypad and LCD screen, a simple alarm clock can look much sharper, and work much better. Such a clock is constructed by combining the E157 FPGA board with the HC11 to control and generate the keypad inputs and LCD display outputs. The FPGA and the on board clock oscillator will generate accurate timing signals and debounce keypad inputs, while the HC11 will store the time value, handle alarm clock functions, and generate the control signals to the LCD. The audible alarm will simply be a square wave signal generated by the FPGA amplified by a set of external computer speakers.

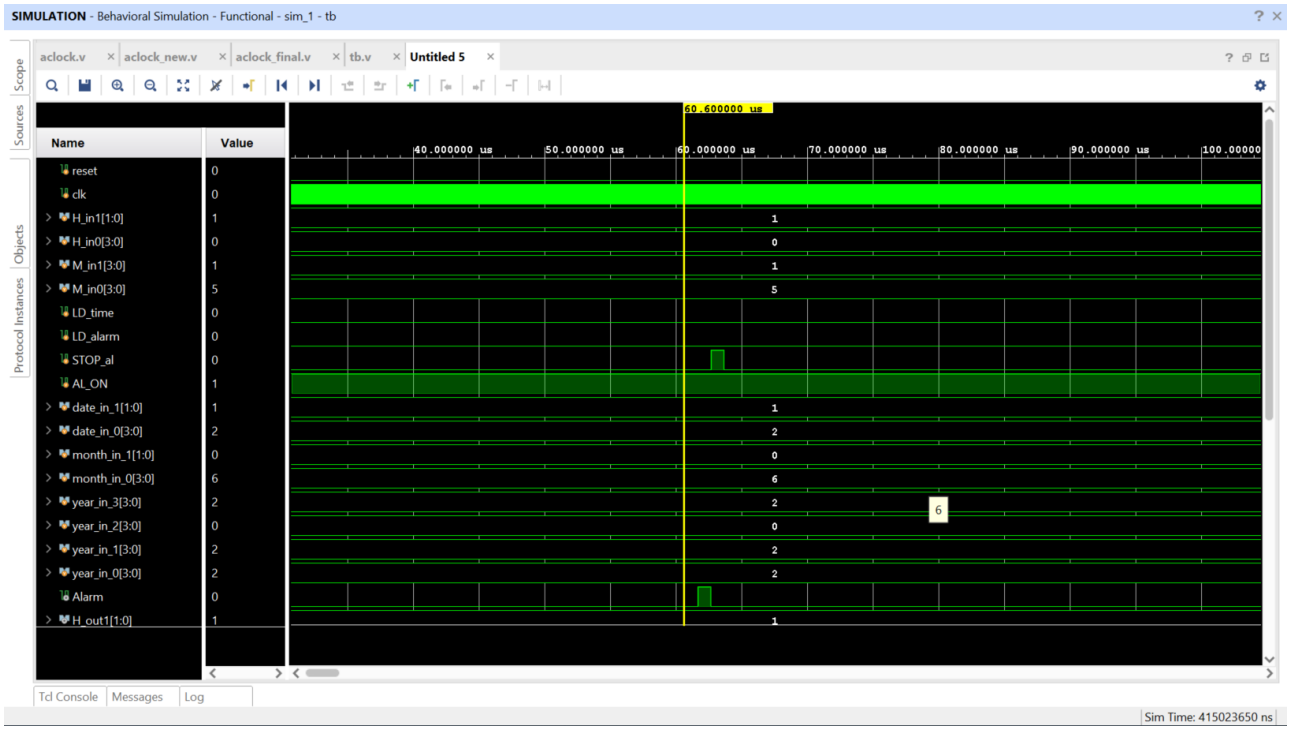
DETAILED DESCRIPTION

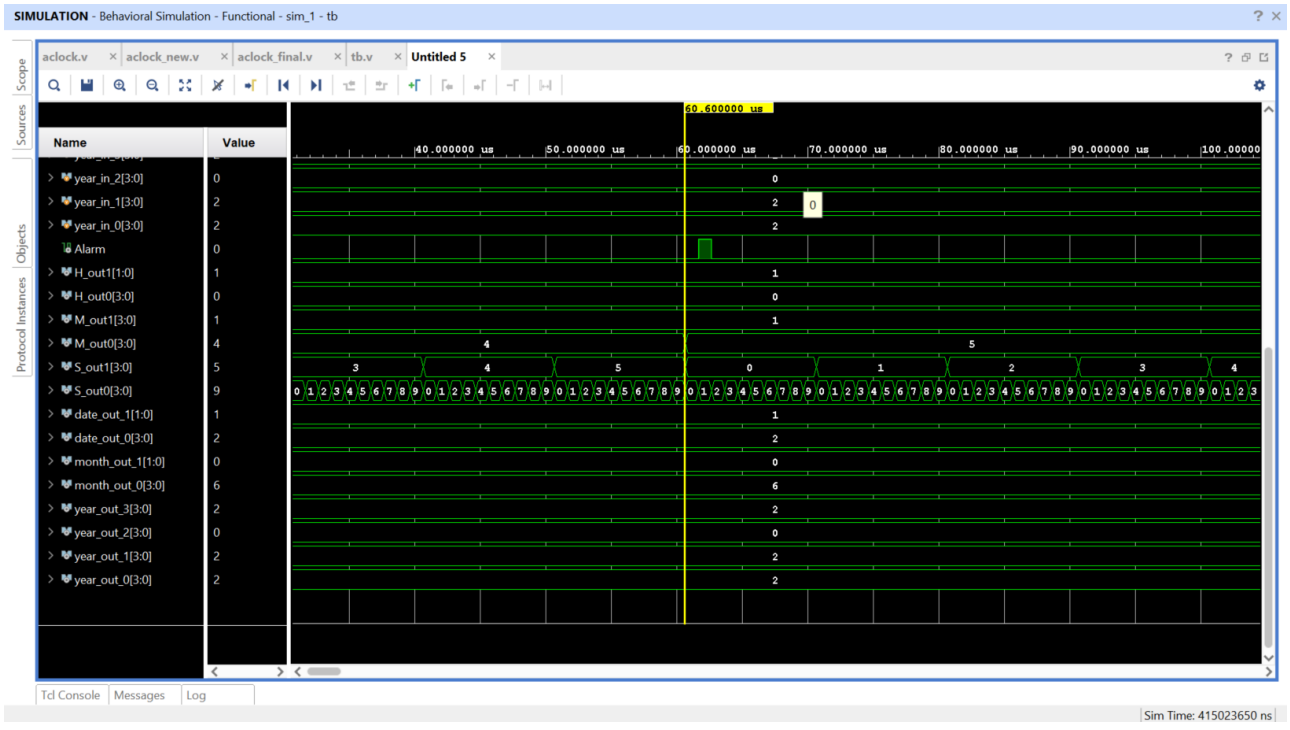


The CLK input to the alarm clock would have a frequency of 10 Hz, which means the clock time would be incremented by 1 second after ten cycles of CLK. Therefore, to implement the design using the Y9 input clock pin of Zedboard, a clock divider has been used. When reset is high, the clock time is set based on the given input. When reset is low, the clock starts working and time increments accordingly. Using the LD_alarm input, the alarm time can be set to a desired time. LD_time is used to set the clock time to any value. When it is low, clock operates normally. AL_ON is used to turn the alarm on. When alarm time = clock time, the ALARM output goes high. Setting STOP_AL = 1 lowers the alarm output. The alarm clock is designed in such a way that it can take any input time (Hr:Min:Sec), date, month and year and set alarm for any instant. The OLED display of Zedboard has been interfaced in such a way that it can display the time.

RESULTS

Simulation waveforms for the alarm clock are shown below:





Resource utilization report can be seen below:

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	197	0	0	53200	0.37
LUT as Logic	197	0	0	53200	0.37
LUT as Memory	0	0	0	17400	0.00
Slice Registers	79	0	0	106400	0.07
Register as Flip Flop	79	0	0	106400	0.07
Register as Latch	0	0	0	106400	0.00
F7 Muxes	42	0	0	26600	0.16
F8 Muxes	10	0	0	13300	0.08

Power consumption report can be seen below:

1. Summary

Total On-Chip Power (W)	16.310 (Junction temp exceeded!)
Design Power Budget (W)	Unspecified*
Power Budget Margin (W)	NA
Dynamic (W)	15.270
Device Static (W)	1.039
Effective TJA (C/W)	11.5
Max Ambient (C)	0.0
Junction Temperature (C)	125.0
Confidence Level	Low
Setting File	---
Simulation Activity File	---
Design Nets Matched	NA

1.1 On-Chip Components

On-Chip	Power (W)	Used	Available	Utilization (%)
Slice Logic	1.425	667	---	---
LUT as Logic	1.274	374	53200	0.70
CARRY4	0.097	34	13300	0.26
Register	0.038	174	106400	0.16
BUFG	0.016	2	32	6.25
Others	0.000	3	---	---
Signals	1.892	613	---	---
I/O	11.953	99	200	49.50
Static Power	1.039			
Total	16.310			

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3. Detailed Reports
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3.1 By Hierarchy
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+--------+-----------+
| Name   | Power (W) |
+--------+-----------+
| aclock |    15.270 |
+--------+-----------+
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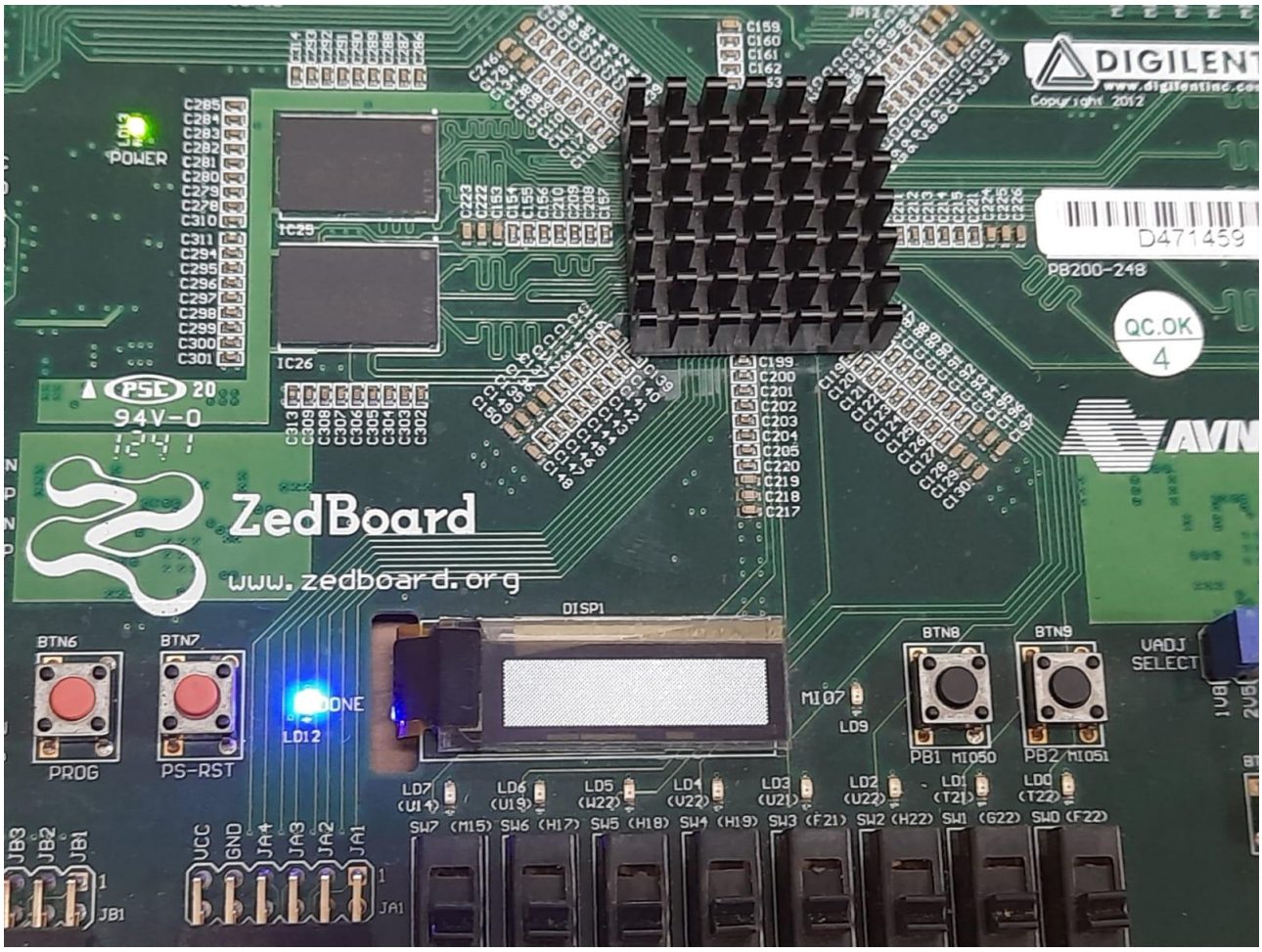
OLED interfacing in the Zedboard:



CONCLUSION

In this project we have made an alarm clock which takes input from user including the date, month, and year to set an alarm on the specified time. The alarm then is displayed on OLED in the Zedboard.

The FPGA is a unique electronic device since it has many positive attributes and few (if any) negative ones depending on the application. It has evolved into the preferred digital processor for many applications because of these factors. It is feasible to have performance, low power, and cheap cost (owing to effective use of the die's gates) together with relative simplicity of embedding high-level designs and algorithms, but without line-by-line coding, by choosing an FPGA tailored to the design. The design may be tested, debugged, and updated with little to no delay or significant NRE because to the advantages of field programmability, even if requirements change or are misinterpreted.

Utilizing the most recent developments in microelectronics fabrication techniques, FPGA vendors are constantly looking for new features to add to their products to expand the range of applications for which they can be used. They may simply be improvements or extensions to resources that were already present, but in other cases, architectures may be expanded with new resources to address long-standing issues or to boost performance.

REFERENCES

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