

# VLSI PROJECT

# **SYNTHESIS OF REVERSIBLE UNIVERSAL LOGIC AROUND QCA WITH ONLINE TESTABILITY**

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# QCA CELL LAYOUTS OF RUG

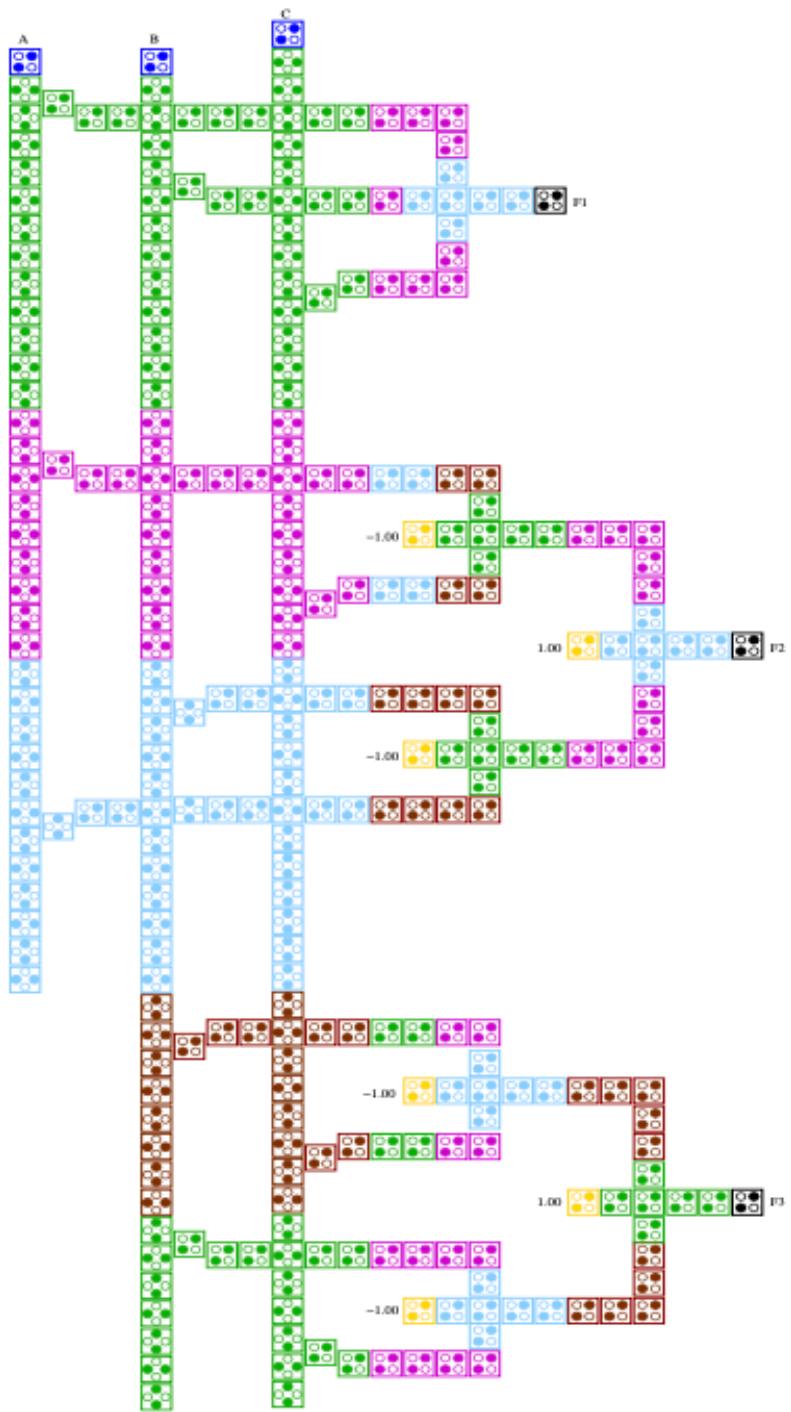
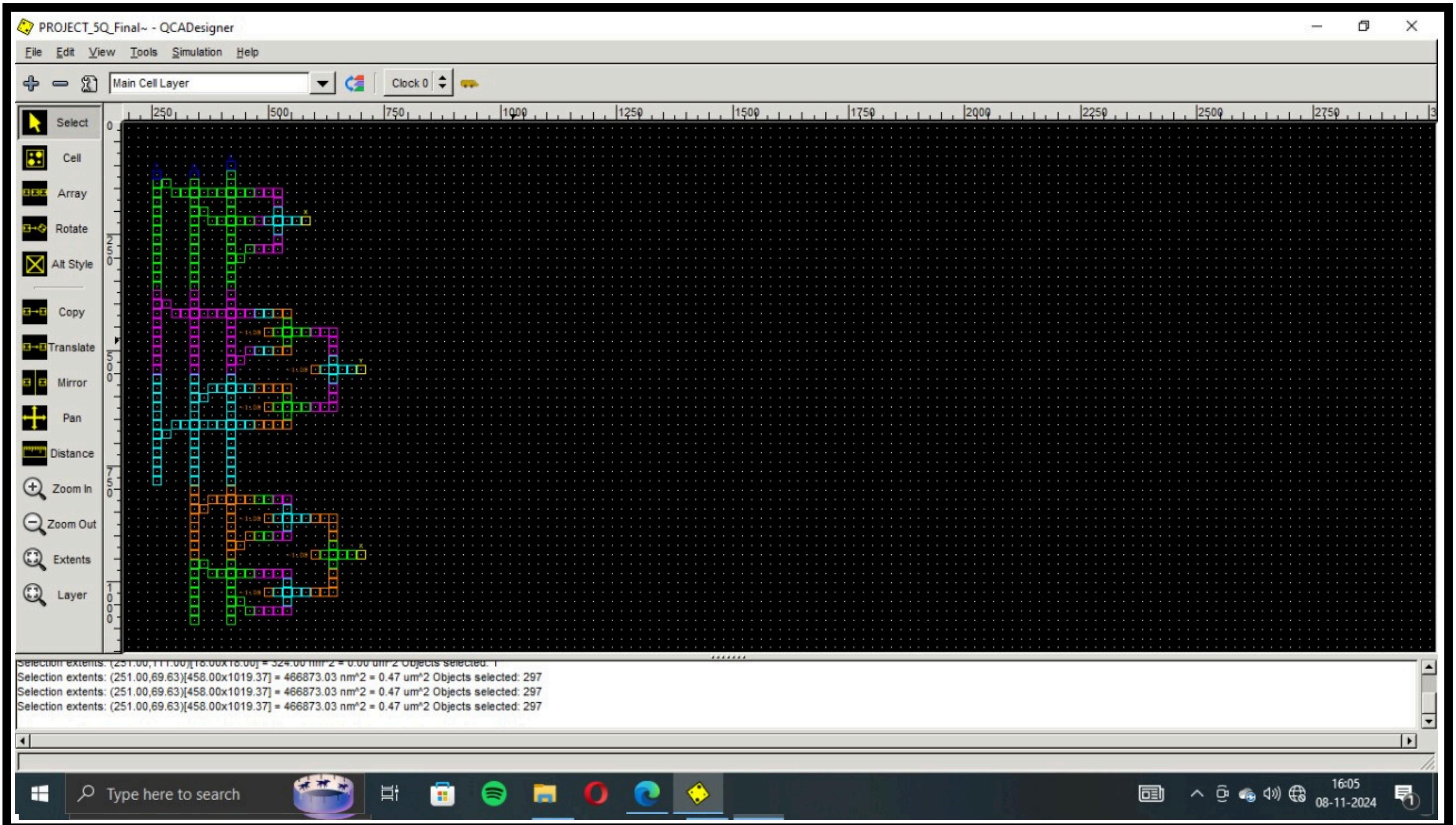
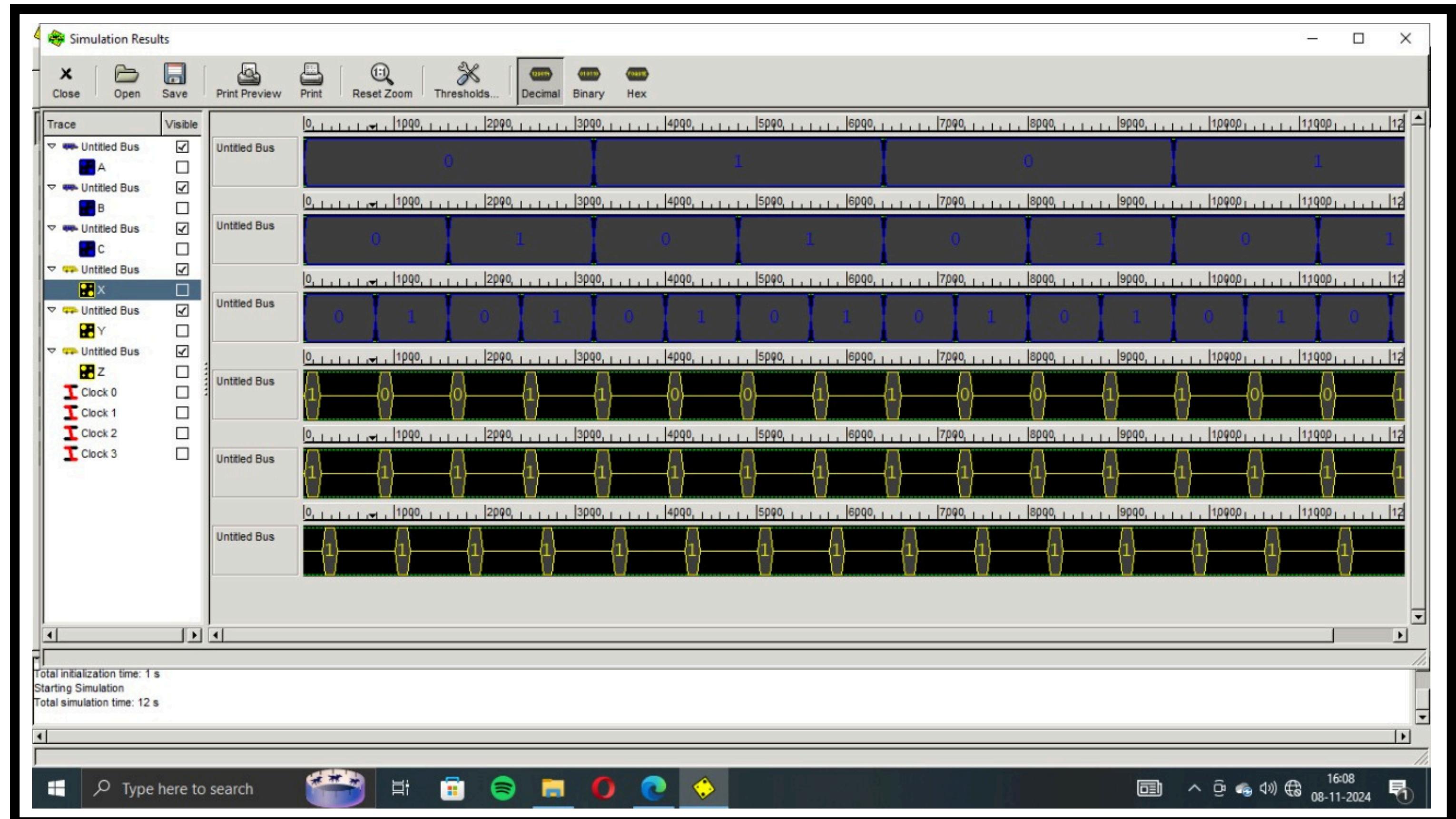
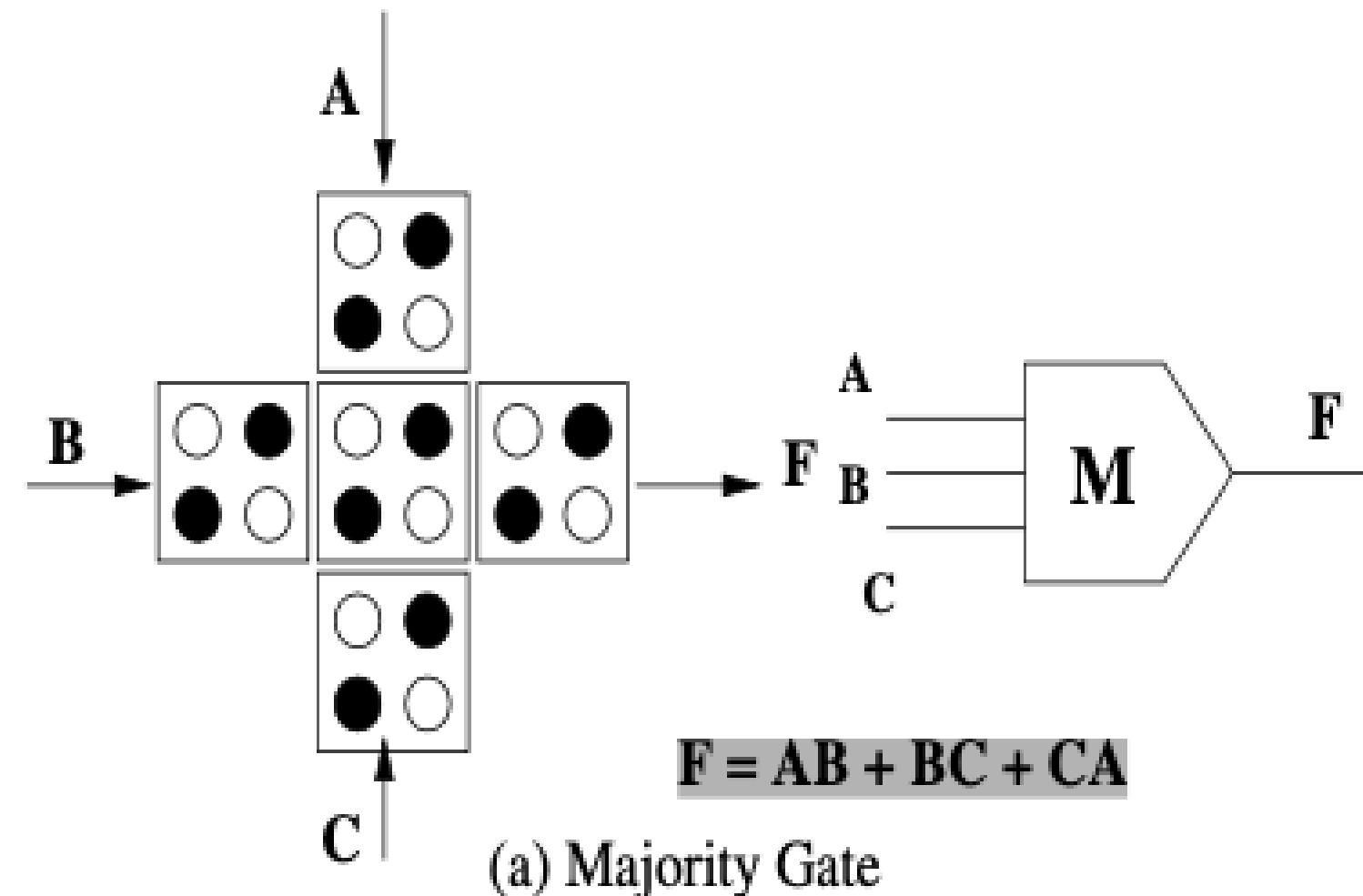


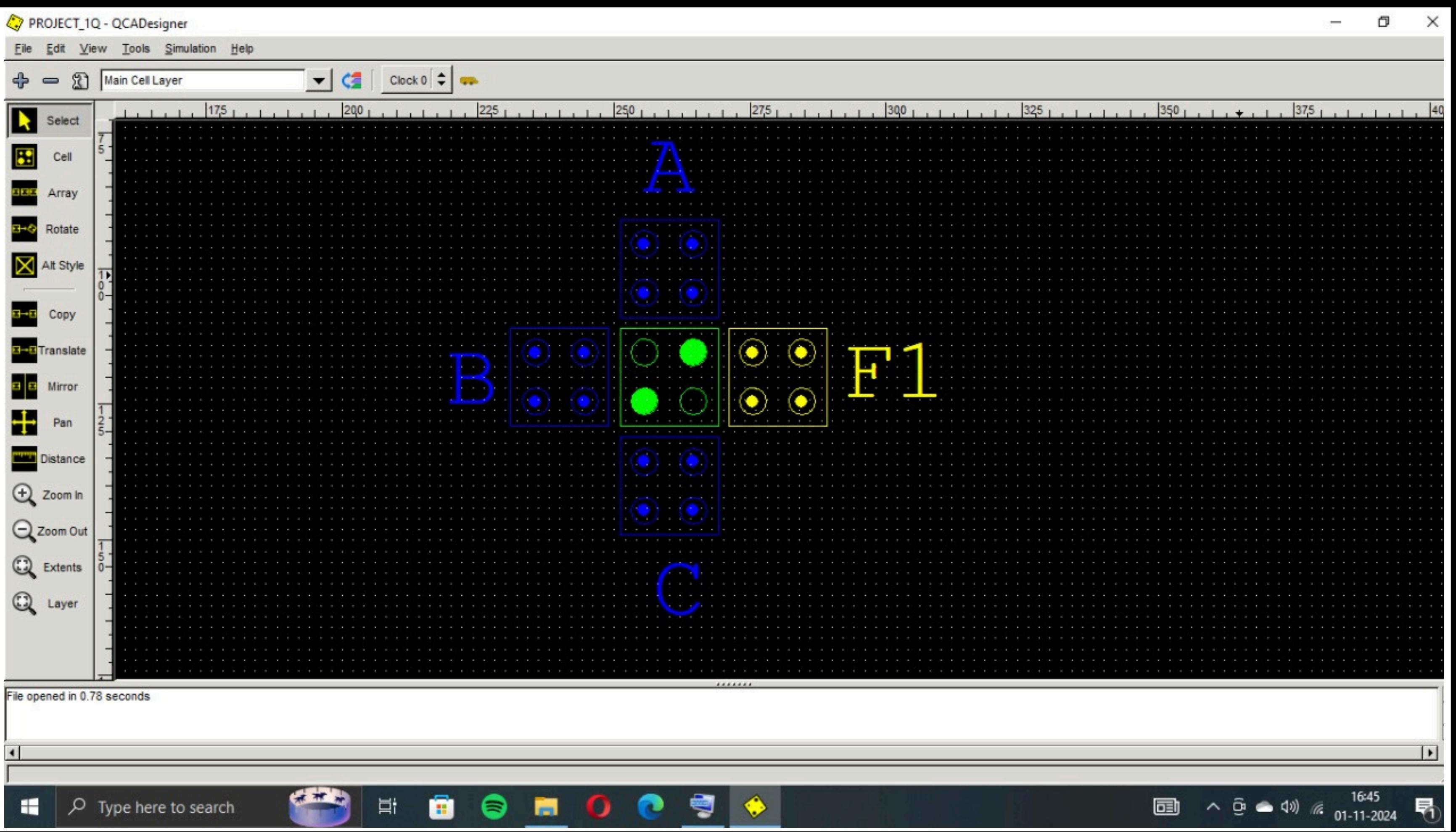
Figure 6. QCA cell layouts of RUG

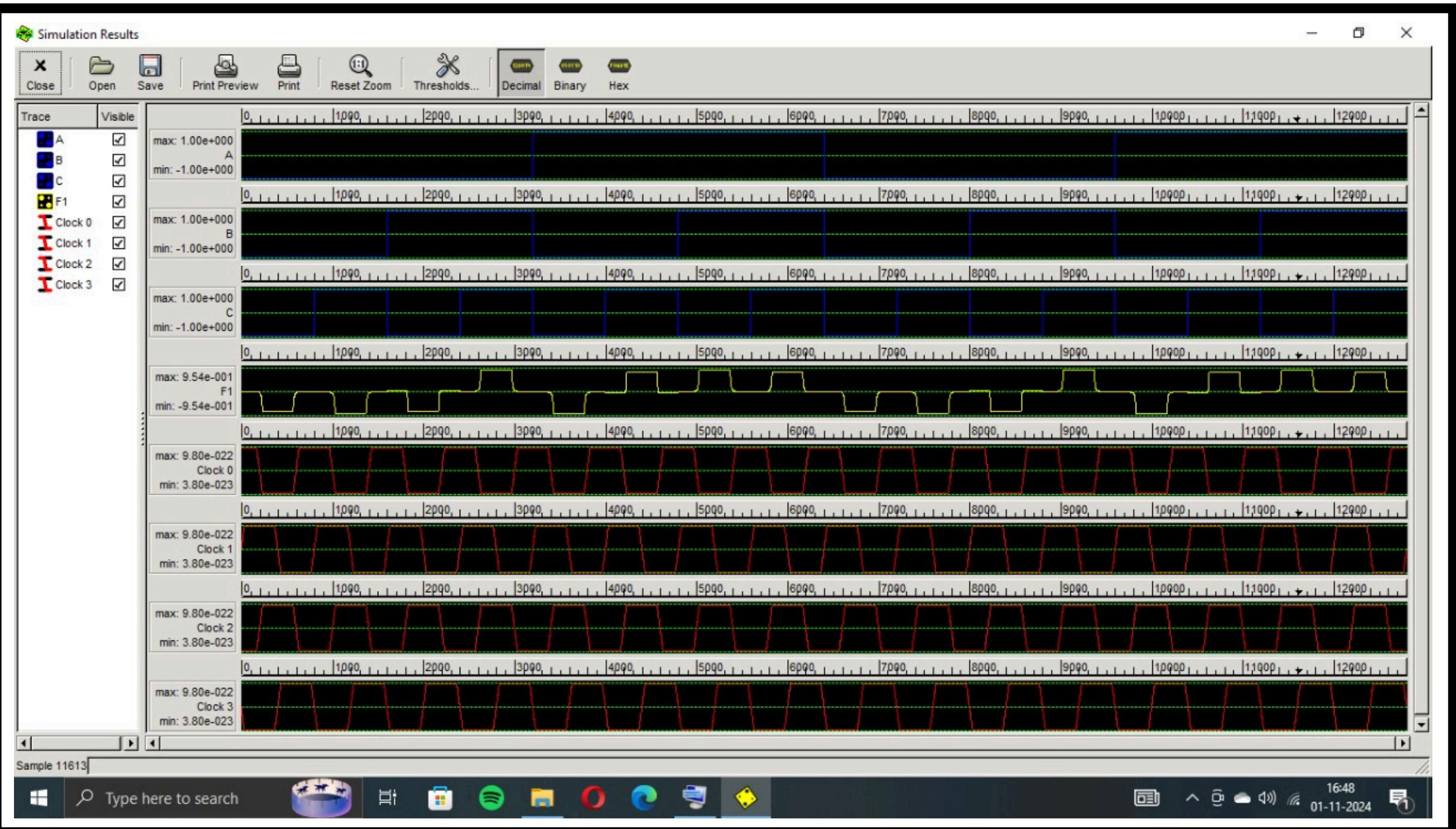




$$F = AB + BC + CA$$

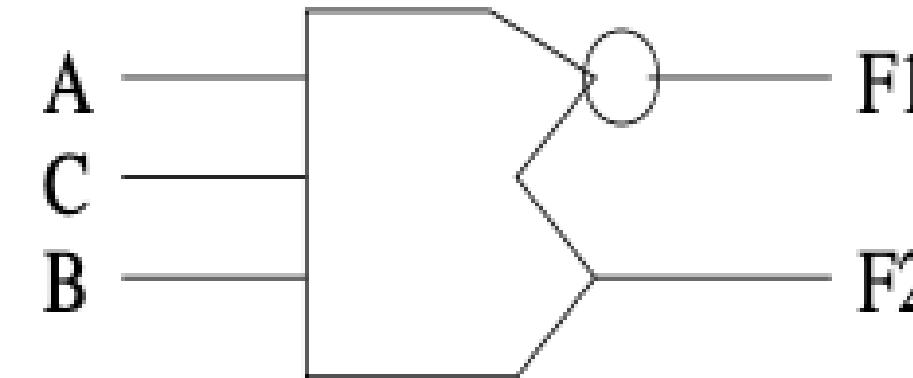
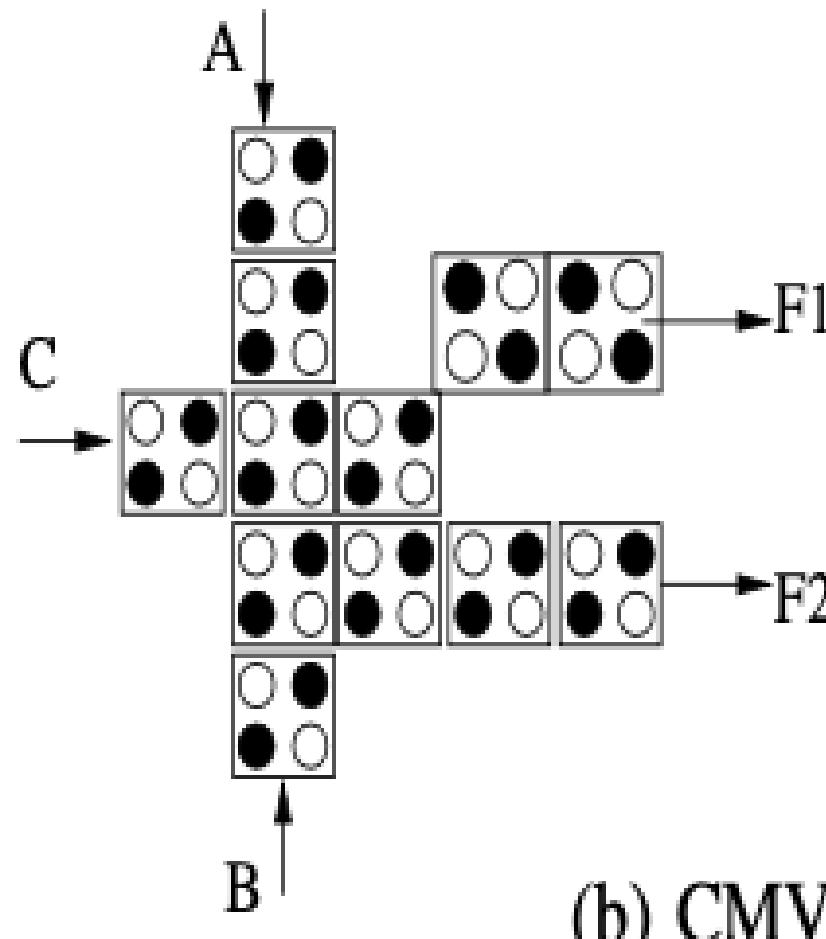






$$F_1 = A'B' + B'C' + A'C'$$

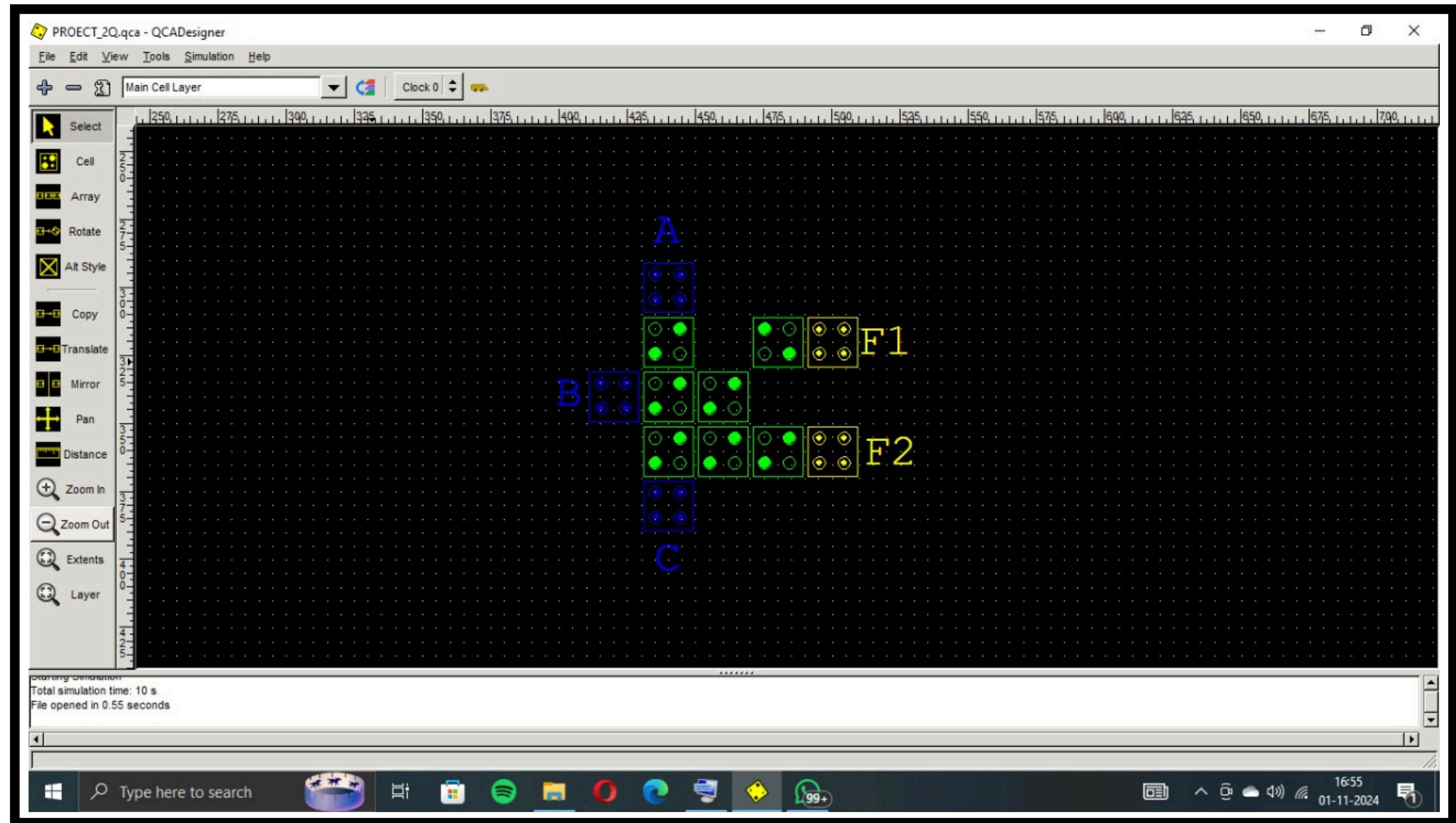
$$F_2 = AB + BC + AC$$

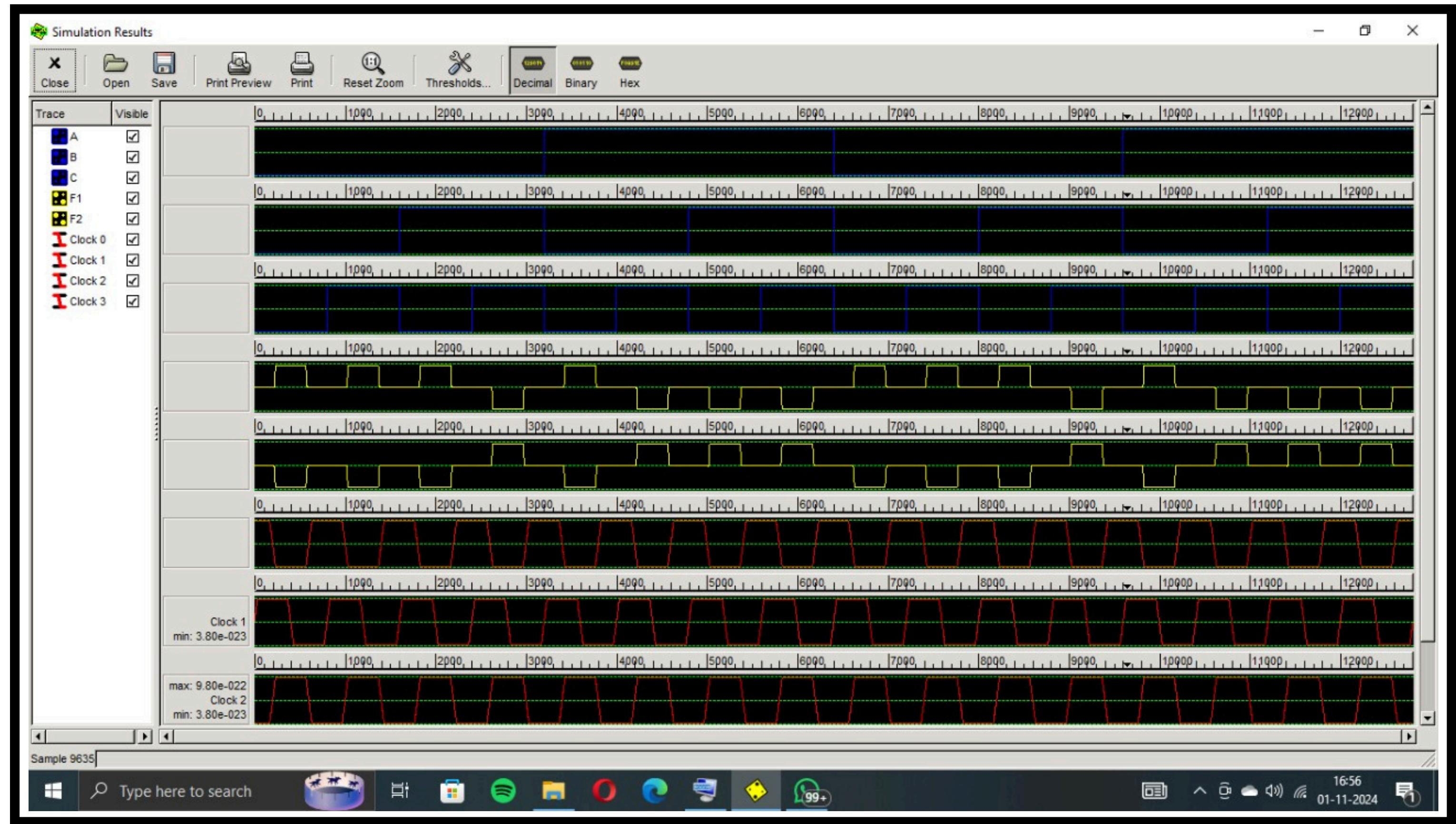


$$F_1 = A'B' + B'C' + A'C'$$

$$F_2 = AB + BC + AC$$

(b) CMVMIN Gate





# WIRE-CROSSING AND INVERTER

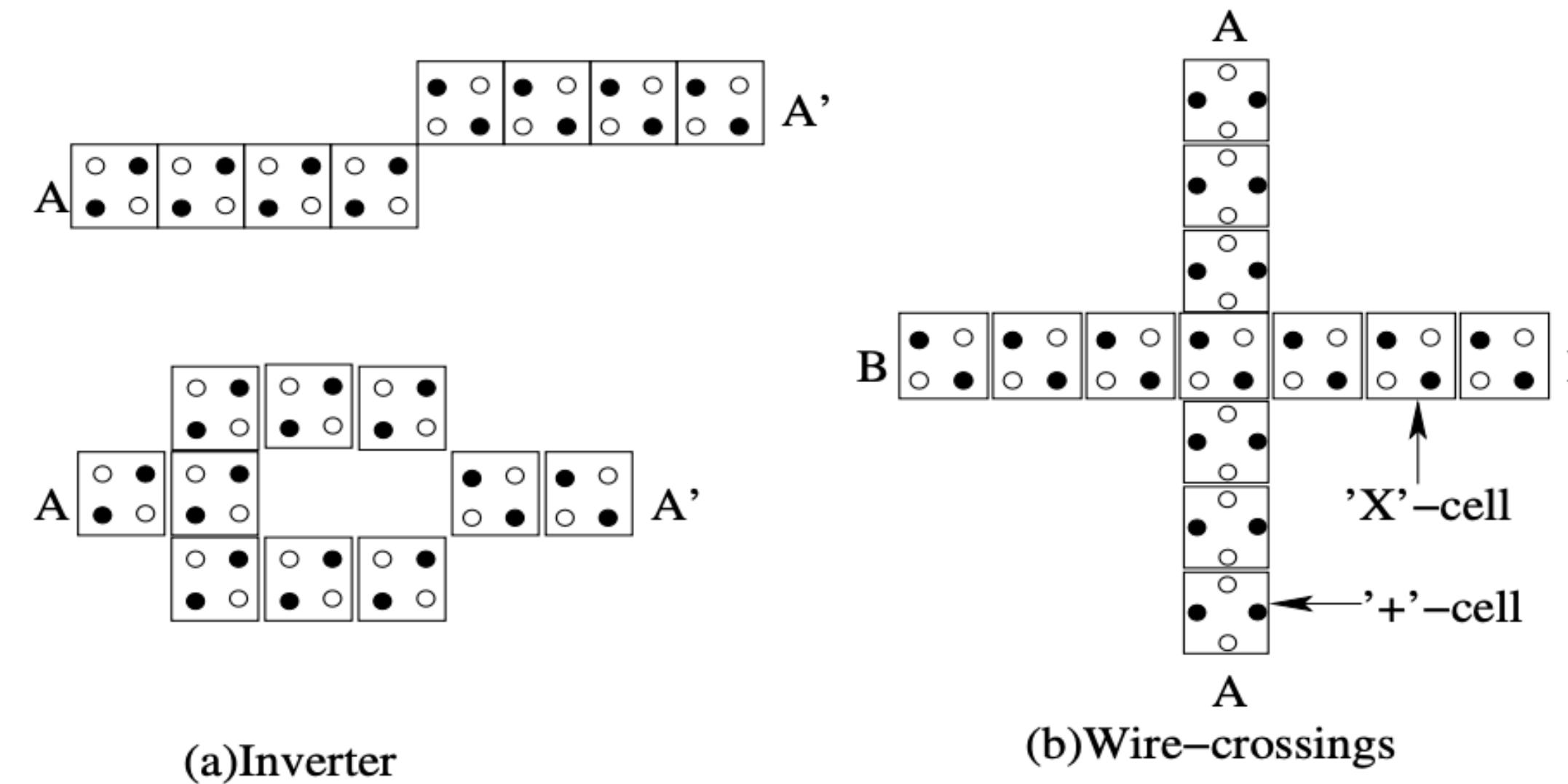
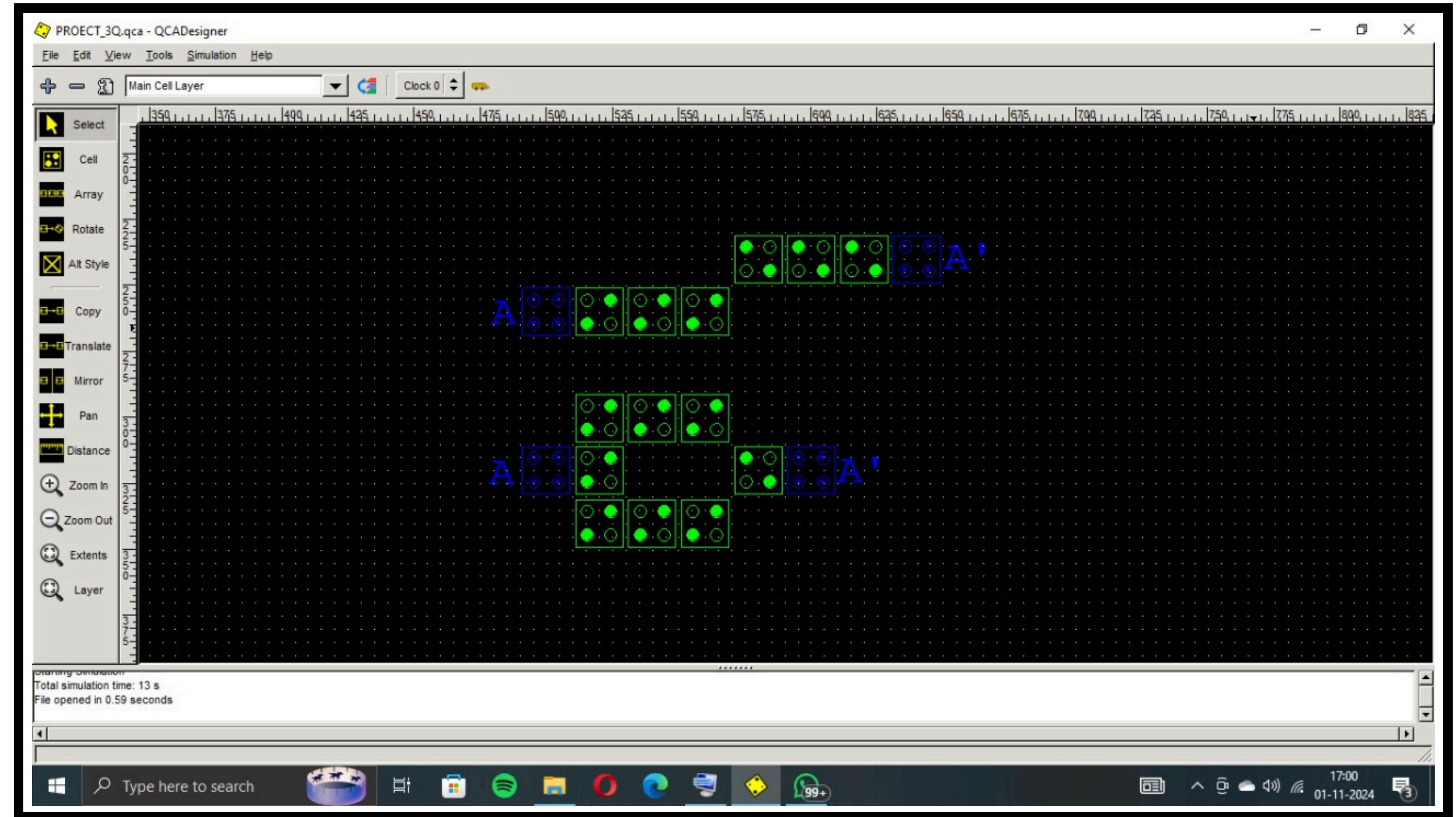
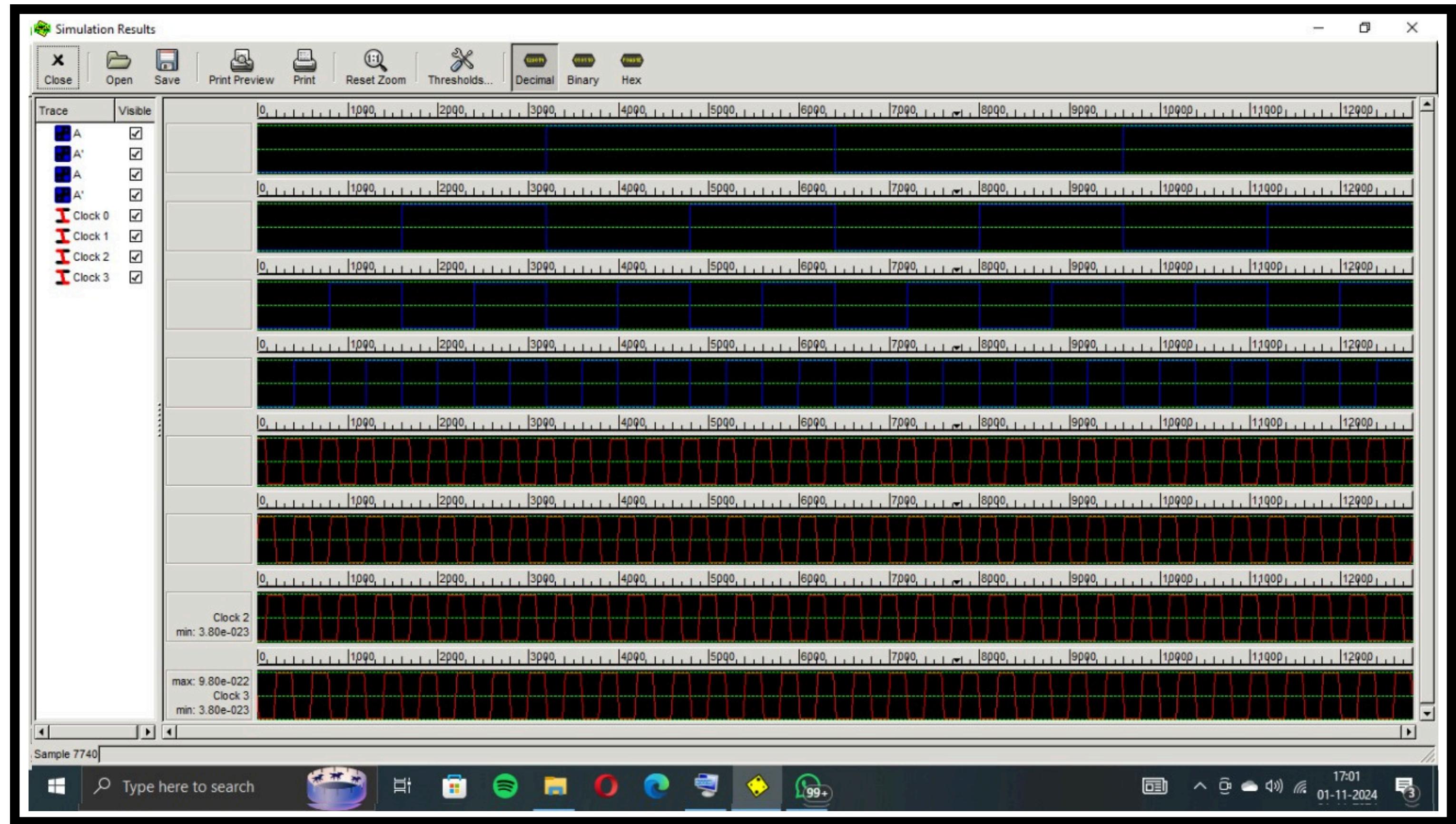
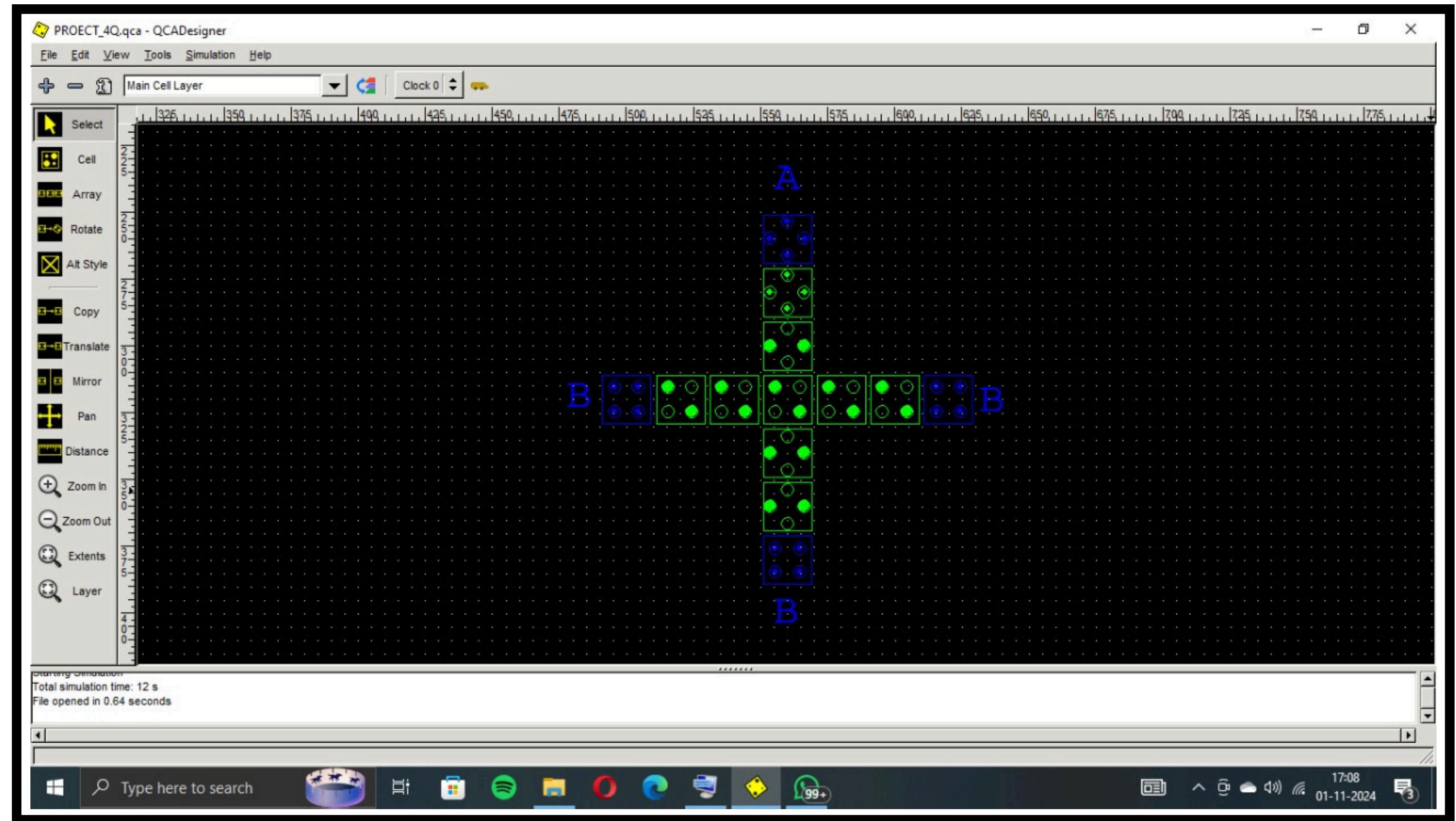
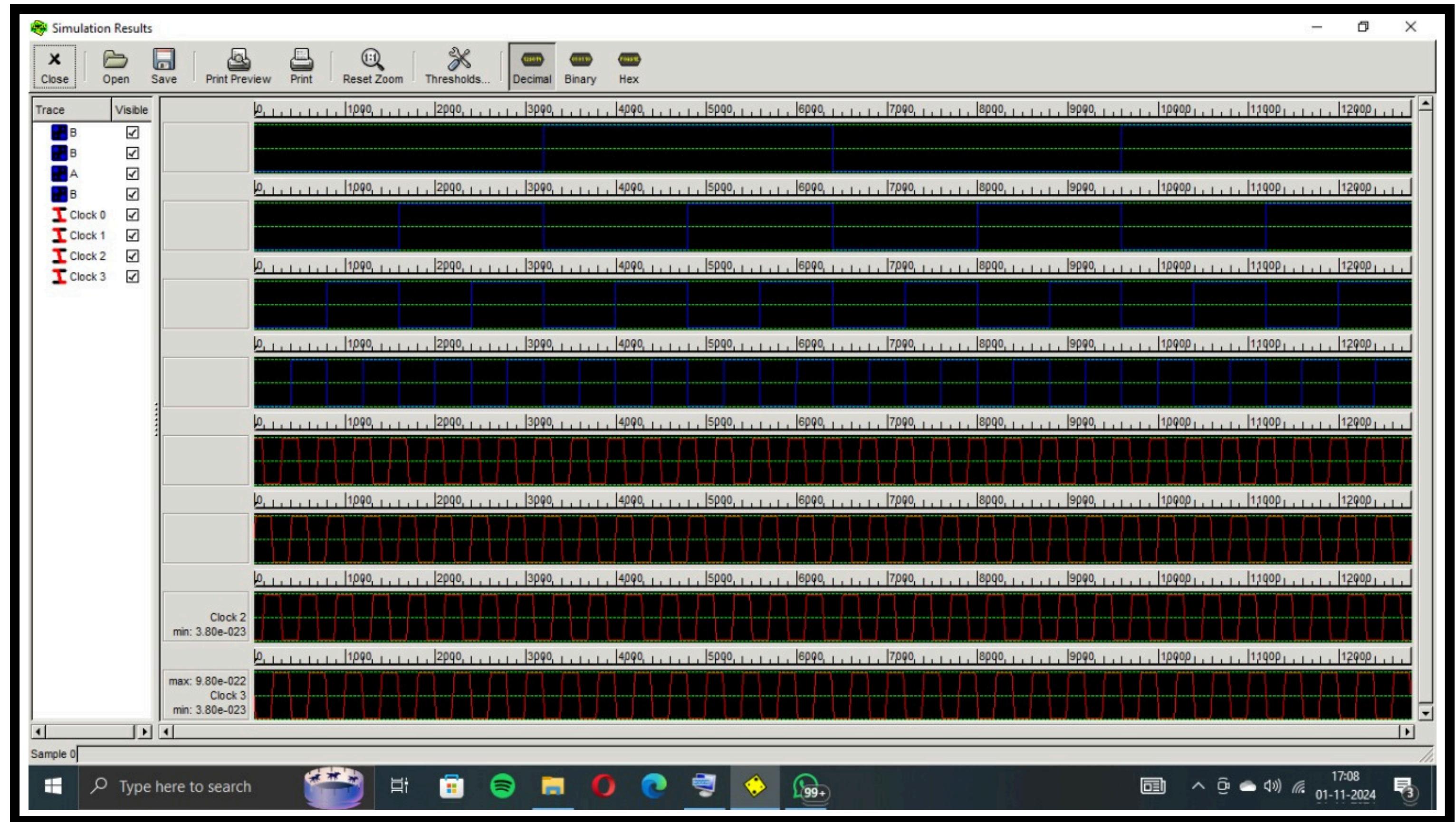


Figure 3. Wire-crossing and inverter









# OUTCOME

Several QCA-based logic gates, such as majority gates, reversible gates, etc., have been successfully designed and simulated to be functional within QCA Designer.



# Thank you

