CAN Protocol Design using Verilog - Final Project Report

Project Title: CAN Protocol Design using Verilog

Date: 2025-08-01

Project Overview:

This project involves the implementation of the Controller Area Network (CAN) protocol using Verilog HDL. The goal is to simulate and verify a CAN communication system by designing and integrating several modules such as a Baud Rate Generator, Frame Generator, Receiver, CRC Checker, and ACK/DONE Status Checker.

Modules Implemented:

1. Baud Rate Generator - Generates baud rate ticks.

2. CAN Frame Generator - Creates a CAN frame with SOF, ID, DLC, DATA, CRC, and EOF.

3. CAN Frame Receiver - Receives the CAN frame and extracts relevant information.

4. CRC Checker - Validates the integrity of the received frame.

5. ACK Checker - Confirms successful transmission by checking CRC match.

6. Top Module & Testbench - Integrates all modules and runs a comprehensive test.

Waveform Analysis Summary:

- Clock and reset signals function correctly.

- Baud rate ticks generated.

- Frame generation completed successfully: Frame = aa5a_5a5a_5a5c_c000.

- CRC Computed = 0x66, ACK signal set correctly.

- Status = 0xAC indicates successful ACK reception.

- Done signal is asserted, marking completion.

Conclusion:

The simulation confirms the successful design of a CAN Protocol System in Verilog. All modules function as expected, and signal transitions validate correct protocol flow. The project is ready for submission.