

GATE CSE MADEEASY HAND NOTES-2020

**9.SUBJECT NAME-
OPERATION SYSTEM**
GATEIESMENTOR

Operating System

GATE NOTES

COMPUTER SCIENCE
MADEEEASY CLASS HAND NOTES

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S. No.	Date	Title <u>(1.01.2018)</u> <u>3 Day Revision</u> <u>1-10.3</u>	Page No.	Teacher's Sign / Remarks
1.		• Introduction of Operating system.	1-6	
2.		<ul style="list-style-type: none"> • Process Management : (a) <u>Process concept.</u> (1) (b) <u>Threads.</u> (1) (c) <u>Interprocess communication.</u> (2) (d) <u>Concurrency.</u> (CS) (2) (e) <u>Synchronization.</u> (2) (f) <u>Deadlock.</u> (3) (g) <u>CPU Scheduling.</u> (*) (1) 	40%	
3.		<ul style="list-style-type: none"> • Memory Management : (a) <u>Memory management</u> & (4) virtual memory. 	40%	
4.		<ul style="list-style-type: none"> • File System : (a) <u>File and Device management.</u> (5) 		

Date 06/04/2019

INTRODUCTION OF OS

- What is operating System?

→ An Operating System acts as an intermediary between the user of a computer and the computer hardware. An operating system is a software that manages the computer hardware.

```

graph TD
    User([Users]) --> App[Application Software]
    App <--> OS[Operating System Software]
    OS --> HW[Hardware System]
    
```

(Basic Diagram)

- **Hardware:** It provides the basic computing resources for the system. It consists of CPU, Memory and I/O Devices.

- **Application programs:** Define the ways in which these resources are used to solve user's computing problems. e.g. word processors, Spreadsheets, Compilers, and web browsers, Accounting software.

- **Components of Operating System:**

- process management.
- Main memory management.
- File management.
- I/O System management.
- Secondary - storage Management.
- protection System.
- Networking.
- Command - Interpretive system.

- **Function of operating System:**

1. program execution.
2. I/O operation.

3. File system manipulation.

4. Communication.

5. Error Detection.

6. Resource allocation.

7. Accounting.

8. Protection System.

- **Program Execution:** The OS helps to load a program into main memory and run it.

- **I/O Operation:** Each running program may request for I/O operation and for efficiency and protection the user can't control I/O devices directly. Thus, the OS must provide some means to do I/O operation.

- **File System Manipulation:** Files are the most important part which needed by programs to read and write the files and files may also be created and deleted by name or by the programs. The OS is responsible for the file management.

- **Communication:** OS performs the communication among various types of processes in the form of shared memory. In the multitasking environment, the processes need to communicate with each other and to exchange their information. These processes are created under a hierarchical structure where the main process is known as parent process and the subprocess are known as child processes.

- **Error Detection:** It is necessary that OS must be aware of possible errors and should take the appropriate action to ensure correct and consistent computing.

- **Resource Allocation:** Allocation of resources to the various processes is managed by O.S.

- **Accounting:** OS may also be used to keep track of the various computer resources and how much and which users are using these resources.

- **Protection:** If a computer system has multiple users and allows

the concurrent execution of multiple processes, then the various processes must be protected from one another's activities.

System call:

main()

```
{ pf(".....");
    sf(".....");
}
```

Internally calls write() system calls in order to communicate with the monitor.

It is the request made by the user program to the OS in order to get any kind of service.

Types of operating system:

The operating system can perform a single operation and also Multiple operations at a time. So there are many types of operating systems those are organized by using their working techniques.

1. Serial processing: The serial processing operating system are those which performs all the instructions into a sequence manner or the instructions those are given by the user will be executed by using the FIFO manner means first in first out. Mainly the punch cards are used for this. In this all the jobs are firstly prepared and stored on the card and after that card will be entered in the system and after that all the instructions will be executed one by one. But the main problem is that a user doesn't interact with the system while he is working on the system, means the user can't be able to enter the data for execution.

2. Batch processing (OS): The batch processing is same as the serial processing technique. But in the batch processing similar types of job are firstly prepared and they are stored in the card and that card will be submit to the system for the processing. The main

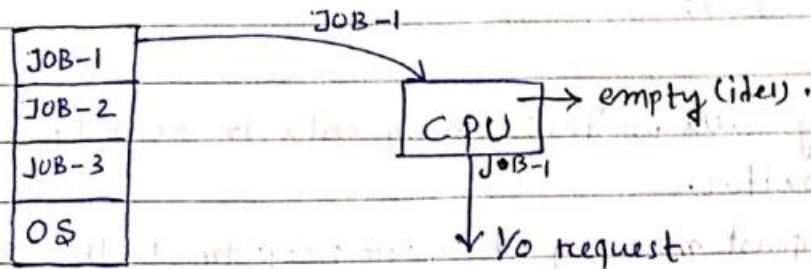
$$\boxed{\text{JOB}} = (\text{CPU time} + \text{IO time})$$

Execution time

Sathu

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The main problem is that the jobs those are prepared for execution must be the same type and If a job requires for any type of input then this will not be possible of the user. The batch contains the jobs and all those jobs will be executed without the user intervention.

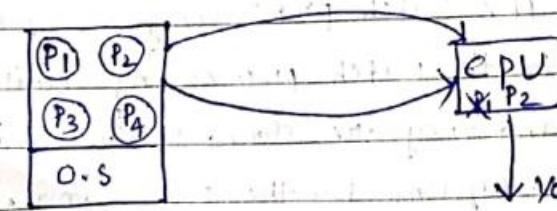


Memory

- If the job is fully completed, then only another job will be scheduled.
- Increased CPU idleness.
- The Throughput of the system will decrease.

Throughput (the number of jobs completed per unit time is called throughput of the system).

* **3. Multiprogramming Operating System:** Executes multiple programs on the system at a time and In the Multiprogramming, the CPU will never get idle, because with the help of Multiprogramming we can execute many programs on the System and when we are working with the program then we can also submit the second or another program for running and the CPU will then execute the second program after the completion of the first program. And In this, we can also specify our input means a user can also interact with the system.



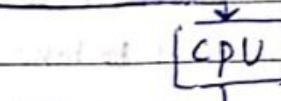
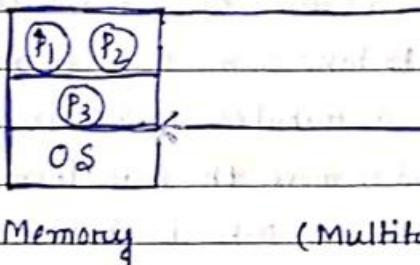
- Increased CPU utilization.

- Increased throughput.

~~4.~~ **Multitasking operating System:** Multiple applications app operated at the same time.

- Multitasking is an extension to Multiprogramming.

- The jobs will be executed in the time sharing mode.

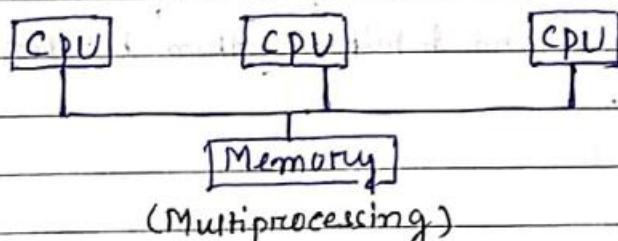


(Illustration)

Memory (Multitasking)

~~5.~~ **Multiprocessing operating System:** In the Multi processing there are two or more CPU in a single operating system, if one CPU will fail, then other CPU is used to providing backup to the first CPU. With the help of multiprocessing, we can execute many jobs at a time.

All the operations are divided into the Number of CPU's. If first CPU completed his work before the second CPU, then the work of second CPU will be divided into the first and second CPU.



(Multiprocessing)

~~6.~~ **Realtime Operating System:** In this, Response time is already fixed. Means time to display the results after processing has fixed by the processor or CPU. Real time system is used at those places in which we requires higher and timely response.

- Hard Real-time System: In the hard real-time system, time is fixed and we can't change any moments of the time of process the data as we enters the data.

- soft Real-time system: in the soft real-time system, some moments can be changed. Means after giving the command to the CPU, CPU performs the operation after a microsecond.

✓ 7. Distributed Operating System: Distributed Means data is stored and processed on Multiple locations. When a data is stored on to the multiple computers, those are placed in different locations. Distributed means in the network, Network collections of computers are connected with each other. Then If you we want to take some data from other computers, then we uses the distributed processing system. And we can also insert and remove the data from one location to another location. In this Data is shared between many users. And we can also Access all the input and output devices are also accessed by multiple users.

8. parallel operating system: These are used to interface multiple networked computers to complete task in parallel. parallel OS are able to use software to manage all of the different resources of the computers running in parallel, such as memory, cache, storage space, and processing power. A parallel OS works by dividing sets of calculations into smaller parts and distributing them between the machines on a network.

PROCESSES - (process management)

R&R

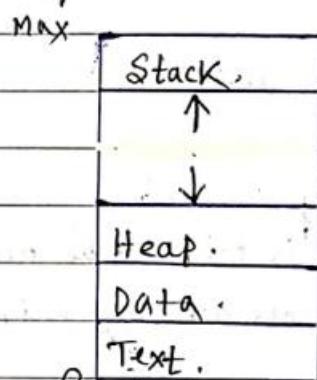
• **Process:** A process can be defined in any of the following ways:

- A process is a program in execution.
- It is a asynchronous activity.
- It is the entity to which processors are assigned.
- It is dispatchable unit.
- It is the unit of work in a system.

A process is more than the program code. When we execute a program, it becomes a process which performs all the task mentioned in the program.

When a program is loaded into memory and it becomes a process, it can be divided into four sections - stack, heap, text and data.

The following image shows a simplified layout of a process inside main memory -



(process in memory)

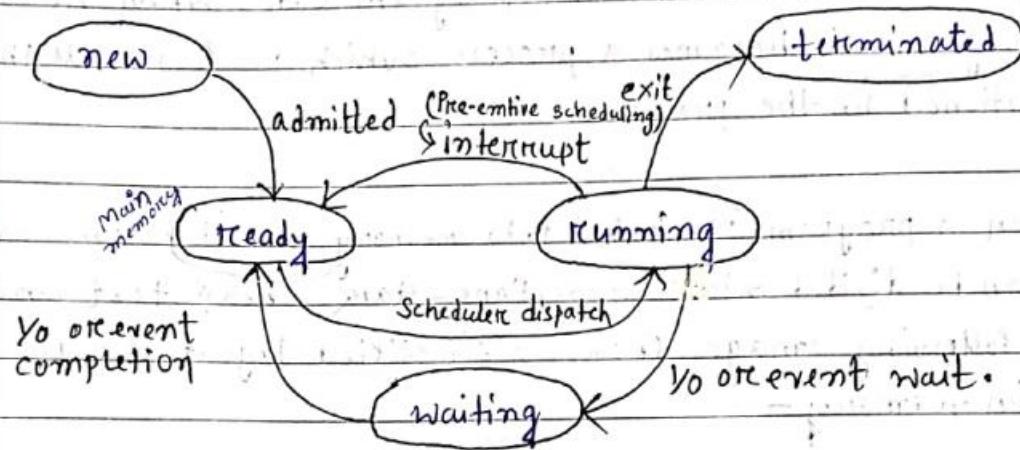
- **Stack :** The process stack contains the temporary data such as function parameters, return address, and local variables.
- **Heap :** This is dynamically allocated memory to process during its run time.
- **Data :** This section contains the global and static variable.
- **Text :** This includes the current activity represented by the value of program counter and the contents of the process's register.
(Code section)

R&R • **Process State Diagram:**

When a process executes, it passes through different states.

This stages may differ in different OS, and the name of these states are arbitrary.

A process can have one of the following five states at a time.



(Diagram of process state.)

1. **Start:** The process is being created.

2. **Running state:** A process is said to be running if it has the CPU, that is, process actually using the CPU at that particular instant.

3. **Waiting (or Blocked) state:** A process is said to be blocked if it is waiting for some event to happen such that as an I/O completion before it can proceed. Note that, a process is unable to run until some external event happens.

4. **Ready:** A process is said to be ready if it uses CPU if one is available. A ready state process is runnable but temporarily stopped running to let another process run.

5. **Terminated state:** The process has finished execution.

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~~RBR~~ • **Process Control Block (PCB) :**

A process in an OS is represented by a data structure known as process control block (PCB) or process descriptor.

A PCB keeps all the information needed to keep track of a process. The architecture of PCB is completely dependent on operating system and may contain different information in different OS.

Process ID
P-state
Pointers
Priority
Program counter
CPU registers
I/O information
Accounting information
etc ..

(PCB Diagram)

1. process state : The current state of process i.e., whether it is ready, running, waiting, or whatever.
2. process privileges : This is required to allow/disallow access to system resources.
3. process ID : Unique identification for each of the process in OS.
4. pointers : A pointer to parent process.
5. program counter : PC is a pointer to the address of the next instruction to be executed for this process.
6. CPU registers : Various CPU registers where process need to be stored for execution for running state.
7. Accounting information : This includes the amount of CPU used for process execution, time limits, execution ID etc.
8. I/O status information : This includes a list of I/O devices allocated to the process.
9. CPU-scheduling information : process priority and other scheduling information

Multiprogramming

with preemption

without preemption.

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Which is required to schedule the process.

10. Memory management information: This includes the information of page table, memory limits, segment table depending on memory used by the OS.

PBR

Schedulers:

Schedulers are special system software which handle process scheduling in various ways. Their main task is to select the jobs to be submitted into the system and to decide which process to run.

Schedulers are of three types -

1. Long Term Scheduling,
2. Short Term Scheduling,
3. Medium Term Scheduling.

1. Long Term Scheduler or job scheduler:

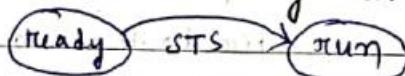
LTS is responsible for creating new processes and bringing them into System. LTS selects processes from job pool (where processes

New \rightarrow LTS \rightarrow Ready (are kept for later execution) and

Load them into memory for execution. LTS controls degree of Multiprogramming.

2. Short term Scheduler or CPU scheduler:

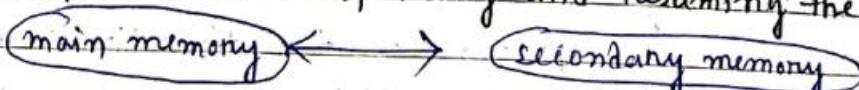
STS is responsible for scheduling one of the process from ready state to running state.



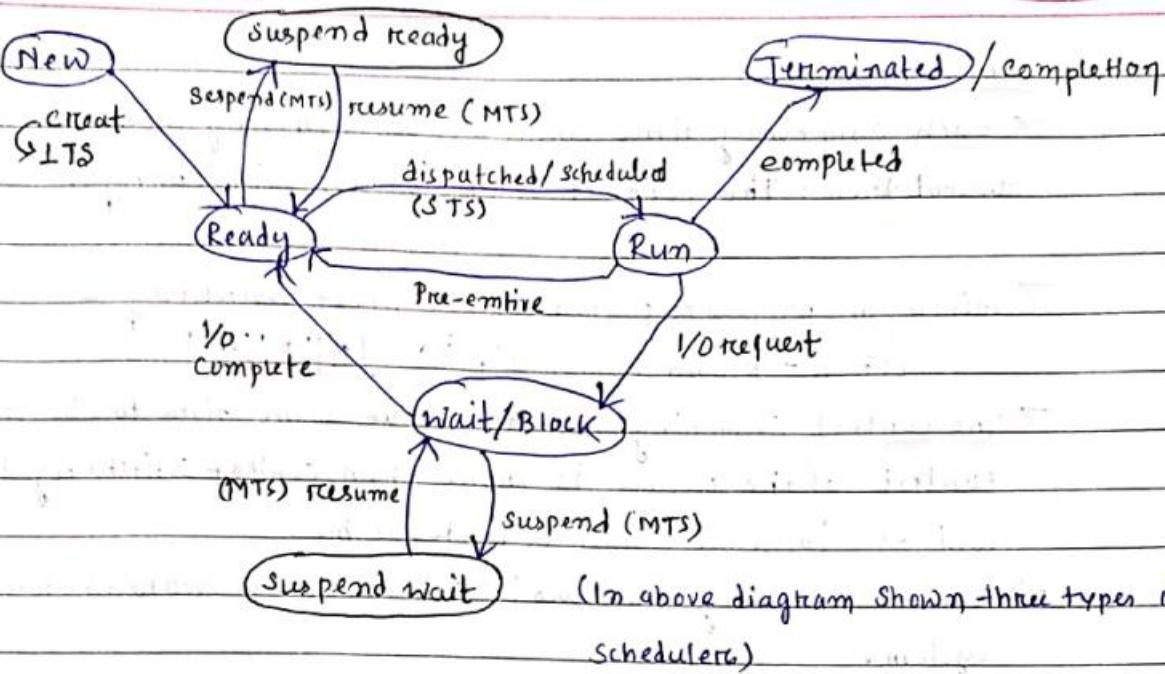
STS selects from main memory among the processes that are ready to execute and allocates the CPU to one of them.

3. Medium Term Scheduler:

MTS is responsible of suspending and resuming the processes.



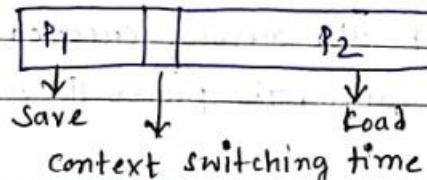
The medium term scheduler are also called a SWAPPER.



Aspects :	LTS	MOTS	STS
called as	It is job scheduler	It is a process swapping	It is a CPU scheduler
Speed	Speed is less than STS	Speed is in between both LTS and STS.	Speed is fastest among two schedulers.
Multiprogramming	It controls the degree of Multiprogramming.	It reduces the degree of multiprogramming.	It provides lesser over control degree of multiprogramming.
Time-sharing system.	It is almost absent or minimal in time sharing system.	It is part of Time sharing system.	It is also nominal minimal.
processes	It selects processes from pool and loads them into memory for execution.	It can reintroduce the process into memory and execution can be continued.	It selects those processes which are ready to execute.

Context Switching :

Saving the context of 1 process and loading the context of another process is called Context switching.



Some points:

- each and every time when process is moving from one state to another, the context of the process will change.
- Minimum process required for context switching '2'.
exception - Round Robin '1'. $(P_1) \boxed{P_1} || P_1 || ..$
- The context switching will also take some time \rightarrow , so if the context of the process is more then context switching time will also increase which is undesirable.
- Context switching time also is considered as overhead for the system.

• Dispatcher :

Dispatcher is responsible for saving the context of 1 process and loading the context of another process. The context switching is done by dispatcher.

RBR • The fork() :

- System call fork() is used to create processes. It takes no arguments and returns a process ID.
- The purpose of fork() is to create a new process, which becomes the child process of the caller.

- After a new child process is created, both processes will execute the next instruction following the fork() system call.
- Therefore, we have to distinguish the parent from the child.

This can be done by testing the returned value of fork():

- If fork() return a negative value, the creation of a child process was unsuccessful.
- If fork() return a zero to the newly created child process.
- If fork() return a positive value, the process ID of the child process.

to the parent. Normally the process ID is an Integer. Moreover, a process can use function ~~getpid~~ getpid() to retrieve the process ID assigned to this process.

- Conclusions -

- If the program contains n fork() calls it will create $2^n - 1$ child processes.

- When the child process is created by using fork system call, both parent and children will have -

- Relative address = Same for both parent and child process.

- Absolute address = Different for both parent and child process.

- fork() system call implementation -

```

main
{
    int pid;
    pid = fork();
    if (pid < 0)
        {
            pf("child process creation failed");
        }
    else if (pid == 0)
        {
            pf("child process");
        }
}

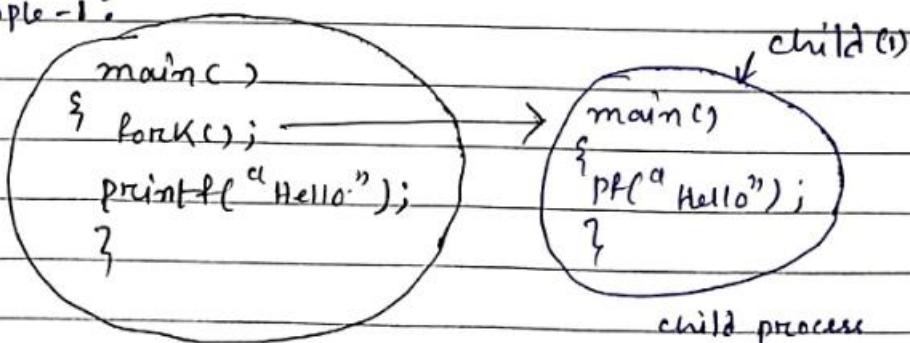
```

```

else
{
    pf("parent process");
}
}

```

- Example - 1 :



Output: Hello

Hello

2 process / 2 time Hello ./ 1 child ($2^n - 1 = 2^1 - 1 = 1$) .

RBR

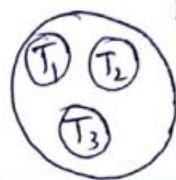
Q. Question on process states -

consider a system with 'N' CPU processors and 'M' processes,
then,

	min	max
Ready	0	M
Running	0	N
Block or Wait	0	M

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THREADS



- **Thread :**

A Thread is a single sequence stream within a process. Because threads have some of the properties of processes, they are sometimes called lightweight processes.

→ A thread can be in any several states (Running, Blocked, Ready, or Terminated)

→ Each thread has its own stack.

→ A thread or consists of a program counter (PC), a register set, and a stack space.

→ Threads are not independent of one other like processes as a result threads shares with other threads their code section, data section, OS resources also known as task, such as open files and signals.

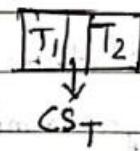
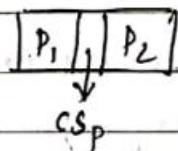
- **Advantages of Thread:**

1. **Responsiveness:**

→ If the process is divided into multiple threads, then 1 thread is completed, then immediately output will be responded.

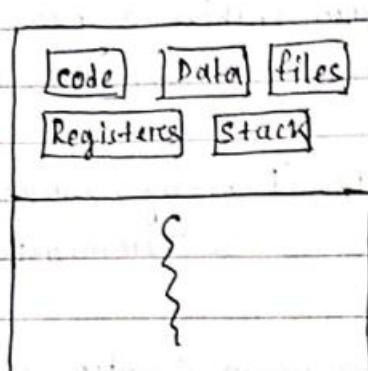
2. **Faster context switching:**

→ The context switching time between the threads is very very less as compared to context switching time between the processes. Because the threads will have less context compared to process.

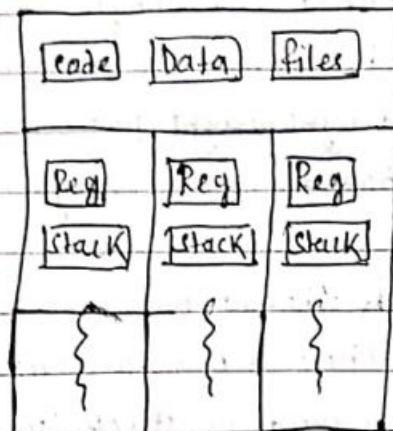


$CS_T \ll CSP$

3. Resource Sharing:



single threaded
process



Multi threaded process

→ The resources like code, data, and files will be shared among all the threads within the process but every thread will have its own stack and registers.

4. Effective Utilization of Multiprocessor Systems:

→ If the process is divided into multiple threads, then different threads of the process can be scheduled onto a different CPU, so that the process execution will be faster.

5. Enhanced throughput of the System:

→ If the process is divided into multiple threads, if we consider 1 thread as 1 job then number of job completed per unit time will increase and throughput of the system will be enhanced.

6. Economical:

→ The implementation of threads does not require any cost. There are various programming languages API's which support implementation of thread e.g. JAVA's API, thread API.

- Types of Threads:

Threads are categorized into 2 types -

- User level threads.
- Kernel level threads.

- Difference between them -

User level thread	Kernel level thread
→ These are created by user or programmers.	→ These are created by operating system (OS).
→ OS can't recognize the user level threads.	→ OS recognizes the Kernel level threads.
→ If one user level thread performing blocking system call, then entire process will be blocked.	→ If one Kernel level thread performing blocking system call, then other another thread will continue the execution.
→ Dependent threads.	→ Independent threads.
→ Designing user level threads is easy.	→ Designing kernel level threads is complicated.
→ Less context.	→ More context.
→ No H/w support required.	→ Scheduling of Kernel level threads requires H/w support.

- * Thread Scheduling also known as GRANU scheduling.

- There are three common ways of establishing relationship between user threads and kernel threads -

- Multi. are two three types -

- Many-to-many model.
- one-to-one model.
- Many-to-one model.

1. Many-to-many model -

→ Allows many user level threads to be mapped to many kernel threads.

2. One-to-one model -

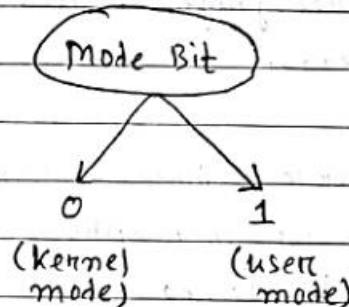
→ Each user level threads maps to kernel thread.

3. Many-to-one model -

→ Many user level threads mapped to single kernel thread.

Double Mode of operation :

User Mode OR Non-privileged Instructions
Kernel Mode OR privileged Instructions



→ The O.S. executes the instructions in 2 different modes -

1) User mode.

2) Kernel mode.

→ The dual mode of operation is required to protection and security to the O.S. and also to the user programs from Errant users (conscripted users).

→ In which particular mode the current instruction is executing will be decided by mode bit.

→ At boot time the system always starts in the Kernel mode.

→ Depending upon the type of instruction the O.S. will decide in which particular mode instruction has to be executed.

→ Generally privileged instructions will be executed in the Kernel mode, and Non-privileged instructions will be executed in the User mode.

- privileged Instructions: (examples)

- 1) Context Switching.
- 2) Disabling Interrupts.
- 3) Set the time of clock.
- 4) Changing the memory map.
- 5) I/O operation (Reading/file data from disc)

- Non-privileged Instructions: (examples)

- 1) Reading time of the clock.
- 2) Sending the final print to the printer.
- 3) Reading the status of the CPU.

✓ Done

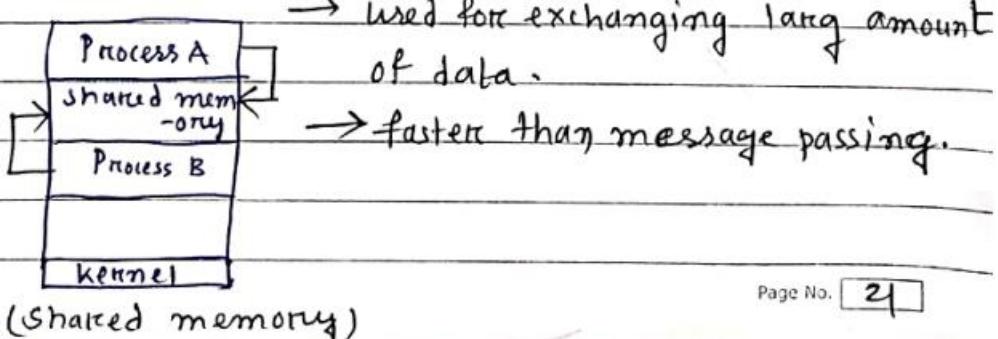
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Inter-Process Communication

- process executing concurrently in the operating system may be either independent or cooperating processes.
- A process is independent ; if it can't affect or be affected by other processes executing in the system.
- A process is a cooperating process , if that shares data with other processes is a cooperating process.
- Advantages of process cooperation are-
 - Information sharing .
 - Computation speed up .
 - modularity and convenience to work on ^{many} task at the same time .
- Cooperating processes require an inter process communication (IPC) mechanism that will allow them to exchange data and information .
- There are 2 fundamental models of IPC :
 - i) Shared Memory .
 - ii) Message passing .

1. Shared memory :

- In this method 2 or more processes share a single chunk of memory to communicate .

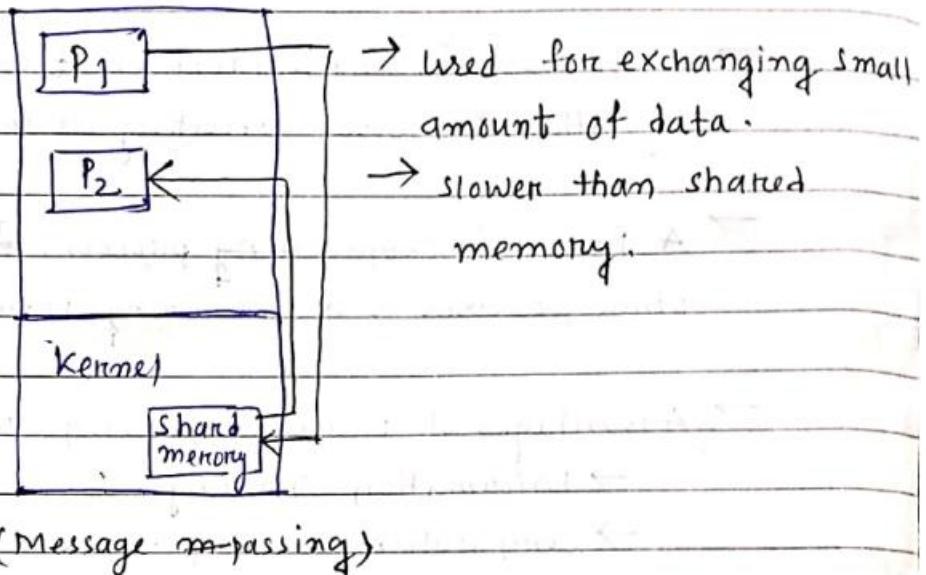


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2. Message passing:

→ shared memory created in the Kernel.

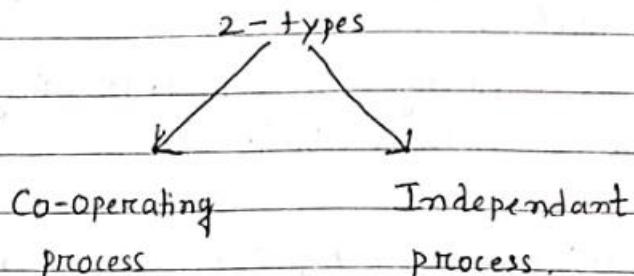
→ System call such as send and receive used for communication.



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PROCESS SYNCHRONIZATION

- * The processes with respect to synchronization are of



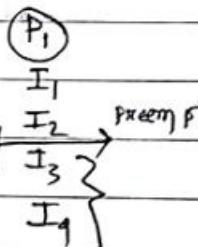
The execution of 1 process affects or is affected by other process then these processes are said to be co-operative processes, otherwise they are said to be independant process.

→ Affection occurs due to shared variable, common shared Resource / Data.

- Some Important points:

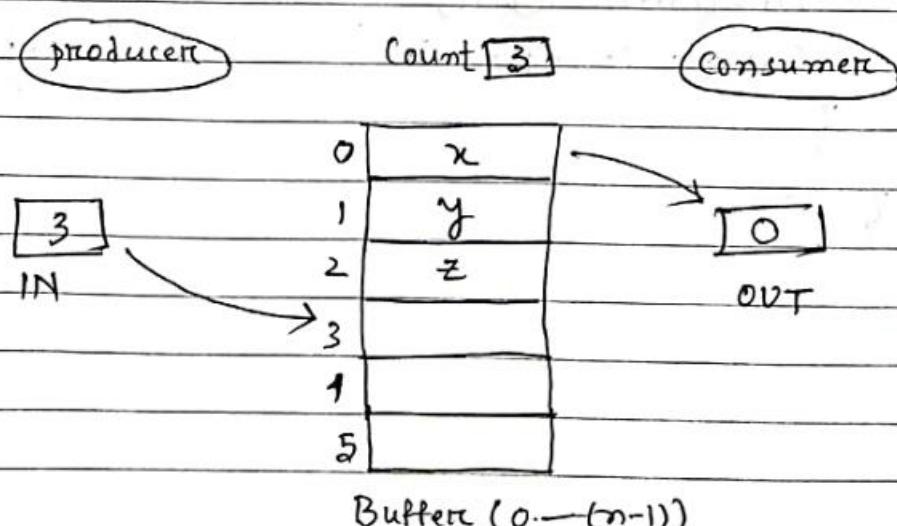
→ The pre-emption is just a temporary stop, the will come back and continue the execution.

→ If there is any possibility of solution becoming wrong by taking the pre-emption.



→ If any solution has the be deadlock, then the progress is not satisfied.

- Producer-consumer problem:



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$\text{IN} \rightarrow$ is a variable used by producer to identify the next empty slot in the Buffer.

$\text{OUT} \rightarrow$ is a variable used by consumer to identify the slot from whence it has to consume the item.

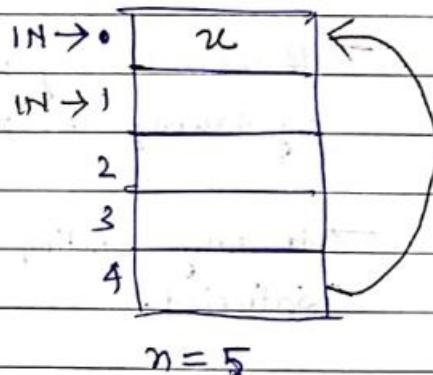
$\text{Count} \rightarrow$ is a variable used by consumer and producer to identify the no of items present in the Buffer at any point of time.

Conditions:-

- 1) \rightarrow When the buffer is full, the producer is not allowed to produce the item.
- 2) \rightarrow When the buffer is empty consumer is not allowed to consume the item.

• Producer Code \rightarrow

```
int count = 0;
void producer(void)
{
    int temp;
    while (TRUE)
    {
        produce-item (Item.p);
        while (count == N);
        Buffer[IN] = Temp;
        IN = (IN+1) MOD N;
        Count = Count + 1;
    }
}
```



count = 1

{ }

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• Consumers Code →

```
void consumer(void)
{
```

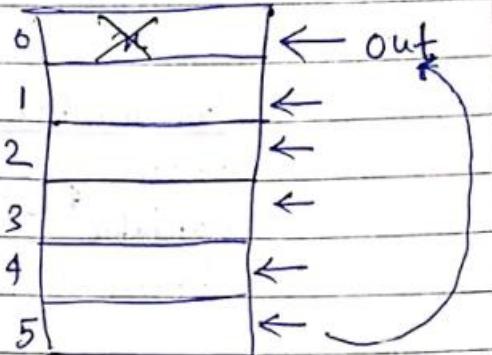
```
    int item c;
    while (TRUE)
    {
```

```
        while (count == 0);
        Item c = Buffer [OUT];
```

```
        OUT = (OUT + 1) MOD N;
```

```
        count = count - 1;
```

```
}
```



Count = X
0

• producer consumer problem Analysis:

⊗ producer

```
count = count + 1;
```

↓

I. LOAD Rp, m[COUNT];

II. INCR Rp

III. STORE m[COUNT], Rp

⊗ consumer

```
count = count - 1;
```

↓

I. LOAD Rc, m[COUNT]

II. DECR Rc

III. STORE m[COUNT], Rc

Analysis -

Race around condition

NOW,

0	x
1	y
2	z
3	
4	

P → I

Rp [3]

P → II

Rp [4]

C → I

Rc [3]

C → II

Rc [2]

✓ C → III

[2] ✓

✓ P → III

[4] ✓

{ different count value for }
{ producer and consumer }

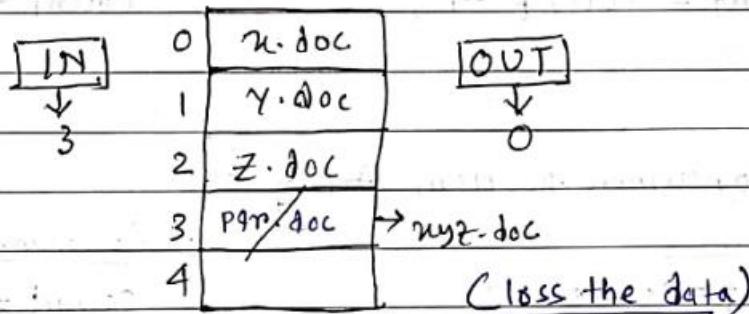
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- producer consumer problem Conclusion -

→ problems of Non-Synchronization.

Inconsistency :- The producer and consumer are not properly synchronized while sharing sharing the common variable COUNT. Hence it is leading inconsistency. No proper synchronization between producer and consumer.

- pointers - spoolers Domain problem -



IN → is a variable used by all processes to identify the next empty place in the spoolers directory.

OUT → is a variable used by only by printers to identify the slot from where it has to print the document.

Enter file -

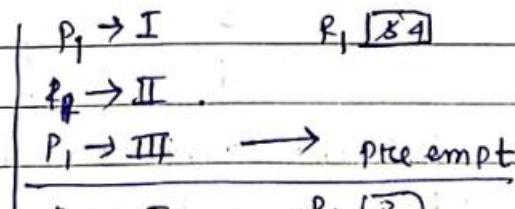
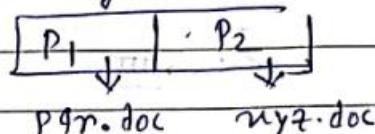
1) Load R_i , m [IN]

2) STORE $S_0[R_i]$, "file name".

3) INCR R_i .

4) STORE m [IN], R_i .

Analysis -



- problem of Non-synchronization:

→ Inconsistency: the producer and consumer are not properly synchronized while sharing the common variable COUNT.
Hence it is leading to inconsistency. No proper synchronization between producer and consumer.

→ Data Loss of Data: The process are not properly synchronized while sharing the common variable [IN], hence it is leading to loss of data.

→ Deadlock: if the process are not properly synchronized there is also a possibility of deadlock.

- Definitions:

- 1) Critical Section (CS): The portion of program text where shared variables are placed.

example - In producer/consumer problem :

$\boxed{\text{count} = \text{count} + 1}$ → CS

- 2) Non-Critical section: The portion of program text where the independent code of the process will be placed.

- 3) Race Condition: The final value of any variable depends on the execution sequence of process. This condition is called as race condition.

- The critical Section problem - Structure -

do

{

entering section)

critical section .

exit section)

reminder section / MCS .

? while (TRUE) ;

- Synchronization conditions :-

- 1) MUTUAL EXCLUSION: No two process may be simultaneously present inside the critical section at any point of time. Only 1 process is allowed into critical section at any point of time.
- 2) progress: No process running outside the critical section should block the other interested process from entering into c-s when the c-s is free.
- 3) Bounded Waiting: No process should have to wait forever from entering into critical section. There should be a bound on getting chance to enter into critical section. If Bounded waiting is not satisfied, then it is possible for starvation.

- Solution Types:

- 1) Software Type :-

- a. Lock variables.

- b. strict Alternation (or) Dekker's Algorithm.

- c. peterson's Algorithm.

- 2) Hardware type :-

- a. TSL Instruction set (Test & set lock)

- 3) O.S Type :-

- a. Counting Semaphores.

- b. Binary semaphores.

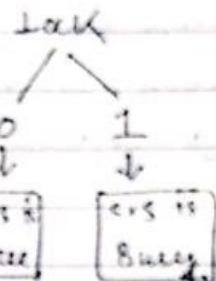
- 4) programming language compiler support type :-

- a. Monitors.

✓ • LOCK variables: $\rightarrow [M \cdot E \rightarrow X, \text{Program} \rightarrow \checkmark, B \cdot W \rightarrow X]$.

Entry section -

- I. Load $R_i, m[\text{lock}]$.
- II. $\text{CMP } R_i, \#0$.
- III. JNZ to step ① .
- IV. $\text{STORE } m[\text{lock}] \#1$
- V. $\boxed{\text{C.S}}$
- VI. $\text{STORE } m[\text{lock}], \#0$.



let, $\text{lock} \Rightarrow 0 \times 1$

$R \cdot A \quad \boxed{P_1 \quad P_2}$

$P_1 \rightarrow I \quad R \boxed{0}$.

$P_1 \rightarrow II$

$P_1 \rightarrow III \rightarrow \text{preempt.}$

$P_2 \rightarrow I \quad R \boxed{0}$

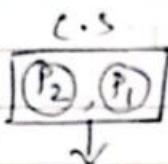
$P_2 \rightarrow II$

$P_2 \rightarrow III$

$P_2 \rightarrow IV, \overline{X}$

$P_1 \rightarrow IV,$

$P_1 \rightarrow \overline{X}$.



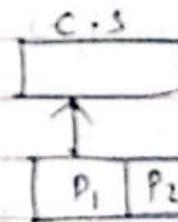
M-E-X
✓ (Mutual exclusion
not satisfy) - \times

Entry section -

- I. LOAD $R_i, m[\text{lock}]$
- II. $\text{CMP } R_i, \#0$.
- III. JNZ to step ① .
- IV. $\text{STORE } m[\text{lock}], \#1$.
- V. $\boxed{\text{C.S}}$? critical section
- VI. $\text{STORE } m[\text{lock}], \#0$.

} entry section

} reminder
locking



$\xrightarrow{\text{lock}=0}$

$P_2 \rightarrow I \quad R \boxed{0}$

$P_2 \rightarrow II, III$

$P_2 \rightarrow IV \rightarrow \text{preempt}$

$P_1 \rightarrow I \quad R \boxed{1}$

$P_1 \rightarrow II, III$

✓ processes are satisfy ✓

✓ Bounded Waiting - \times

(if processes are finite)

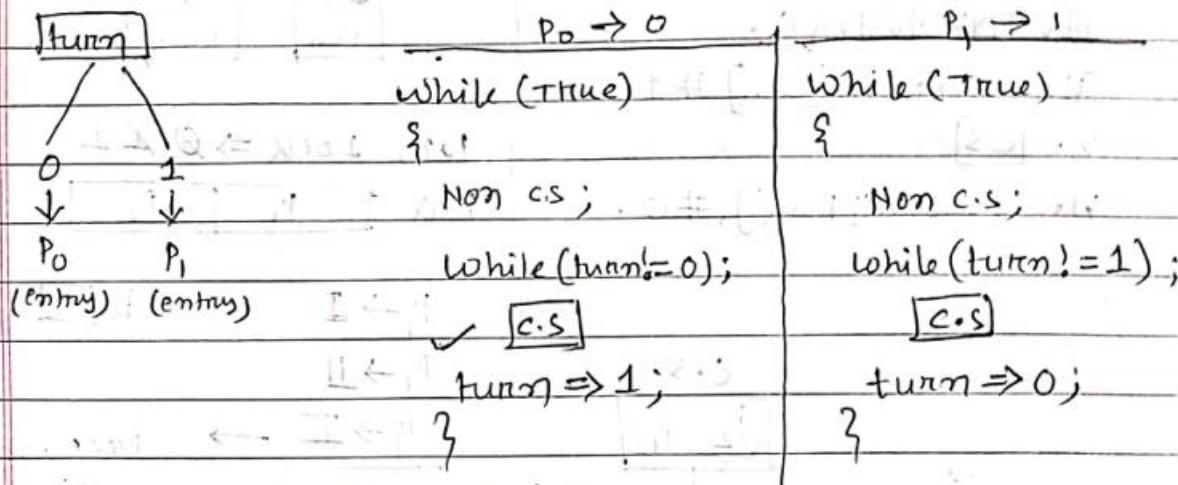
then B-W satisfy

otherwise not satisfy)

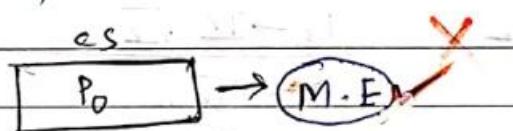
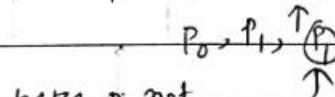
(here no. of processes infinite)

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- strict Alternation (or) Dekker's Algorithm :- $M \cdot E \rightarrow V, P \rightarrow X, B \cdot W \rightarrow V$
- process takes turn to enter into critical section.
- solution will work for 2-process.

 (P_0) (P_1) 

Analysis (for M.E, P, B.W) :-

 $turn \Rightarrow 0$ for finite process $\rightarrow B.W$ ✓ $turn \Rightarrow \emptyset, 1, 0$ here P_0 notinterested to go c.s but for $turn=0$ P_1 can't go cs. (P_0 stored P_1) \rightarrow progress ✗• 2nd definition of progress :-

which process will go next into c.s is decided by only those processes who want to go into c.s. In this decision, the process in the ready section and the process which is not interested to go into the c.s should not take participation.

Date _____

✓ peterson's Algorithm :- ($M \rightarrow \checkmark, P \rightarrow \checkmark, B-W \rightarrow \checkmark$)
 (2 process solution)

define N 2

define TRUE 1

define FALSE 0

int turn;

int interested[N];

void enter-Region(int process)

{

1. int other;

2. other = [1 - process];

3. interested[process] = TRUE;

4. turn = process;

5. while (turn == process && interested[other] == TRUE);

CS;

{

void leave-Region(int process)

{

interested[process] = false;

{

Initially -

{ interested[0] = false.

P₀

{ interested[1] = false.

P₁

↓ ↓

other

other

0

Analysis :-

(next page)

<u>P₀</u>	<u>P₁</u>
1.	1. →
2. Other $\rightarrow 1 - 0 = 1$	2. Other = 0
3. Interested[0] = True.	3. Interested[1] = True.
4. turn = 0	4. turn = 1
5. ↓ CS [P ₀]	5. Loop ↓ CS [P ₀]

{ So, M.F = ✓.
progress = ✓
Bounded waiting = ✓

* peterson practise question :-

Code -

void enter-Region()

{

1. int other ;

2. other = ! process ;

3. Interested[process] = True;

4. turn = process ;

5. while(turn = = process && Interested[other] = = True);

6. CS ;

7

Q. If both the process P₀ and P₁ are trying to enter in CS at same time, then which process will go into CS first.

a. The process which executes statement 2 first.

b. " " " " " 3. b.

c. " " " " " " 4. "

d. We cannot say.

→ Ans → (c).

<u>P₀</u>	<u>P₁</u>
1. →	1. →
2. Other = 1	2. Other = 0
3. Interested[0] = True.	3. Interested[1] = True.
4. turn = 0;	4. turn = 1;
5. ↓	6. S

Date _____

- TSL Introduction: $M.E \rightarrow \checkmark, P \rightarrow \checkmark, B.W \rightarrow X$

→ TSL flag Register flag :- Copies the current value of flag into register and store the value of 1 into the flag in a single atomic cycle, without any preemption.

→ Disabling the interrupt is at H/W level that is why it is called H/W approach.

→ Entry section -

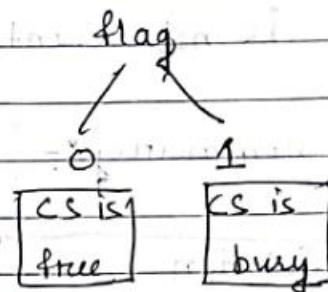
* 1) $TSL R_i, m[\text{flag}]$

2) $\text{cmp } R_i, \# 0$

3) JNZ to step ①

4) $C.S$

5) STORE $m[\text{flag}], \# 0$



Analysis -

$$\text{flag} = 0 \ 1 \ 1$$

$$RQ = [P_1 \ P_2]$$

$$P_1 \rightarrow I$$

$$R_1 [0]$$

$$P_1 \rightarrow II$$

$$P_1 \rightarrow III$$

$$P_1 \rightarrow IV \rightarrow \text{pre-empt}$$

$$\boxed{P_1} \stackrel{\text{CS}}{=}$$

$$M.E \rightarrow \checkmark$$

$$P_2 \rightarrow I$$

$$R_2 [1]$$

$$P_2 \rightarrow II, III$$

$$[P_1 \ | \ P_2]$$

$$\text{flag} = 0 \ 1 \ 1$$

$$CS \boxed{P_1}$$

$$P_1 \rightarrow I \quad R_1 [0] \rightarrow \text{preemptive}$$

$$(P_2 \rightarrow I, II)$$

$$\text{progress} \rightarrow \checkmark$$

where no. of process infinite so, $B.W \rightarrow X$,
(Boling, waiting)

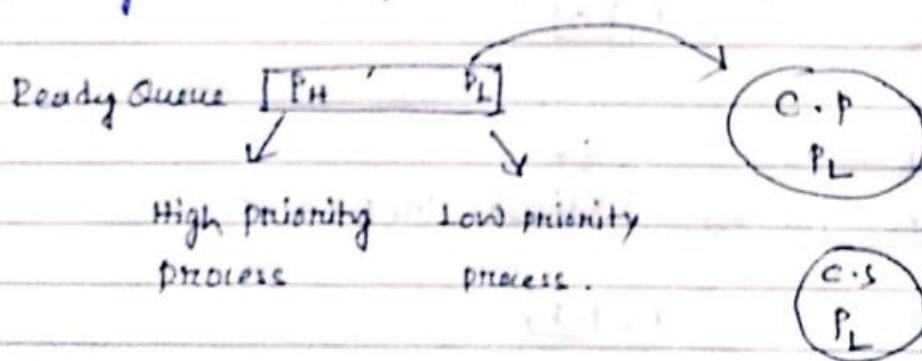
* Some Important points :- (TSL)

- In Lock variables mutual exclusion is not satisfied because loading and storing were not done in same step.
- progress is satisfied in TSL.
- Bounded waiting is not satisfied Because no. of processes is not countable.

* Summary :-

Solution	Mutual exclusion	progress	Bounded waiting
Lock variable	X	✓	X
Strict Alteration	✓	X	✓
Peterson's Solution	✓	✓	✓
TSL	✓	✓	X

* Priority Inversion problem -



→ P_L is currently executing CS code. Now suddenly P_H comes, then we are going to pre-empt P_L. P_H is even though P_H is scheduled by CPU but it cannot enter in CS because it is locked by P_L.

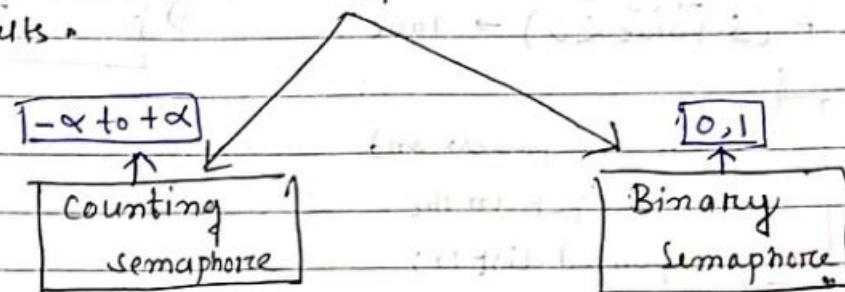
↓
Problem is called Live-Lock

Solution → Priority Inversion / Inheritance.

→ This allows that P_1 can continue its execution in c.s and then leave.

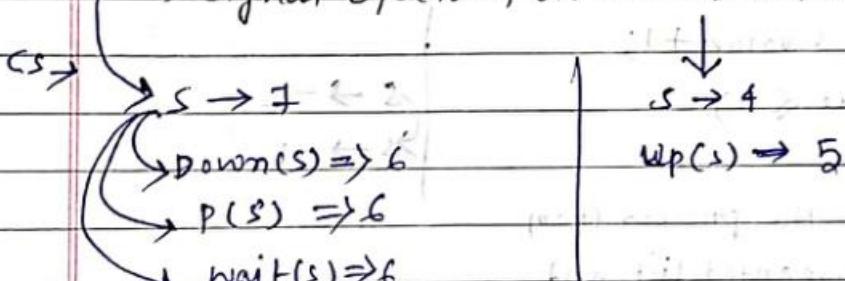
* Semaphore:

→ is an integer variable which is used by various process in a mutual exclusive manner to achieve synchronization. The proper/ improper usage of semaphore will give improper results.



Two different operations performed on semaphore variable are -

- 1) Down Operation on p() or wait().
- 2) signal Operation on v() or release() or up().



$$bs \Rightarrow 1$$

$$\text{down}(bs) \Rightarrow 0$$

$$bs \Rightarrow 0$$

$$\text{up}(bs) \Rightarrow 1$$

Counting Semaphore -

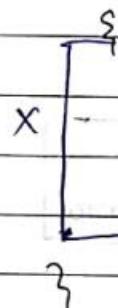
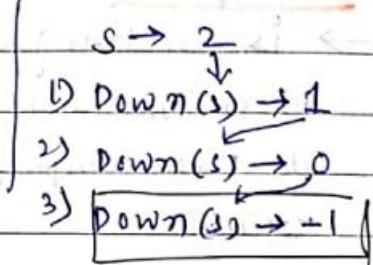
→ Down operation -

Down operation (Semaphore s)

{

$$s.value = s.value - 1;$$

If ($s.value < 0$) → True



Block the process and

Place the PCB in the

Suspended list();

→ Up operation - (always successful)

Up operation (Semaphore s)

{

$$s.value = s.value + 1;$$

If ($s.value \leq 0$)

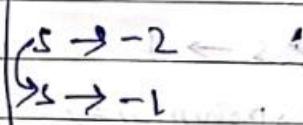
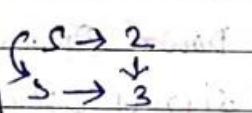
{

Select the process from

Suspended list and

wakeup();

{



{

→ After performing the down operation, if the process is getting suspended, then it is called unsuccessful down operation.

→ After performing the down operation, if the process is not getting suspended, then it is called successful down operation.

Date / /

- If it is successful down operation, then only the process will continue the execution. The down operation on the counting Semaphore is successful only if the semaphore value is ≥ 1
- There is no unsuccessful up operation, the up operation is always successful because it does not suspend any process.
- If $s = +6$ it means we can perform 6 successful down operations.
- If $s = -6$ it means that there are already 6 suspended processes.

* Question -

Consider a system where a counting Semaphore value is initialized to +17.

The various Semaphore Operations like -

23P, 18V, 16P, 14aV, 1P are performed.

What is the final value of semaphore?

$$\Rightarrow 17 - 23 + 18 - 16 + 14 - 1$$

$$\Rightarrow 9 - 6 + 2 + 13$$

$$\Rightarrow 7,$$

 Binary Semaphore: $\begin{matrix} \nearrow 0 \\ \searrow 1 \end{matrix}$

→ Down Operation

Down (Semaphore s)

{

if ($s.value == 1$)

$s.value = 0;$

else

{

Block the process and
place the PCB in the
Suspended list();

}

}

→ Up Operation

up (Semaphore s)

{

if (Suspended list() is empty,
 $s.value = 1;$

else

{

Select a process from
Suspended list and Wakeup();

?

→ After performing down operation if the process is getting suspended then it is called unsuccessful down operation.

→ After performing down operation, if the process not getting suspended then it is called successful down operation.

→ The down operation on the Binary semaphore is successful only if the semaphore value is 1.

→ If it is successful down operation, then only the process will continue the execution.

→ There is no unsuccessful up operation. The up operation will be always successful. The process performing the up operation will definitely continue the execution.

✓ Question : (i) (ii) (iii)

Each process $P_i = 1 \text{ to } 9$ executes the following code -

repeat

$p(\text{mutex});$

c.s

$v(\text{mutex});$

forever

\Rightarrow The initial value of Binary Semaphore
 $\text{mutex} = 1.$

The process P_{10} execute the following code .

\Rightarrow What is the maximum no. of process may be present inside the CS at any point of time ?

repeat

$v^{P_{10}}(\text{mutex});$

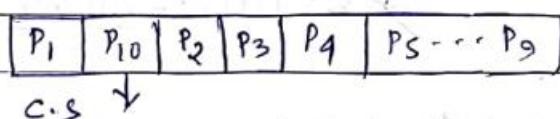
c.s

$v(\text{mutex});$

forever

$(\text{mutex} \Rightarrow 1)$

$\text{mutex} \rightarrow 1 \otimes 1$



\rightarrow Ans : 10 process . ✓

$\Rightarrow p(\text{mutex});$ then find ?

\rightarrow $\text{mutex} = 1 \otimes 1$

P_1	P_{10}	P_2
-------	----------	-------

$\downarrow \text{c.s}$ $\downarrow -3(P)$

\rightarrow Ans : 3 process . ✓

$\Rightarrow p(\text{mutex});$ then find ?

$\text{mutex} = 1 \otimes 1$

P_1

$\downarrow \text{c.s}$

\rightarrow Ans : 1 process .

• GATE-2003 Question :-

Consider the two concurrent process 'P' and 'Q' executing their respective codes.

process 'P' code
while (TRUE)
 {

 ① w: p(T) ¹
 printf('0');
 printf('0');

 ② x: v(s) ⁰
 {

process 'Q' code
while (TRUE)
 {

 ③ y: p(s) ¹
 printf('1');
 printf('1');

 ④ z: v(T) ¹
 {

what should be the
semaphore operations on
w,x,y,z respectively. And
what should be the initial
value of Binary semaphore
's' and 'T' in order to get the
output as 01100100 ...

✗ w = p(T), x = v(T), y = p(s),
z = v(s), s = T = 1;

✗ w = p(T), x = v(T), y = p(s),
z = v(s), s = 1, T = 0

✗ w = p(T), x = v(s), y = p(s), z = v(T), s = 1, T = 1;

✓ w = p(T), x = v(s), y = p(s), z = v(T), s = 0, T = 1

→ P & Q ...

• Question :- process code same.

which of the following will ensure that the output string
never contains a substring of the form 0ⁿ0 or 1ⁿ1 where
n is odd.

(a) w = p(s), x = v(s), y = p(T), z = v(T), s = T = 1;

(b) w = p(s), x = v(T), y = p(T), z = v(s), s = T = 1;

✗ (c) w = p(s), x = v(s), y = p(s), z = v(s), s = T = 1;

(d) w = p(s), x = v(T), y = p(s), z = v(T), s = T = 1;

S →

→ 00110011 ...

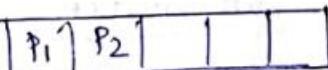
- producer & consumer problem, solve with the help of Semaphore.

semaphore $s = 1$

semaphore $F = n$

here $n =$ is of size of buffer

Semaphore $E = 0$



C.S.

* void producer()

{
while(T)
{

produce()

wait/sdown(E) -

wait(s)/down(s)

append()

signal(s)/up(s)

signal(F)/up(F)

?

}

Let $s = \times 0 X 0 1$

$E = \cancel{S} \cancel{X} 3$

$F = 0 X 2$

* void consumer()

{

while(T)

{

wait(F)/down(F)

wait(s),

take c)

signal(s)/up(s),

signal(E)

? free(c)

?



$s = X 0 1$

$E = \cancel{S} \cancel{X} 4$

$F = 0 Z 1$

• READ-WRITE PROBLEM:

(Solve by semaphore)

(here using red 3 semaphore)

for writer

I. $\text{wait}^{(1)}(\text{wrt})$

$\text{wrt} = \emptyset 0$

II. write operation

III. $\text{signal}(\text{wrt})/\text{up}(\text{wrt})$.

for read

I. $\text{wait}^{(1)}(\text{mutex})$

I. $\text{mutex} = X \emptyset 1$

II. $\text{readcount}++$

II. $\text{readcount} = \emptyset 0$

III. If ($\text{readcount} == 1$)

III. $\text{wrt} = \emptyset_1$ (no writer can enter
in critical section :).

wait(wrt)

IV. $\text{signal}(\text{mutex})$

on

V. read operation.

VI. $\text{wait}(\text{mutex})$

VII. $\text{readcount}--$

VIII. If ($\text{readcount} == 0$)

signal(wrt)

IX. $\text{signal}(\text{mutex})$.

* At a time more than one read operation done in critical section.

* At a time only one write operation ~~can~~ done in C.S.

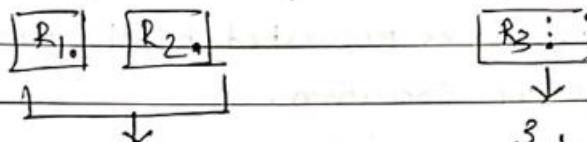
DEADLOCK

- Definition:- If two or more processes are waiting for some event to occur, which never happens, the processes are said to be involved in deadlock.
- Resource Allocation Graph (RAG):

→ Basics:- process will be represented with circle.

(P₁) (P₂)

Resources will be represented with rectangle.



single instance

* Requesting edge

(P₁)

process P₁ is requesting
1 instance of R₁

[R₁]

(P₁)

one instance of 'R'₁
is allocated to 'P'₁.

[R₁]

(P₂)

process P₂ is requesting
for 2 instances of R₂.

[R₂]

(P₂)

Two instances of 'R'₂
is allocated to 'P'₂.

[R₂]

→ Resource request and Resource allocation will be represented in the represented in the resource allocation graph (RAG).

$$(L \cdot A \cdot G) = G_G(V, E)$$

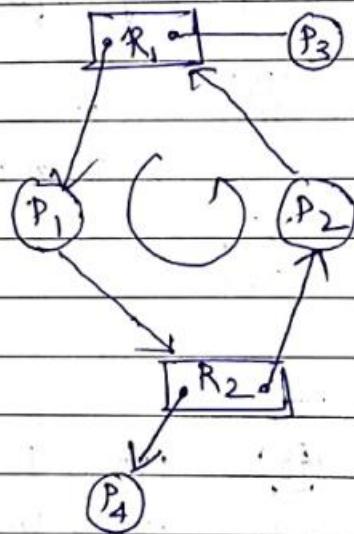
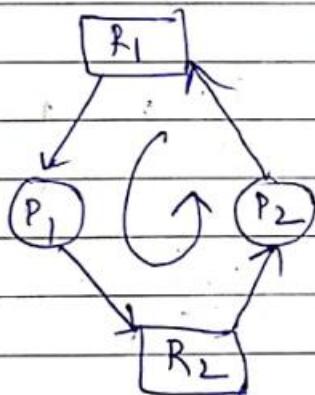
V → processes & resources. (vertex)

E → Requesting and Allocation edge

• Resource Request and Release life cycle.

→

- 1) The process will request for the resource. $(P_1) \rightarrow [R_1]$
- 2) O.S validates the request of the process.
- 3) If the request made by process is valid, the O.S checks for availability of the resource.
- 4) If the resource is freely available, it will be allocated to the process, otherwise process has to wait.
- 5) If all the resources requested by the process are allocated then it will go into execution.
- 6) Once the execution of the process completed, then the process will release all the resources.



Deadlock is involved in
(RAGI)

No Deadlock even if

cycle is present.

Deadlock Q-1

Consider a system with n processes and 6 tape drives. If each process requires 2 tape drives to complete their execution, then what is the maximum value of n which ensures deadlock free operation?

→ $R \Rightarrow 6$ (Tape)

5

P → need {2}

* $n-1$

P ₁	P ₂	P ₃	P ₄	P ₅	P ₆
X ₂	1	1	1	1	1

 $m = 1$

↳ execution complete.

first, $m = 6$ (deadlock)if $m = 5(P)$ then it will be deadlock free operation.

• Deadlock Q-2:

Consider a system with 3 processes, where each process requires 2 tape drives to complete their execution, then what is the minimum number of resources required to ensure deadlock free execution. ①

→ here, process = 3, $m = 3$, $R = ?$

P →	P ₁	P ₂	P ₃
R →	1	1	1

$$R = 3 + 1 = 4$$

minimum number of resources required to ensure deadlock free execution are 4(R).

• Deadlock Q-3:

consider a system with m processes and 6 tape drives. If each process require 3 tape drives to complete their execution. What is the maximum value of m which ensures deadlock free execution.

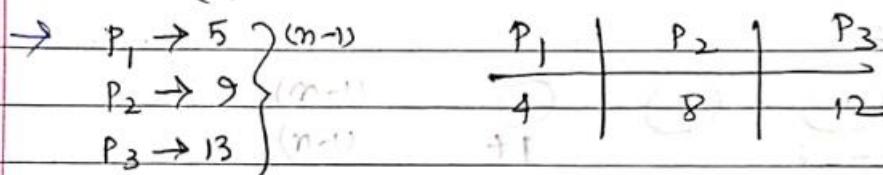
P ₁	P ₂	P ₃
2	2	2
3	3	X

 $R \rightarrow 6$

$n \rightarrow ?$ so, m will be 2(P).
need(3)

• Deadlock Question - 1 :

Consider a system with 3 processes P_1, P_2, P_3 . The peak demand of every process is $5, 9, 13$ respectively for the Resource (R). Then for what minimum no of resources, the execution is deadlock free. (25)



$$R \rightarrow 4 + 8 + 12$$

$$= 24$$

+ 1

$$R = 25 \checkmark$$

• Deadlock characteristic introduction -

(Behaviour of Deadlock)

(I) Mutual exclusion.

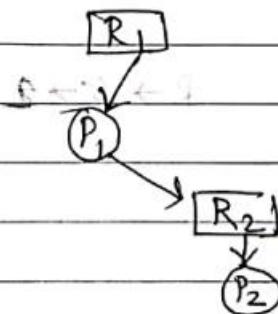
(II) Hold and wait.

(III) NO - Preemption.

(IV) circular wait.

1. Mutual exclusion :- The resource has to be allocated to only one process or it is freely available. There should be a one to one relationship between the resource and process.

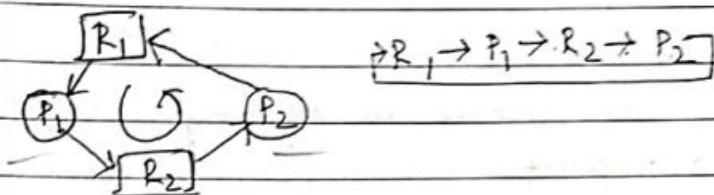
2. Hold and wait :- The process is holding some resources and waiting on some other resource simultaneously.



3. No-preemption :- The resource has to be voluntarily released by the process after the completion of execution. It is not allowed to forcefully pre-empt the resources from process.

4. Circular wait :-

The processes are circularly waiting on each other for the resources.



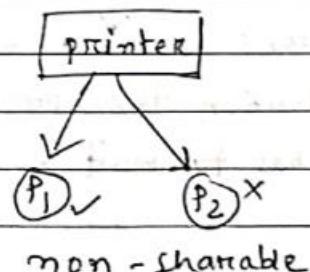
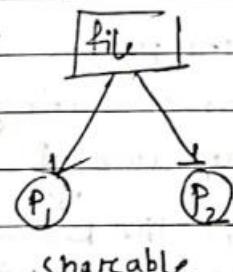
All 4 MUST occur simultaneously, Then Definitely Deadlock is there.

All the above 4 conditions are not truly independent because circular wait includes hold & wait.

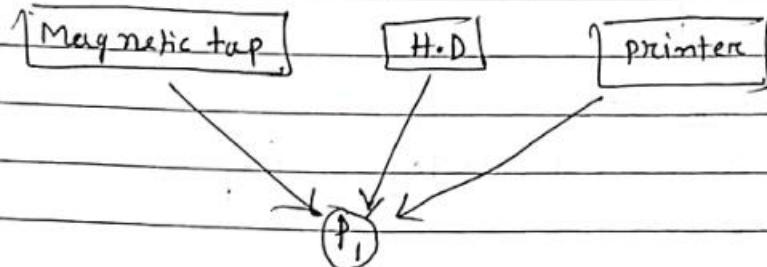
Deadlock prevention Schemes :

(1) Deadlock prevention: It is not always possible to dissatisfaction mutual exclusion because of shareable and non-shareable resource.

→ If there are shareable resources then mutual exclusion can be dissatisfaction and if they are non-shareable resource then Mutual exclusion cannot be dissatisfaction.



(2) Hold and wait :- (i) Allocate all the resources required by the process before start of execution.



→ Low device utilization.

(ii) The process should release all existing resource before making new request.

$$P_1 \rightarrow 100 R$$

$P_1 \rightarrow 100 R$	$P_1 \leftarrow 85 R$
$P_1 \rightarrow 100 R$	$P_1 \leftarrow 40 R$
$P_1 \rightarrow 100 R$	$P_1 \leftarrow 100 R$

↓
(starvation)

(3) No preemption : The process ' P_1 ' is requesting for resource ' R_1 '. $P_1 \rightarrow [R_1]$

If resource R_1 is free
then it will be allocated
to process ' P_1 '.

$$[R_1] \rightarrow P_1$$

The resource R_1 is not free.
and it is allocated to process
 P_2 .

$$[R_1] \rightarrow P_2$$

If the process P_1 is in the
execution then process
 P_1 has to wait.

The process P_2 is not executing
and is waiting for the other
resource R_2 .

↓
Preempt the resource R_1 from
process P_2 and Assign it to process
 P_1 .

(4) Circular Wait : The resources will be assigned with a numerical numbers. The process can request for the resource only in increasing order of enumeration.

$R_1, R_2, R_3, \dots, R_{12}$

$P_1 \rightarrow R_5 \checkmark$

$P_1 \rightarrow R_7 \checkmark$

$P_1 \rightarrow R_9 \checkmark$

$\boxed{P_1 \rightarrow R_6} \times$

$P_1 \rightarrow R_9 \checkmark$

✓ Bankers Algorithm :

- Deadlock Avoidance (BANKERS ALGORITHM)

Total Resources \Rightarrow

A	B	C
10	5	7

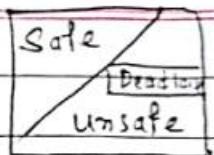
Instance

	Max Need			current Allocation			Remaining Need			Current Available		
	A	B	C	A	B	C	A	B	C	A	B	C
(1) $P_0 \rightarrow$	7	5	3	0	1	0	3	4	3	3	3	2
X $(P_1 \rightarrow)$	3	2	2	2	0	0	1	2	2	5	3	2
(2) $P_2 \rightarrow$	9	0	2	3	0	2	6	0	0	7	4	3
X $(P_3 \rightarrow)$	2	2	2	2	1	1	0	1	1	7	5	3
X $(P_4 \rightarrow)$	4	3	3	0	0	2	4	3	1	15	5	5
				7	2	5				10	5	7

$\boxed{P_1, P_3, P_0, P_2, P_4}$

safe sequence

• Deadlock Avoidance Conclusion :



* Remaining need = Max - current Allocation.

→ If we can satisfy the remaining need of the process with the current available resources, then system is said to be in the safe state otherwise, the system is said to be in the unsafe state.

→ If the system is in the unsafe state, then it is possible for deadlock.

→ The order in which we satisfy the remaining need of all the process is called safe sequence.

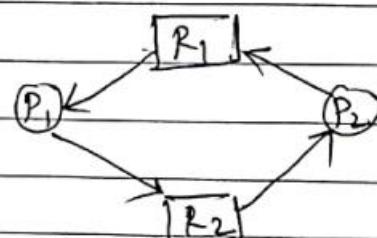
→ The safe sequence may not be unique. we can have multiple safe sequence.

→ Deadlock Avoidance is more restrictive than deadlock prevention.

→ The unsafe state purely depends on the behaviour of the process.

• Deadlock Detection :

(i) All the resources are of single instance type.



If all the resources are of single instance type, then cycle in the RAG is necessary and sufficient condition for occurring of

deadlock. If all the resources are of single instance type, then cycle in the RAG is just a necessary condition but not sufficient condition for occurring of deadlock.

(ii) The resources are of multiple instance type.

total resources

A	B	C
7	2	6

Process	Current Allocation			Remaining need			Current Available		
	A	B	C	A	B	C	A	B	C
P0	0	1	0	0	0	0	0	0	0
P1	2	0	0	2	0	2	0	1	0
P2	3	0	3	0	0	0	3	1	3
P3	2	1	1	1	0	0	5	1	3
P4	0	0	2	0	0	2	7	2	4
	7	2	6				7	2	6

$\rightarrow P_0 \rightarrow P_2 \rightarrow P_1 \rightarrow P_3 \rightarrow P_4 \rightarrow$ safe sequence.

* What happens if P2 is demanding for 001 resources?

total resources

A	B	C
7	2	6

Process	Current Allocation			Remaining need			Current Available		
	A	B	C	A	B	C	A	B	C
P0	0	1	0	0	0	0	0	0	0
P1	2	0	0	2	0	0	0	1	0
P2	3	0	3	0	0	1			
P3	2	1	1	1	0	0			
P4	0	0	2	0	0	2			
	7	2	6						

deadlock

$(P_0 \rightarrow)$

$P_1, P_2, P_3, P_4 \rightarrow$ deadlock.

• Deadlock Recovery :-

i) Killing the process :-

(a) Killing all the processes involved in the deadlock.

✓ (b) Kill one by one till the deadlock is cracked / resolved.

i) low priority process.

ii) % of process completion $P_1 \rightarrow 95\%$ $P_2 \rightarrow 5\%$ X

iii) no of resources the process is holding.

$\checkmark P_1 \leftarrow 20R$ $P_2 \leftarrow 2R$

iv) no of resources the process is requesting.

$P_1 \rightarrow 1R$ $P_2 \rightarrow 20R$ ✓

ii) Resource pre-emption: The resources from the process which are involved in the deadlock will be preempted and the pre-empted resources will be allocated to other process so that there is a possibility of recovering the system from deadlock.

→ If resource pre-emption is followed, there is a possibility of starvation.

1) selection of victim

2) Roll back

3) starvation

Date / / CPU SCHEDULING - (numerical)

PBR • Basic Introduction:

Where? → In the ready state to running.

Who? → Short term scheduler / CPU scheduler.

When? →

- 1) Run → termination, Run → wait, Run → Ready.
- 2) Wait → Ready.
- 3) New → Ready.

• Functionality: To allocate the CPU to the process.

• GOAL: 1) Increase the CPU utilization and throughput of the system.

2) Minimize the Average waiting time, average turn around time of the process.

PBR • Some Basic terms:

① Arrival time (A.T) → The time when the process is arrived into ready state is called as Arrival time.

② Burst time (B.T) → The time is required by the process for its execution is called as Burst time of the process.

③ Completion time (C.T) → The time when the process is completed or completes its execution is called completion time.

④ Turn around time $\overset{(C.T-A.T)}{\rightarrow}$ The time difference between completion time and arrival time is called turn around time of process.

$$T.A.T = C.T - A.T$$

⑤ Waiting time (W.T) → The difference between T.A.T and B.T

$$W.T = T.A.T - B.T$$

⑥ Response time (R.T) → The difference between 1st response and arrival time is called as Response time.

PBR

- First Come First Served (FCFS) Scheduling:

selection criteria: Arrival time.

Mode: Non-pre-emptive.

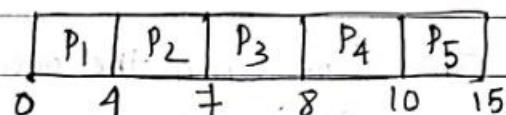
$$\begin{aligned} T.A.T &= C.T - A.T \\ &= W.T + B.T \end{aligned}$$

- Question-1:

process.no	A.T	B.T	C.T	T.A.T	W.T
1	0	4	4	4	0
2	1	3	7	6	3
3	2	1	8	6	5
4	3	2	10	7	5
5	4	5	15	11	6

$$W.T = T.A.T - B.T$$

Guantt chart



$$\text{Average waiting time} = \frac{0+3+5+5+6}{5}$$

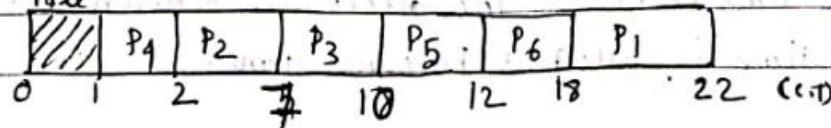
$$\begin{aligned} &= \frac{19}{5} \\ &= 3.8 \text{ ms.} \end{aligned}$$

- Question-2:

P.NO	A.T	B.T	C.T	T.A.T	W.T
1	6	4	22	16	12
2	2	5	7	5	0
3	3	3	10	7	4
4	1	1	2	1	0
5	4	2	12	8	6
6	5	6	18	13	7

Guantt chart

idle



$$\text{average waiting time} = \frac{12+4+6+7}{6}$$

$$= \frac{29}{6} = 4.8$$

Date _____ / _____ / _____

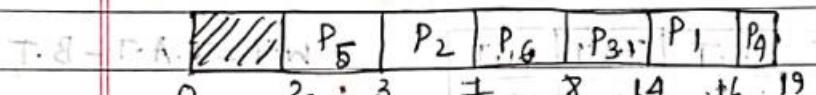
- * If the Arrival time of the process are same/matching, then schedule the process which has lowest process id.

• Question no-3 :

P.NO	A.T	B.T	C.T	T.A.T	W.T	
1	8✓	2	16	8	6	
2	3✓	4	7	4	0	
3	7✓	6	14	7	1	
4	10✓	3	19	9	6	
5	2✓	1	3	1	0	
6	3✓	1	8	5	4	

$T.A.T = C.T - A.T$
 $W.T = T.A.T - B.T$

Gantt chart



$$\text{So, average waiting time} = \frac{6+1+6+9}{6}$$

$$= \frac{17}{6}$$

$$= 2.83 \text{ ms.}$$

• Question no-4 :

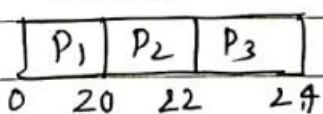
(a)

P.NO	A.T	B.T	W.T
1	0	20	0
2	1	2	19
3	2	2	20

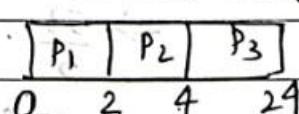
(b)

P.NO	A.T	B.T	W.T
1	0	2	0
2	1	2	1
3	2	20	2

Gantt chart

CONVOY
Effect

Gantt chart



average waiting time,

$$\frac{0+19+20}{3} \rightarrow 13$$

average waiting time,

$$\frac{0+1+2}{3} = 1$$

^{RB²} In FCFS, if the 1st process is having large burst time then it will have drastic effect on average waiting time of all the processes. This effect is called convoy Effect.

^{R.B.F} ✓ Shortest job first (SJF) scheduling:

Solution criteria:- Burst time

Mod:-

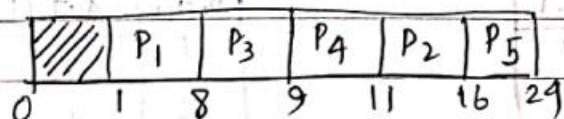
- Non-pre-emptive.
- * → Pre-emptive. * (Important for gate)

• Question 2:- SJF Non pre-emptive.

P.NO	A.T	B.T	C.T	T.A.T	W.T
v 1	1	7	3	7	0
v 2	2	5	16	14	9
v 3	3	1	9	6	5
v 4	4	2	11	7	5
v 5	5	8	24	19	11

$W.T = T.A.T - B.T$

Gantt chart



Average T.A.T. (Turnaround time),

$$\Rightarrow 7 + 14 + 6 + 7 + 19$$

5

$$\Rightarrow \frac{53}{5}$$

Average W.T (Waiting time),

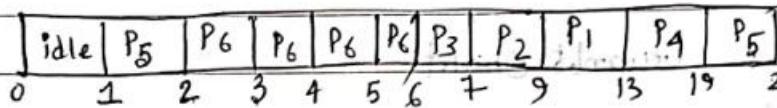
$$= \frac{0+9+5+5+11}{5} \Rightarrow \frac{30}{5} \Rightarrow 6$$

Date _____ / _____ / _____

- Question - 2 :- SJF Non pre-emptive.

P.NO	A.T	B.T	C.T	T.A.T	W.T
✓ 1	3	4	13	10	6
✓ 2	4	2	9	5	3
✓ 3	5	1	7	2	1
✓ 4	2	6	19	17	11
5	1	8	26	25	17
✓ 6	2	4	6	4	0

Gantt chart



Average T.A.T = $\frac{10+5+2+17+25+4}{6}$
 $= \frac{63}{6} \rightarrow 10.5$

Average W.T = $\frac{6+3+1+11+17+0}{6}$
 $= \frac{38}{6}$
 $= 6.33$

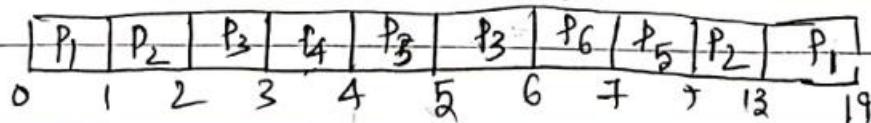
- Question - 1 :- SJF pre-emptive.

* SJF is also called SRTF.

SRTF \Rightarrow shortest Remaining Time first.

P.NO	A.T	B.T	C.T	T.A.T	W.T
1	0	7	19	19	12
2	1	5	13	12	17
3	2	3	6	4	1
4	3	1	4	1	0
5	4	2	9	5	3
6	5	1	7	2	1

Gantt chart :-



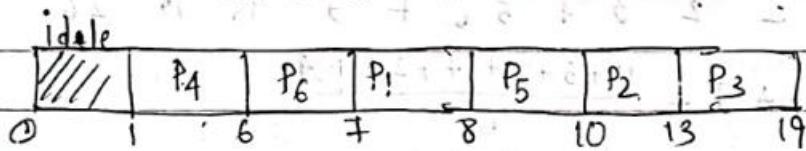
Date _____ / _____ / _____

* Note:- If the Burst time of the process are same/matching then schedule the process which has lowest Arrival time.

• Question: SJF → Non-pre-emptive.

P.NO	A.T	B.T	C.T	T.A.T	W.T
1	6	1	8	2	1
2	3	3	19	10	7
3	4	6	19	15	9
4	1	5	6	5	0
5	2	2	10	8	6
6	5	1	7	2	1

Gantt Chart



$$\text{avg T.A.T} = \frac{2+10+15+5+8+1}{6} \Rightarrow \frac{42}{6} = 7$$

$$\text{avg W.T} = \frac{1+7+9+6+1}{6} \Rightarrow \frac{24}{6} = 4$$

• Question:- SJF pre-emptive.

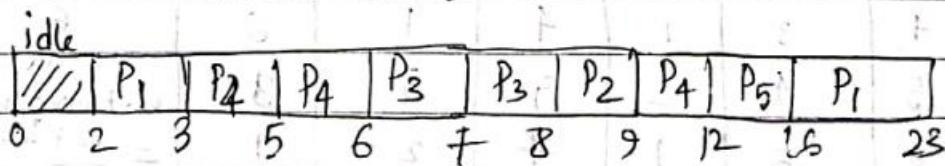
$$W.T = T.A.T - B.T$$

P.NO	A.T	B.T	C.T	T.A.T	W.T
1	2	8	23	21	13
2	7	1	9	2	1
3	6	21	8	2	0
4	3	6	12	9	3
5	5	4	16	11	7

Avg T.A.T = $\frac{21+2+7+0+3+7}{5} = 9$

Avg W.T = $\frac{13+1+0+3+7}{5} = \frac{24}{5} = 4.8$

Gantt chart



Date _____ / _____ / _____

P.B.R

- GATE 2011 Question :- SJF pre-emptive.

P.NO	A.T	B.T	C.T	T.A.T	W.T
1	0	9	13	13	4
2	1	4	5	4	0
3	2	9	22	20	11

Gantt chart

P ₁	P ₂	P ₃	P ₄	P ₅
0	1	2	5	13 22

$$\text{avg T.A.T} = \frac{13+4+20}{3} \Rightarrow \frac{37}{3} \Rightarrow 12.33$$

$$\text{avg W.T} = \frac{15}{3} = 5$$

- GATE 2004 :- SJF pre-emptive.

P.NO	A.T	B.T	C.T	T.A.T	W.T
1	0	5	12	12	7
2	1	3	4	3	0
3	2	3	8	6	3
4	3	1	5	2	1

Gantt chart

P ₁	P ₂	P ₃	P ₄	P ₅	P ₆	P ₇
0	1	2	3	4	5	8 12

$$\text{Avg T.A.T} = \frac{23}{4} \Rightarrow 5.75$$

$$\text{Avg W.T} = \frac{11}{4} = 2.75$$

OPTIMIZATION

$$\text{Throughput} = \frac{\text{No. of Processes}}{\text{C.F}}$$

Date _____

Saathi

- GATE 2006 Question :- SJF pre-emptive.
What is the waiting time of process P₂?

P. No	A.T	B.T	C.T	T.A.T	W.T
1	0	20	20	20	0
2	15	25	55	40	15
3	30	10	40	10	0
4	45	15	70	25	10

Waiting time of (P₂)

Gantt chart

P ₁	P ₁	P ₂	P ₃	P ₂	P ₂	P ₄
0	15	20	30	40	45	55

So, W.T of P₂ process is 15.

RGB

priority Based scheduling :

Selection criteria :- priority. (high-priority)

Mode :- Non-pre-emptive.

B.1 →

P. No	A.T	B.T	Priority
1	0	4	4 ✓
2	1	5	5 ✓
3	2	1	7 ✓
4	3	2	2 ✓
5	4	3	1 ✓
6	5	6	6 ✓

C.T	T.A.T	W.T
4	4	0
16	15	10
5	3	2
18	15	13
21	17	14
11	6	0

high priority

low-priority

Gantt chart

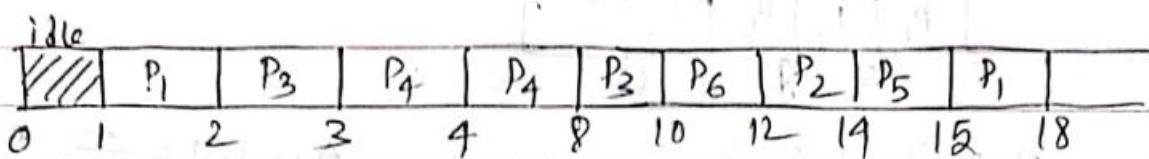
P ₁	P ₃	P ₆	P ₂	P ₄	P ₅
0	4	5	11	16	18

$$\begin{aligned} \text{Avg Waiting time (W.T)} &= \frac{0+10+2+13+14+0}{6} \\ &= \frac{39}{6} \Rightarrow 6.5 \end{aligned}$$

- Priority Based :- pre-emptive. (Q1)

Priority	P.No.	A.T	B.T	C.T	T.A.T	W.T
low \leftarrow ①	1	1	4 3	13	17	13
5	2	2	2	11	12	10
7	3	2	3 2	10	8	5
high \leftarrow ⑧	4	3	5 4	8	5	0
5	5	3	1	15	12	11
6	6	4	2	12	8	6

Gantt chart



Avg W.T,

$$= \frac{13+10+5+0+11+6}{6}$$

$$= \frac{45}{6} \Rightarrow 7.5$$

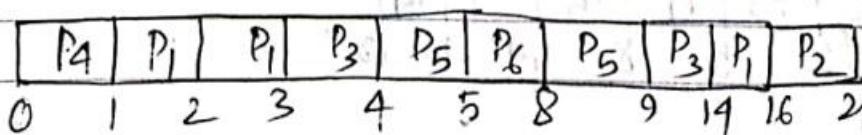
- Priority Based :- pre-emptive. (Q2)

$$\begin{aligned} T.A.T &= C.T - A.T \\ W.T &= T.A.T - B.T \end{aligned}$$

Priority	P.No.	A.T	B.T	C.T	T.A.T	W.T
low priority \leftarrow ⑤	1	1	4 3	16	15	11
2	2	2	5	21	19	14
6	3	3	8 5	14	11	5
4	4	0	1	1	1	0
7	5	4	2 1	9	5	3
high priority \leftarrow ⑧	6	5	3	8	3	0

Gantt chart

$$\text{So Avg W.T} = \frac{33}{6} = 5.5$$



Date _____



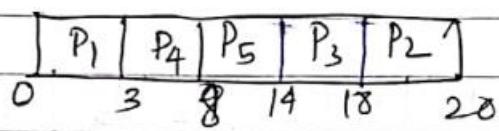
Largest job First: opposite of SJF.

Celution criteria \rightarrow Brust / Mode \rightarrow Non-preemptive and preemptive.

Q-1 (Non-preemptive)

P.No	A.T	B.T	C.T	T.A.T	W.T
1	0	3	3	3	0
2	1	2	20	19	17
3	2	4	18	16	12
4	3	5	8	5	0
5	4	6	19	10	9

Gantt chart



$$\text{Avg T.A.T} = \frac{53}{5} \Rightarrow 10.6$$

$$\text{Avg W.T} = \frac{33}{5}$$

$$= 6.6$$

Q-2 L.J.F \rightarrow Non-preemptive.

* \rightarrow If the Brust time of the process are matching, they schedule the process which has the lowest arrival time.

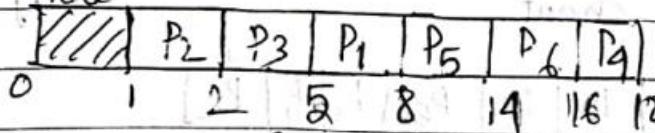
P.No	A.T	B.T	C.T	T.A.T	W.T
1	3	3	8	5	2
2	1	1	2	1	0
3	2	3	5	3	0
4	4	2	18	14	12
5	6	6	14	8	2
6	2	2	16	19	12

$$\text{Avg T.A.T} = \frac{45}{6} \Rightarrow 7.5$$

$$\text{Avg W.T} = \frac{28}{6} = 4.66$$

Gantt chart

idle



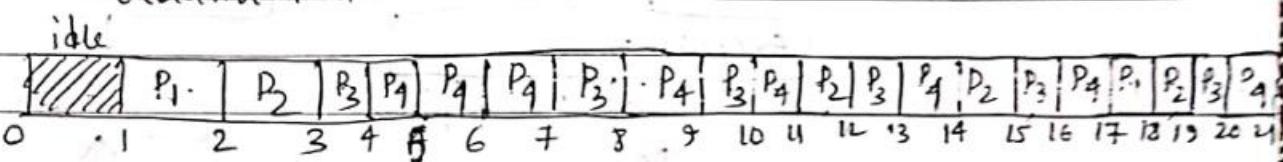
Date _____

* (LRFT)

- LRF → pre-emptive \Rightarrow (Largest Remaining Time First).

P.N.O	A.T	B.T	C.P	T.A.T	W.T
1	1	2	13	17	15
2	2	4	19	17	13
3	3	6	20	17	11
4	4	8	24	17	9

Gantt chart



$$\text{Avg T.A.T} = 17$$

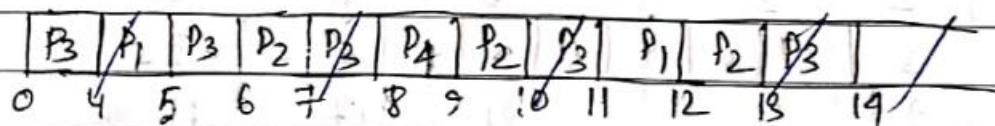
$$\text{Avg W.T} = \frac{48}{4} \Rightarrow 12$$

- * C2066
* GATE Problem :- LRTF.

= What is avg T.A.T using LRTF.

P.N.O	A.T	B.T	C.T	T.A.T	W.T
1	0	2	12	12	10
2	0	4	13	13	9
3	0	8	14	14	6

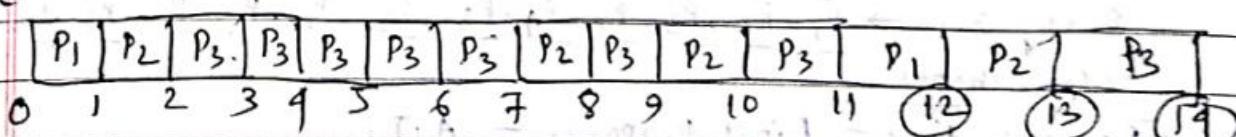
Gantt chart



$$\text{Avg T.A.T} = \frac{39}{3} \Rightarrow 13$$

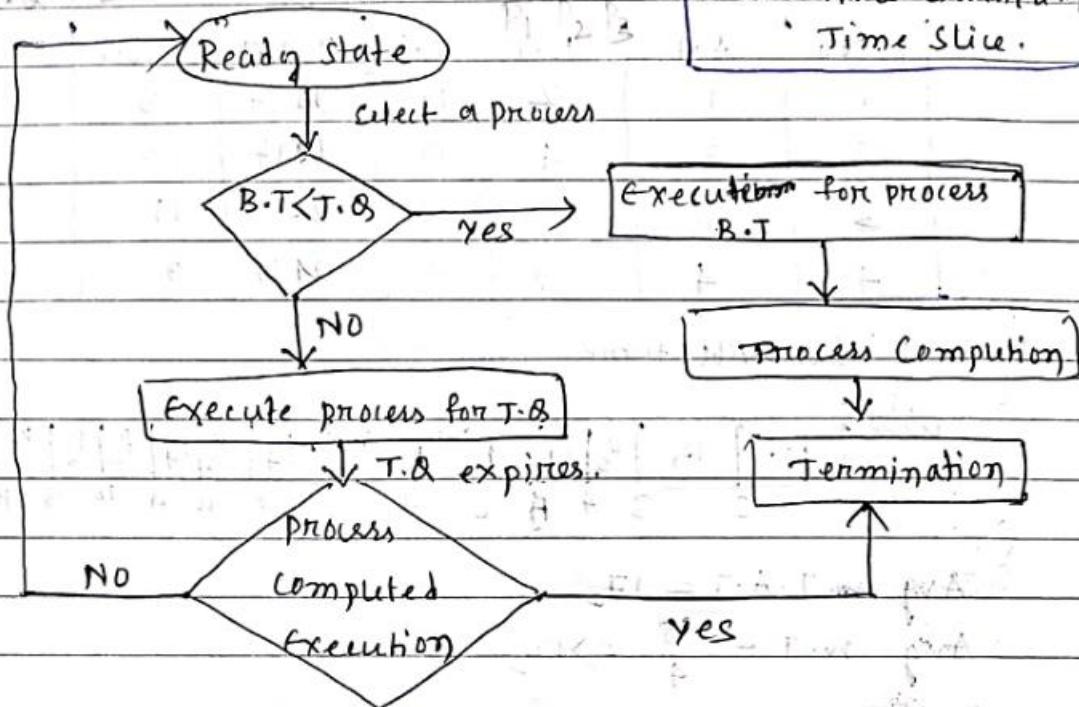
Arg W.T = $\frac{25}{3} \Rightarrow 8.3$.

Gantt chart



RR

Round Robin Scheduling Algorithm:



• Round Robin scheduling :- (Q-1)

* Selection criteria: Time Quantum or Time slice.

* Mode: pre-emptive.

$$(T.Q = 2)$$

R.T	P.NO	A.T	B.T	C.T	T.A.T	W.T
0	1	0	4	8	8	4
1	2	1	5	18	17	12
2	3	2	2	6	4	2
3	4	3	1	9	6	5
4	5	4	6	21	17	11
5	6	5	3	19	14	9

$$\text{Avg R.T} = \frac{23}{6} \Rightarrow 3.8$$

Gantt chart

$$\text{Avg} = \frac{66}{6} = 11$$

$$\text{Avg} = \frac{45}{6} = 7.5$$

P ₁	P ₂	P ₃	P ₁	P ₄	P ₅	P ₂	P ₆	P ₅	P ₂	P ₆	P ₅
0	2	4	6	8	9	11	13	15	17	18	19

Ready Queue $\rightarrow P_1, P_2, P_3, P_1, P_4, P_5, P_2, P_6, P_5, P_2, P_6, P_5$
 (flow chart)

$$\text{Response time} = \text{First Response} - A.T$$

Date _____

• Round Robin Scheduling :- (Q-2)

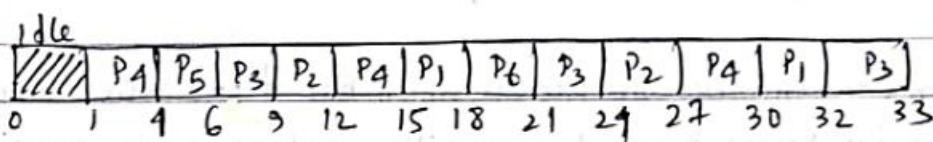
$$T \cdot Q = 3$$

P.NO	A.T	B.T	C.T	T.A.T	W.T
1	5	5 ₂	32	27	22
2	4	6 ₃	27	23	17
3	3	7 ₄	33	30	23
4	1	9 ₅	30	29	20
5	2	2 ₆	6	4	2
6	6	3 ₇	21	15	12

(Time sharing process)

Ready Queue $\rightarrow P_4, P_5, P_3, P_2, P_1, P_6, P_3, P_2, P_4, P_1, P_3$

Gantt chart



$$\text{Avg - T.A.T} = \frac{128}{6} \Rightarrow 21.3$$

$$\text{Avg - W.T} = \frac{96}{6} \Rightarrow 16$$

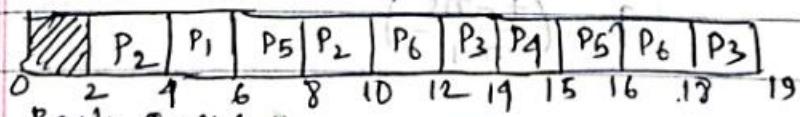
• Round Robin scheduling :- (Q-3)

$$T.Q = 2$$

P.NO	A.T	B.T	C.T	T.A.T	W.T
1	3	2	6	3	1
2	2	4 ₂	10	8	4
3	6	3 ₁	19	13	10
4	8	1	15	7	6
5	4	3 ₁	16	12	9
6	5	4 ₂	18	13	9

Gantt chart

$$\text{avg} = \frac{56}{6} \quad \text{avg} = \frac{39}{6} \Rightarrow 6.5 \\ = 9.3$$



Ready Queue

$\rightarrow P_2, P_1, P_5, P_2, P_6, P_3, P_4, P_5, P_6, P_3$

Date _____ / _____ / _____

(1)

Question :- consider a system with 4 processes P_1, P_2, P_3, P_4 .

The Burst time requirements of these process are 4, 1, 8, 1 respectively. Then what is the completion time of process P_1 , assuming Round Robin scheduling.

$$(T, Q, ITs = 1)$$

$$\Rightarrow P_1 \rightarrow 4 \quad \text{Let; Arrival time of all process '0'}$$

$$\Rightarrow P_2 \rightarrow 1 \quad \text{then,}$$

$$P_3 \rightarrow 8$$

$$\Rightarrow P_4 \rightarrow 1$$

Ready queue $\rightarrow P_1, P_2, P_3, P_4, P_1, P_3, P_1, P_3, P_1, P_3$

P_1	P_2	P_3	P_4	P_1	P_3	P_4	P_3	P_1	P_3
0	1	2	3	4	5	6	7	8	9

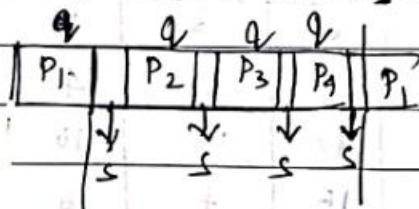
so, the completion time of P_1 is = 9.

(2)

Question :- consider the process which has 'n' processes sharing the CPU in Round Robin fashion. The Context switching time is 's' units. Then what must be the time quantum 'q' such that each process is guaranteed to get its turn at the CPU for every t seconds of time.

$$(1) q = \frac{t - ns}{n+1} \quad (2) q = \frac{t + ns}{n-1} \quad (3) q = \frac{t - ns}{n-1} \quad (4) q = \frac{t - ns}{n+1}$$

\rightarrow Let, $n=4$ (P_1, P_2, P_3, P_4)

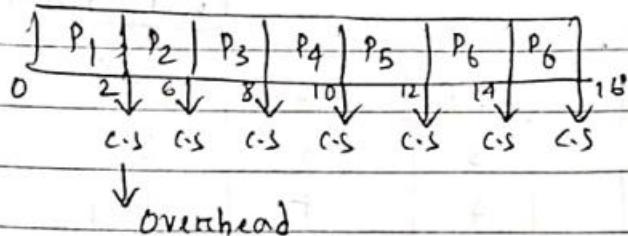


$$\text{total time, } t = 3q + 4s$$

$$\text{So, for } n \text{ processes} - t = ns + (n-1)q$$

$$q = \left(\frac{t - ns}{n-1} \right)$$

Date _____ / _____ / _____



* Time Quantum ($T \cdot Q$) $\downarrow \rightarrow C.S. \uparrow$
 \rightarrow Response time decrease.

* $T.Q \uparrow \rightarrow C.S. \downarrow$
 \rightarrow Response time increase.

* $T.Q \uparrow \uparrow \rightarrow FCFS$.

• Round Robin scheduling conclusion:

\rightarrow If the time quantum is less, then the no of context switching -es will increase and response time will be less.

\rightarrow If the time quantum is large, then number of context switches will decrease and response time will be more.

\rightarrow If the time quantum is very very large, the algorithm degenerates to FCFS Algorithm.

\rightarrow Round Robin is used to decrease the response time.

Highest Response Ratio Next (HRRN)

selection criteria \rightarrow Response Ratio. (high)

Mode \rightarrow Non-pre-emptive.

$$\boxed{\text{Response Ratio (RR)} = \frac{W+S}{S}}$$

W \rightarrow waiting time.

S \rightarrow service time or Burst time.

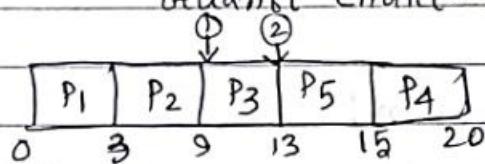
The HRRN favours the shortest jobs and also limits the waiting time of larger jobs.

$$W.T = T.A.T - B.T$$

• Question 1: HNAP-HRRN.

P.NO	A.T	B.T	C.T	T.A.T	W.T
v1	0	3	3	3	0
v2	2	6	9	7	1
v3	4	4	13	9	5
v4	6	5	20	14	9
v5	8	2	15	7	5

Gantt chart



$$\text{avg} = \frac{20}{5} \Rightarrow 4$$

$$(I) RR_3 = \frac{W+S}{S} \\ = \frac{(9-4)+4}{4} \\ = \text{avg } 2.5$$

$$RR_4 = \frac{W+S}{S} \\ = \frac{(9-6)+5}{5} \\ = \frac{8}{5} \Rightarrow 1.6$$

$$RR_5 = \frac{(9-8)+2}{2} \\ = \frac{3}{2} \Rightarrow 1.5$$

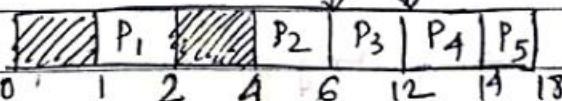
$$(II) RR_4 = \frac{(13-6)+5}{5} \\ = \frac{12}{5} = 2.4 \\ RR_5 = \frac{(13-8)+2}{2} \\ = \frac{7}{2} = 3.5$$

So, Average waiting time (W.T) = 4.

• Question 2: HRRN.

P.NO	A.T	B.T	C.T	T.A.T	W.T	avg W.T = $\frac{19}{5}$
v1	1	1	2	1	0	$= 2.8$ ✓
v2	4	2	6	2	0	
v3	5	6	11	7	1	
v4	6	2	14	8	6	
v5	7	9	18	11	7	

Gantt chart



$$(I) RR_3 = \frac{(6-5)+6}{6} \\ = \frac{1}{6} \\ = 1$$

$$(II) RR_4 = \frac{(12-6)+2}{2} \\ = 4$$

$$RR_5 = \frac{(12-7)+4}{4} \\ = \frac{9}{4} = 2.25$$

Date _____

RRR

✓ CPU Scheduling & I/O Scheduling -

- Question :-) what is completion time of process P_1, P_2, P_3 using SRTF.

P.NO	A.T	CPU time	I/O time	CPU time	
1	0	1	2	2	
2	1	2	4	5	
3	2	3	6	8	

Note :-

(1) The process first spends CPU time followed by I/O time, followed by CPU time.

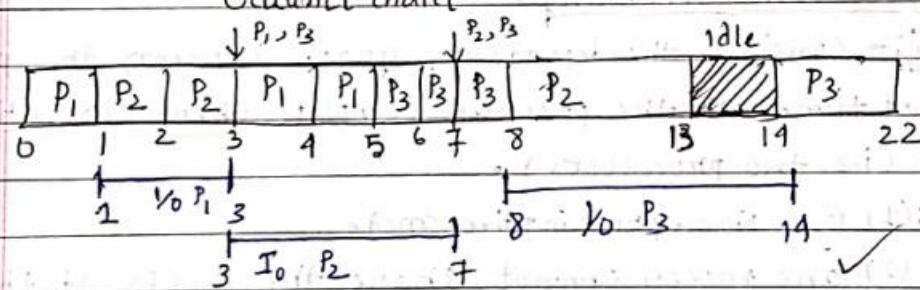
(2) I/O time of the process can be overlapped as much as possible.

→

P.NO	A.T	CPU time	I/O time	CPU time	E.T
1	0	1	2	2	5
2	1	2	4	5	13
3	2	3	6	8	22

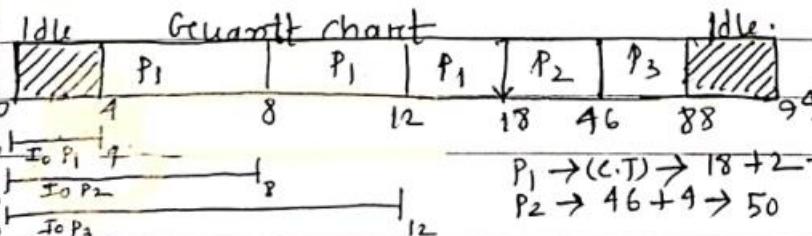
} Completion time

Gantt chart



- Question 2 :-) Using SRTF

P.NO	A.T	I/O time	CPU time	I/O time		E.T
1	0	40	14	2		
2	0	8	28	4		
3	0	12	42	6		



$$P_1 \rightarrow (C.T) \rightarrow 18 + 2 \rightarrow 20$$

$$P_2 \rightarrow 46 + 4 \rightarrow 50$$

$$P_3 \rightarrow 88 + 6 \rightarrow 94$$

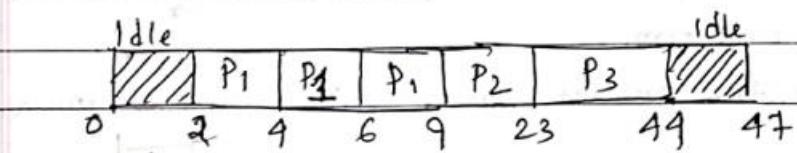
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Date: / /

PBT ✓ GATE problem: 2006 Question. → SJF.

P.NO	A.T	B.I Total	I/O time(20%)	CPU time(70%)	W.O time(10%)
P ₁	0	10	2	8	1
P ₂	0	20	4	14	2
P ₃	0	30	6	21	3

Gantt chart



so, computation time of P₁ = 9 + 1 \Rightarrow 10

$$P_2 = 23 + 2 \Rightarrow 25$$

$$P_3 = 44 + 3 \Rightarrow 47$$

Total time C.P.U idle time, $\Rightarrow 23$

$$\Rightarrow 5 \Rightarrow \frac{5}{47} \times 100 \Rightarrow 10.6\%$$

Multi processor Scheduling:

Question:- Consider the dependency graph between the process.

At what time all the processes complete their execution using 2 CPU's (i.e two processors).

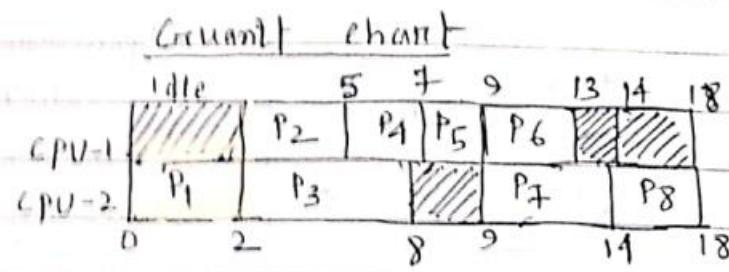
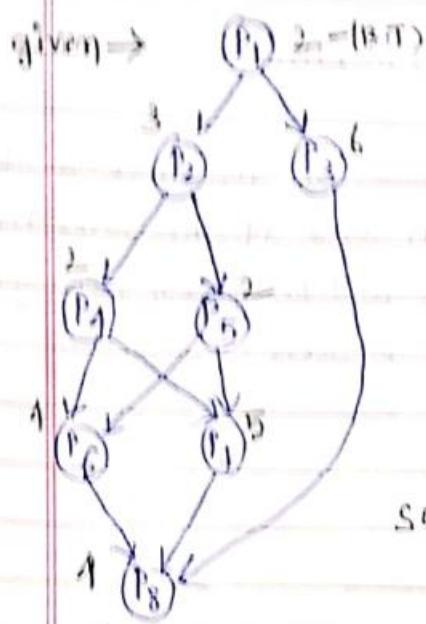
Note: (1) Use Non-preemptive mode.

(2) one process cannot share the 2 CPS at the same time.

(A) 17 (B) 18 (C) 19 (D) 20

Given -

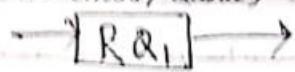
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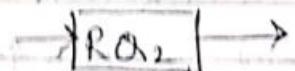
So, completion time $\rightarrow 18$.

Multilevel Queue Scheduling :

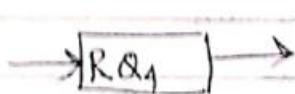
(Ready Queue)



\rightarrow Depending on the priority of the process, In which particular queue, the process has to be placed will be decided.



\rightarrow The high priority process will be placed in the top level ready queue and low priority process will be placed in the Bottom level ready queue.



\rightarrow only after completion of all the processes from the top level ready queue, the further level ready queue process will be scheduled.

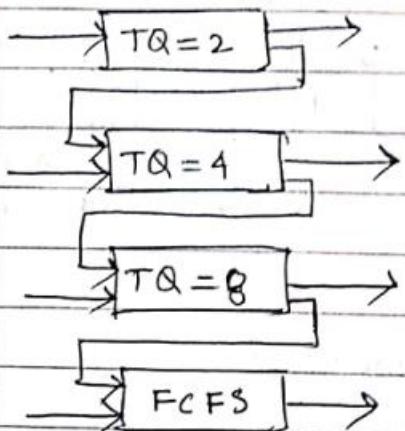
\rightarrow If this is the strategy which is followed then the processes which are placed in the bottom level ready queue will suffer from STARVATION.

STARVATION: The Indefinite waiting of a process is called as STARVATION.

\rightarrow It is also possible to use different scheduling algorithms in the different ready queue.

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MULTILEVEL FEEDBACK QUEUE SCHEDULING -



→ Algorithm avoids the problem of starvation and at the same time preference will be given to high priority process.

Question :- Consider the system which has CPU Bound Bottleneck process which requires Burst time of 40 time units. Multilevel feedback queue scheduling is used. The time quantum is 2 units and it will be incremented by 5 units in each level. How many time the process will be interrupted and in which queue, process will complete the execution?

(a) 4, 5 (b) 5, 6 (c) 3, 4 (d) 5, 5.

	remain
→ TQ-2	① 38
→ TQ-7	② 31
→ TQ-12	③ 19
→ TQ-17	④ 2
→ TQ-22	⑤ 0

• 5th level complete.

• 4 time interrupted.

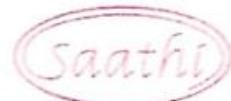
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Conclusion :-

Algorithm	Starvation
1) FCFS	(No)
2) SJF (NP)	yes
3) SRTF	yes
4) RR	(No)
5) LJE (NP)	yes
6) LRFT	yes.
7) HRRN	(No)
8) priority (NP)	yes.
9) priority (P)	yes
10) MLQ	yes
11) MLFQ	(No)

Date _____

Saathi

MEMORY MANAGEMENT

/* INTRODUCTION */(1)

- **Functionality :-** Allocating and deallocating memory to the process.
- **GOAL :-** Efficient utilization of memory by using minimizing the internal and external fragmentation.

$$\left\{ \begin{array}{l} 2^{10} \Rightarrow 1024 \approx 10^3 \Rightarrow 1K \\ 2^{20} \Rightarrow 1M \\ 2^{30} \Rightarrow 1G \\ 2^{40} \Rightarrow 1T \end{array} \right.$$

✓ Memory Organization Map -

0	<u>1010</u> <u>1101</u> <u>2</u>	<u>000</u>	1 word \rightarrow 8 bits
1	-----	<u>001</u>	Capacity of the memory in Bytes,
2	-----	<u>010</u>	\Rightarrow [no of words * word size]
3	-----	<u>011</u>	
4	-----	<u>100</u>	$\Rightarrow 8 * 8$
5	-----	<u>101</u>	
6	-----	<u>110</u>	$\Rightarrow 64$ bit
7	-----	<u>111</u>	$\Rightarrow 8$ byte.

(Memory)

$$[8-\text{words}] \rightarrow 2^3$$

- ✓ Q-1 Consider a system which has 256 KW and each has size of 64 bits. Then what is the capacity of memory in bytes.

$$\rightarrow \# \text{ no of words} \Rightarrow 256 \text{ K} \quad \text{--- (1)}$$

$$\text{size of word} = 64 \text{ bit.}$$

$$= 8 \text{ byte.} \quad \text{--- (2)}$$

$$\begin{aligned} \text{Capacity} &= (1) * (2) \\ &= (256 \times 8) \text{ byte.} \Rightarrow 2^8 \times 2^{10} \times 2^3 = 10^{21} \text{ byte} \\ &= 2 \times 2^{26} = 2 \text{ MB.} \end{aligned}$$

MINIMUM MEMORY

Q-3 Consider a system which has 512 M words and each word has the size of 16 bytes then capacity of memory is -

$$\rightarrow \# \text{ no of words} = 512 \text{ M} \quad \text{--- (1)}$$

$$\text{size of each word} = 16 \text{ bytes} \quad \text{--- (2)}$$

$$\text{capacity of memory} = (1) \times (2)$$

$$= 512 \text{ M} \times 16$$

$$= 512 \times 2^{20} \times 2^4$$

$$= 2^9 \times 2^{20} \times 2^4$$

$$= 2^{33} \Rightarrow 2^{30} \times 2^3$$

$$= [8 \text{ GB}]$$

Q-3 Consider a System where 32 binary bits are used to represent all the words of memory and each word has the size of 32 bits. Then what is the capacity of memory in Bytes -

$$\rightarrow \# \text{ no of words} = 2^{32}$$

$$\text{word size} = 32 \text{ bit}$$

$$\Rightarrow 4 \text{ bytes.}$$

$$\text{Capacity} = 2^{32} \times 4$$

$$= 2^{32} \times 2^2$$

$$= 2^{34}$$

$$= 2^{30} \times 2^4$$

$$= 16 \text{ GB.}$$

Ram Chip Introduction :-

RAM chip Implementation -

Q-1

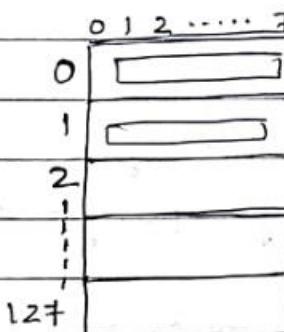
Ram chip size = 128 Bytes.

Organize the memory capacity of 16 KB by using above Ram chip -

a) No of RAM chips required.

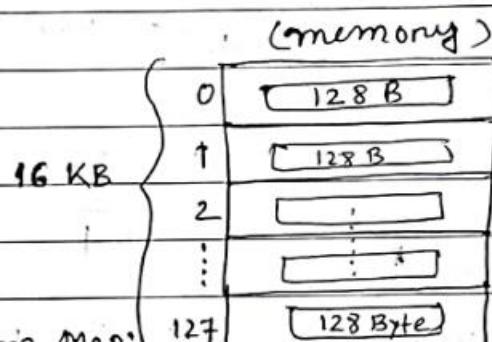
b) Draw the memory Organization Map.

$\rightarrow 128(B)$
 no of word word size.



(a) NO of RAM chip required,

$$\begin{aligned}
 &= 16 \text{ KB} \\
 &= \frac{128 \text{ B}}{128 \text{ B}} \\
 &= \frac{2^7 \times 2^{10}}{2^7} \\
 &= 2^7 \\
 &= 128
 \end{aligned}$$



(b) memory organization map:

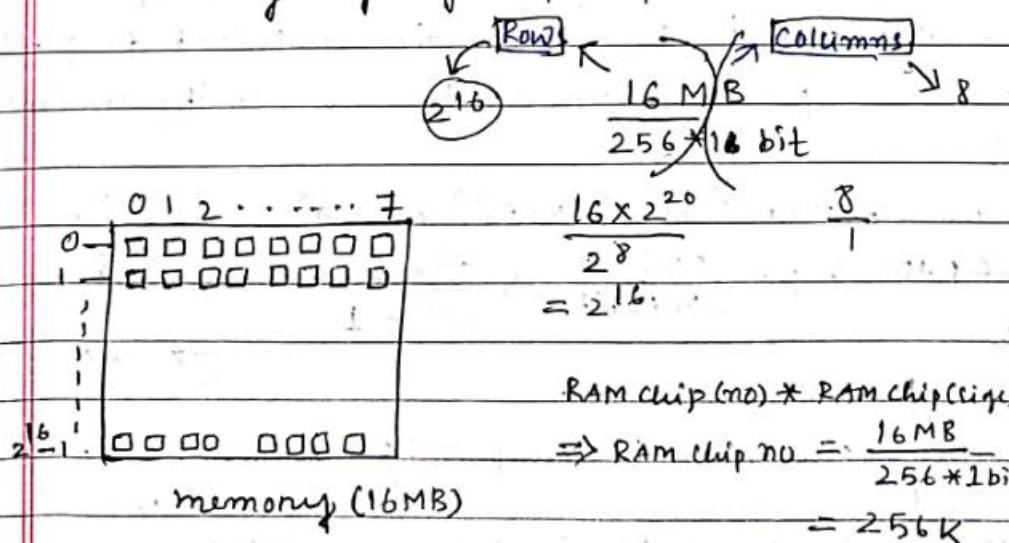
• Q-3 (Ram chip implementation)

RAM chip :- 256×1 bit.

Memory capacity = 16 MB.

$$\text{i) NO of RAM chip require} = \frac{16 \text{ MB}}{256 \times 1 \text{ bit}} \Rightarrow \frac{2^4 \times 2^{20} \times 2^3}{2^8 \times 2^1} \Rightarrow 2^{19} \Rightarrow 2^9 \times 2^{10} \Rightarrow 256 \text{ K}$$

ii) Memory organization map:



$$\text{RAM chip (no)} * \text{RAM chip (size)} = 16 \text{ MB}$$

$$\Rightarrow \text{RAM chip no} = \frac{16 \text{ MB}}{256 \times 1 \text{ bit}} = 256 \text{ K}$$

• Q-3 Ram chip implementation -

Ram chip size = 512×2 bit.

Memory capacity = ~~2^8~~ 32 MB.

$$\text{D) No of Ram chip} = \frac{32 \text{ MB}}{512 \times 2 \text{ bit}} \Rightarrow \frac{2^5 \times 2^{20} \times 2^3}{2^9 \times 2^1}$$

$$= 2^{38} 2^{18}.$$

(2^{16}) Row \swarrow \rightarrow column (4)

~~32 MB~~
~~512 \times 2 bit~~

$$\frac{2^5 \times 2^{20}}{2^9} = 2^{11} 2^0$$

$$= 2^{11} 1$$

ii) Map -

	0	1	2	3
0	□	□	□	□
1	:	:	:	:
2	:	:	:	:
$2^{16}-1$	□	□	□	□

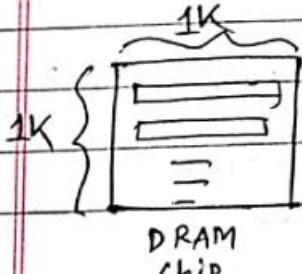
main memory (32 MB) :

GATE (2010)-Q:

A main memory unit with capacity of 4 MB is built using $1M \times 1$ bit DRAM chips. Each DRAM chip has $1K$ rows of cells with $1K$ cells in each row. The time taken for single refresh operation is 100 ns. The time required to perform one refresh operation on all the cells in the memory unit is -

- a) 100 ns b) 100×2^{10} ns c) 100×2^{20} ns d) 3200×2^{20} ns

$$\rightarrow \text{no of RAM chip} = \frac{4 \text{ MB}}{1 \text{ M} \times 1 \text{ bit}} \Rightarrow \frac{2^2 \times 2^{20} \times 2^3}{2^{20} + 2^0} \Rightarrow 2^5 = 32$$



cells in one DRAM chip, = $1K \times 1K$

$$= 2^{10} \times 2^{10} \Rightarrow 2^{20} \text{ cells.}$$

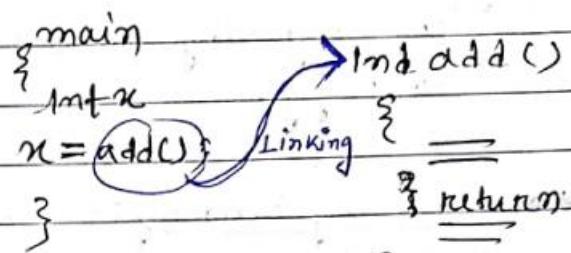
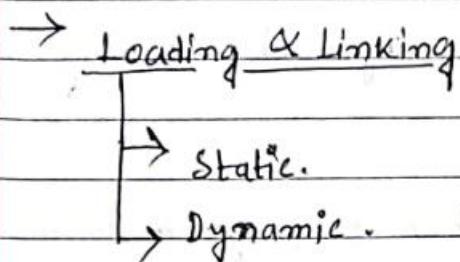
$$\text{Total cell to build (4 MB) main memory} = 32 \times 2^{20}$$

~~2023 PAPER~~

$$\rightarrow 32 \times 2^{20} \times 100 \text{ ns}$$

$$= 3200 \times 2^{20} \text{ ns}$$

✓ Loading, Linking and Address Binding:



Loading: When program load in main memory.

• Static :-

- Loading the entire program into memory before the start of the program execution is called static loading.
- Inefficient utilization of memory because whether it is required or not required, the entire program is brought into main memory.
- The program execution will be faster.

Linking → Linking all the modules / functions of the program.

- If the static loading is used, then static linking will be applied.

• Dynamic :-

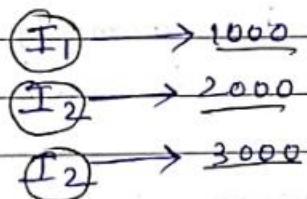
- Loading the program into memory on demand is called as dynamic loading.
- The efficient utilization of memory.
- The program execution will be slower.
- If the dynamic loading is used accordingly the dynamic

-linking will be applied.

→ The majority of O.S will use dynamic loading/linking strategy.

- Addressing Binding :- Association of program instruction and data to the actual physical memory locations is called Address Binding.

Program P₁



Type of Address Binding :-

- Compile time Address Binding (compiler)
- Load time A·B (loader)
- Dynamic or Execution time A·B (processor).

* compile time A·B :-

→ If the compiler is responsible of association of program instructions and data to the actual physical memory locations is called compile time A·B.

→ The compile time Address Binding will be done before Loading the program into the main memory.

→ The compiler leads to interrupt with O.S memory manager to perform compile time address binding.

- * Load time A.B :- The Load time A.B will be done after the program is loaded into main memory.
- * Execution time or dynamic A.B :- The Address binding will be postponed even after the loading the program into main memory.
 - This type of A.B will be done at the time of program execution.
 - Processors does this type of A.M.
 - The Majority of the o.s uses the Dynamic A.B.

Memory Management Techniques Introduction :-

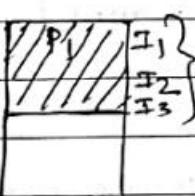
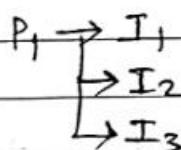
Memory Management Techniques



Contiguous

→ fixed partition schemes.

→ variable partition.



(contiguous)

Non-contiguous

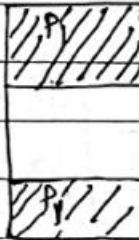
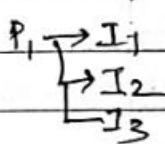
→ paging.

→ multi-level.

→ Inverted.

→ Segmentation.

→ segmented paging.



Non contiguous.

• Fixed partition Schemes :-

Contiguous Allocation Schemes

0		50KB
1		100KB
2		200KB
3		160 KB
4		350 KB
5	██████████	70 KB
6		120 KB
7		200 KB

memory = 8

→ In fixed partition Schemes memory will be divided into fixed no of partitions. $P_1 = 60KB$

→ fixed means no of partitions are fixed not the size of partition.

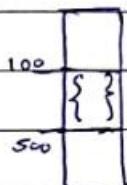
→ In one partition only 1 process will be accommodated. = 8 process.

→ the degree of multiprogramming is restricted by the no of partitions in the main memory.

→ Internal fragmentation.

Every partition is associated with the limit Registers -

1) Lower limit :- starting address of the partition.



2) Upper limit :- Ending address of the partition.

• Variable partition Schemes :-

Contiguous Allocation Schemes

120KB	P_1 150KB
Execution complete	P_2 50 KB
Fragmentation	P_3 200KB
Execution complete	P_4 350KB
Fragmentation	P_5 70 KB
Execution complete	P_6 150 KB

HOLE
 $(50+70)KB = 120KB$ (free)

→ In this Scheme, initially the memory will be single contiguous free block.

→ Whenever the request by the process is accordingly the partition will be made.

$P_1 \rightarrow 150KB$ | $P_4 \rightarrow 350KB$

$P_2 \rightarrow 50KB$ | $P_5 \rightarrow 70KB$

$P_3 \rightarrow 200KB$ | $P_6 \rightarrow 150KB$

| $P_7 \rightarrow 100KB$

To Avoid the problem of External fragmentation:

* Compaction :- is undesirable. Moving all the process towards the top or towards the bottom to make the free available memory in a single contiguous place is called as compaction.

→ Compaction is undesirable to implement because it disturbs all the running process in the memory.

• Partition Allocation Schemes:

When more than one partition is freely available to satisfy the request of the process then for the decision making of selecting a partition will be done by partition allocation methods.

1) First fit :- Allocate the process in the partition which is first sufficient partition from the top of the memory.

2) Best fit :- Allocate the process in the partition which has the smallest sufficient partition among the free available partition.

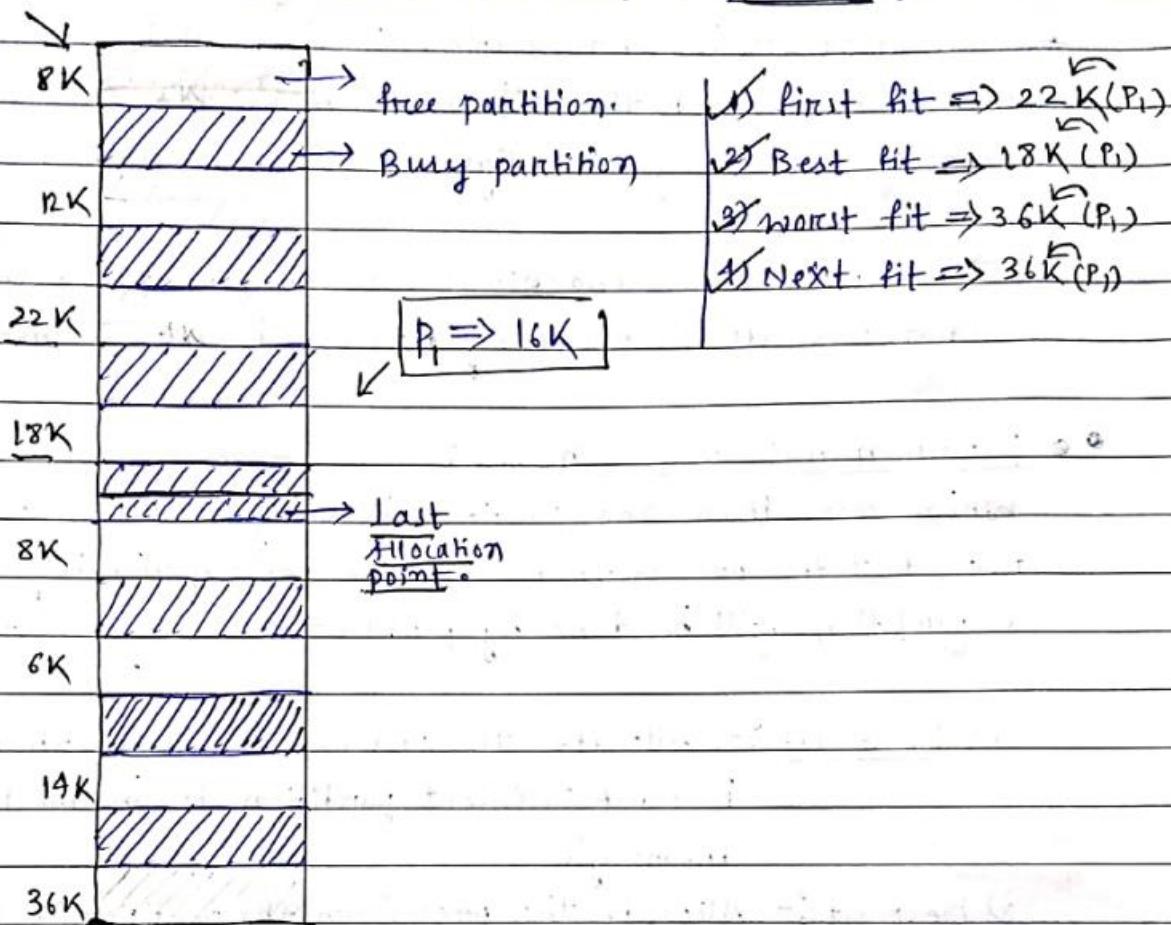
To do this, we need to do searching. To find out the smallest partition, it requires searching all the partitions in the memory.

3) Worst fit :- Allocate the process in a partition which is largest sufficient among all the free available partition.

To find out the largest sufficient, it requires to search all the partitions in the memory.

4) Next fit :- Next fit also works like the first fit but it will search for first sufficient partition from the last allocation point.

- Best fit, first fit, worst fit, & next fit (Question-1):



(Question-2) :- How many successive request of 6K will be satisfied by using the first fit and assuming variable partition scheme? (from above diagram)

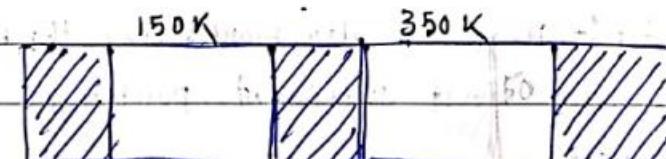
- a) 16 b) 17 c) 18 d) 19.

$$\rightarrow 1+2+3+3+1+1+2+6 = 19$$

Create

(Question-3) :-

Request from the process are 300K, 25, 125K, and 50K respectively.



The above request could be satisfied with
(Assume variable partition scheme)

a) Both best fit and first fit.

First fit but not Best fit.

c) Best fit but not first fit.

d) neither best fit nor first fit.

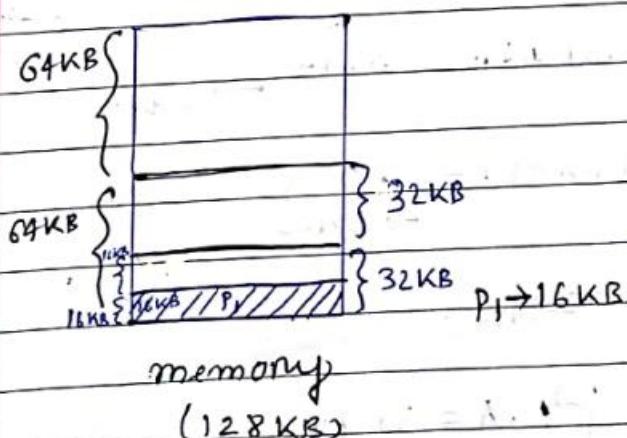
		X(best fit)	
→	W(first fit)	150K	350K
		125K	50K
		OK	OK

		X(best fit)	
→		150K	350K
		25K	50K
		25K	25K

Buddy System Theory: In the Buddy System initially the memory will be single continuous free block.

→ whenever the request by process comes in the memory will be divided into 2 half blocks.

→ If the request still small, the lower block of the memory is further divided into 2 half block again. In the buddy system, the memory will be allocated from the lower level blocks to the higher blocks.



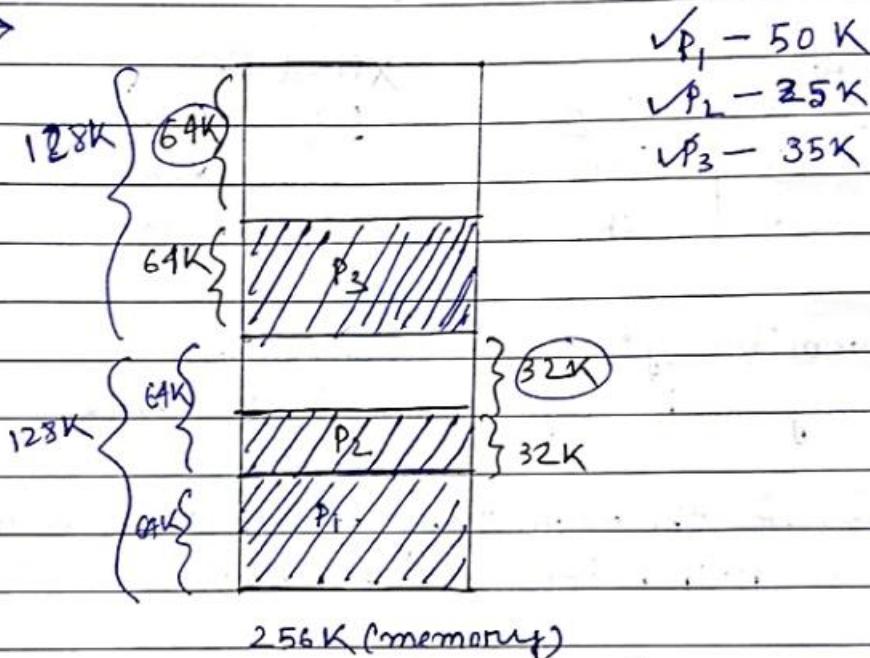
• Question - 1 (Buddy System) -

In a Buddy system of memory management, successive request of 50K, 25K, and 35K are satisfied with 256K of Available memory. How many blocks (with size) are left.

Two Block (32K, 64K).

- b) one block (94K)
 c) one block (145K)
 d) Memory blocks with varying sizes.

→



GATE
**

PAGING (Non Contiguous) (11)

Logical Address Space (LAS) or virtual Address space (VAS)

Logical Address or virtual Address (VA) → Bits.

Physical Address space (PAS) → Bits.

Physical Address (PA) → Bits.

$$(1) L.A.S = 128 MW$$

$$\Rightarrow 2^7 * 2^{20}$$

$$\Rightarrow 2^{27}$$

$$\boxed{L.A = 27 \text{ bits}}$$

$$(2) L.A = 38 \text{ bits}$$

$$LAS = 2^{38}$$

$$= 2^8 * 2^{30}$$

$$= 256 GW$$

$$(3) P.A = 16 bits$$

$$PAS = 2^{16}$$

$$= 2^6 * 2^{10} \Rightarrow 64 KW$$

$$(4) PAS = 32 MW$$

$$= 2^5 * 2^{20}$$

$$= 2^{25}$$

$$\boxed{PA = 25 \text{ bits}}$$

- LAS and PAS :

* CPU always generates Logical Address.

$LA \gg PA$

→ The technique of mapping processor generated logical Address to physical Address is called as paging.

- LAS division into Pages -

$$L.A \Rightarrow 13 \text{ bits} \rightarrow L.A.S \Rightarrow 2^{13} \Rightarrow 2^3 \times 2^{10} \Rightarrow 8 \text{ KW} \Rightarrow 8 \text{ pages.}$$

$$P.A \Rightarrow 12 \text{ bits} \rightarrow P.A.S \Rightarrow 2^{12} \Rightarrow 4 \text{ KW.}$$

① L.A.S. will be divided into equal size pages.

Page size = 1KW

$$\# \text{ pages} = \frac{L.A.S}{\text{page size}} \Rightarrow \frac{8 \text{ KW}}{1 \text{ KW}} \Rightarrow 8$$

L.A.S	
0	← 000
1	← 001
2	← 010
3	← 011
4	← 100
5	← 101
6	← 110
7	← 111

↑
page no's
↓

\$ 3 bits.

- PAS division into Frames -

PAS is divided into equal size frames.

*

Page SIZE is Always same as frame size

Frame size \Rightarrow 1KW

$$\# \text{ frames} \Rightarrow \frac{P.A.S}{\text{frame size}} \Rightarrow \frac{4 \text{ KW}}{1 \text{ KW}} \Rightarrow 4$$

page table

0	P ₇	00
1	P ₅	01
2	P ₃	10
3	P ₁	11

↑
frame No.
↓

2 bits.

* Some Important Conclusions -

$$\rightarrow \boxed{\# \text{ pages} = \frac{\text{I.A.S.}}{\text{Page size}}}$$

I.A.S. is divided into equal size pages.

$$\boxed{\# \text{ frames} = \frac{\text{P.A.S.}}{\text{frame size}}}$$

P.A.S. is divided into equal size frames.

PAGE size is Always same as FRAME size

Whenever the paging is applied to the page, the page table will be maintained.

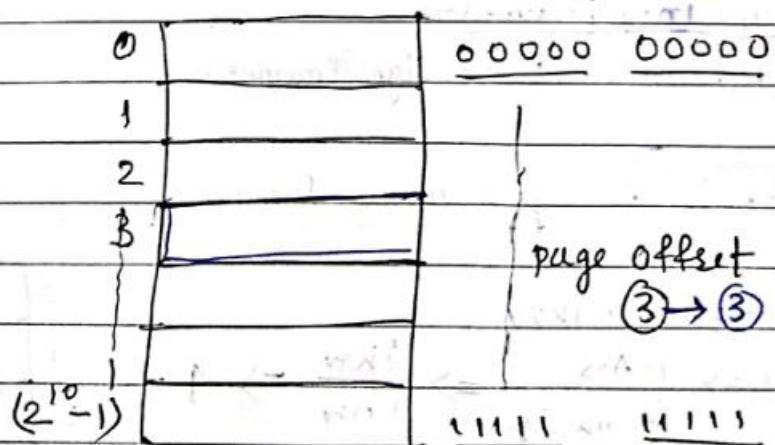
→ No of entries ^{in the} page table is same as no of page in L.A.S.

→ page table entry contains the frame no.

• 1KB page Details:

1KB page will look like this.

$1K$
 $2^{10} \rightarrow$ (10 bits)



• Paging Diagram -

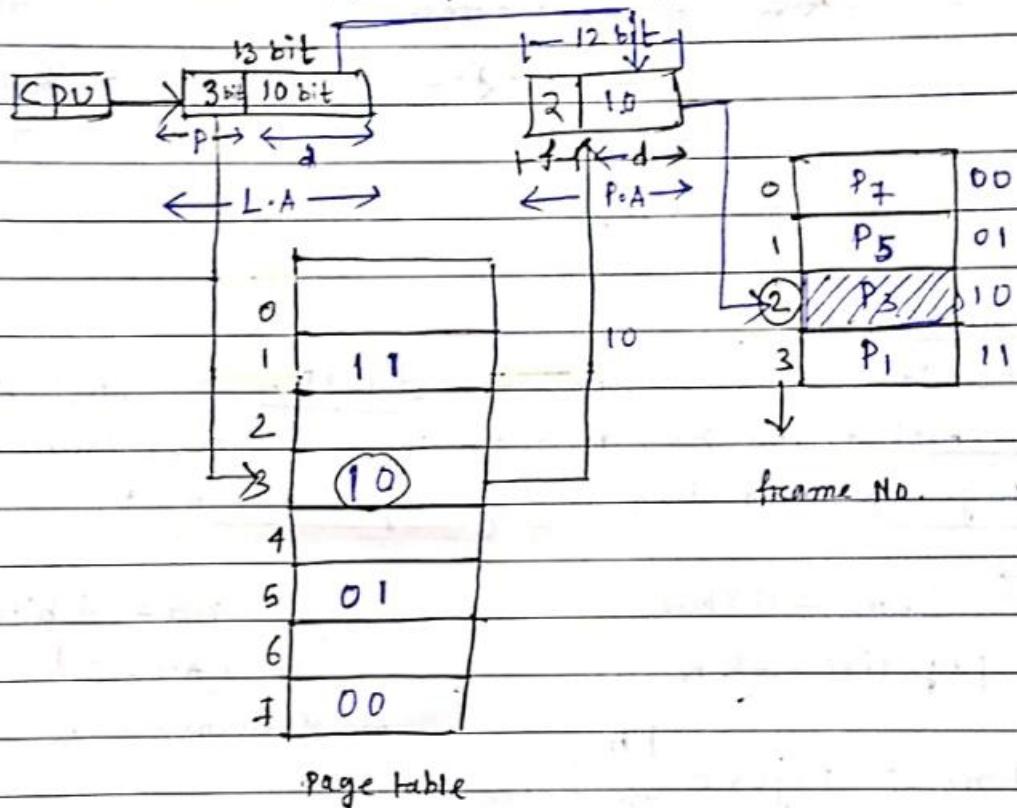
When: L.A \Rightarrow 13 bits.

P.A \Rightarrow 12 bits.

p \rightarrow no of bits required to represent pages of L.A.S on page no.

d \rightarrow no of bits required to represent the pages offset.

f \rightarrow The no of bits required to represent the frame no.



✓ Paging Technique Question - ① :-

Consider a system which has Logical Address = 27 bits and physical address = 21 bits, and page size = 4 KW. calculate no of pages and no of frames. [page size = frame size]

$$\rightarrow L.A = 27 \text{ bits}$$

$$L.A.S \Rightarrow 2^{27}$$

$$P.A = 21 \text{ bits}$$

$$P.A.S = 2^{21} \text{ bits}$$

$$\# \text{no of pages} = \frac{L.A.S}{4 \text{ KW}}$$

$$= \frac{2^{27}}{2^2 \times 2^{10}} \Rightarrow 2^{15}$$

$$\# \text{No of frames} = \frac{P.A.S}{4 \text{ KW}} \Rightarrow \frac{2^{21}}{2^2 \times 2^{10}}$$

$$\Rightarrow 2^9$$

Question - 2.

Consider a system which has no of pages = 2^k and page size is 4KB . The physical Address is 18 bits then calculate L.A.S and no of frames.

$$\text{P.A} = 18.$$

$$\begin{aligned}\rightarrow \# \text{ no of pages} &= \frac{\text{L.A.S.}}{\text{page size}} \\ \Rightarrow \text{L.A.S.} &= 2^k * 4\text{KB} \\ &= 2^k * 2^{10} * \frac{2}{2} * 2^{10} \\ &= 2^k * 2^{20} \\ &= 2^{\underline{23}}.\end{aligned}$$

$$\boxed{\text{L.A.S.} = 23 \text{ bits}}$$

$$\begin{aligned}\# \text{ no of frames} &= \frac{\text{P.A.S.}}{\text{no. of space}} \\ &= \frac{2^{18}}{4\text{KB}} \Rightarrow \frac{2^{18}}{2^2 * 2^{10}} \\ &= \underline{\underline{64}} \\ &= 64\end{aligned}$$

Question - 3.

Consider a system with L.A.S of 128MW and physical Address = 24 bits. The P.A.S divided into 8K frames. Then what is the page size and how many pages in L.A.S?

$$\rightarrow \text{L.A.S.} = 128\text{MW}$$

$$\text{page size} = 2\text{K.W}$$

$$\text{P.A} = 24 \text{ bits}$$

$$\text{P.A.S.} = 2^{24}$$

$$\text{no of frames} = 8\text{K}$$

$$\begin{aligned}\# \text{ no of pages} &= \frac{\text{P.A.S.}}{\text{size of page}} \\ &= \frac{128 * 2^{20}}{2 * 2^{10}} \\ &= \frac{2^7 * 2^{20}}{2^{11}} \\ &= 2^{16} \\ &= 2^6 * 2^{10} \\ &= 64\text{K}\end{aligned}$$

$$\# \text{ no of frames} = \frac{\text{P.A.S.}}{\text{frame size}}$$

$$\Rightarrow \text{frame size} = \frac{2^{24}}{8\text{K}}$$

$$= \frac{2^{24}}{2^3 * 2^{10}} \Rightarrow 2^{11}$$

$$= 2 * 2^{10}$$

$$= 2\text{K}$$

$$\underline{(\text{page size} = \text{frame size})}$$

Grade-2002

• Question - 4

Consider a system with L.A equal to 32 bits. The P.A.S is 64 MB. The page size is 4 KB. The memory is byte addressable. The page table entry size of 2 bytes. what is the approximate size of page table in bytes.

- (A) 1MB (B) 2MB (C) 4 MB (D) 8 MB.

→ \rightarrow (No of entries in page table = No of pages in L.A.S)

$$\begin{aligned} \text{No. of pages} &= \frac{\text{L.A.S}}{\text{page size}} & \left| \begin{array}{l} \text{L.A.S} \\ \text{page size} \end{array} \right. \\ &= \frac{2^{32}}{4\text{KB}} & \left| \begin{array}{l} \text{L.A} = 32 \text{ bits} \\ 1\text{.A.S} = 2^{32} \text{ bits} \end{array} \right. \\ &= \frac{2^{32}}{2^2 \times 2^{10}} \\ &= 2^{20} \end{aligned}$$

$$\begin{aligned} \text{So approximate size of page table} &= \text{No of entries} \times \text{entry size} \\ &= 2^{20} \times 2 \\ &= 2 \times 2^{20} = 2^{21} \end{aligned}$$

• Question - 5

Consider a system having a page table with 4K entries. The L.A is 29 bits. what is the physical Address if the System has 512 frames.

→ L.A = 29 bits.

$$\text{L.A.S} = 2^{29}$$

$$\# \text{no of page} = \frac{\text{L.A.S}}{\text{page size}}$$

$$\begin{aligned} \text{page size} &= \frac{2^{29}}{2^2 \times 2^{10}} \text{ (4K)} \\ &= 2^{17} \end{aligned}$$

of entries in PT
=
of page is L.A.S

$$\text{no of frames} = 512$$

$$\begin{aligned} \# \text{no of frames} &= \frac{\text{P.A.S}}{\text{frame size}} \\ \text{frame size} &= \frac{\text{P.A.S}}{512} \end{aligned}$$

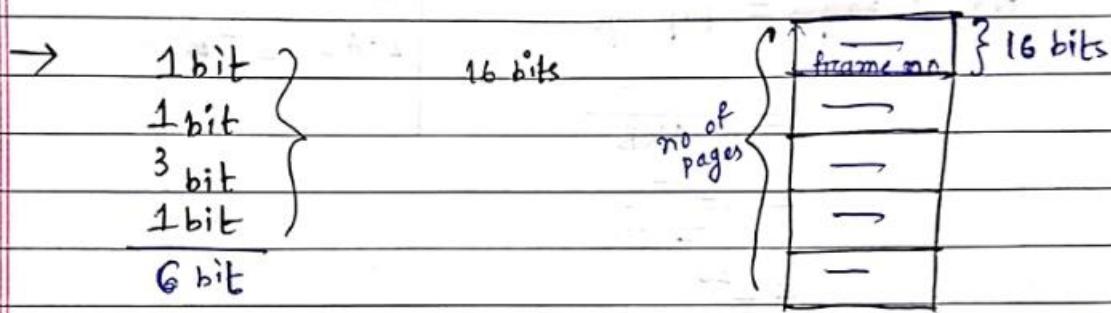
$$\begin{aligned} \Rightarrow \text{P.A.S} &= 512 \times 2^{17} \\ &= 2^9 \times 2^{17} \\ &= 2^6 \times 2^{20} \\ &= 64 \times 2^{26} \end{aligned}$$

frame
size =
page size

$\checkmark \boxed{\text{P.A} = 2.6}$

Question -⑥

Consider a question system where the $L.A.S = P.A.S = 2^{16}$ bytes and page size $\Rightarrow 512$ bytes. The memory is byte addressable. The page table entry size is 2 bytes. The page table entry also contains other information like 1 bit for valid and invalid, 1 bit for reference, 3 bit for page information/protection and 1 bit for dirty bit. How many bits are still available in page table entry to store Ageing information.



$$\text{no of frame (pg entry)} = \frac{P.A.S}{\text{frame size}}$$

$$= \frac{2^{16}}{512} \Rightarrow \frac{2^{16}}{2^9} \Rightarrow 2^7$$

7 bit required to identify a particular frame no.

$$16 - (6+7) \\ = 3 \text{ bits (freely available)}$$

to store Ageing information.

Question -⑦

Consider a system which has L.A.S of 256 MB. The physical Address = 24 bits. The memory is byte addressable. The P.A.S is divided into 8 KB frames. Then how many pages are there in the L.A.S.

$$\rightarrow L.A.S = 256 \text{ MB}$$

$$P.A = 24 \text{ bits.}$$

$$\text{no of frames} = 8 \text{ KB}$$

$$\text{no of page} = \frac{L.A.S}{\text{page size}} \Rightarrow \frac{2^8 \times 2^{20}}{8 \text{ KB}}$$

$$\Rightarrow \frac{2^8 \times 2^{20}}{2^{13}}$$

$$\Rightarrow 2^{15}$$

$$\Rightarrow 32K$$

● Question - 8

* The internal fragmentation in the paging is considered as $\frac{P}{2}$ where P is the page size]

consider a system $L.A.S = P.A.S = 'S' \text{ Bytes}$, and
 $\text{page size} = 'P' \text{ Bytes}$.

$\text{page table entry size} = 'e' \text{ Bytes}$.

The memory is byte addressable. What is the optimal value of page size by minimizing the memory overhead of maintaining page table and internal fragmentation in the paging.

① $P = \sqrt{2se^2}$ ② $P = \sqrt{2s^2e}$ ③ $P = \sqrt{2se}$ ④ $P = \sqrt{2(se)^2}$

$$\rightarrow \text{No of pages} = \frac{L.A.S}{\text{page size}} \\ = \frac{s}{P}$$

$$\frac{P.T + I.F}{\frac{se}{P} + \frac{P}{2}} \Rightarrow \frac{d}{dp}$$

$$P.T = \frac{s}{P} * \text{size of entry} \\ = \frac{se}{P}$$

$$\Rightarrow \frac{d}{dp} \left(\frac{se}{P} + \frac{P}{2} \right) = 0$$

$$\Rightarrow -P^{-2}se + \frac{1}{2} = 0$$

$$\Rightarrow P^{-2}se = \frac{1}{2}$$

$$\Rightarrow P^{-2} = \frac{1}{2se}$$

$$\Rightarrow P^2 = 2se$$

$$\boxed{P = \sqrt{2se}}$$

● Performance of paging:

- The page table of the processes will be stored in the main memory.
- The main memory Access time = M ,
- If the page table stored in the main memory, the formula for effective memory Access time (EMAT).

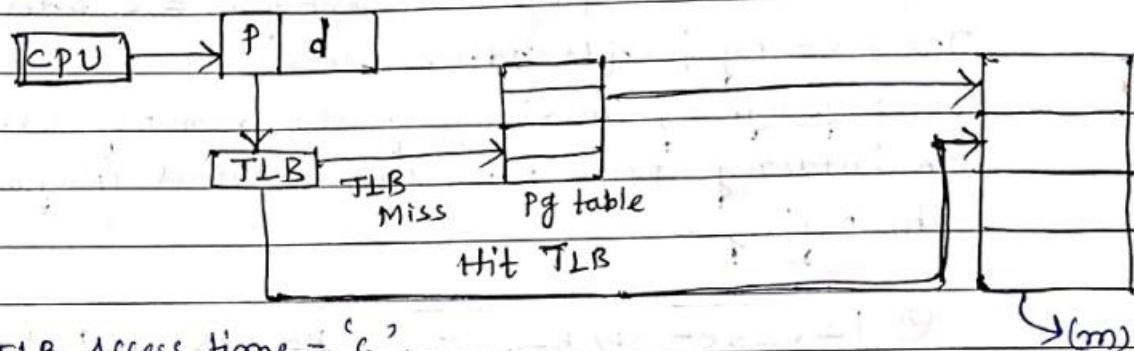
$$\boxed{\text{EMAT} = 2m}$$

- TLB Introduction :

(Translation Lookaside Buffer).

→ This is added to improve the performance of paging.

→ The TLB contains frequently referred page numbers and corresponding frame numbers.



$$\text{TLB Access time} = c$$

$$\text{TLB hit ratio} = \alpha$$

$$\text{EMAT} \Rightarrow \alpha(c+m) + (1-\alpha)(c+m+m)$$

$$\text{EMAT} \Rightarrow (\alpha(c+m)) + (1-\alpha)(c+2m)$$

\downarrow TLB hit \downarrow TLB miss

- Q-1

Consider a system which has main memory Access time = 100 ns and TLB access time = 20 ns and TLB hit ratio 95% then what is the effective memory access time with TLB and without TLB.

$$\rightarrow m = 100 \text{ ns}$$

$$\text{TLB} = 20 \text{ ns}$$

$$\alpha = 95\% \Rightarrow 0.95$$

(i) with TLB:

$$\text{EMAT} = \alpha(m+c) + (1-\alpha)(c+2m)$$

$$= 0.95(120) + (1-0.95)(20+200)$$

$$= 0.95 * 120 + 0.05 * 220$$

$$= 114 + 11$$

$$= 125 \text{ ns}$$

(iii) without TLB:

$$EMAT = 2m$$

$$= 2 \times 100$$

$$= 200 \text{ ns}$$

Q. 2

What hit ratio is required to reduce effective memory access time from 300ns without TLB to 250 with TLB.

TLB Access time is 60ns.



$$\text{without TLB} = 300 \text{ ns}$$

$$EMAT \Rightarrow 2m \Rightarrow 300 \text{ ns}$$

$$m \Rightarrow 150 \text{ ns.}$$

with TLB = 250.

$$EMAT = x(c+m) + (1-x)(c+2m)$$

$$\Rightarrow 250 = x(60+150) + (1-x)(60+300)$$

$$\Rightarrow 250 = 210x + 360 - 360x$$

$$\Rightarrow 150x = 110$$

$$\Rightarrow x = 11/15$$

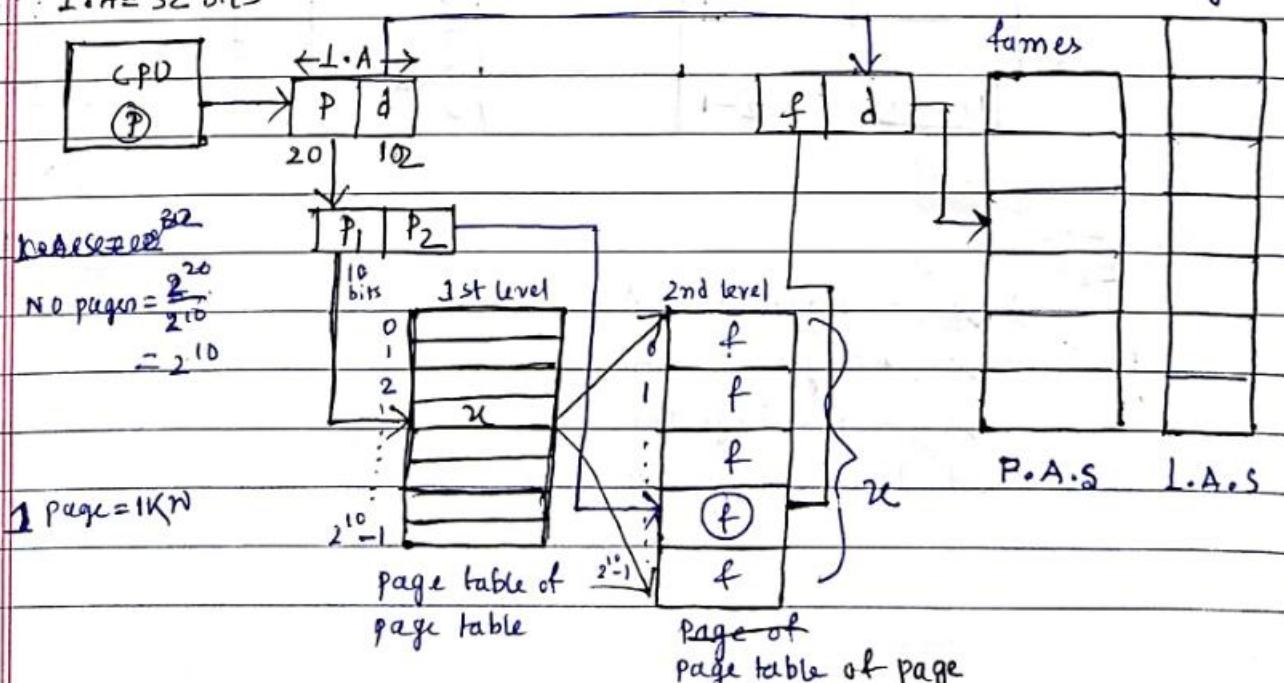
$$\Rightarrow x = .733$$

$$\Rightarrow x = 73.3\%$$

MULTI LEVEL Paging:

L.A = 32 bits

Pages



→ To avoid overhead of maintaining large page tables, the multilevel paging will be implemented.

→ In the multilevel paging, the paging will be applied on page table.

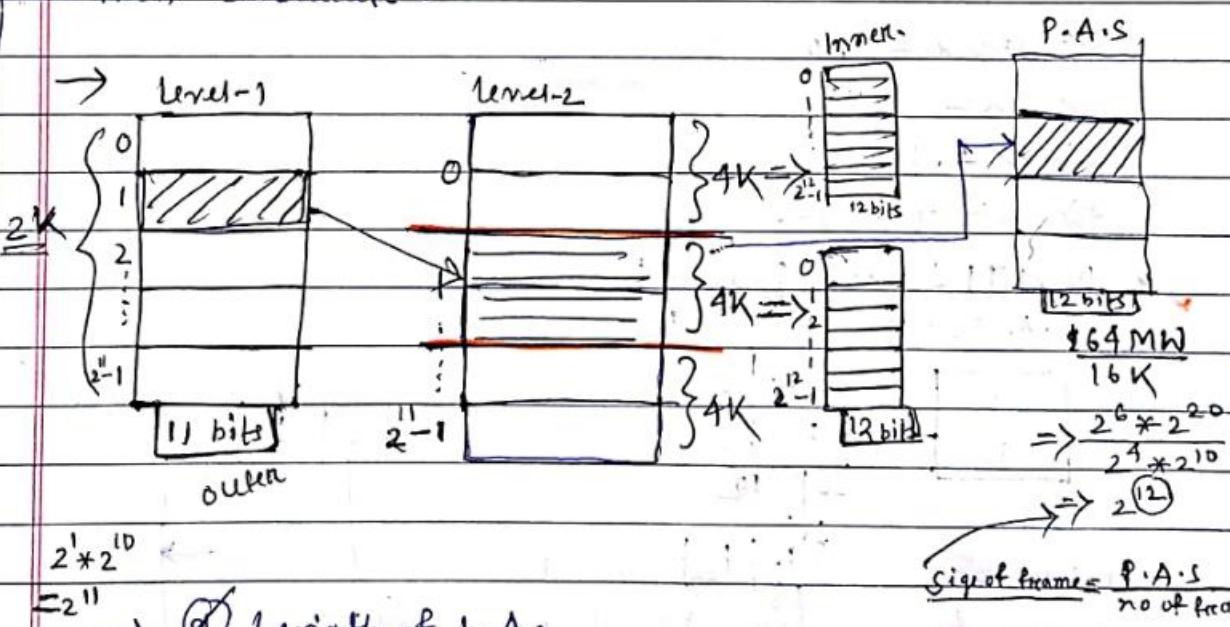
$P_1 \rightarrow$ No of bits required to represent the page of page table.

$P_2 \rightarrow$ The no of bits required to represent the page size of page table.

$\kappa \rightarrow$ Address of page of page table.

Q-1 Consider a system with 2 level paging applicable.

The page table has been divided into 2K pages. Each of size 4K words. If P.A.S is having 64 MW, which is divided into 16 K frames, and the page table entry size is 4 Bytes, then calculate.



- Length of L.A. 2^{11}
- Length of PA 2^{12}
- Outer page table size $2^{11} \times 2^{10}$
- Inner page table size $2^{12} \times 2^{10}$
- Size of frame = $\frac{P.A.S}{\text{no of frame}}$

$$(a) (11+12+12) \Rightarrow 35 \text{ bits.}$$

$$(b) 64 \text{ MB} \Rightarrow 2^6 \times 2^{20} \Rightarrow 2^{26}$$

$$= 26 \text{ bits}$$

$$(c) 2K \times 4 \text{ Byte}$$

$$\Rightarrow 2^10 \times 4$$

$$\Rightarrow 2^{13} \text{ Bytes.}$$

$$(d) 4K \times 4 \text{ Bytes.}$$

$$= 2^{12} \times 2^2$$

$$= 2^{14} \text{ Bytes.}$$

Q3-2

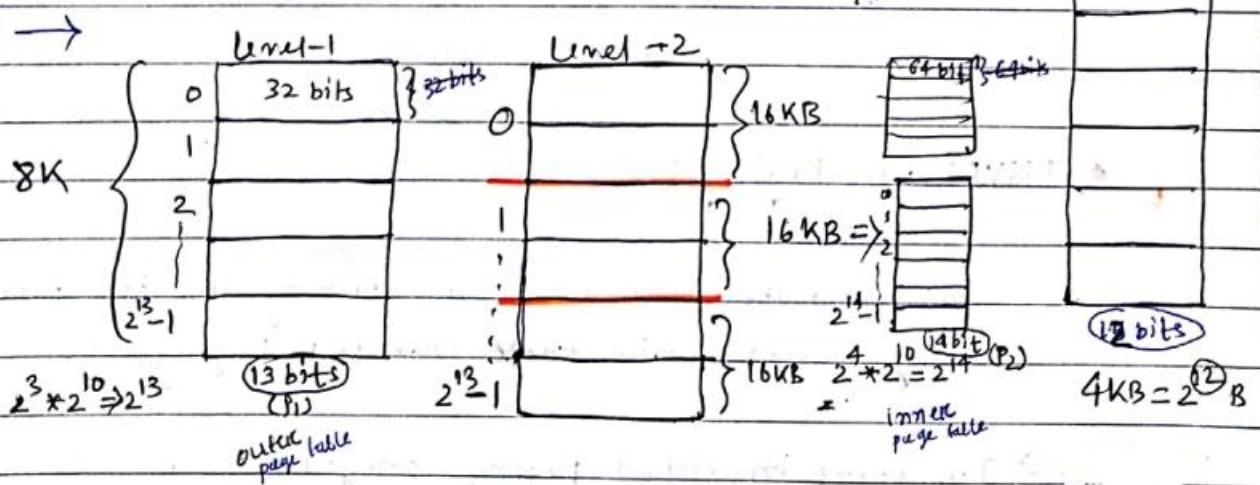
Consider a system with 2-level paging applicable. The page table is divided into 8K pages, each of 16KB. The memory is byte addressable. If the P.A.S is 128 megabytes which is divided into 1KB frames. The page table entry size of outer page table is 32-bits and page table entry size of inner page table is 64-bits. The calculate -

a) Length of LA. $(13+14+18)$ bits $\Rightarrow 45$ bits.

b) Length of PA. $2^{27} \Rightarrow 27$ bits.

c) Outer page table size. $32 \times 8K \Rightarrow 2^5 \times 2^9 \times 2^{10} \Rightarrow 2^{24}$ bits $\Rightarrow 2^{15}$ Bytes

d) Inner page table size. $\frac{64 \times 16 \text{ KB}}{\text{bit}} = \frac{(2^{6-3} \times 2^{4+10}) \text{ B}}{2^{11}} \Rightarrow 2^{17}$ Bytes. P.A.S

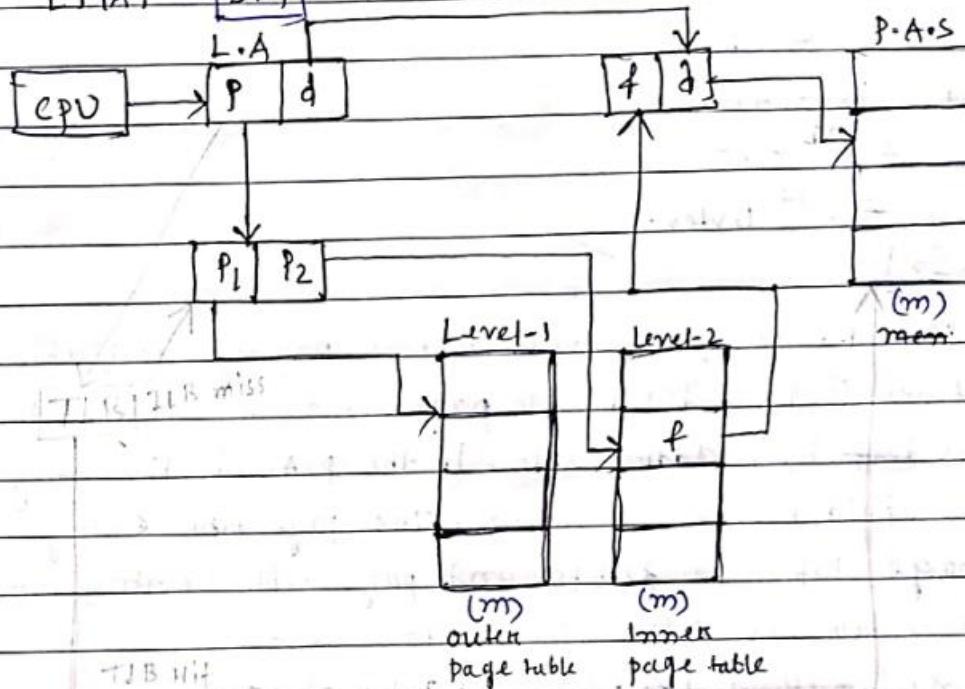


• Performance of 2 Level paging without TLB :-

Let the main memory access time = m^2 .

→ If all the page tables are stored in the main memory.

$$EMAT = 3m$$



→ If the TLB is added to improve the performance. The TLB contains frequently referred page No's and corresponding frame no.

$$EMAT = \alpha(c + m) + (1 - \alpha)(c + 3m)$$

TLB HIT

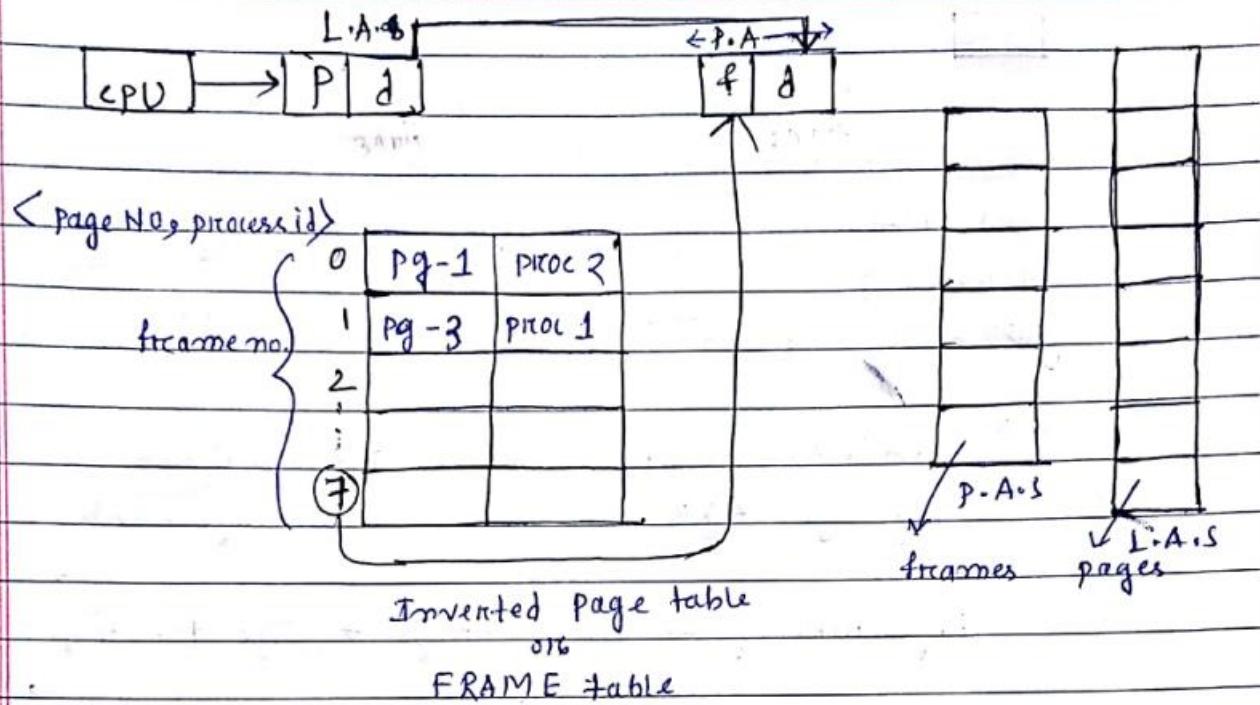
TLB miss

$\alpha = TLB \text{ access time}$

✓ INVERTED Paging :-

→ To Avoid the overhead of maintaining the page table of every process, the ~~not~~ Inverted paging will be implemented.

→ In Invert Inverted paging only 1 page table is maintained for all the process.



Q-1

Consider a system with Logical Address = 34 bits and physical Address = 29 bits. The page size is 16 KB. The memory is byte Addressable. The page table entry size is 8 bytes. The calculate

1) conventional page table size.

✓ 2) Inverted page table size.

→ 1) conventional p.T size,

$$\boxed{\text{No of entry} = \text{no of page}}$$

$$\text{P.T size} = \frac{\text{No of entry}}{\text{size of entry}} \times \text{size of page table}$$

$$\text{No of entry} = \frac{\text{P.A.S}}{\text{page size}} \Rightarrow \frac{2^{34} \text{ bits}}{16 \text{ KB}} \Rightarrow \frac{2^{34}}{2^{19}} \Rightarrow 2^{20}$$

$$\text{P.T size} = 2^{20} \times 8 \text{ byte}$$

$$= 8 \text{ MB.}$$

✓ 2) Inverted page table size,

$$\boxed{\text{No of entry} = \text{no of frames}}$$

$$\text{No of entry} = \frac{\text{L.A.S}}{\text{frame size}} \Rightarrow \frac{2^{34}}{16 \text{ KB}} \Rightarrow \frac{2^{34}}{2^{19}} \Rightarrow 2^{15} \text{ bytes}$$

$$\text{P.T size} = 2^{15} \times 8 \text{ b} \Rightarrow 2^{18} \text{ B}$$

$$\Rightarrow 2^8 \times 2^{10} \text{ B} \Rightarrow 256 \text{ KB.}$$

Q-2

Consider virtual Address space of 32 bits and page size of 4 KB.
 Consider RAM of 128 KB. The what will be the ratio of page table and inverted page table size of each entry in both is of 4 Bytes?

- (a) $2^{15}:1$ (b) $2^{20}:1$ (c) $2^{10}:1$ (d) None of the above.

$$\rightarrow L.A(v.A) = 32 \text{ bits}$$

$$\text{page size} = 4 \text{ KB}$$

$$P.A.S = 128 \text{ KB}$$

$$\text{frame size} = 4 \text{ KB}$$

$\text{Page table size} = \text{no of entries} * \text{size of entries}$

$$\begin{aligned} P.T_N &= \left(\frac{2^{32}}{4 \text{ KB}} \right) * 4B \\ &= \left(\frac{2^{32}}{2^{12}} \right) * 4B \\ &= 2^{20} * 4B. \end{aligned}$$

$$\begin{aligned} P.T_{INV} &= \left(\frac{2^7 * 2^{10}}{4K} \right) * 4B \\ &= \frac{2^7}{2^{12}} * 4B \\ &= 2^5 * 4B. \end{aligned}$$

$$\text{ratio} \Rightarrow \frac{P.T_N}{P.T_{INV}} \Rightarrow \frac{2^{20} * 4}{2^5 * 4} \Rightarrow \frac{2^{15}}{1} = 2^{15}:1$$

Q-3

Suppose that a certain computer with paged virtual memory has 4 KB pages. A 32-bit byte addressable virtual address and 30 bit byte addressable physical address. The system manages an inverted page table. Where each entry includes the page number plus 12 overhead bits. How big is the basic inverted page table including number and overhead bits?

- (a) 2^{10} Bytes (b) 2^{20} Bytes (c) 2^{30} Bytes (d) 2^{32} Bytes.

$$\rightarrow \text{Page size} = 4 \text{ KB}$$

$$P.A = 30 \text{ bit}$$

$$L.A = 32 \text{ bits}$$

P.T size = no of entries * size of entry

$$\begin{aligned}
 &= \left(\frac{P.A.S}{\text{Size of frame}} \right) * \left(\frac{20 \text{ bit}}{\text{Pg.NO} + 12 \text{ bits}} \right) \\
 &= \left(\frac{2^{30}}{2^{12}} \right) * (20 \text{ bit} + 12 \text{ bit}) \\
 &= 2^{18} * 32 \text{ bit} \\
 &= 2^{18} * 4 \text{ Bytes.} \\
 \boxed{\text{P.T size} = 2^{20} \text{ Bytes}}
 \end{aligned}$$

Q-4 Assume a machine with 64 MB physical memory and 32 bit virtual Address. If the page size is 4 KB, then what is the approximate size of the page table?

- (a) 16 MB (b) 1 MB (c) 24 MB (d) 2 MB

\rightarrow P.T size = no of entries * P.T entry size

(i) $P.A.S = 64 \text{ MB}$ | $2^6 * 2^{20} = 2^{26}$

(ii) $P.A = 26 \text{ bit}$

(iii) virtual address ($V.A$) = 32 bits

(iv) page size = $4 \text{ KB} = 2^{12} \text{ Byte}$.

$$\frac{\text{no of entry}}{\text{per page}} = \frac{2^{32}}{2^{12}} \Rightarrow 2^{20}$$

$P.T \text{ entry size} = 19 \text{ bit} (= 16 \text{ bit})$
 \downarrow
frame size

$P.T \text{ size} = 2^{20} * 16 \text{ bit}$

$= 2^{20} * 2 \text{ byte}$

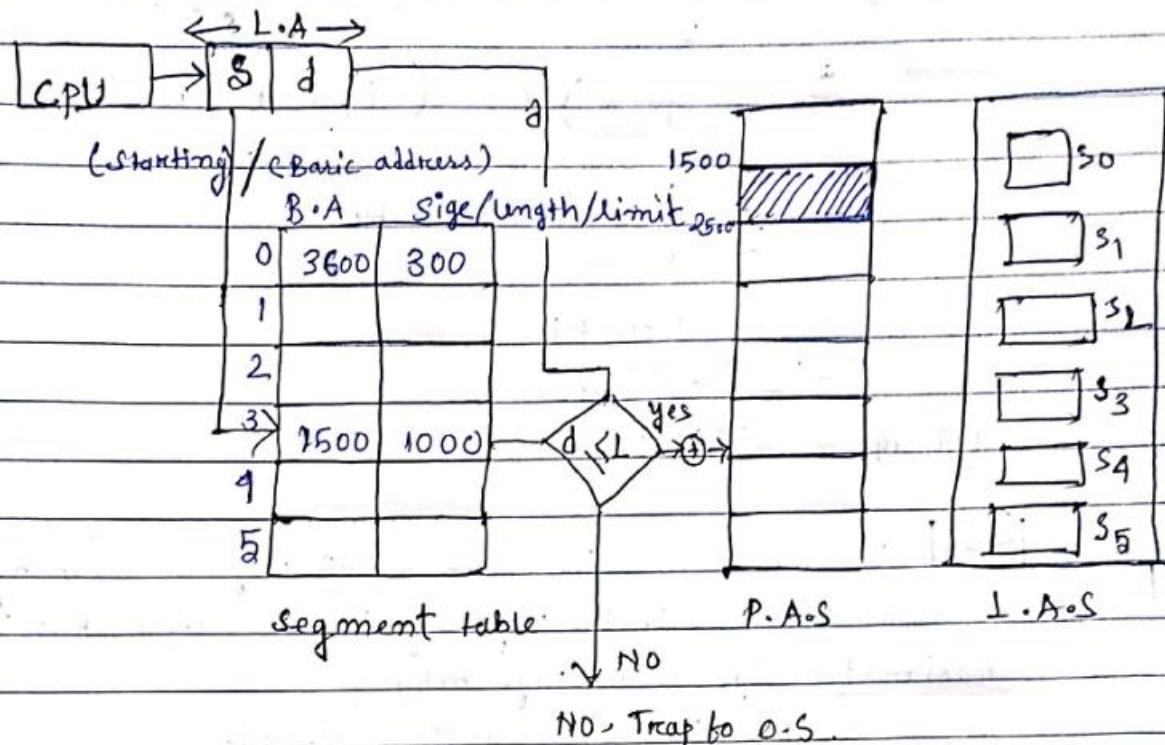
$= 2 \text{ MB}$

$$\text{no of frame} = \frac{P.A.S}{\text{Page size}}$$

$$= \frac{2^{26}}{2^{12}}$$

$$= 2^{14}$$

SEGMENTATION & SEGMENTED PAGING:



Some points:-

- No of entries in segment table = No of segments in L.A.S.
- The paging does not follow the user's view of memory allocation.
- To achieve user's view of memory allocation, the segmentation will be implemented.
- In segmentation, the L.A.S is divided into segments.
- The segments will vary in size.
- ⑤ → No of bits required to represent the segments of L.A.S or segment no.
- ⑥ → Segment offset No of bits required to represent segment size are word no of the segment.

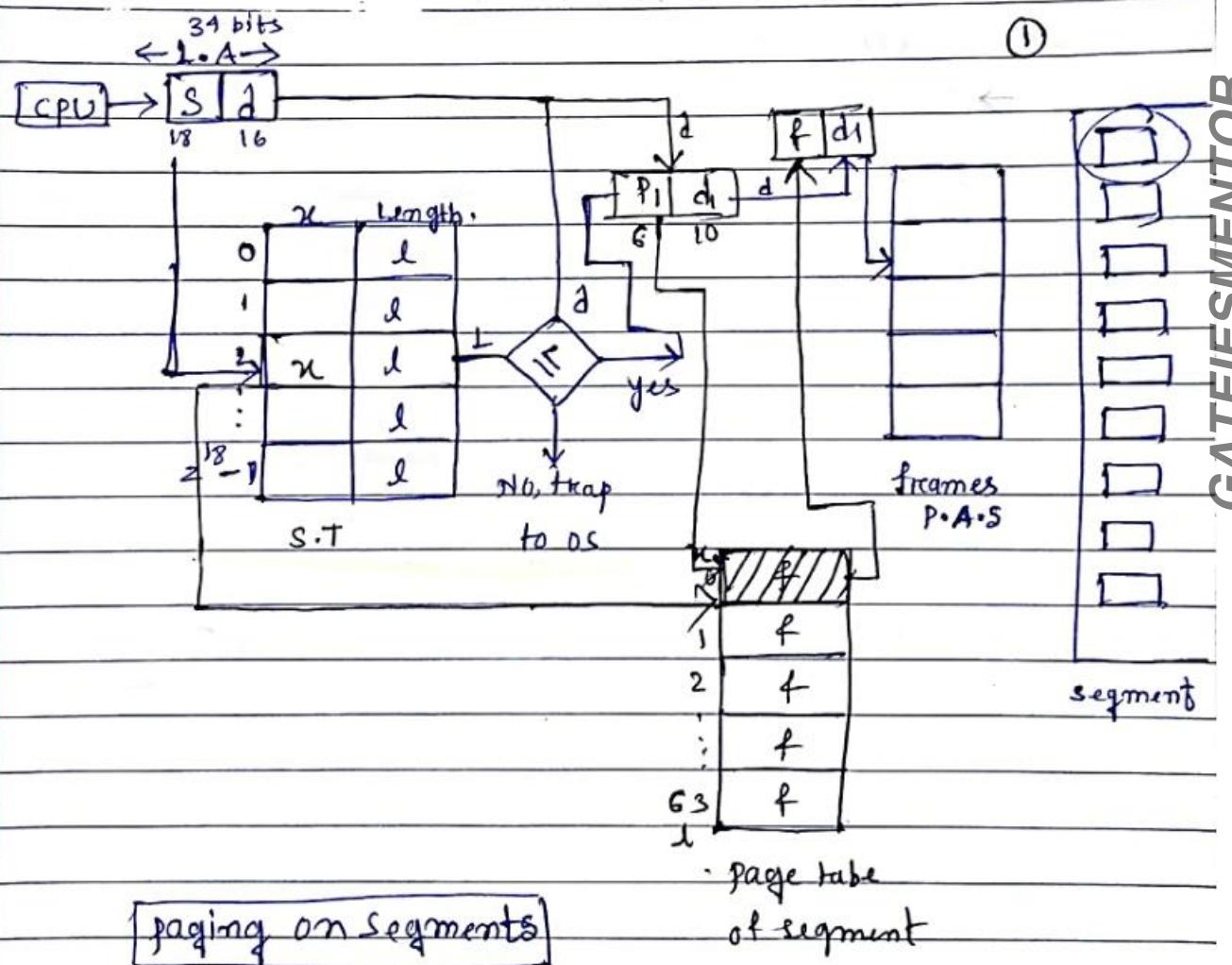
→ The variable size segments are brought into P.A.S so that the segmentation is just behaving like variable partition scheme.



Hence it suffers from External fragmentation.

- Paging on segmentation when segment size increase:

→ problems of external fragmentation and lengthy search times can be solve by paging the segments.



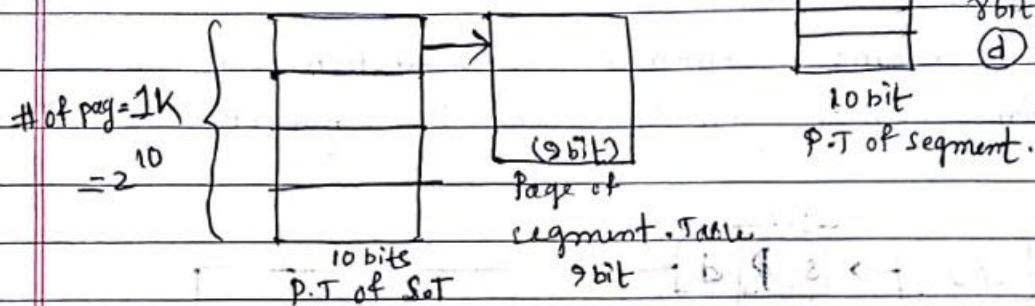
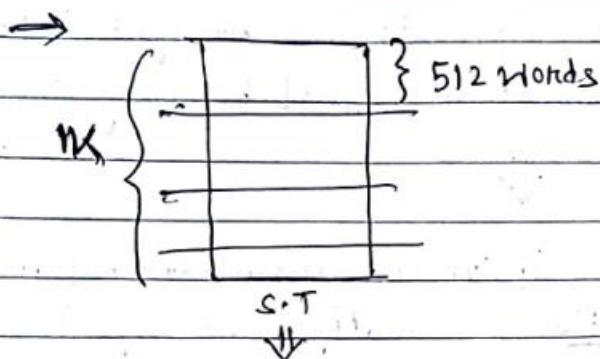
calculate -

1) length of L.A. $\rightarrow (10+9+10+8) \rightarrow 37$ bit

2) Length of P.A. $\rightarrow 18$ bit + 8 $\rightarrow 26$ bit

3) Page table size of segment $\rightarrow 1K \times 9$ byte $\rightarrow 4KB$,

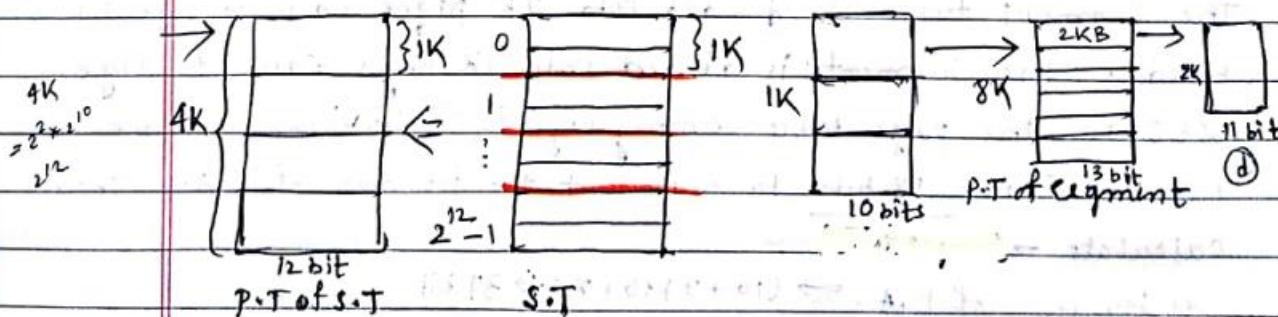
4) Page table size of segment table $\rightarrow 1K \times 4B \rightarrow 4KB$

55
512
8

Q-2

Consider a system using segment paging Architecture. The segment is divided into 8K pages each of size 2KB and segment table is divided into 4K pages each of size 1KB. The memory is byte addressable. The P.A.S is 64 MB. The page table entry size is 32 bits. Then calculate -

- ✓ 1) Length of L:A. $\rightarrow (12 + 10 + 13 + 11) \rightarrow 46$ bit.
- ✓ 2) Length of P.A. $\rightarrow 26$ bits.
- ✓ 3) page table size of segment $\rightarrow 2^{13} * 4$ byte $\rightarrow 2^{15}$ Byte $\rightarrow 32$ KB
- ✓ 4) page table size of S.T. $\rightarrow 4K * 4B \rightarrow 16$ KB
- 5) The no of frames in P.A.S $\rightarrow 2^{15}$ Byte.



$$\text{no of frame} = \frac{\text{P.A.S}}{\text{Byte of frame}} = \frac{2^{26} B}{2^{15} B} = 2^{15} = 2^{22} \text{ M}$$

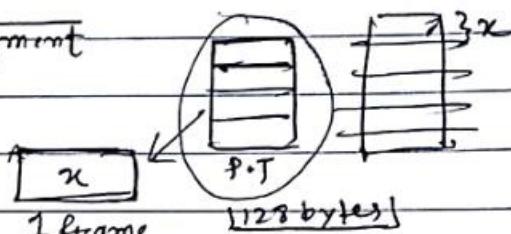
Q-3

Consider a system using segmented paging architecture where $L.A.S = P.A.S = 2^{16}$ Bytes.

$L.A.S$ is divided into 8 equal size segments. The segment is divided into equal size pages which are in the powers of 2 in term of page size. The memory is byte addressable. The page table entry size is 2 bytes. The page tables are stored in the main memory. What must be the page size of segment in Bytes so that the page table of the segment exactly fits in 1 page frame?

$$\rightarrow \text{size of segment} = \frac{2^{16}}{8} = \frac{L.A.S}{\text{no of segment}} \\ = 2^{13} \text{ bytes.}$$

$$P.T \text{ size} = \frac{2^{13}}{n} * 2 \text{ byte}$$



$$\Rightarrow \frac{2^{14}}{n} = n \\ \Rightarrow \frac{2^{14}}{2^y} = 2^y$$

$$\Rightarrow 2^{2y} = 2^{14}$$

$$y = 7$$

$$[P.T \text{ size} = \text{no of entry} * \text{size of entry}] \\ = \left(\frac{\text{no of pages}}{n} \right) * 2$$

$$2^7 = 128$$

- **VIRTUAL MEMORY:**

Virtual Memory gives an illusion to the programmers that programs of larger size than actual physical memory can be executed.

Example :- If program size = 200KB

And Available P.A.s = 100KB.

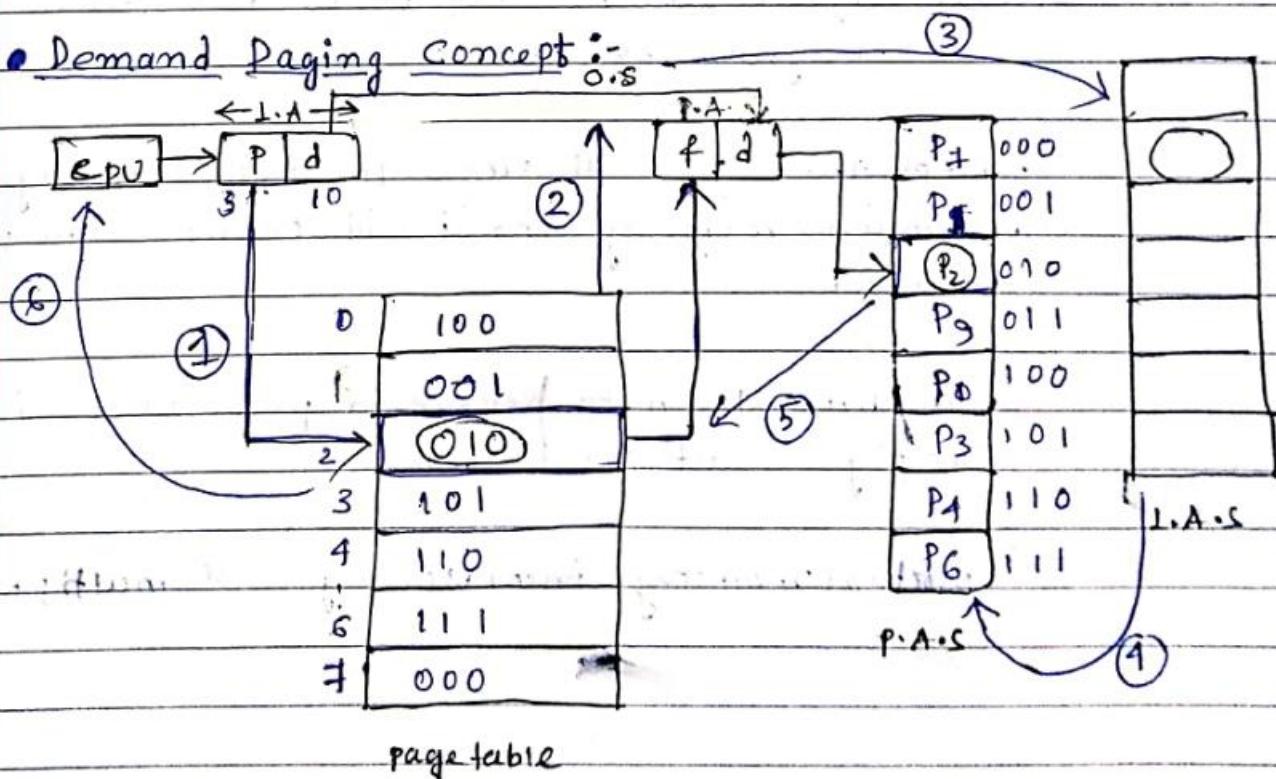
- Virtual Memory will be implemented using -

- ① Demand paging,
- ② Demand segmentation.

→ If we are using paging technique as memory management technique then we use demand paging.

→ If we are using segmentation as Memory Management technique, we use demand segmentation.

- Demand Paging Concept :-



pagetable

- Demand paging Conclusion :

Step 1):- The CPU is trying to access a page which is not available in the main memory, hence page fault occurs.

Step 2):- The program execution will be stopped and the signal will be send to the O.S regarding the page fault. Then the O.S authenticates the validity of the process.

Step 3):- Then O.S will be search for required page in the L.A.S.

Step 4):- The required page will be brought from L.A.S to P.A.S. The page replacement Algorithms will be used, for decision making of replacing of page in the P.A.S.

Step 5):- The page table will be uploaded accordingly.

Step 6):- Signal will be sent to CPU to continue the program execution.

Then CPU the CPU will access the required page from the main memory and it will continue the program execution:

→ The time taken to service a page fault is called as page fault service time.

→ Virtual memory increases degree of multiprogramming.

• Demand Paging Performance:

→ Loading the page into memory on Demand.
(Whenever the page fault occurs)

→ The page fault service time includes the time required to perform all the 6 steps.

→ If page fault service time = S

Main memory access time = M .

page fault rate = P .

Then
$$\text{EMAT} = P \times S + (1-P) M$$

As $S \gg M$.

page table access time is negligible in comparison to S , so we ignore it for page fault.

Virtual memory (Q-1)

Consider a system which has main memory access time = 10 ms
page fault service time = 200 ms . page hit ratio is 95%
What is EMAT. (S) (P)

→
$$\text{EMAT} = P \times S + (1-P) \times m$$

(Page fault)
 $P = 1 - 0.95$
 $= 0.05$

$$\Rightarrow 0.05 \times 200 + (1 - 0.05) \times 10$$

$$= 2 \times 95 + 0.5 \times 10 \Rightarrow 190 + 5$$

$$= 195 \text{ ms.}$$

$$= 195 \text{ ms.}$$

* $1\text{ms} = 10^6\text{ns}$

B-2

Suppose if an instruction takes i microseconds and additional j usec if the page fault occurs. What is the effective instruction Access time. If the page fault occurs on an average for every K instruction.

- (a) $i + \frac{j}{K}$ (b) $j + \frac{i}{K}$ (c) $K + \frac{i}{j}$ (d) $i + \frac{j}{K}$.

$$\rightarrow \begin{cases} m \Rightarrow i & \text{(1)} \\ s \Rightarrow i + j \text{ usec} & \text{(2)} \end{cases}$$

$$P \Rightarrow \frac{1}{K} \quad \text{(3)}$$

$$\begin{aligned} EMAT &= P * s + (1-P) * m \\ &= \frac{1}{K} (i + j) + (1 - \frac{1}{K}) * i \\ &= \frac{(i+j)}{K} + \frac{(K-1)}{K} * i \\ &= \frac{1}{K} (i + j + K(i - 1)) \\ &= \frac{j}{K} + i \end{aligned}$$

$EMAT = i + \frac{j}{K}$

GATE
2011

B-3 (3) the page fault service time is 10ms and the main memory access time is 20 ms. If one page fault is generated for every 10^6 memory access. Then what is the effective Access time for memory.

- (a) 21 ns (b) 30 ns (c) 23 ns (d) 35 ns.

$$\rightarrow s \Rightarrow 10\text{ms} \Rightarrow 10^7\text{ns},$$

$$m \Rightarrow 20\text{ms},$$

$$P = \frac{1}{10^6}$$

$$EMAT = P * s + (1-P) * m$$

$$\begin{aligned} &= \frac{1}{10^6} * 10^7 + (1 - \frac{1}{10^6}) * 20 \\ &= 10 + 20 - \frac{20}{10^6} \\ &= 30 - \left(\frac{20}{10^6} \right) \Rightarrow 30 - 0 \\ &\approx 0 \Rightarrow 30. \end{aligned}$$

Q-4

Consider a demand paging environment and it takes 8ms to service a page fault, if either an empty frame is available or replaced page is not modified and it takes 20ms, if the replaced page is modified. Assuming main memory access time is 1ms. Further assume that page to be replaced is modified 70% of time. Then what is the maximum acceptable page fault rate to get an EMAT not more than 2ms.

(a) $P = 0.32$ (b) $P = 0.064$

(c) $P = 0.16$ (d) $P = 0.72$.

→

$$S \rightarrow 8 \text{ ms} \quad (\text{pg modified}) \times \left\{ \begin{array}{l} 70\% \\ 20 \text{ ms} \quad (\text{pg modified}) \end{array} \right. \quad P = ?$$

$$\downarrow \quad \downarrow$$

$$m \rightarrow 1 \text{ ms}$$

$$E.MAT = P \times S + (1-P) \times m$$

$$P \times [0.70 \times 8 \text{ ms} + (0.30 \times 20 \text{ ms})] + P(1-P) \leq 2$$

$$15.4P \leq 1$$

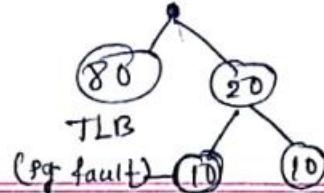
$$P \leq 0.069.$$

Q-5 Consider a system where the page fault service time is 200ms and main memory access time = 10ms. The TLB is added to improve the performance. The 80% references are found in the TLB and that of remaining 10% cause page fault. The TLB access time and page table access time are negligible, then what is EMAT.

(a) 12.8 ms (b) 13.8 ms (c) 14.8 ms (d) 15.8 ms

$$S \rightarrow 200 \text{ ms}$$

$$m \rightarrow 10 \text{ ms.}$$



$$EMAT = .80 * (10 \text{ ms}) + .20 [P * s + (1-P) * m]$$

$$= .8 + .20 [1 * 200 + 0.9 * 10]$$

$$= .80 + [13.8 \text{ ms}]$$

✓ • Page Replacement : (Algorithms) -

- 1) FIFO \rightarrow First in First out.
- 2) optimal page Replacement.
- 3) Least Recently Used (LRU).
- 4) Most Recently Used (MRU)

Page replacement FIFO -

Question-1

Reference string : 7, 0, 1, 2, 0, 3, 0, 4, 2, 3, 0, 3, 2, 1, 2, 0, 1, 7, 0, 1
1, 7, 0, 1

Assume 4 frames are allocated to the process.

→	7	0	1	2	0	3	0	4	2	3	0	3	2	1	2	0	1	7	0	1
				2	2	1	2	2	2	2	2	2	2	X	1	1	1	1	1	
				1	1	1	1	1	1	X	0	0	0	0	0	0	0	0	0	
				0	0	0	0	X	4	4	4	4	4	4	4	4	4	X	7	
				7	7	7	7	X	3	3	3	3	3	3	X	2	2	2	2	
*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	

↓
(page fault)

10 page faults

Q-2

Reference string : 7, 0, 1, 2, 0, 3, 0, 4, 2, 3, 0, 3, 2, 1, 2, 0, 1, 7, 0, 1.

Assume 3 frames are allocated to the process.

7	0	1	2	0	3	0	4	2	3	0	3	2	1	2	0	1	7	0	1
		1	1	1	1	0	0	0	3	3	3	3	3	2	2	2	2	2	2
0	0	0	0	3	3	3	2	2	2	2	2	1	1	1	1	1	0	0	
†	†	†	2	2	2	4	4	4	0	0	0	0	0	0	0	0	†	†	†

↖ * * * * (page fault)

total page fault - 15]

Q-3

Reference String: 1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5.

(1) Using 3 frames.

1	2	3	4	1	2	5	1	2	3	4	5
		3	3	3	2	2	2	2	3	4	4
2	2	2	1	1	1	1	1	1	3	3	3
1	1	1	4	4	5	5	5	5	5	5	5

total page fault - 9]

(2) Using 4 frames.

1	2	3	4	1	2	5	1	2	3	4	5
		4	4	4	4	4	4	4	3	3	3
3	3	3	3	3	3	3	2	2	2	2	2
2	2	2	2	2	2	1	1	1	1	1	5

total page fault - 10]

CONCLUSION -

In Reference string 1, 2, 3, 4, 2, 5, 1, 2, 3, 4, 5.

3 frames → 9 page fault.

4 frames → 10 page fault.

BELADY'S ANAMOLY

By increasing the no of frames to the process, we should get less no of page fault, but instead they are increasing. This problem is called as Bellady's Anomaly.

Page Replacement (LRU):

(Least Recently Used)

[Q-1]

[In the event of page fault replace the page which is least recently used].

Reference String :- 7, 0, 1, 2, 0, 3, 0, 4, 2, 3, 0, 3, 2, 1, 2, 0, 1, 7, 0, 1.

(i) Using 3 frames.

①	0	1	②	0	3	0	4	2	3	0	3	2	1	2	0	1	7	0	1
	1	1	1	X	3	3	3	2	2	2	2	2	2	2	X	7	7	7	
	0	0	0	0	0	0	0	X	3	3	3	3	3	X	0	0	0	0	

page fault \rightarrow 12.

Page Replacement (Optimal PR):

[Q-1] [in the event of page fault replace the page which is not used for longest duration of time in future].

Reference String :- 7, 0, 1, 2, 0, 3, 0, 4, 2, 3, 0, 3, 2, 1, 2, 0, 1, 7, 0, 1.

(ii) Using 4 frames.

7	0	1	2	0	③	②	4	2	3	0	3	2	①	2	0	1	7	0	1
	2	2	2	2	2	2	2	2	2	2	2	2	2	2	X	2	2	2	
	1	1	1	1	X	4	4	4	4	4	4	4	4	X	4	4	4	7	

FIFO

Total page fault \rightarrow 88

• Page Replacement

• Most Recently Used (MRU):

In the event of page fault, replace the page which is most recently used.

(Q-1)

Reference string: 7, 0, 1, 2, 0, 3, 0, 4, 2, 3, 0, 3, 2, 1, 2, 0, 1,
7, 0, 1.

(i) Using 4 frames.

7	0	1	2	①	3	0	4	2	3	0	3	2	1	2	0	1	7	0	1
				2	2	2	2	2	②	③	①	③	2	2	②	0	0	0	0
.	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	0	①	③	①	9	4	4	4	4	4	4	4	4	4	4	4	4
7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7
*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*

Total page fault $\rightarrow 11$

• **(Q-practice)** (second)

The Address Sequence generated by tracing a particular program executing in a pure Demand paging System with 100 records per page with 1 free memory frame is given as follows.

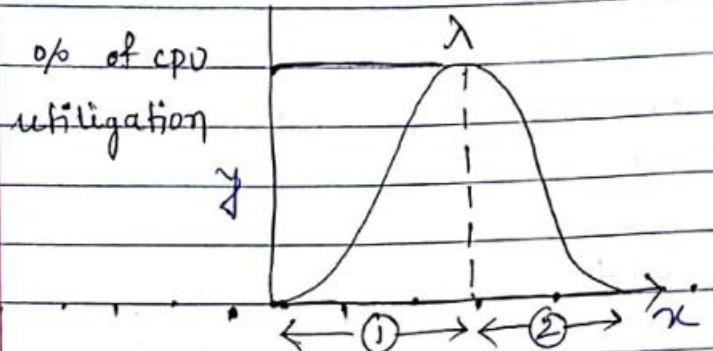
0100, 0200, 0400, 0499, 0510, 0530, 0560, 0120, 0220,
0240, 0260, 0320, 0370.

What is the number of page fault?

- A 7 B 8 C 9 D 10.

records	page no	here frame $\rightarrow 1$
0-99	0	reference string -
100-199	1	1, 2, 4, 4, 5, 5, 5, 1, 2, 2, 2, 3, 3
200-299	2	1 2 4 4 5 5 5 1 2 2 2 3 3
300-399	3	X X 4 4 5 5 5 1 2 2 2 3 3
400-499	4	* * * * *
500-599	5	Total page fault $\rightarrow 7$

• Thrashing Introduction:



→ In the initial degree of multiprogramming the CPU utilization is very high and the system resources are utilized 100%.

→ If you further increase the degree of multiprogramming after some extent of point i.e. the CPU utilization will drastically fall down and time taken to complete every request will increase and system will spend more time only in page replacement. This is called Thrashing.

Example - Let free frames = 300.

Phase ① - # of process = 100

③

Phase ② - # of process = 300

①

• Thrashing Causes And Recovery

ⓐ Causes :-

- ① High degree of multiprogramming.
- ② Lack of frames.

ⓑ Recovery from Thrashing :-

① Don't allow the system to go into thrashing. Insist the long term scheduler not to bring process beyond the point of λ .

② Allow the system to go into thrashing, then insist the mid term scheduler to suspend the processes so that system may recover from thrashing.

- Thrashing practice [question - 1]

Consider a system with below statistics observation.

1) CPU utilization \rightarrow 10 %.

2) paging on disk \rightarrow 90 % \rightarrow (page replacement).

Then which one of following will increase the CPU utilization-

1) Install the faster CPU \rightarrow NO

2) Install the faster disk \rightarrow NO

3) Increase degree of multiprogramming \rightarrow NO

4) Decrease the degree of multiprogramming \rightarrow YES.

5) Install more main memory \rightarrow YES

6) Decrease the page size \rightarrow NO

7) Increase the page size \rightarrow YES.

✓

FILE AND DEVICE MANAGEMENT

- File : → collection of logically related entities.

Attributes :-

- file context
 ↓
 FCB
 ↓
 file control block
- 1) Name .
 - 2) size .
 - 3) type .
 - 4) Permissions
 - 5) Location .
 - 6) Creation date .
 - 7) Last Modified date .
 - 8) owner / Author .
 - 9) password .

Types of files :-

- 1) . doc
- 2) . jpg .
- 3) . pdf .
- 4) . dll .
- 5) . obj .

- Operations on the file -

- 1) creat .
- 2) open .
- 3) read .
- 4) write .
- 5) update .
- 6) truncate .
- 7) scan
- 8) copy
- 9) delete
- 10) Rename
- 11) close .

- Access Methods of files -

↓
 Sequential Access

↓
 Random Access

* For better classification of files they stored in ^{are} the Directories.

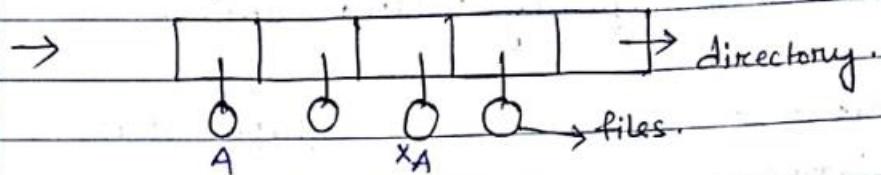
Directory Structure :

↓
 single Level

↓
 True Level / multi level

↓
 Acyclic Graph

Single level Directory :-



Advantage:- Implementation is Easy.

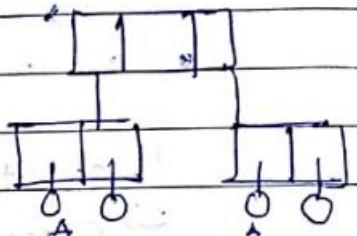
Disadvantage: → Searching time for a specific file will be more.

→ we cannot have two files of same name.

Tree Level Directory :-

Advantage: → Searching time for a specific file will be less.

→ Better classification of files.

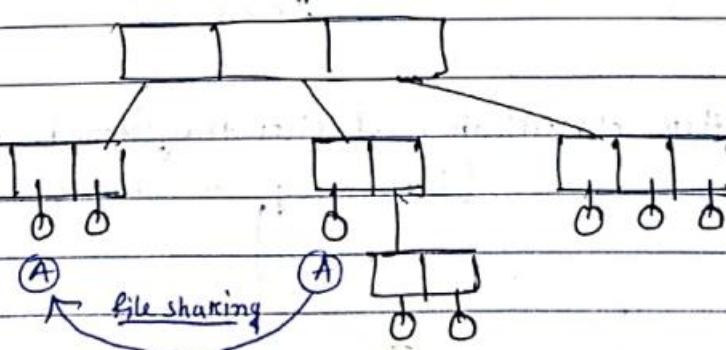


Disadvantages

→ Implementation is difficult.

→ If same file enters in 2 different directories and if 1 file is updated, the other file has to be updated accordingly. If other file is not updated, then there will be inconsistency of data.

Acrylic Graph Directory :-

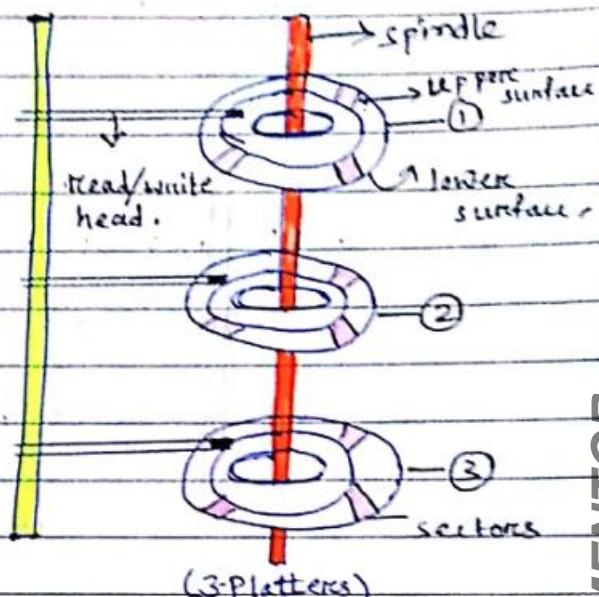
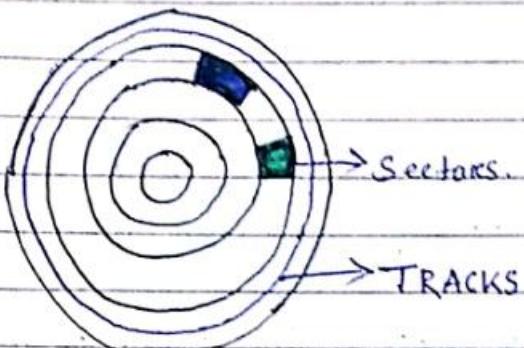


→ Implementation is difficult.

→ Searching time is less.

→ If the same file exist in 2 different directories and 1 file is updated, then other file will be updated automatically by using the concept of file sharing.

- Disk Structure:



Q-1

Consider a disc which has 16 platters. Each platter has 2 surfaces. Every Surface is having 1K tracks. Each track is divided into 512 sectors. Every sector can store the data of 2KB.

calculate

✓ Capacity of disk. (32 GB)

✓ How many bits are required to identify a particular sector of a disk. (24 bit)

→ # of platters → 16

platters have 2 surface.

1K track in each surface.

track divided into 512 sector

(1) →

$$(16 * 2 * 1K * 512 * 2KB)$$

$$\Rightarrow 2^4 * 2^1 * 2^{10} * 2^9 * 2^{11}$$

$$\Rightarrow 2^{35}$$

$$\Rightarrow 32 \text{ (GB)}$$

(2) → Bits to Identify platter. → 4 bit

 + Bits to Identify surface → 1 bit

 + Bits to identify track → 10 bit

 + Bits to identify sector → 9 bit

→ 24 bit

- Disc Terminology:

- DISK I/O Operation:

- { → seek time
- Rotational Latency.
- Transfer time.
- Transfer rate.



The read/write heads can never be outside the tracks.
It will always point to any particular track of the surface.

• Seek time → The amount of time taken to move the R/W heads from its current position to desired track. This time is called as seek time.

• Rotational Latency → the amount of time taken to rotate the R/W heads on the track so that the header comes to exact position (sector).

The rotational latency is considered as $\frac{1}{2}$ of rotation time.

ie.
$$\boxed{\text{Rotational latency} = \frac{1}{2} * \text{Rotation time}}$$

• Transfer time → The amount of time required to transfer the required data, once the read/write heads comes on the desired sector.

→ The transfer time depends on rotational rate of the disk and total size of the track.

• Transfer Rate → The no of bytes transferred per unit time is called as transfer rate of the disk.

18-9

Consider a disk system which has an average seek time of 30 ms and rotational rate of 360 rpm. Each track of the disk has 512 sectors, each of size 512 B.

(i) What is time taken to read 4 successive sectors?

- (a) 0.32 sec (b) 0.16 sec (c) 0.084 sec (d) 0.52 sec.

(ii) What is the data transfer rate?

- (a) 1536 Kbps (b) 1636 Kbps (c) 1436 Kbps (d) 1736 Kbps.

(i) Solution = seek time + Rotational latency + transfer time

$$\begin{aligned} &= 30 \text{ ms} + \frac{1}{2} \times \frac{1}{6} \text{ sec} + 0.0013 \text{ sec} \\ &= 30 \times 10^{-3} \text{ sec} + 0.0833 \text{ sec} + 0.0013 \text{ sec} \\ &= [0.084] \end{aligned}$$

$$\begin{aligned} 1 \text{ m} &= 360 \text{ R} \\ 1 \text{ R} &= \frac{60}{360} \text{ sec} \\ R &= \frac{1}{6} \text{ sec} \end{aligned}$$

Transfer time logic = In one rotation time,
we can transfer the total data of the track.

→ To transfer the required data how much time required

Total size of the track = (Sectors * Sector size)

$$= 512 \times 512$$

$$= 2^{18}$$

$$= 256 \text{ KB}$$

Required data = 4 * sector	$256 \text{ KB} \rightarrow \frac{1}{6} \text{ sec.}$
$= 4 \times 512 \text{ B}$	$2 \text{ KB} = \frac{2}{6 \times 256} \text{ sec}$
$= 2 \text{ KB}$	$2 \text{ KB} = 0.0013 \text{ sec}$

(ii) Data transfer rate: In one rotation → we can transfer total size of track.

$$\frac{1}{6} \text{ sec} = 256 \text{ KB.}$$

$$\begin{aligned} 1 \text{ sec} &= 6 \times 256 \text{ KB} \\ &= [1536 \text{ KB.}] \end{aligned}$$

(8-2)

Consider a disk having average seek time of 60 ns and rotational rate of 3600 rpm. Each track of the disk has 512 sectors, each of size of 2 KB.

- (i) What is approx time required to read 1200 random sectors
 (a) 10 sec (b) 20 sec (c) 30 sec (d) 40 sec.
- (ii) What is effective data transfer rate.
 (a) 30 MBPS (b) 40 MBPS (c) 50 MBPS (d) 60 MBPS.

$$\rightarrow \text{① Seek time} = 60 \text{ ns} \\ = 60 \times 10^{-9} \text{ sec.}$$

$$3600 \text{ R} = 60 \text{ sec.}$$

$$1R = \frac{1}{60} \text{ sec.}$$

$$\text{② } R \cdot L = \frac{1}{2} (\text{R.T})$$

$$= \frac{1}{2} \times \frac{1}{60}$$

$$= \frac{1}{120}$$

$$\text{Total track size} = 512 \times 2 \text{ KB} \\ = 2^9 \times 2^{11} \text{ B} \\ = 2^{20} \text{ B}$$

$$2^{20} \text{ B} = \frac{1}{60}$$

$$1 \text{ sec} = 60 \text{ tracks}$$

$$1 \text{ B} = \frac{1}{60 \times 2^{20}} \text{ (T.T)}$$

$$2 \text{ KB} = \frac{2^{11}}{60 \times 2^{20}}$$

$$2 \text{ KB} = 3.255 \times 10^{-5} \text{ sec.}$$

Required time to read 1200 random sectors -

$$(\text{seek time} + \text{rotational latency} + \text{Transfer time}) * 1200 \\ = (60 \times 10^{-9} \text{ sec} + 8.33 \times 10^{-3} \text{ sec} + 3.255 \times 10^{-5} \text{ sec}) * 1200 \\ = [10 \text{ sec Approx}] \quad \text{(i)}$$

(ii) Effective data transfer rate -

$$\frac{1}{60} \text{ sec} = 2^{20} \text{ B} \quad (\text{data transfer per second})$$

$$1 = 2^{20} \times 60 \Rightarrow [60 \text{ MBPS}] \quad \text{(ii)}$$

Q-4

How long does it take to load 64 KB of program from a disk whose 1 rotation time is 20 ms , and seek time is 30 ms and the total size of the track is 32 KB . The paging is applied to the program and program is divided into page of size 2 KB . Assume that pages are spread randomly over the disc.

- (a) 1120 ms (c) 1320 ms
 (b) 1230 ms (d) 1450 ms

$$\rightarrow ① \text{Seek time} = 30 \text{ ms}$$

$$\begin{aligned} ② R.T.L &= \frac{1}{2} \times (R.I) \\ &= \frac{1}{2} \times 20 \\ &= 10 \text{ ms} \end{aligned}$$

of pages 32 ~~KB~~size of the track = 32 KB

$$20 \text{ ms} \rightarrow 32 \text{ KB}$$

$$\begin{aligned} ? &\rightarrow 2 \text{ KB} && (1 \text{ pg transfer} \\ (1.25 \text{ ms}) && (1 \text{ page}) & \text{time}) \end{aligned}$$

$$\begin{aligned} \text{Total time} &= (30 \text{ ms} + 10 \text{ ms} + 1.25 \text{ ms}) * 32 \\ &= 1320 \text{ ms} \end{aligned}$$

Q-5

How long does it take to load 128 KB of program from a disk whose rotation time is 40 ms , and seek time = 60 ms . The total size of the track is 64 KB . The paging is applied on the program and it is divided into 128 pages. Assume that the pages are randomly spread over the disc.

- (a) 30 sec (b) 20.4 sec (c) 10.25 sec (d) 40 sec .

 \rightarrow

$$① \text{Seek time} = 60 \text{ ms}.$$

$$② \text{Rotation time} = 40 \text{ ms}$$

$$\begin{aligned} ③ R.T.L &= \frac{1}{2} * 40 \\ &= 20 \text{ ms}. \end{aligned}$$

$$\text{size of page} = 1 \text{ KB}.$$

$$\text{track size} = 64 \text{ KB}$$

$$64 \text{ KB} = 64000 \text{ ms}$$

$$1 \text{ KB} = \frac{40}{64} \Rightarrow 0.625 \text{ ms}.$$

$$\begin{aligned} \text{Total time} &= (60 \text{ ms} + 20 \text{ ms} + 0.625 \text{ ms}) \\ &= 80.625 * 128 \\ &= 102.625 \text{ ms}. \\ &= 10.24 \text{ sec} \end{aligned}$$

Disc last Question - 6

Consider a disc with below specifications.

- 1) No of surfaces $\rightarrow 8$.
- 2) Inner diameter $\rightarrow 4 \text{ cm}$.
- 3) Outer diameter $\rightarrow 12 \text{ cm}$.
- 4) Inner track distance $\rightarrow 0.2 \text{ mm}$.
- 5) No of sectors per tracks $\rightarrow 20$.
- 6) Sector size $\rightarrow 4 \text{ KB}$.
- 7) Rotational rate of the disc $\rightarrow 3600 \text{ rpm}$.

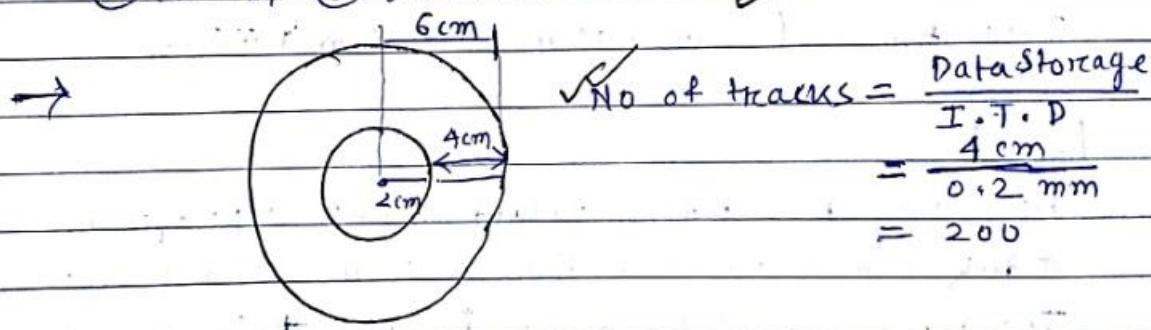
Qs-1

What is the capacity of the disk.

- (a) 128 MB (b) 256 MB (c) 512 MB (d) 1 GB.

Qs-2 What is the data transfer rate of the disc.

- (a) 1800 Kbps (b) 2800 Kbps (c) 3800 Kbps (d) 4800 Kbps



$$\text{Capacity of 1 surface} = 200 * 20 * 4 \text{ KB}$$

$$\begin{aligned} \text{① Capacity of 8 surface} &= 8 * 200 * 20 * 4 \text{ KB} \\ &= [128 \text{ MB}] \end{aligned}$$

② Data transfer rate -

$$60 \text{ sec} = 3600 \text{ R}$$

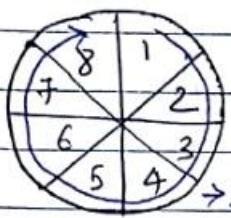
$$1 \text{ R} = \frac{1}{60} \text{ sec.}$$

$$1 \text{ track} = 80 \text{ KB}$$

$$\frac{1}{60 \text{ sec}} = 80 \text{ KB}$$

$$\begin{aligned} 1 \text{ sec} &= 80 * 60 \text{ R} \\ &= [480 \text{ Kbps}] \end{aligned}$$

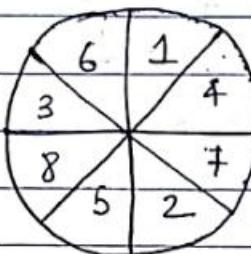
• Disk Interleaving:



NO Interleaving



single Interleaving



double Interleaving

why Interleaving:

Disc Rotation is very fast & hence it cannot detect
(Read/ write @ head)

Q-1

Consider the disc with double interleaving where track is divided into 8 sectors and seek time of the disc is 3 ms and rotational rate of the disc is 3600 rpm. The sector size is 2 KB and rotational latency is still considered as $\frac{1}{2}$ of rotation time. Then calculate

Q1) How much time is required to read all 8 sectors of the track using Double Interleaving disk.

- (a) 74 ms (b) 84 ms (c) 94 ms (d) 104 ms

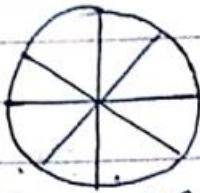
Q2) What is the time difference to read all 8 sectors of the track if the disk is non-interleaving disk.

- (a) 19 ms (b) 55 ms (c) 29 ms (d) 37 ms

Q3) What is the data transfer rate if it is double interleaving disc-

- (a) 249 KBps (b) 319 KBps (c) 149 KBps (d) 449 KBps

→ Q1)



$2.75R$ (Rotation need)

Seek Time + R.T + Transfertime

↓ ↓ ↓

$$30\text{ms} + 0.5R + 2.75 \\ = 30\text{ms} + \underbrace{0.5R + 2.75}_{3.25R}$$

$$3600R = 60\text{ms}$$

$$1R = \frac{1}{60}\text{ms}$$

$$3.25R$$

$$3.25R = \frac{3.25}{60}$$

$$= 30\text{ms} + 54\text{ms}$$

$$= 0.054\text{ms}$$

$$= \boxed{84\text{ ms}}$$

$$= 54\text{ ms}$$

→ Q2)

Total time = (seek time + R.T + T.T)

$$= 30\text{ms} + 0.5R + 1R \\ \downarrow$$

$$1R = \frac{1}{60}\text{ms}$$

$$1.5R = \frac{1.5}{60}\text{ms}$$

$$(1.5R) \rightarrow 25\text{ms}$$

$$= 0.025\text{ms}$$

$$= \boxed{55\text{ ms}}$$

$$= 25\text{ ms}$$

$$84\text{ ms} - 55\text{ ms} = \boxed{29\text{ ms}} \text{ time difference.}$$

→ Q3)

$$2.75R * \frac{60\text{ms}}{3600} = 16\text{KB}$$

$$1\text{ms} = \frac{16\text{KB} * 60\text{ms}}{2.75R}$$

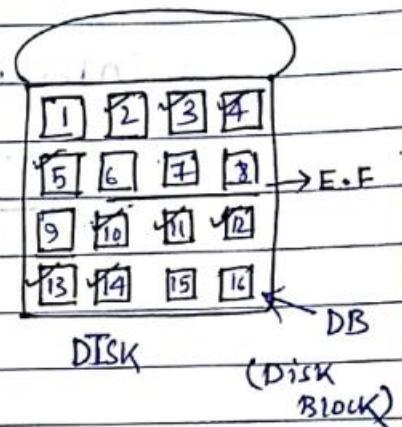
$$= \boxed{349\text{ Kbps.}}$$

• Disk Space Allocation Methods:

- 1) Contiguous Allocation
- 2) Non-Contiguous Allocation / Linked Allocation.
- 3) Indexed allocation.

(1) Contiguous Allocation =

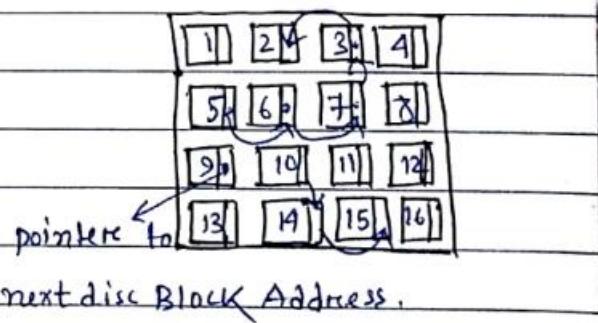
file	starting DBA	size
ABC.doc	2	4
XYZ.doc	10	5



- In contiguous Allocation disc blocks will be allocated in a contiguous manner.
- Increasing the file size is not possible, always.
- It is suffering from external fragmentation.
- Internal fragmentation may exist in the last disc block of the file.
- It supports sequential and Random Access of the file.

(2) Non-Contiguous Allocation =

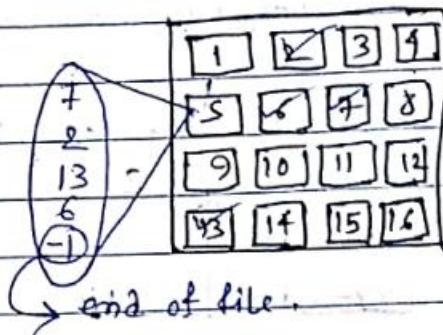
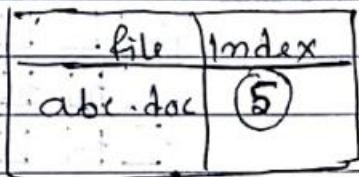
file	starting DBA	ending DBA
abc.doc	5	2
xyz.doc	10	15



- Increasing the file size is possible if free disc block is available.

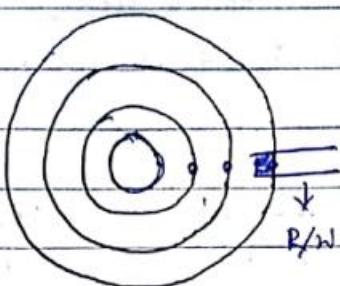
- NO external fragmentation.
- Internal fragmentation may exist in the last disc block or block.
- There is overhead of maintaining the pointer in every disc block. It supports only sequential access of file.

(3) Indexed Allocation -



- In Index Allocation 1 disc block is used just to maintain the disc block address of the file.
- Every file is associated with its own index node.
- If the file is very large 1 disc block may not be sufficient to store disc block address of the file.
- If the file is very very small, wastage of disk block to store the address to maintain the disc block address.

* • DISC SCHEDULING:



GOAL \Rightarrow To minimize the Average Seek time of the disc.

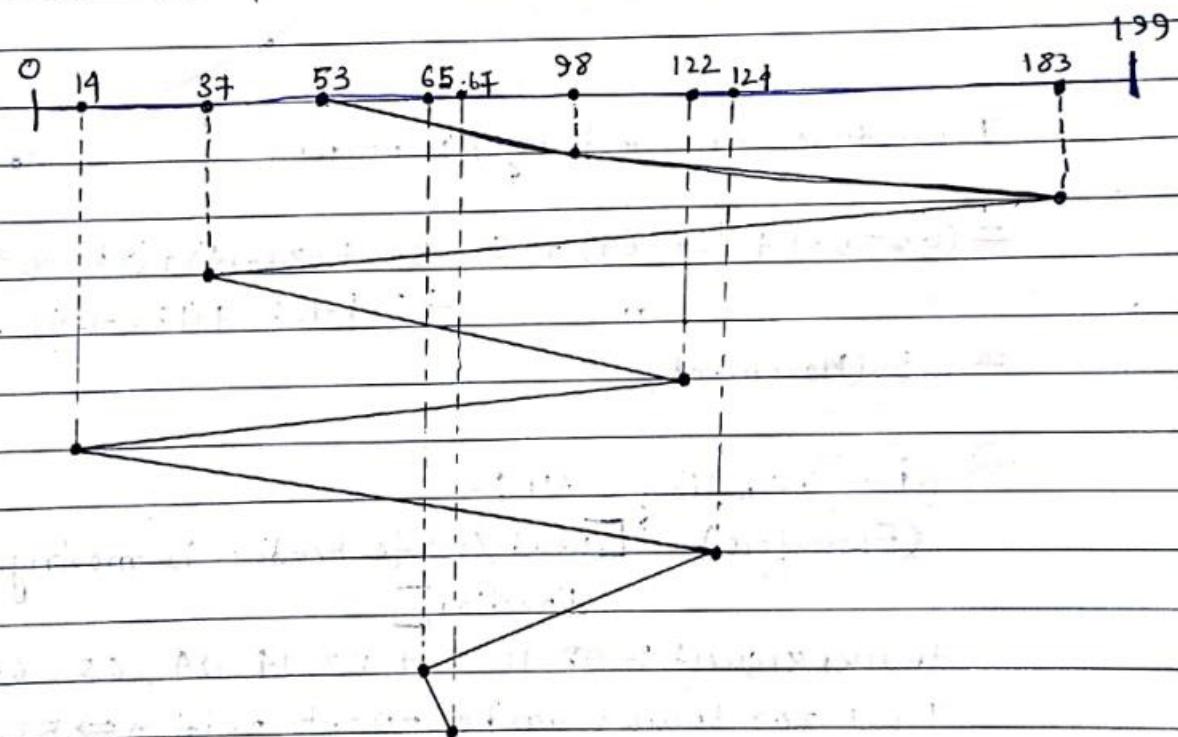
- 1) FCFS
- 2) SSTF
- 3) SCAN
- 4) C-SCAN
- 5) LOOK
- 6) C-LOOK

① FCFS :-

Track Request :- (1) 98, (2) 183, (3) 37, ..., (8) 67.

surface of disc :- 200 tracks. (first come first serve)

current track :- 53.



Total track movement by Read/write header,

$$= (98 - 53) + (183 - 98) + (183 - 37) + (122 - 37) + (122 - 14) + \\ (124 - 14) + (124 - 67) + (67 - 65).$$

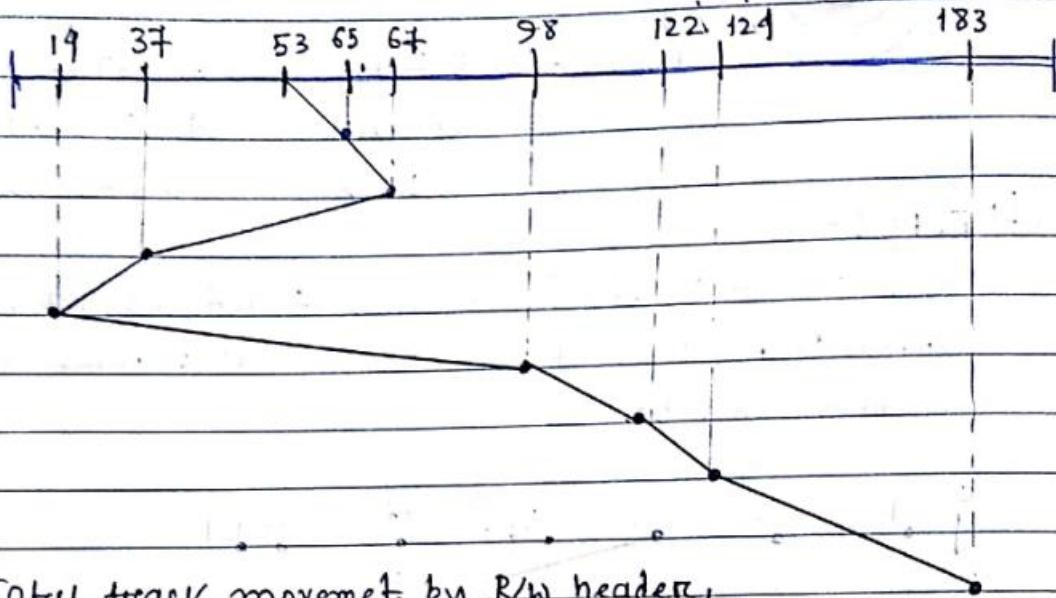
$$= 640$$

② Disc scheduling SSTF :-

(Shortest Seek time first or Nearest track Next)

Track Request :- 98, 183, 37, 122, 14, 124, 65, 67.

Total 200 tracks and current position \Rightarrow 53.



Total track movements by R/W headers,

$$= (65 - 53) + (67 - 65) + (67 - 37) + (37 - 14) + (98 - 14) + (122 - 98) \\ + (124 - 122) + (183 - 124).$$

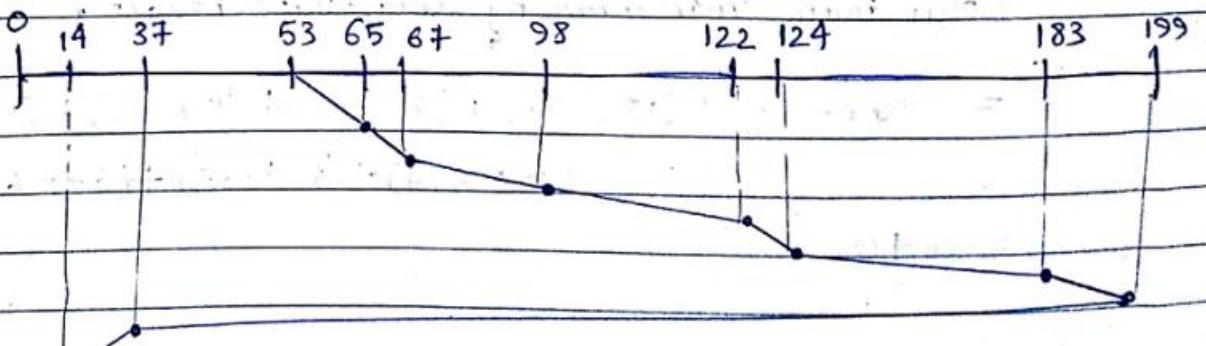
$$= 236 \text{ (Movement)}$$

③ Disc scheduling SCAN :-

(Elevator) [read / write headers is moving towards right direction]

Tracks request :- 98, 183, 37, 122, 14, 124, 65, 67.

Total 200 tracks and current position \Rightarrow 53.

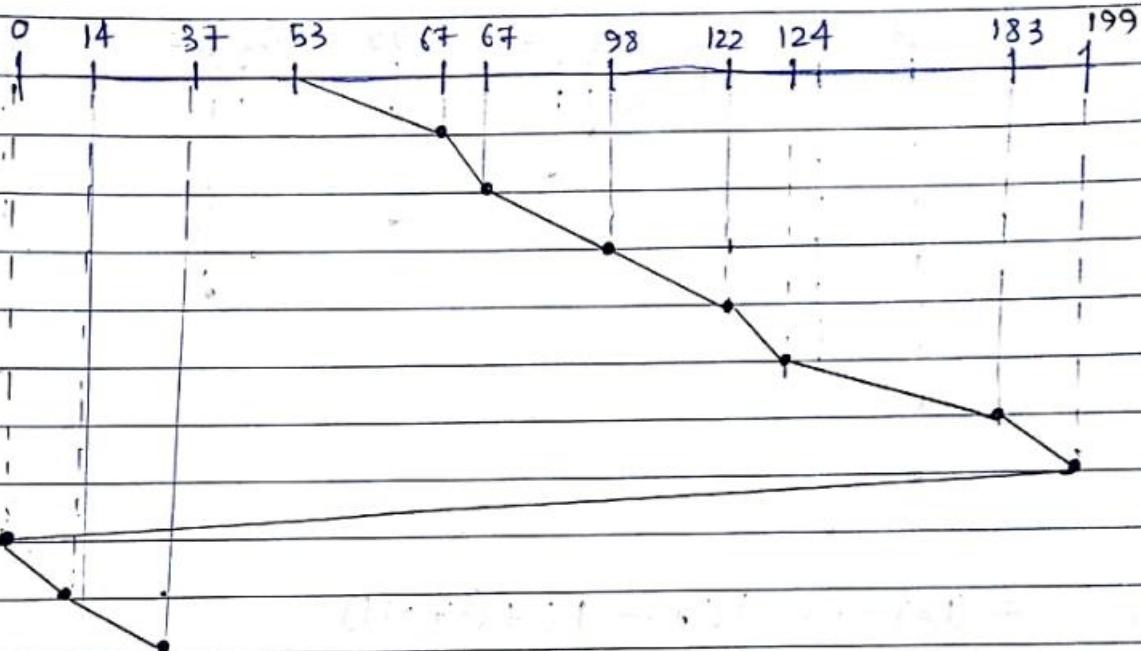


$$= (199 - 53) + (199 - 14) \Rightarrow 331 \text{ (movement)}.$$

④ Disc Scheduling Circular-SCAN :-
(C-SCAN)

Track Request :- 98, 183, 37, 122, 14, 124, 65, 67.

Total 200 track request and current position \Rightarrow 53.



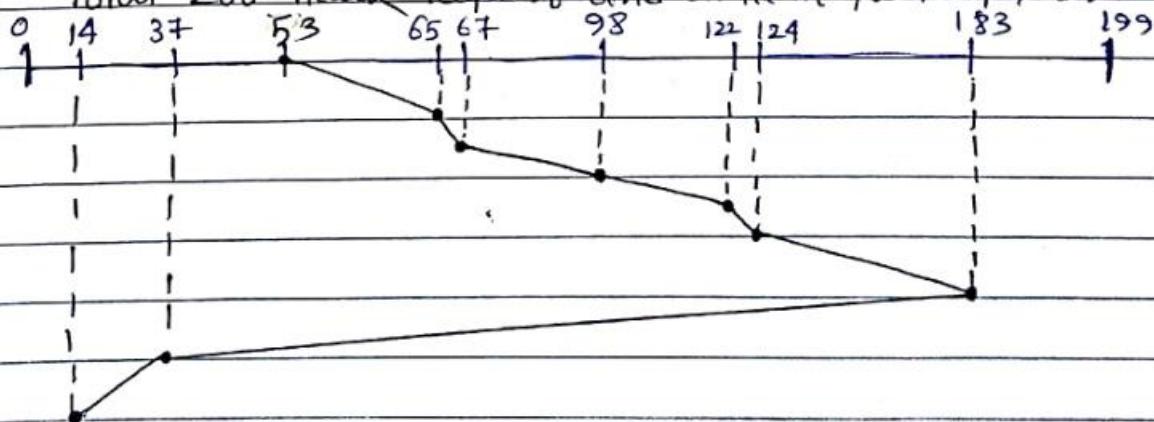
$$\begin{aligned}\text{Total R/W head movement} &= (199 - 53) + (199 - 0) + (37 - 0) \\ &= 382 \text{ (Movement)}\end{aligned}$$

⑤ Disc scheduling LOOK :-

Look for the last pending request in the direction of R/W header.

Track request :- 98, 183, 37, 122, 14, 124, 65, 67.

Total 200 track request and current position \Rightarrow 53.



$$= (183 - 53) + (183 - 14)$$

$$= 130 + 169.$$

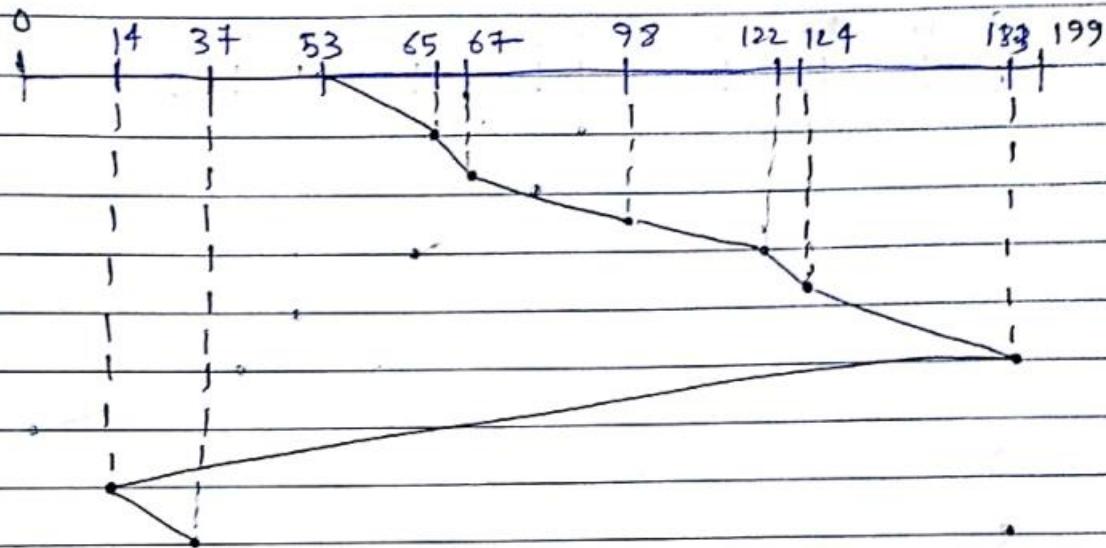
$$= 299$$

⑥ Disc Scheduling Circular LOOK :-

[C-LOOK]

Track request :- 98, 183, 37, 122, 14, 124, 65, 67.

Total tracks \Rightarrow 200 and current position \Rightarrow 53.



$$= (183 - 53) + (183 - 14) + (37 - 14)$$

= 322 (Movement)