Saikumar Sunka

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Location: Hyderabad

Career Objective:

To be a good Design Verification Engineer in the VLSI Industry, and to master my skills and knowledge, and work hard for the success of the organization.

Course Outline:

Verilog HDL, System Verilog,UVM, PERL.

Work Experience:

- *Moschip Institute of Silicon Systems (M-ISS), Hyderabad: Design Verification Trainee (June 2023 to Dec 2023)*
  - Training on Advanced Design and Verification concepts.
  - Hands on experience in tools like Questasim for Design simulation and Verification and EDA tools.
  - Creating state-of-the-art validation environments and infrastructure, including drivers, monitors, tests, etc.
  - Perform IP level functional verification using SystemVerilog/UVM.

Technical Skills:

- Verilog HDL.
- System Verilog
- UVM
- RAL
- PERL

Academic Education:

- B.E (ECE): MATRUSRI ENGINEERING COLLEGE | Hyderabad | CGPA : 7.12 | 2019-2023.
- INTERMEDIATE (MPC): SRI CHAITANYA JUNIOR COLLEGE | Hyderabad | 97.1% | 2017-2019.
- SCHOOL (SSC): Z.P.H.S NIZAMPET | MEDAK | CGPA : 8.7 | 2017.

Experience on Projects:

- *APB based ETHERNET PROTOCOL VERIFICATION:*

  Description:

  Ethernet is a communication protocol that can facilitate communication within a network at a speed of 10/100 Mbps supporting half duplex communication.

  Tool: Questasim

  Responsibilities:

  - Understanding the Ethernet architecture and functionality.
  - Preparation of the Verification Plan, Test plan, Coverage plan and Assertion plan.
  - Involving the IP level verification using UVM environment for Ethernet IP Core.
  - Implementation of the test scenarios to verify the functionality of Ethernet IP Core.
  - Code coverage and Functional coverage analysis and assertion based formal verification based on design specifications.

❖ *AMBA-APB Protocol*

Description:

The AMBA APB Protocol supports low-performance, low-frequency system designs. The APB protocol is not pipelined. Used it to connect to low-bandwidth peripherals that do not require the high performance of the AXI protocol.

Tool: Questasim

Responsibilities:

- Understanding the APB protocol specification.
- Preparation of the Verification Plan, Test plan, Coverage plan and Assertion plan.
- Protocol verification with a single master and single slave in both SV and UVM verification environments.
- Implementation of the Functional coverage model and Assertions.
- Developing the master environment to test the functionality of the salve design through self-check update.
- Coverage based verification and analysis.

❖ *UP-DOWN COUNTER:*

Description:

Based on the selection of signals it operates as up count or down count.

Tool: Questasim

Responsibilities:

- Understanding the specification.
- Implemented the up down Design.
- Verified the implemented Design in SV Environment.
- Prepared the test plan, verification plan and coverage plan.
- Implemented Coverage and Assertions to check the functionality of DUT.

❖ *ALU:*

Description:

Based on the OPCODE(Decoder) it selects the block which has a different set of operations.The blocks that contain in ALU are arithmetic, code conversion, comparator, logical operations, shifter and rotate.

Tool: Questa Sim

Responsibilities:

- Understanding the specification.
- Implemented the ALU Design.
- Verified the implemented Design in VERILOG.
- Verified the design by writing checkers/self check to the design.

Soft Skills:

- ➢ Communication skills
- ➢ Team handling
- ➢ Adaptability
- ➢ Smart working

Personal Details:

Name	:	S.Saikumar
Date of Birth	:	3rd November 2001.
Fathar Name	:	S.Shankar
Hobbies	:	Playing Chess, Watching Movies.
Interests	:	Photography, Travelling and Music.
Languages Known	:	English and Telugu.
Address	:	H-No: 8-26, Dharmajipet, Dubbak, Siddipet, TS, PN-502103.

Declaration:

I hereby declare that the information mentioned above is true to the best of my knowledge.

SAIKUMAR SUNKA