

# **M.2 2280 SSD (CTL Center) (PS5018-E18) Kioxia TLC Specification**

**Version 1.3**



## **Phison Electronics Corporation**

No.1, Qun-Yi Road, Jhunan, Miaoli County, Taiwan 350, R.O.C.

Tel: +886-37-586-896 Fax: +886-37-587-868

E-mail: [sales@phison.com](mailto:sales@phison.com) / [support@phison.com](mailto:support@phison.com)

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## REVISION HISTORY

Revision	Draft Date	History	Author
1.0	2022/02/08	First Release	Tim Hsu
1.1	2022/05/24	<ol style="list-style-type: none"> <li>1. P.5 Modify performance</li> <li>2. P.17 Modify weight configuration description</li> </ol>	Tim Hsu
1.2	2022/10/19	<ol style="list-style-type: none"> <li>1. P.5, P.17 Modify performance and add 4TB single side 32CE configuration.</li> <li>2. P.17 Add 4TB single side 32CE weight configuration.</li> <li>3. P.5, P.20 Add 4TB single side 32CE configuration power consumption.</li> <li>4. P.4, P.16 Add I/O+ technology description</li> <li>5. P.14, Modify Description of Sanitize Operation</li> </ol>	Tim Hsu
1.3	2023/4/12	<ol style="list-style-type: none"> <li>1. P.4, P.5, P.10, P.18 Modify performance and add 4TB double side 32CE configuration.</li> <li>2. P.18 Add 4TB double side 32CE weight configuration.</li> <li>3. P.5, P.21 Add 4TB double side 32CE configuration power consumption.</li> </ol>	Eason Wang

## PRODUCT OVERVIEW

- |   |  |
|---|--|
| <ul style="list-style-type: none"> <li>■ Capacity                             <ul style="list-style-type: none"> <li>— 500, 1000, 2000, 4000, 8000GB</li> <li>— 512, 1024, 2048, 4096, 8192GB</li> </ul> </li> <li>■ Form Factor                             <ul style="list-style-type: none"> <li>— E18 M.2 2280-D2-M (BGA132 x 8)</li> <li>— E18 M.2 2280-S2-M (BGA132 x 4)</li> </ul> </li> <li>■ PCIe Interface                             <ul style="list-style-type: none"> <li>— PCIe Gen4 x 4</li> </ul> </li> <li>■ Compliance                             <ul style="list-style-type: none"> <li>— NVMe 1.4</li> <li>— PCI Express Base 4.0</li> </ul> </li> <li>■ Flash Interface                             <ul style="list-style-type: none"> <li>— Transfer rate up to 1600MBps</li> <li>— Up to 8pcs of BGA132 flash</li> </ul> </li> <li>■ Performance<sup>1</sup> <ul style="list-style-type: none"> <li>— Read: up to 7200 MB/s</li> <li>— Write: up to 6850 MB/s</li> </ul> </li> <li>■ Reliability                             <ul style="list-style-type: none"> <li>— Mean Time Between Failure (MTBF)<br/>1.6 million hours</li> <li>— Uncorrectable Bit Error Rate (UBER)<br/>&lt; 1 sector per 10<sup>16</sup> bits read</li> </ul> </li> </ul> | <ul style="list-style-type: none"> <li>■ Advanced Flash Management                             <ul style="list-style-type: none"> <li>— Advanced Wear Leveling</li> <li>— Bad Block Management</li> <li>— TRIM</li> <li>— SMART</li> <li>— Over-Provision</li> <li>— Firmware Update</li> </ul> </li> <li>■ Power Management                             <ul style="list-style-type: none"> <li>— Support APST</li> <li>— Support ASPM</li> <li>— Support L1.2</li> </ul> </li> <li>■ Power Consumption<sup>2</sup> <ul style="list-style-type: none"> <li>— L1.2 &lt; 3 mW</li> </ul> </li> <li>■ Temperature Range<sup>3</sup> <ul style="list-style-type: none"> <li>— Operation: 0°C ~ 70°C</li> <li>— Storage: -40°C ~ 85°C</li> </ul> </li> <li>■ RoHS compliant</li> <li>■ Features Support                             <ul style="list-style-type: none"> <li>— End to end data path protection</li> <li>— Thermal throttling</li> <li>— SmartECCTM</li> <li>— SmartRefreshTM</li> <li>— Drive log</li> <li>— TCG Pyrite</li> <li>— TCG OPAL<sup>4</sup></li> <li>— I/O+ Technology<sup>4</sup></li> </ul> </li> </ul> |
|---|--|

### NOTES:

1. Refer to Chapter 2 for more details.
2. Refer to Chapter 4, Section 4.2 Power Consumption for more details.
3. Operational temperature is measured by device temperature sensor.
4. Supported by a separate firmware setting. Further information available upon request.

## PERFORMANCE AND POWER CONSUMPTION

### KIOXIA Bics5 TLC

Form Factor	Capacity	Flash Structure (BGA Package)	Performance			
			CrystalDiskMark		IOMeter	
			Read (MB/s)	Write (MB/s)	Read (IOPS)	Write (IOPS)
M.2 2280 Single Side	500, 512GB	1024Gb x 4, 8CE, 512Gb DDP	7000	3750	450K	920K
	1000, 1024GB	2048Gb x 4, 16CE, 512Gb QDP	7200	6000	750K	1000K
	2000, 2048GB	4096Gb x 4, 32CE, 512Gb ODP	7200	6850	1000K	1000K
	4000, 4096GB	8192Gb x 4, 16CE, 1Tb ODP	7200	6400	550K	1000K
	4000, 4096GB	8192Gb x 4, 32CE, 1Tb ODP	7200	6850	1000K	1000K
M.2 2280 Double Side	2000, 2048GB	2048Gb x 8, 32CE, 512Gb QDP	7200	6850	1000K	1000K
	4000, 4096GB	4096Gb x 8, 32CE, 512Gb ODP	7200	6850	1000K	1000K
	4000, 4096GB	4096Gb x 8, 32CE, 1Tb QDP	7200	6850	1000K	1000K
	8000, 8192GB	8192Gb x 8, 32CE, 1Tb ODP	7000	5900	900K	1000K

Form Factor	Capacity	Flash Configuration (BGA Package)	Power Consumption			
			Read (W)	Write (W)	PS3 (mW)	PS4 (mW)
M.2 2280 Single Side	500, 512GB	1024Gb x 4, 8CE, 512Gb DDP	8.5	7.0	40	3
	1000, 1024GB	2048Gb x 4, 16CE, 512Gb QDP	9.5	7.7	40	3
	2000, 2048GB	4096Gb x 4, 32CE, 512Gb ODP	9.8	9.6	45	3
	4000, 4096GB	8192Gb x 4, 16CE, 1Tb ODP	10.3	10.0	50	3
	4000, 4096GB	8192Gb x 4, 32CE, 1Tb ODP	11.2	10.8	50	3
M.2 2280 Double Side	2000, 2048GB	2048Gb x 8, 32CE, 512Gb QDP	10.5	10.0	45	3
	4000, 4096GB	4096Gb x 8, 32CE, 512Gb ODP	11.3	10.9	50	3
	4000, 4096GB	4096Gb x 8, 32CE, 1Tb QDP	11.3	10.9	50	3
	8000, 8192GB	8192Gb x 8, 32CE, 1Tb ODP	11.5	11.0	50	3

### NOTES:

- Performance is the first time measured results on a fresh slave drive and based on the following conditions:
  - CrystalDiskMark 7.0.0, 1GB range, QD=16, Thread=1
  - IOMeter, 1GB range, 4K data size, QD=128, 16 worker, 4k aligned
- Performance is based on AMD Gen4 X570 + 8 Core CPU + DDR4 (3200Hz) 16GB.
- Power consumption is measured during the sequential read and write operations performed by CrystalDiskMark with the conditions described in 1(B).
- Power consumption during read and write operation is measured on Gen4 X570 + 6 Core CPU

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# 1. INTRODUCTION

## 1.1. General Description

Phison PS5018-E18 M.2 2280 delivers all the advantages of flash disk technology with PCIe Gen4 x4 interface and is fully compliant with the standard Next Generation Form Factor (NGFF) called M.2 Card Format. PS5018-E18 M.2 2280 offers a wide range capacity up to 8000GB and its performance can reach up to 7200 MB/s (for read) and 6850 MB/s (for write) based on KIOXIA Bics5 TLC NAND flash with the choice of 512MB/1GB/2GB DDR4<sup>2</sup>. Moreover, the power consumption of PS5018-E18 M.2 2280 is much lower than traditional hard drives, making it the best embedded solution for new platforms.

### NOTES:

1. Achieved by 2000GB SSD with external 2GB DDR4 at FOB (fresh-out-of-box) state on CrystalDiskMark v7.0.0.
2. The choice of DDR4 depends on drive capacity.  
DDR size = 0.1% of SSD capacity 512G to 2TB DS  
DDR size = 0.05% of SSD capacity 2TB SS and 4TB.  
DDR size = 0.025% of SSD capacity 4TB SS and 8TB.

## 1.2. Controller Block Diagram

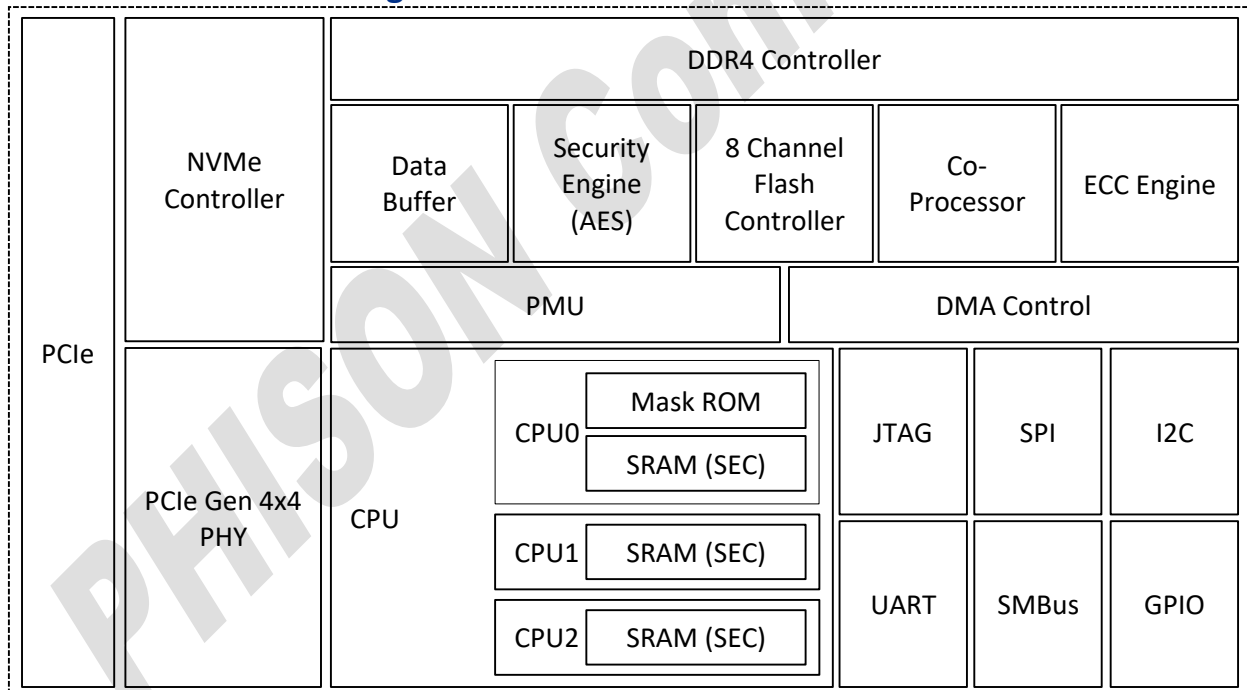


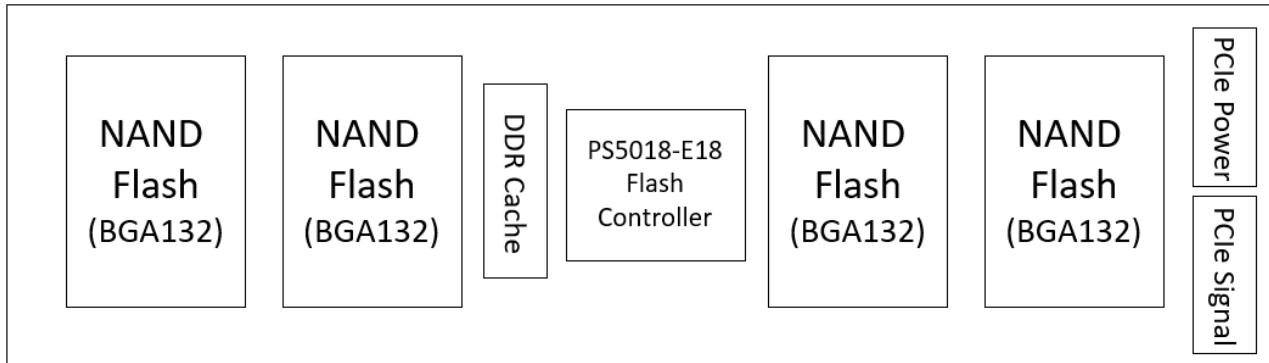
Figure 1-1 PS5018-E18 Controller Block Diagram

### NOTES:

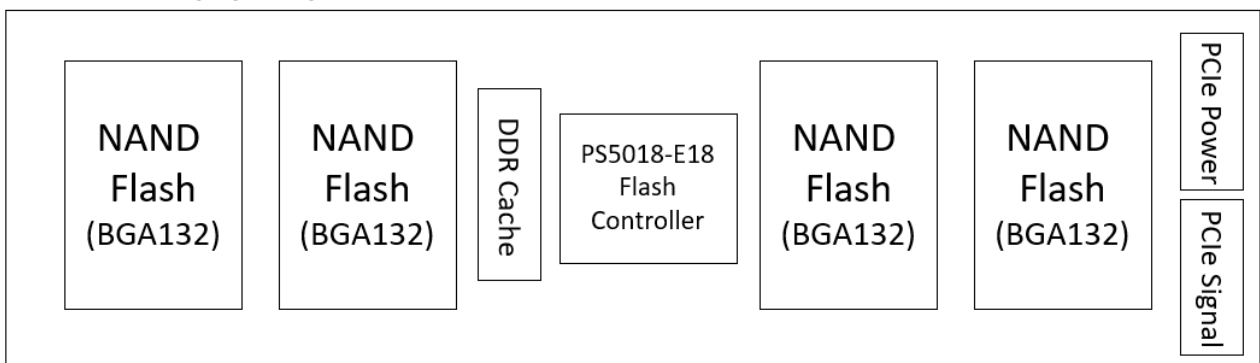
1. PMU: Power Management Unit
2. SEC: Single Bit Error Correct

### 1.3. Product Block Diagram

#### M.2 2280-S2



#### M.2 2280-D2 (Top side)



#### M.2 2280-D2 (Bottom side)

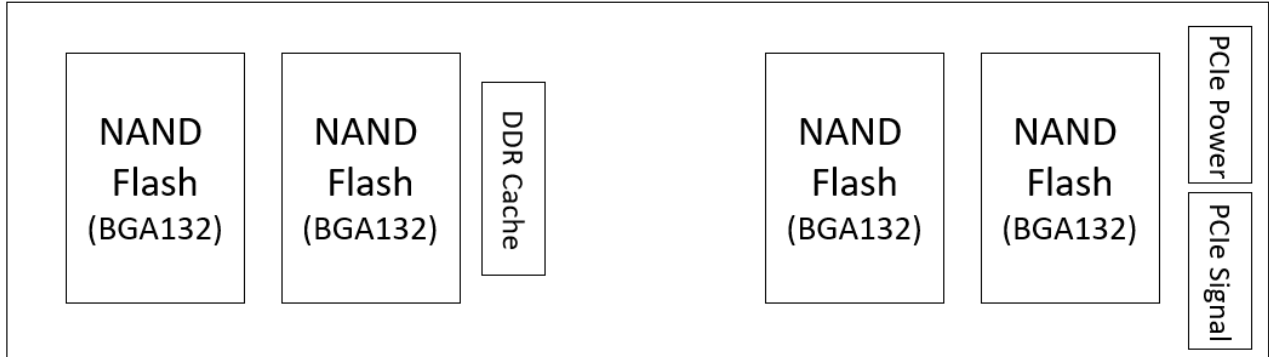


Figure 1-2 PS5018-E18 M.2 2280 Product Block Diagram

### 1.4. Flash Management

#### 1.4.1. Error Correction Code (ECC)

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, PS5018-E18 PCIe SSD applies the fourth generation LDPC (Low Density Parity Check) of ECC algorithm, which can detect and correct errors occur during read process, ensure data been read correctly, as well as protect data from corruption.

#### *1.4.2. Wear Leveling*

NAND flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some areas get updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Wear Leveling is applied to extend the lifespan of NAND Flash by evenly distributing write and erase cycles across the media.

Phison provides advanced Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static Wear Leveling algorithms, the life expectancy of the NAND flash is greatly improved.

#### *1.4.3. Bad Block Management*

Bad blocks are blocks that do not function properly or contain more invalid bits causing stored data unstable, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Early Bad Blocks”. Bad blocks that are developed during the lifespan of the flash are named “Later Bad Blocks”. Phison implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages bad blocks that appear with use. This practice prevents data being stored into bad blocks and further improves the data reliability.

#### *1.4.4. TRIM*

TRIM is a feature which helps improve the read/write performance and speed of solid-state drives (SSD). Unlike hard disk drives (HDD), SSDs are not able to overwrite existing data, so the available space gradually becomes smaller with each use. With the TRIM command, the operating system can inform the SSD which blocks of data are no longer in use and can be removed permanently. Thus, the SSD will perform the erase action, which prevents unused data from occupying blocks all the time.

#### *1.4.5. SMART*

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is an open standard that allows a hard disk drive to automatically detect its health and report potential failures. When a failure is recorded by SMART, users can choose to replace the drive to prevent unexpected outage or data loss. Moreover, SMART can inform users of impending failures while there is still time to perform proactive actions, such as copy data to another device.

#### ***1.4.6. Over-Provision***

Over Provisioning refers to the inclusion of extra NAND capacity in a SSD, which is not visible and cannot be used by users. With Over Provisioning, the performance and IOPS (Input/Output Operations per Second) are improved by providing the controller additional space to manage P/E cycles, which enhances the reliability and endurance as well. Moreover, the write amplification of the SSD becomes lower when the controller writes data to the flash.

#### ***1.4.7. Firmware Upgrade***

Firmware can be considered as a set of instructions on how the device communicates with the host. Firmware will be upgraded when new features are added, compatibility issues are fixed, or read/write performance gets improved.

#### ***1.4.8. Thermal Throttling***

The purpose of thermal throttling is to prevent any components in a SSD from over-heating during read and write operations. PS5018-E18 is designed with an on-die thermal sensor and with its accuracy, firmware can apply different levels of throttling to achieve the purpose of protection efficiently and proactively via SMART reading.

### **1.5. Advanced Device Security Features**

#### ***1.5.1. NVMe Format***

Secure Erase is a standard NVMe format command and will write all "0x00" to fully wipe all the data on hard drives and SSDs. When this command is issued, SSD controller will erase its storage blocks and return to its factory default settings.

#### ***1.5.2. Physical Presence SID (PSID)***

Physical Presence SID (PSID) is defined by TCG Pyrite as a 32-character string and the purpose is to revert SSD back to its manufacturing setting when the drive is set via TCG Pyrite (non-SED). PSID code is printed on a SSD label.

#### ***1.5.3. Manufacturer's Secure ID (MSID)***

Manufacturer's Secure ID (MSID) is defined by TCG Pyrite as a 32-character string and is assigned during the

manufacturing process, which is a password that cannot be changed by the host system. MSID can be obtained electronically from the drive across the interface. When the drive is delivered, user should personalize the drive by defining a new password. Failure to do so means that anyone can use the MSID to preempt the owner and take control of the drive. Such an attack on the drive is known as Denial of Service (DoS) since the rightful owner has been locked out.

#### 1.5.4. Sanitize Operation

Sanitize feature set an alternative to existing secure erase capabilities via Format NVM command and makes stronger guarantees on data security by ensuring that user data from the drive's media, caches and the Controller Memory Buffer are all wiped through block erase operations, overwriting, or destroying the encryption key. The table below illustrates the type of sanitize operations that are supported by E18 SSD.

Drive Security Type	Sanitize Operation			TCG Commands	
	Overwrite	Block Erase	Crypto Erase	PSID Revert Process	Instant Security Erase
Non-SED (TCG Pyrite)	Yes	Yes	No	Yes	No
SED (TCG Opal)	Yes	Yes	Yes	Yes	Yes

NOTES:

1. Instant Security Erase is a feature that erases all data of SED drive with TCG-activated encrypted data structure by reverting SSD with PSID. Since the key is reset, the previously encrypted data cannot be accessed anymore.

## 1.6. SSD Lifetime Management

TBW (Terabytes Written) is a measurement of SSDs' expected lifespan, which represents the amount of data written to the device. To calculate the TBW of a SSD, the following equation is applied:

$$TBW = [(NAND\ Endurance) \times (SSD\ Capacity)] / [WAF]$$

**NAND Endurance:** NAND endurance refers to the P/E (Program/Erase) cycle of a NAND flash.

**SSD Capacity:** The SSD capacity is the specific capacity in total of a SSD.

**WAF:** Write Amplification Factor (WAF) is a numerical value representing the ratio between the amount of data that a SSD controller needs to write and the amount of data that the host's flash controller writes. A better WAF, which is near 1, guarantees better endurance and lower frequency of data written to flash memory.

TBW in this document is based on JEDEC 218/219 workload.

#### *1.6.1. Media Wear Indicator*

Actual life indicator reported by SMART Attribute byte index [5], Percentage Used, recommends User to replace drive when reaching to 100%.

#### *1.6.2. Read Only Mode (End of Life)*

When drive is aged by cumulated program/erase cycles, media worn- out may cause increasing numbers of later bad block. When the number of usable good blocks falls outside a defined usable range, the drive will notify Host through AER event and Critical Warning to enter Read Only Mode to prevent further data corruption. User should start to replace the drive with another one immediately.

### **1.7. An Adaptive Approach to Performance Tuning**

#### *1.7.1. Throughput*

Based on the available space of the disk, PS5018-E18 will regulate the read/write speed and manage the performance of throughput. When there still remains a lot of space, the firmware will continuously perform read/write action. There is still no need to implement garbage collection to allocate and release memory, which will accelerate the read/write processing to improve the performance. Contrarily, when the space is going to be used up, PS5018-E18 will slow down the read/write processing, and implement garbage collection to release memory. Hence, read/write performance will become slower.

#### *1.7.2. Predict & Fetch*

Normally, when the Host tries to read data from the PCIe SSD, the PCIe SSD will only perform one read action after receiving one command. However, PS5018-E18 applies “Predict & Fetch” to improve the read speed. When the host issues sequential read commands to the PCIe SSD, the PCIe SSD will automatically expect that the following will also be read commands. Thus, before receiving the next command, flash has already prepared the data. Accordingly, this accelerates the data processing time, and the host does not need to wait so long to receive data.

#### *1.7.3. SLC Caching*

PS5018-E18's firmware design currently adopts dynamic caching to deliver better performance for better endurance and consumer user experience. The SLC caching size is up to 1/3 of full capacity.

## 1.8. I/O+ Technology

I/O+ technology optimize the SSD for sustained read workloads that run for hours, Phison's I/O+ technology does not compromise classical workloads as shown in the benchmarks on display today. Moreover, the biggest gains seen with I/O+ technology are on tasks that emphasize medium to large IO (Input/Output) in the 32K to 1MB block size range. Smaller block size data can also benefit from I/O+ technology also when the transfers are streamed. With I/O+ technology, games can run for hours sessions with no drop in the available bandwidth that must stay steady to eliminate visual hitching or stutters during gameplay. There are also benefits for non-gaming workloads, too. For example, the chrome browser source code can compile data significantly faster when using I/O+ technology firmware.



## 2. PRODUCT SPECIFICATIONS

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### ■ Capacity

- 500GB, 1000GB, 2000GB, 4000, 8000GB
- 512GB, 1024GB, 2048GB, 4096, 8192GB

### ■ Electrical/Physical Interface

- PCIe Interface
- Compliant with NVMe 1.4
- PCIe Express Base Ver 4.0
- PCIe Gen 4 x 4 lane & backward compatible to PCIe Gen3, Gen 2 and Gen 1
- 8 IO queues supported (1 admin queue and 8 IO queue). Each IO queue supports 256 entries.
- Support power management

### ■ Supported NAND Flash

- Support up to 32 Flash Chip Enables (CE) within a single design
- Support up to 8pcs BGA132 flash (M2 2280-D2)
- Support 8-bit I/O NAND Flash
- Support ONFI 2.3, ONFI 3.0, ONFI 3.2, ONFI 4.0 and ONFI 4.2 interface
- Support Toggle 1.0, Toggle 2.0, Toggle 3.0 and Toggle 4.0 interface
  - KIOXIA Bics5 TLC

### ■ ECC Scheme

- PS5018-E18 PCIe SSD applies the fourth LDPC generation of ECC algorithm.

### ■ Supported Sector size

- 512Bytes
- 4KB

### ■ UART / GPIO

### ■ Support SMART and TRIM commands

### ■ LBA Range

- IDEMA standard

### ■ Certification & Compliance

- RoHS
- WHQL
- PCI Express Base 4.0

— UNH-IOL NVM Express Logo

■ Weight

— KIOXIA Bics5

Form Factor	Capacity	Flash Configuration	Flash Type	Weight (g)
M.2 2280 Single Side	500, 512GB	128GB x 4	BGA132, Bics5 TLC, 512Gb DDP	7.7
	1000, 1024GB	256GB x 4	BGA132, BICS5 TLC, 512Gb QDP	7.7
	2000, 2048GB	512GB x 4	BGA132, BICS5 TLC, 512Gb ODP	7.8
	4000, 4096GB	1024GB x 4	BGA132, BICS5 TLC, 1Tb ODP	8.2
	4000, 4096GB	1024GB x 4	BGA132, BICS5 TLC, 1Tb ODP	8.2
M.2 2280 Double Side	2000, 2048GB	256GB x 8	BGA132, BICS5 TLC, 512Gb QDP	9.6
	4000, 4096GB	512GB x 8	BGA132, BICS5 TLC, 512Gb ODP	10.4
	4000, 4096GB	512GB x 8	BGA132, BICS5 TLC, 1Tb QDP	10.4
	8000, 8192GB	1024GB x 8	BGA132, BICS5 TLC, 1Tb ODP	10.2

■ TBW

— KIOXIA Bics5

Capacity	Flash Type	TBW
500, 512GB	Bics5 TLC, 512Gb	350
1000, 1024GB	Bics5 TLC, 512Gb	700
2000, 2048GB	Bics5 TLC, 512Gb	1400
4000, 4096GB	Bics5 TLC, 512Gb	3000
4000, 4096GB	Bics5 TLC, 1Tb	3000
8000, 8192GB	Bics5 TLC, 1Tb	6000

■ Performance

— KIOXIA Bics5

Form Factor	Capacity	Flash Structure (BGA Package)	Performance <sup>1</sup>			
			CrystalDiskMark		IOMeter	
			Read (MB/s)	Write (MB/s)	Read (IOPS)	Write (IOPS)
M.2 2280 Single Side	500, 512GB	1024Gb x 4, 8CE, 512Gb DDP	7000	3750	450K	920K
	1000, 1024GB	2048Gb x 4, 16CE, 512Gb QDP	7200	6000	750K	1000K
	2000, 2048GB	4096Gb x 4, 32CE, 512Gb ODP	7200	6850	1000K	1000K
	4000, 4096GB	8192Gb x 4, 16CE, 1Tb ODP	7200	6400	550K	1000K
	4000, 4096GB	8192Gb x 4, 32CE, 1Tb ODP	7200	6850	1000K	1000K
M.2 2280 Double Side	2000, 2048GB	2048Gb x 8, 32CE, 512Gb QDP	7200	6850	1000K	1000K
	4000, 4096GB	4096Gb x 8, 32CE, 512Gb ODP	7200	6850	1000K	1000K
	4000, 4096GB	4096Gb x 8, 32CE, 1Tb QDP	7200	6850	1000K	1000K
	8000, 8192GB	8192Gb x 8, 32CE, 1Tb ODP	7000	5900	900K	1000K

NOTES:

- Performance is measured on a fresh slave drive and based on the following conditions:
  - CrystalDiskMark 7.0.0, 1GB range, QD=16, Thread=1
  - IOMeter, 1GB range, 4K data size, QD=128, 16 worker, 4k aligned
- Performance is based on AMD Gen4 X570 + 8 Core CPU + DDR4 (3200Hz) 16GB.
- Performance may differ according to flash configuration and platform.

4. The tables are for reference only. Any criteria for accepting goods shall be further discussed based on different flash configurations.

### 3. ENVIRONMENTAL SPECIFICATIONS

#### 3.1. Environmental Conditions

##### 3.1.1. Temperature and Humidity

Table 3-1 High Temperature

	Temperature	Humidity
Operation	70°C	0% RH
Storage	85°C	0% RH

Table 3-2 Low Temperature

	Temperature	Humidity
Operation	0°C	0% RH
Storage	-40°C	0% RH

Table 3-3 High Humidity

	Temperature	Humidity
Operation	40°C	90% RH
Storage	40°C	93% RH

Table 3-4 Temperature Cycling

	Temperature
Operation	0°C
	70°C <sup>1</sup>
Storage	-40°C
	85°C

#### NOTES:

1. Operation temperature is measured by device temperature sensor. Airflow is suggested and it will allow device to be operated at appropriate temperature for each component during heavy workloads environment.

##### 3.1.2. Shock

Table 3-5 Shock

	Acceleration Force
Non-operational	1500G

##### 3.1.3. Vibration

Table 3-6 Vibration

	Condition	
	Frequency/Displacement	Frequency/Acceleration
Non-operational	20Hz~80Hz/1.52mm	80Hz~2000Hz/20G

### 3.1.4. Drop

Table 3-7 Drop

	Height of Drop	Number of Drop
Non-operational	80cm free fall	6 face of each unit

### 3.1.5. Bending

Table 3-8 Bending

	Force	Action
Non-operational	≥ 20N	Hold 1min/5times

### 3.1.6. Durability

Table 3-9 Durability

	Condition
operational	1000 mating cycles

### 3.1.7. Electrostatic Discharge (ESD)

Table 3-10 ESD

Specification	+/-4KV
EN 55024, CISPR 24 EN 61000-4-2 and IEC 61000-4-2	Device functions are affected, but EUT will be back to its normal or operational state automatically.

### 3.1.8. EMI Compliance

Table 3-11 EMI

Specification
EN 55032, CISPR 32(CE) AS/NZS CISPR 32(CE) ANSI C63.4 (FCC) VCCI-CISPR 32 (VCCI) CNS 13438 (BSMI)

## 3.2. MTBF

MTBF, Mean Time Between Failures, is a measure of reliability of a device. Its value represents the average time between a repair and the next failure. The unit of MTBF is in hours. The higher the MTBF value, the higher the reliability of the device.

Our MTBF result is based on simulation software (Relax7.3). Please note that a lower MTBF should be expected for higher capacity drives, and we apply the lowest MTBF for all capacities.

## 4. ELECTRICAL SPECIFICATIONS

### 4.1. Supply Voltage

Table 4-1 Supply Voltage

Parameter	Rating
Operating Voltage	Min = 3.14V Max = 3.47 V
Rise Time (Max/Min)	100 ms / 0.1 ms
Fall Time (Max/Min)	5 s / 1 ms
Min. Off Time1	1 s

NOTES:

1. Minimum time between power removed from SSD ( $V_{cc} < 100$  mW) and power re-applied to the drive.

### 4.2. Power Consumption

Table 4-2 Power Consumption of KIOXIA Bics5 TLC in W

Form Factor	Capacity	Flash Configuration	CE#	Read		Write	
				Max.	Avg.	Max.	Avg.
M.2 2280 Single Side	500, 512GB	1024Gb x 4, 512Gb DDP	8	8.5	8.4	7.0	6.9
	1000, 1024GB	2048Gb x 4, 512Gb QDP	16	9.5	9.4	7.7	7.6
	2000, 2048GB	4096Gb x 4, 512Gb ODP	32	9.8	9.6	9.6	9.2
	4000, 4096GB	8192Gb x 4, 1Tb, ODP	16	10.3	10.0	10.0	8.3
	4000, 4096GB	8192Gb x 4, 1Tb, ODP	32	11.2	10.9	10.8	8.9
M.2 2280 Double Side	2000, 2048GB	2048Gb x 8, 512Gb, QDP	32	10.5	10.4	10.0	9.7
	4000, 4096GB	4096Gb x 8, 512Gb, ODP	32	11.3	11.0	10.9	9.0
	4000, 4096GB	4096Gb x 8, 1Tb, QDP	32	11.3	11.0	10.9	9.0
	8000, 8192GB	8192Gb x 8, 1Tb, ODP	32	11.5	11.4	11.0	9.1

NOTES:

1. Based on EIFM1xxx-/EIFM5xxx-series under ambient temperature.
2. Use CrystalDiskMark 7.0.0, 1GB range, QD=16, Thread=1. Measure power consumption during sequential Read and sequential Write.
3. Power Consumption may differ according to flash configuration and platform.
4. The measured power voltage is 3.3V.
5. Power Consumption during read and write operation is measured on Gen4 X570 + 6 Core CPU

Table 4-3 Power Consumption of KIOXIA Bics5 TLC in mW

Form Factor	Capacity	Flash Configuration	CE#	Active			PS3	PS4
				PS0	PS1	PS2		
M.2 2280 Single Side	500, 512GB	1024Gb x 4, 512Gb DDP	8	8500	3600	3400	40	3
	1000, 1024GB	2048Gb x 4, 512Gb QDP	16	9500	3900	3500	40	3
	2000, 2048GB	4096Gb x 4, 512Gb ODP	32	9800	3800	3500	45	3
	4000, 4096GB	8192Gb x 4, 1Tb, ODP	16	10000	4200	3700	50	3
	4000, 4096GB	8192Gb x 4, 1Tb, ODP	32	11200	4200	3900	50	3
M.2 2280 Double Side	2000, 2048GB	2048Gb x 8, 512Gb QDP	32	10500	3800	3600	45	3
	4000, 4096GB	4096Gb x 8, 512Gb, ODP	32	11300	4200	3900	50	3
	4000, 4096GB	4096Gb x 8, 1Tb, QDP	32	11300	4200	3900	50	3
	8000, 8192GB	8192Gb x 8, 1Tb, ODP	32	11500	4300	4000	50	3

## NOTES:

1. Based on EIFM1xxx-/EIFM5xxx-series under ambient temperature.
2. The average value of power consumption is achieved based on 100% conversion efficiency.
3. The measured power voltage is 3.3V.
4. The temperature of a storage device in PS1 should remain constant or should slightly decrease for all workloads so the actual power in PS1 should be lower than PS0.
5. The temperature of a storage device in PS2 should decrease sharply for all workloads so the actual power in PS2 should be lower than PS1.
6. Power Consumption during read and write operation is measured on Gen4 X570 + 6 Core CPU.

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## 5. INTERFACE

### 5.1. Pin Assignment and Descriptions

Table 5-1 defines the signal assignment of the internal NGFF connector for SSD usage, described in the PCI Express M.2 Specification version 1.1 of the PCI-SIG.

Table 5-1 Pin Assignment and Description of PS5018-E18 M.2 2280

Pin No.	PCIe Pin	Description
1	GND	CONFIG_3 = GND
2	3.3V	3.3V source
3	GND	Ground
4	3.3V	3.3V source
5	PETn3	PCIe TX Differential signal defined by the PCI Express M.2 spec
6	N/C	No connect
7	PETp3	PCIe TX Differential signal defined by the PCI Express M.2 spec
8	N/C	No connect
9	GND	Ground
10	LED1#	Open drain, active low signal. These signals are used to allow the add-in card to provide status indicators via LED devices that will be provided by the system.
11	PERn3	PCIe RX Differential signal defined by the PCI Express M.2 spec
12	3.3V	3.3V source
13	PERp3	PCIe RX Differential signal defined by the PCI Express M.2 spec
14	3.3V	3.3V source
15	GND	Ground
16	3.3V	3.3V source
17	PETn2	PCIe TX Differential signal defined by the PCI Express M.2 spec
18	3.3V	3.3V source
19	PETp2	PCIe TX Differential signal defined by the PCI Express M.2 spec
20	N/C	No connect
21	GND	Ground
22	N/C	No connect
23	PERn2	PCIe RX Differential signal defined by the PCI Express M.2 spec
24	N/C	No connect
25	PERp2	PCIe RX Differential signal defined by the PCI Express M.2 spec
26	N/C	No connect
27	GND	Ground
28	N/C	No connect
29	PETn1	PCIe TX Differential signal defined by the PCI Express M.2 spec
30	N/C	No connect
31	PETp1	PCIe TX Differential signal defined by the PCI Express M.2 spec
32	N/C	No connect
33	GND	Ground
34	N/C	No connect
35	PERn1	PCIe RX Differential signal defined by the PCI Express M.2 spec
36	N/C	No connect
37	PERp1	PCIe RX Differential signal defined by the PCI Express M.2 spec

Pin No.	PCIe Pin	Description
38	N/C	No connect
39	GND	Ground
40	SMB_CLK (I/O)(0/1.8V)	SMBus Clock; Open Drain with pull-up on platform
41	PETn0	PCIe TX Differential signal defined by the PCI Express M.2 spec
42	SMB_DATA (I/O)(0/1.8V)	SMBus Data; Open Drain with pull-up on platform.
43	PETp0	PCIe TX Differential signal defined by the PCI Express M.2 spec
44	ALERT#(O) (0/1.8V)	Alert notification to master; Open Drain with pull-up on platform; Active low.
45	GND	Ground
46	N/C	No connect
47	PERn0	PCIe RX Differential signal defined by the PCI Express M.2 spec
48	N/C	No connect
49	PERp0	PCIe RX Differential signal defined by the PCI Express M.2 spec
50	PERST#(I)(0/3.3V)	PE-Reset is a functional reset to the card as defined by the PCIe Mini CEM specification.
51	GND	Ground
52	CLKREQ#(I/O)(0/3.3V)	Clock Request is a reference clock request signal as defined by the PCIe Mini CEM specification; Also used by L1 PM Sub-states.
53	REFCLKn	PCIe Reference Clock signals (100 MHz) defined by the PCI Express M.2 spec.
54	PEWAKE#(I/O)(0/3.3V)	PCIe PME Wake. Open Drain with pull up on platform; Active Low.
55	REFCLKp	PCIe Reference Clock signals (100 MHz) defined by the PCI Express M.2 spec.
56	Reserved for MFG DATA	Manufacturing Data line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform Socket.
57	GND	Ground
58	Reserved for MFG CLOCK	Manufacturing Clock line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform Socket.
59	Module Key M	Module Key
60	Module Key M	
61	Module Key M	
62	Module Key M	
63	Module Key M	
64	Module Key M	
65	Module Key M	
66	Module Key M	
67	N/C	No connect
68	N/C	No connect
69	N/C	PEDET (NC-PCIe)
70	3.3V	3.3V source
71	GND	Ground
72	3.3V	3.3V source
73	GND	Ground
74	3.3V	3.3V source
75	GND	Ground



## 6. SUPPORTED COMMANDS

### 6.1. NVMe Command List

Table 6-1 Admin Commands

Identifier	O/M	Command Description	Supported
00h	M	Delete I/O Submission Queue	Supported
01h	M	Create I/O Submission Queue	Supported
02h	M	Get Log Page	Supported
04h	M	Delete I/O Completion Queue	Supported
05h	M	Create I/O Completion Queue	Supported
06h	M	Identify	Supported
08h	M	Abort	Supported
09h	M	Set Feature	Supported
0Ah	M	Get Feature	Supported
0Ch	M	Asynchronous Event Request	Supported
10h	O	Firmware Commit	Supported
11h	O	Firmware Image Download	Supported
14h	O	Device Self-test	Not Supported
80h	O	Format NVM	Supported
81h	O	Security Send	Supported
82h	O	Security Receive	Supported
84h	O	Sanitize	Not Supported

Table 6-2 I/O Commands

Identifier	O/M	Command Description	Supported
00h	O	Flush	Supported
01h	O	Write	Supported
02h	O	Read	Supported
04h	O	Write Uncorrectable	Not Supported
05h	O	Compare	Supported
08h	O	Write Zeroes	Supported
09h	O	Dataset Management	Supported

Table 6-3 Set Feature Commands

Identifier	O/M	Command Description	Supported
00h		Reserved	
01h	M	Arbitration	Supported
02h	M	Power Management	Supported
03h	O	LBA Range Type	Not Supported
04h	M	Temperature Threshold	Supported
05h	M	Error Recovery	Supported
06h	O	Volatile Write Cache	Supported
07h	M	Number Of Queues	Supported
08h	M	Interrupt Coalescing	Supported
09h	M	Interrupt Vector Configuration	Supported
0Ah	M	Write Atomicity Normal	Supported
0Bh	M	Asynchronous Event Configuration	Supported
0Ch	O	Autonomous Power State Transition	Supported

Identifier	O/M	Command Description	Supported
0Dh	O	Host Memory Buffer	Not Supported
0Eh	O	Timestamp	Supported
10h	O	Host Controlled Thermal Management	Supported
11h	O	Non-Operational Power State Config	Supported
0Eh - 7Dh		Reserved	
80h	O	Software Progress Marker	Supported

Table 6-4 Get Log Page Commands

Identifier	O/M	Command Description	Supported
00h		Reserved	
01h	M	Error Information	Supported
02h	M	SMART / Health Information	Supported
03h	M	Firmware Slot Information	Supported
04h	O	Changed Namespace List	Not Supported
06h	O	Device Self-test	Supported
09h - 7Fh		Reserved	
81h	O	Sanitize Status	Not Supported
82h - FFh		Reserved	

## 6.2. Identify Device Command

The following table details the sector data returned by the IDENTIFY DEVICE command.

Table 6-5 Identify Controller Data Structure

Bytes	O/M	Description	Default Value
01:00	M	PCI Vendor ID (VID)	0x1987
03:02	M	PCI Subsystem Vendor ID (SSVID)	0x1987
23:04	M	Serial Number (SN)	TBD
63:24	M	Model Number (MN)	TBD
71:64	M	Firmware Revision (FR)	TBD
72	M	Recommended Arbitration Burst (RAB)	0x01
75:73	M	IEEE OUI Identifier (IEEE)	TBD*
76	O	Controller Multi-Path I/O and Namespace Sharing Capabilities (CMIC)	0x00
77	M	Maximum Data Transfer Size (MDTS)	0x09
79:78	M	Controller ID (CNTLID)	0x0001
83:80	M	Version (VER)	0x00010400
87:84	M	RTD3 Resume Latency (RTD3R)	0x00989680
91:88	M	RTD3 Entry Latency (RTD3E)	0x00989680
95:92	M	Optional Asynchronous Events Supported (OAES)	0x00000200
99:96	M	Controller Attributes (CTRATT)	0x0002
100:101	O	Read Recovery Level support bitmap (rrls)	0x00
110:102	-	Reserved	0x00
111	M	Controller Type, if support NVMe 1.4 shall be set to other than 0 (cntrltype)	0x01
127:112	O	FRU Globally Unique Identifier (fguid[16])	0x00
129:128	O	Command Retry Delay Time 1 (crdt1)	0x00

Bytes	O/M	Description	Default Value
131:130	O	Command Retry Delay Time 2 (crdt2)	0x00
133:132	O	Command Retry Delay Time 3 (crdt3)	0x00
255:134	-	Reserved	0x00
257:256	M	Optional Admin Command Support (OACS)	0x0017
258	M	Abort Command Limit (ACL)	0x03
259	M	Asynchronous Event Request Limit (AERL)	0x03
260	M	Firmware Updates (FRMW)	0x12
261	M	Log Page Attributes (LPA)	0x08
262	M	Error Log Page Entries (ELPE)	0x3E
263	M	Number of Power States Support (NPSS)	0x4
264	M	Admin Vendor Specific Command Configuration (AVSCC)	0x01
265	O	Autonomous Power State Transition Attributes (APSTA)	0x01
267:266	M	Warning Composite Temperature Threshold (WCTEMP)	0x0157 (70C)
269:268	M	Critical Composite Temperature Threshold (CCTEMP)	0x017F (110C)
271:270	O	Maximum Time for Firmware Activation (MTFA)	0x0064
275:272	O	Host Memory Buffer Preferred Size (HMPRE)	0x00000000
279:276	O	Host Memory Buffer Minimum Size (HMMIN)	0x00000000
295:280	O	Total NVM Capacity (TNVMCAP)	**
311:296	O	Unallocated NVM Capacity (UNVMCAP)	0x00
315:312	O	Replay Protected Memory Block Support (RPMBS)	0x00
317:316	O	Extended Device Self-test Time (edstt)	0x000A
318	O	Device Self-test Options (dsto)	0x00
319	M	Firmware Update Granularity (fwug)	0x01
321:320	M	Keep Alive Support (kas)	0x0000
323:322	O	Host Controlled Thermal Management Attributes (hctma)	0x0001
325:324	O	Minimum Thermal Management Temperature (mntmt)	0x0111
327:326	O	Maximum Thermal Management Temperature (mxtmt)	0x0160
331:328	O	Sanitize Capabilities (sanicap)	0x00
335:332	O	Host Memory Buffer Min. Descriptor Entry Size (hmminds)	0x00
337:336	O	Host Memory Maximum Descriptor Entries (hmmxd)	0x00
339:338	O	NVM Set ID Maximum (nsetidmax)	0x00
341:340	O	Endurance Group ID Maximum (endgidmax)	0x00
342	O	ANA Maximum Transition Time (anatt)	0x00
343	O	Asymmetric Namespace Access Capabilities (anacap)	0x00
347:344	O	ANA Group ID Maximum (anagrpxmax)	0x00
351:348	O	Number of ANA Group IDs (nanagrpid)	0x00
355:352	O	Persistent Event Log Size (pels)	0x00
511:356	-	Reserved	0x00
<b>NVM Command Set Attributes</b>			
512	M	Submission Queue Entry Size (SQES)	0x66
513	M	Completion Queue Entry Size (CQES)	0x44

Bytes	O/M	Description	Default Value
515:514	M	Maximum Outstanding Commands (maxcmd)	0x0200
519:516	M	Number of Namespaces (NN)	0x00000001
521:520	M	Optional NVM Command Support (ONCS)	0x005D
523:522	M	Fused Operation Support (FUSES)	0x0000
524	M	Format NVM Attributes (FNA)	0x00
525	M	Volatile Write Cache (VWC)	0x07
527:526	M	Atomic Write Unit Normal (AWUN)	0x00FF
529:528	M	Atomic Write Unit Power Fail (AWUPF)	0x0000
530	M	NVM Vendor Specific Command Configuration (NVSCC)	0x01
531	M	Namespace Write Protection Capabilities (nwpc)	0x00
533:532	O	Atomic Compare & Write Unit (ACWU)	0x0000
535:534	M	Reserved	0x0000
539:536	O	SGL Support (SGLS)	0x00000000
543:540	O	Maximum Number of Allowed Namespace, if supports ANA Reporting shall not be 0 and less than NN (mnan)	0x00
767:544	-	Reserved	0x00
<b>IO Command Set Attributes</b>			
1023:768	M	NVM Subsystem NVMe Qualified Name (subnqn)	0x00
1791:1024	-	Reserved	0x00
2047:1792	-	Refer to the NVMe over Fabrics specification	0x00
2079:2048	M	Power State 0 Descriptor (PSD0)	0x0370
2111:2080	O	Power State 1 Descriptor (PSD1)	[2081:2080] 0x02C6 [2095:2092] 0x01010101
2143:2112	O	Power State 2 Descriptor (PSD2)	[2113:2112] 0x0208 [2127:2124] 0x02020202
2175:2144	O	Power State 3 Descriptor (PSD3)	[2149:2144] 0x000007D0000007D01100026C [2159:2156] 0x03030303
2207:2176	O	Power State 4 Descriptor (PSD4)	[2185:2176] 0x000061A8000061A8110001B8 [2191:2188] 0x04040404
2239:2208	O	Power State 5 Descriptor (PSD5)	0x00
2271:2240	O	Power State 6 Descriptor (PSD6)	0x00
2303:2272	O	Power State 7 Descriptor (PSD7)	0x00
2335:2304	O	Power State 8 Descriptor (PSD8)	0x00
2367:2336	O	Power State 9 Descriptor (PSD9)	0x00
2399:2368	O	Power State 10 Descriptor (PSD10)	0x00
2431:2400	O	Power State 11 Descriptor (PSD11)	0x00
2463:2432	O	Power State 12 Descriptor (PSD12)	0x00
2495:2464	O	Power State 13 Descriptor (PSD13)	0x00
2527:2496	O	Power State 14 Descriptor (PSD14)	0x00
2559:2528	O	Power State 15 Descriptor (PSD15)	0x00
2591:2560	O	Power State 16 Descriptor (PSD16)	0x00
2623:2592	O	Power State 17 Descriptor (PSD17)	0x00
2655:2624	O	Power State 18 Descriptor (PSD18)	0x00
2687:2656	O	Power State 19 Descriptor (PSD19)	0x00
2719:2688	O	Power State 20 Descriptor (PSD20)	0x00
2751:2720	O	Power State 21 Descriptor (PSD21)	0x00

Bytes	O/M	Description	Default Value
2783:2752	O	Power State 22 Descriptor (PSD22)	0x00
2815:2784	O	Power State 23 Descriptor (PSD23)	0x00
2847:2816	O	Power State 24 Descriptor (PSD24)	0x00
2879:2848	O	Power State 25 Descriptor (PSD25)	0x00
2911:2880	O	Power State 26 Descriptor (PSD26)	0x00
2943:2912	O	Power State 27 Descriptor (PSD27)	0x00
2975:2944	O	Power State 28 Descriptor (PSD28)	0x00
3007:2976	O	Power State 29 Descriptor (PSD29)	0x00
3039:3008	O	Power State 30 Descriptor (PSD30)	0x00
3071:3040	O	Power State 31 Descriptor (PSD31)	0x00
<b>Vendor Specific</b>			
4095:3072	O	Vendor Specific (VS)	Phison Reserved

\*The OUI shall be a valid IEEE/RAC assigned identifier that may be registered at <http://standards.ieee.org/develop/regauth/oui/public.html>

\*\*Depends on the using of capacity

Table 6-6 Identify Namespace Data Structure & NVM Command Set Specific

Bytes	O/M	Description	Default Value
7:0	M	Namespace Size (NSZE)	TBD*
15:8	M	Namespace Capacity (NCAP)	TBD*
23:16	M	Namespace Utilization (NUSE)	TBD*
24	M	Namespace Features (NSFEAT)	0x00
25	M	Number of LBA Formats (NLBAF)	0x01
26	M	Formatted LBA Size (FLBAS)	0x00
27	M	Metadata Capabilities (MC)	0x00
28	M	End-to-end Data Protection Capabilities (DPC)	0x00
29	M	End-to-end Data Protection Type Settings (DPS)	0x00
30	O	Namespace Multi-path I/O and Namespace Sharing Capabilities (NMIC)	0x00
31	O	Reservation Capabilities (RESCAP)	0x00
32	O	Format Progress Indicator (FPI)	0x00
33	O	Deallocate Logical Block Features (dlfeat)	0x09
35:34	O	Namespace Atomic Write Unit Normal (NAWUN)	0x0000
37:36	O	Namespace Atomic Write Unit Power Fail (NAWUPF)	0x0000
39:38	O	Namespace Atomic Compare & Write Unit (NACWU)	0x0000
41:40	O	Namespace Atomic Boundary Size Normal (NABSN)	0x0000
43:42	O	Namespace Atomic Boundary Offset (NABO)	0x0000
45:44	O	Namespace Atomic Boundary Size Power Fail (NABSPF)	0x0000
47:46		Namespace Optimal IO Boundary (noiob)	0x0000
64:48	O	NVM Capacity (NVMCAP)	500GB: 0x7470C06000 1000GB: 0xE8E0DB6000 2000GB: 0x01D1C1116000 4000GB: 0x03A3817D6000 8000GB: 0x000747025560
65:64	O	Namespace Preferred Write Granularity (npwg)	0x00

Bytes	O/M	Description	Default Value
67:66	O	Namespace Preferred Write Alignment (npwa)	0x00
69:68	O	Namespace Preferred Deallocation(Trim) Granularity (npg)	0x00
71:70	O	Namespace Preferred Deallocation(Trim) Alignment (npda)	0x00
73:72	O	Namespace Optimal Write Size (nows)	0x00
91:74	-	Reserved	0x00
95:92	O	ANA Groput Identifier (anagrpId)	0x00
98:96	-	Reserved	0x00
99	O	Namespace Attributes (nsattr)	0x00
101:100	O	NVM Set Identifier (nvmsetid)	0x00
103:102	O	Endurance Group Identifier // NVMe 1.4 add (endgid)	0x00
119:104	O	Namespace Globally Unique Identifier (NGUID)	TBD**
127:120	O	IEEE Extended Unique Identifier (EUI64)	TBD**
131:128	M	LBA Format 0 Support (LBAF0)	0x02090000
135:132	O	LBA Format 1 Support (LBAF1)	0x010C0000
139:136	O	LBA Format 2 Support (LBAF2)	0x00000000
143:140	O	LBA Format 3 Support (LBAF3)	0x00000000
147:144	O	LBA Format 4 Support (LBAF4)	0x00000000
151:148	O	LBA Format 5 Support (LBAF5)	0x00000000
155:152	O	LBA Format 6 Support (LBAF6)	0x00000000
159:156	O	LBA Format 7 Support (LBAF7)	0x00000000
163:160	O	LBA Format 8 Support (LBAF8)	0x00000000
167:164	O	LBA Format 9 Support (LBAF9)	0x00000000
171:168	O	LBA Format 10 Support (LBAF10)	0x00000000
175:172	O	LBA Format 11 Support (LBAF11)	0x00000000
179:176	O	LBA Format 12 Support (LBAF12)	0x00000000
183:180	O	LBA Format 13 Support (LBAF13)	0x00000000
187:184	O	LBA Format 14 Support (LBAF14)	0x00000000
191:188	O	LBA Format 15 Support (LBAF15)	0x00000000
383:192	-	Reserved	0x00
4095:384	O	Vendor Specific (VS)	0x00

\*See IDEMA SPEC

\*\*See IEEE EUI-64 SPEC

Table 6-7 List of Identify Namespace Data Structure for Each Capacity

Capacity (GB)	Byte[7:0]: Namespace Size (NSZE)	Byte[7:0]: Namespace Size (NSZE) (Dec)
500	3A386030	976,773,168
1000	74706DB0	1,953,535,168
2000	E8E088B0	3,907,029,168
4000	1D1C0BEB0	7,814,037,168
8000	3A3812AB0	15,628,053,168



### 6.3. SMART Attributes

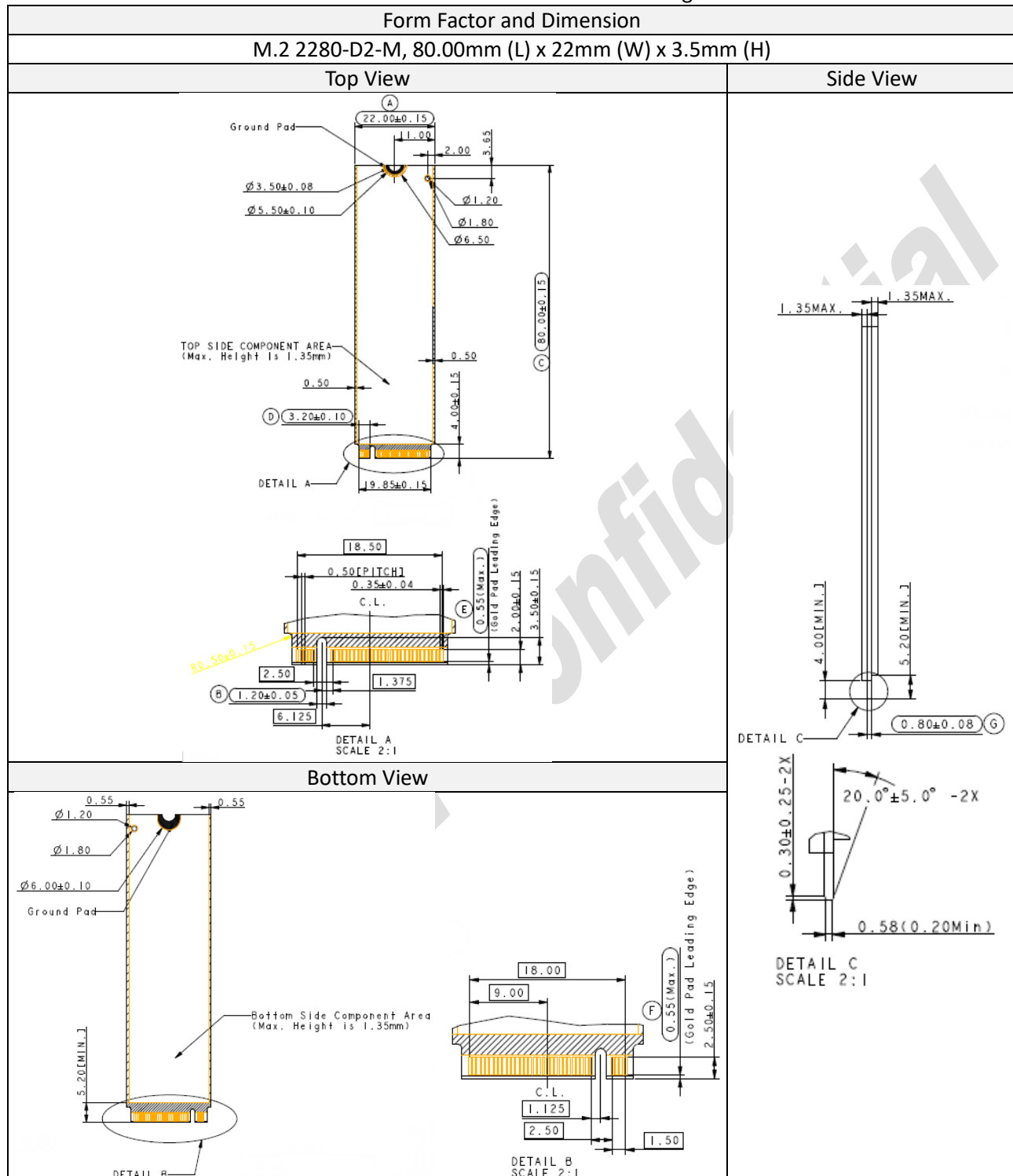
Table 6-8 SMART Attributes (Log Identifier 02h)

Bytes Index	Bytes	Description
[0]	1	Critical Warning
[2:1]	2	Composite Temperature
[3]	1	Available Spare
[4]	1	Available Spare Threshold
[5]	1	Percentage Used
[31:6]	26	Reserved
[47:32]	16	Data Units Read
[63:48]	16	Data Units Written
[79:64]	16	Host Read Commands
[95:80]	16	Host Write Commands
[111:96]	16	Controller Busy Time
[127:112]	16	Power Cycles
[143:128]	16	Power On Hours
[159:144]	16	Unsafe Shutdowns
[175:160]	16	Media and Data Integrity Errors
[191:176]	16	Number of Error Information Log Entries
[195:192]	4	Warning Composite Temperature Time
[199:196]	4	Critical Composite Temperature Time
[201:200]	2	Temperature Sensor 1 (Current Temperature)
[203:202]	2	Temperature Sensor 2 (N/A)
[205:204]	2	Temperature Sensor 3 (N/A)
[207:206]	2	Temperature Sensor 4 (N/A)
[209:208]	2	Temperature Sensor 5 (N/A)
[211:210]	2	Temperature Sensor 6 (N/A)
[213:212]	2	Temperature Sensor 7 (N/A)
[215:214]	2	Temperature Sensor 8 (N/A)
[511:216]	296	Reserved

## 7. PHYSICAL DIMENSION

### 7.1. M.2 2280-D2-M

Table 7-1 M.2 2280-D2-M Mechanical Diagram





## 7.2. M.2 2280-S2-M

### Table 7-2 M.2 2280-S2-M Mechanical Diagram

**Form Factor and Dimension**

**M.2 2280-S2-M, 80.00mm (L) x 22mm (W) x 2.15mm (H)**

Top View	Side View
<p><b>Top View</b></p> <p>Ground Pad</p> <p>TOP SIDE COMPONENT AREA (Max. Height Is 1.35mm)</p> <p>DETAIL A</p> <p>DETAIL B</p> <p>DETAIL C</p> <p>DETAIL D</p> <p>DETAIL E</p> <p>DETAIL F</p> <p>Scale: 2:1</p>	<p><b>Side View</b></p> <p>DETAIL C</p> <p>Scale: 2:1</p>
<p><b>Bottom View</b></p> <p>Don't allow any component on the Bottom side.</p> <p>DETAIL B</p> <p>DETAIL C</p> <p>DETAIL D</p> <p>DETAIL E</p> <p>DETAIL F</p> <p>Scale: 2:1</p>	

## 8. APPLICATION NOTES

### 8.1. Wafer Level Chip Scale Packaging (WLCSP) Handling Precautions

There are a lot of components assembled on a single SSD device. Please handle the drive with care especially when it has any WLCSP (Wafer Level Chip Scale Packaging) components such as PMIC, thermal sensor or load switch. WLCSP is one of the packaging technologies that is widely adopted for making smaller footprints, but any bumps or scratches may damage those ultrasmall parts so gentle handling is strongly recommended.

- ⚠ DO NOT DROP SSD
- ⚠ INSTALL SSD WITH CARE
- ⚠ STORE SSD IN A PROPER PACKAGE

### 8.2. M Key M.2 SSD Assembly Precautions

M Key M.2 SSD is only compatible to M Key socket. As shown in Use Case 2, misuse may cause severe damages to SSD including burn-out.

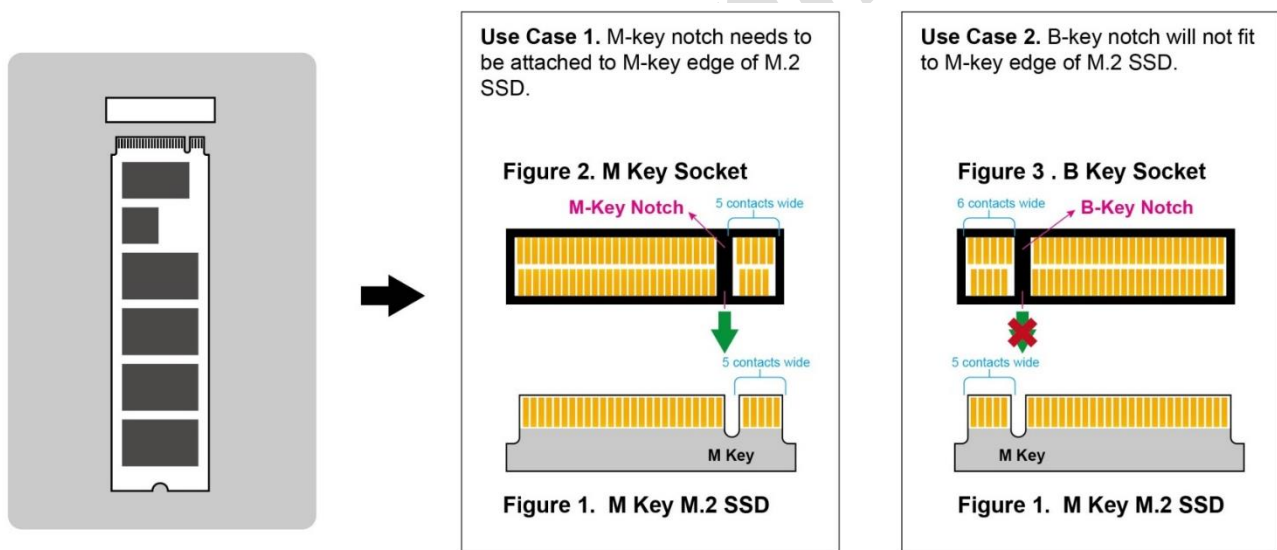


Figure 8-1 M Key M.2 Assembly Precautions

## 9. PRODUCT WARRANTY POLICY

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In the event the Product does not conform to the specification within Phison agreed warranty period and such inconformity is solely attributable to Phison's cause, Phison agrees at its discretion replace or repair the nonconforming Product. Notwithstanding the foregoing, the aforementioned warranty shall exclude the inconformity arising from, in relation to or associated with:

- (1) alternation, modification, improper use, misuse or excessive use of the Product;
- (2) failure to comply with Phison's instructions;
- (3) Phison's compliance with customer (including customer's suppliers, subcontractors or downstream customers) indicated instructions, technologies, designs, specifications, materials, components, parts;
- (4) combination of the Product with other materials, components, parts, goods, hardware, firmware or software not developed by Phison; or
- (5) other error or failure not solely attributable to Phison's cause (including without limitation, normal wear or tear, manufacturing or assembly wastage, improper operation, virus, unauthorized maintenance or repair).

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## 10. REFERENCE

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The following table is to list out the standards that have been adopted for designing the product.

Table 10-1 List of References

Title	Acronym/Source
RoHS	Restriction of Hazardous Substances Directive; for further information, please contact us at <a href="mailto:sales@phison.com">sales@phison.com</a> or <a href="mailto:support@phison.com">support@phison.com</a> .
M.2	<a href="http://www.pcisig.com">http://www.pcisig.com</a>
PCI Express Base 4.0	<a href="https://www.pcisig.com/specifications/pciexpress/base3/">https://www.pcisig.com/specifications/pciexpress/base3/</a>
NVM Express Specification Rev.1.4	<a href="http://www.nvmexpress.org/">http://www.nvmexpress.org/</a>
Solid-State Drive Requirements and Endurance Test Method (JESD219A)	<a href="http://www.jedec.org/standards-documents/docs/jesd219a">http://www.jedec.org/standards-documents/docs/jesd219a</a>

## 11. TERMINOLOGY

The following table is to list out the acronyms that have been applied throughout the document.

Table 11-1 List of Terminology

Term	Definitions
ATTO	Commercial performance benchmark application
DDR	Double data rate (SDRAM)
ASPM	Active States Power Management
APST	Autonomous Power State Transition
LBA	Logical block addressing
MB	Mega-byte
GB	Giga-byte
TB	Tera-byte
MTBF	Mean time between failures
PCIe	PCI Express / Peripheral Component Interconnect Express
S.M.A.R.T.	Self-monitoring, analysis and reporting technology
SSD	Solid state disk