



Industrial microSD 3.0 Specification

(FxPrem II Series, MLC)

Version 2

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1. INTRODUCTION

1.1. Product Overview

Based on NAND Flash technology Memory, Renice X5 2.5" IDE SSD (Solid State Drive) is a storage device with high performance and high reliability. Equipped with powerful Error Correction Coding (ECC) and flash interface, Renice X5 2.5" IDE SSD can support new generation NAND flash and keep much more stability in data transmission.

Renice X5 2.5" IDE SSD offers advanced technology to transfer data to the host via a high efficiency DMA engine and utilizes the internal memory buffer in a sufficient way. With Renice's optimized wear leveling, bad block management and flash management technologies, Renice X5 2.5" IDE SSD delivers extraordinary performance in data read/write speed and data reliability. Furthermore, with Internal detectors for power fail protection, over voltage and inrush current protection hardware design, Renice X5 2.5" IDE SSD can be a high-end IDE storage device for areas including industrial, automobile, military and medical, etc.

1.2. Feature

- Performance:
Read/Write: 118/109MB/s (@128GB)
- Form factor: 2.5-inch (100.0mm x 70.0mm x 9.5mm) L×W×H
- Interface standard: 44 PIN PATA IDE
- Density: 8GB, 16GB, 32GB, 64GB, 128GB
- Input voltage: 5.0V (±5%)
- Industrial operating temperature range from -40°C to +85°C
- Flash management algorithm: static and dynamic wear-leveling, bad block management algorithm.
- Supports dynamic power management and SMART (Self-Monitoring, Analysis and Reporting Technology).
- Internal detectors for power fail protection and Over voltage and inrush current protection hardware design.
- Hardware BCH ECC capable of correcting errors up to 72-bit/1KB ● Write endurance: >8 years @ 100GB write/day (8GB SLC SSD)
- Read endurance: unlimited
- Data retention: JESD47 compliant
- MTBF: 3,000,000 Hours



2.3. Internal detectors for power fail protection

- Built-in 1.2V power-on reset
- Built-in 2.7V voltage detectors for power fail protection

3. Interface Description

3.1. Pin Assignment

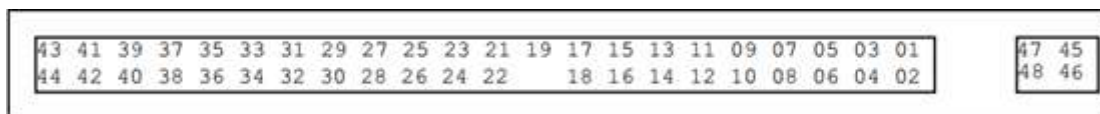


Figure 3: Pin Assignment

3.2. Pin Description

| Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name |
|---------|----------|---------|----------|---------|----------|---------|----------|
| 1 | RESET | 14 | D13 | 27 | IORDY | 40 | GND |
| 2 | GND | 15 | D1 | 28 | CSEL | 41 | VCC35I |
| 3 | D7 | 16 | D14 | 29 | DMACK | 42 | VCC35I |
| 4 | D8 | 17 | D0 | 30 | GND | 43 | GND |
| 5 | D6 | 18 | D15 | 31 | INTRQ | 44 | NC |
| 6 | D9 | 19 | GND | 32 | NC | 45 | GND |
| 7 | D5 | 20 | NC | 33 | A1 | 46 | CCSEL |
| 8 | D10 | 21 | DMARQ | 34 | DIAG | 47 | NC |
| 9 | D4 | 22 | GND | 35 | A0 | 48 | CSEL |
| 10 | D11 | 23 | IOWR | 36 | A2 | | |
| 11 | D3 | 24 | GND | 37 | CS0 | | |
| 12 | D12 | 25 | IORD | 38 | CS1 | | |
| 13 | D2 | 26 | GND | 39 | DASP | | |

3.3. Master/ Slave settings instructions

Master disk: No connect

Slave disk: Connect 45 and 46

CableSelect: Connect 48 and 46

4. Electric Specifications

This chapter contains preliminary information and may be updated in a later version.

4.1. DC Characteristics

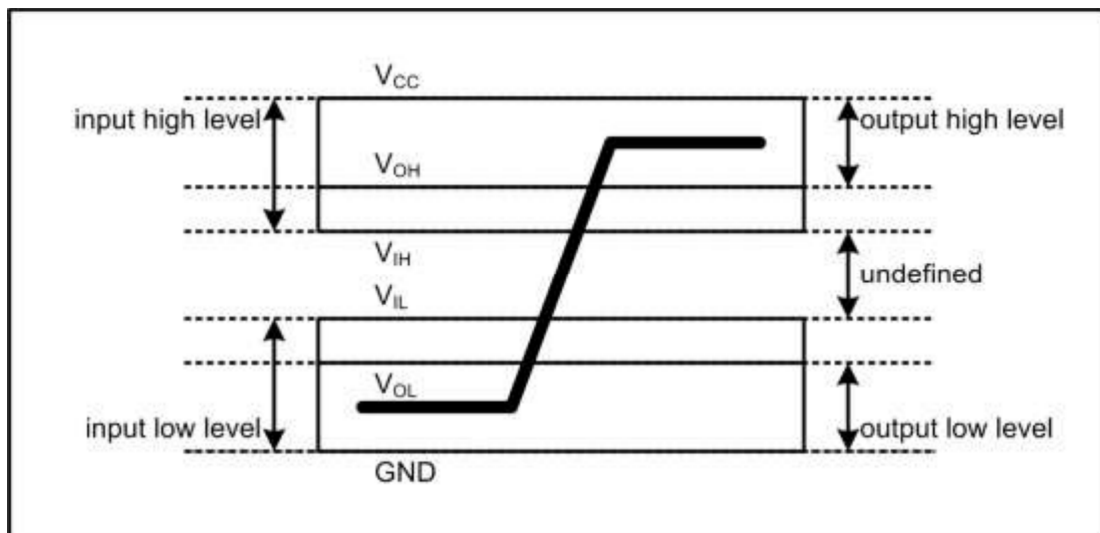


Figure 4: Bus Signal Level

DC Characteristics for Host Interface ($V_{CC} = 5V$)

| Parameter | Symbol | Min | Max | Unit | Remark |
|---------------------------|--------|-----------|------|------|---------------------|
| Supply Voltage | VCC | 4.5 | 5.5 | V | |
| High Level Output Voltage | VOH | VCC - 0.8 | | V | |
| Low Level Output Voltage | VOL | | 0.8 | V | |
| High Level Input Voltage | VIH | 4.0 | | V | Non-schmitt trigger |
| | | 2.92 | | V | Schmitt trigger[1] |
| Low Level Input Voltage | VIL | | 0.8 | V | Non-schmitt trigger |
| | | | 1.70 | V | Schmitt trigger[1] |
| Pull-Up Resistance | RPU | 50 | 73 | kΩ | |
| Pull-Down Resistance | RPD | 50 | 97 | kΩ | |

DC Characteristics for Host Interface ($V_{CC} = 3.3V$)

| Parameter | Symbol | Min | Max | Unit | Remark |
|---------------------------|--------|-----------|------|------|---------------------|
| Supply Voltage | VCC | 2.97 | 3.63 | V | |
| High Level Output Voltage | VOH | VCC - 0.8 | | V | |
| Low Level Output Voltage | VOL | | 0.8 | V | |
| High Level Input Voltage | VIH | 2.4 | | V | Non-schmitt trigger |
| | | 2.05 | | V | Schmitt trigger[1] |
| Low Level Input Voltage | VIL | | 0.6 | V | Non-schmitt trigger |
| | | | 1.25 | V | Schmitt trigger[1] |
| Pull-Up Resistance | RPU | 52.7 | 141 | kΩ | |
| Pull-Down Resistance | RPD | 47.5 | 172 | kΩ | |

The I/O Pins other than Host Interface

| Parameter | Symbol | Min | Max | Unit | Remark |
|---------------------------|--------|-----|-----|------|---------------------|
| Supply Voltage | VCC | 2.7 | 3.6 | V | |
| High Level Output Voltage | VOH | 2.4 | | V | |
| Low Level Output Voltage | VOL | | 0.4 | V | |
| High Level Input Voltage | VIH | 2.0 | | V | Non-schmitt trigger |
| | | 1.4 | 2.0 | V | Schmitt trigger[1] |
| Low Level Input Voltage | VIL | | 0.8 | V | Non-schmitt trigger |
| | | 0.8 | 1.2 | V | Schmitt trigger[1] |
| Pull-Up Resistance | RPU | 40 | | kΩ | |
| Pull-Down Resistance | RPD | 40 | | kΩ | |

Notes:

[1] Include CE1#, CE2#, HREG#, HOE#, HIOE#, HWE#, HIOW# pins. [2] Include RST#, T0, T1, and T2 pin.

4.2. Internal IP Characteristics

1.2V Power On Reset

| Parameter | Min | Max | Unit |
|-------------------------|------|------|------|
| Detect Voltage | | 1.3 | V |
| Operating Voltage Range | 0 | 1.65 | V |
| Delay Time | Rise | 4.5 | μs |
| | Fall | 2 | μs |

2.7V Voltage Detector

| Parameter | Min | Max | Unit |
|----------------------|------|-----|------|
| Detect Voltage Range | VRR | 1.4 | 2.9 |
| | VFR | 1.3 | 2.8 |
| Delay Time | Rise | 4.5 | us |
| | Fall | 1.5 | us |

4.3. AC Characteristics

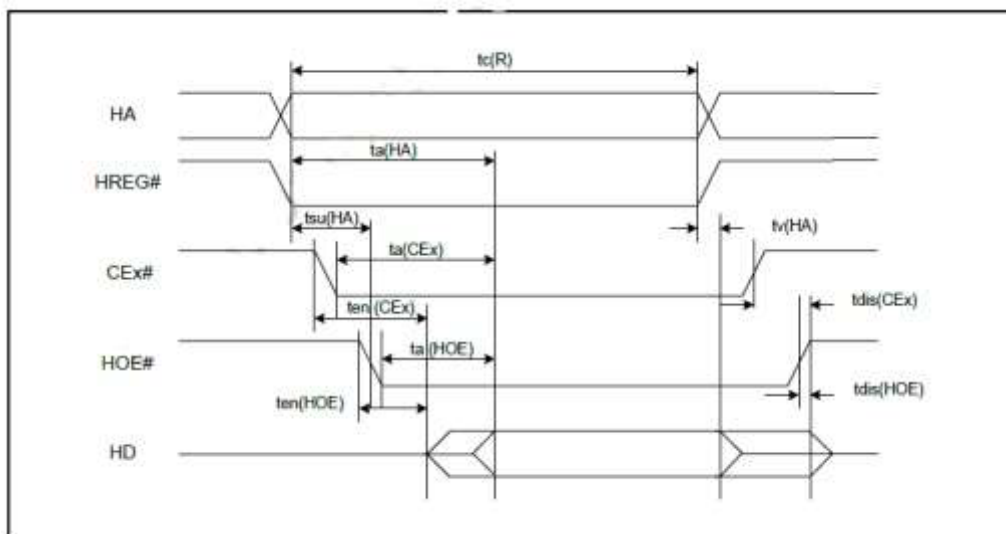
Attribute Memory Read Timing

| Speed Version | | 300 ns | | Unit |
|-------------------------------|-----------|--------|-----|------|
| Item | Symbol | Min | Max | |
| Read Cycle Time | tc(R) | 300 | | ns |
| Address Access Time | ta(HA) | | 300 | ns |
| Card Enable Access Time | ta(CEX) | | 300 | ns |
| Output Enable Access Time | ta(HOE) | | 150 | ns |
| Output Disable Time from CEX# | tdis(CEX) | | 100 | ns |
| Output Disable Time from HOE# | tdis(HOE) | | 100 | ns |

| | | | | |
|--------------------------------|----------|----|--|----|
| Address Setup Time | tsu(HA) | 30 | | ns |
| Output Enable Time from CEx# | ten(CEx) | 5 | | ns |
| Output Enable Time from HOE# | ten(HOE) | 5 | | ns |
| Data Valid from Address Change | tv(HA) | 0 | | ns |

Note: All time intervals are recorded in nanoseconds. HD refers to data provided by the PATA Card to the system. The CEx# signal or both the HOE# signal and the HWE# signal are deasserted between consecutive cycle operations.

Figure 5: Attribute Memory Read Timing

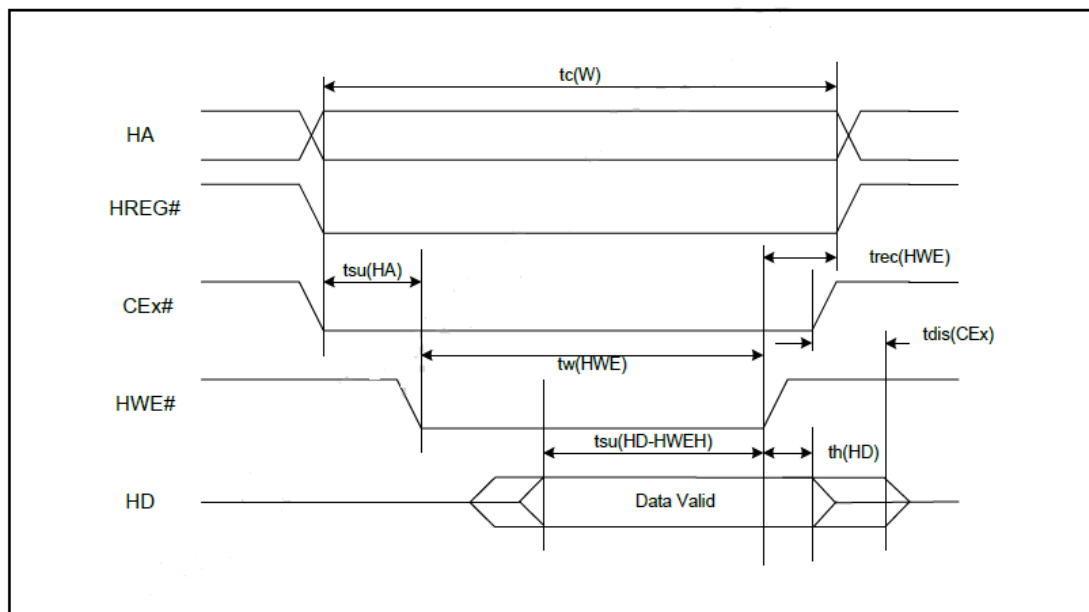


Configuration Register (Attribute Memory) Write Timing

| Speed Version | | 250 ns | | Unit |
|--------------------------|--------------|--------|-----|------|
| Item | Symbol | Min | Max | |
| Write Cycle Time | tc(W) | 250 | | ns |
| Write Pulse Width | tw(HWE) | 150 | | ns |
| Address Setup Time | tsu(HA) | 30 | | ns |
| Write Recovery Time | trec(HWE) | 30 | | ns |
| Data Setup Time for HWE# | tsu(HD-HWEH) | 80 | | ns |
| Data Hold Time | th(HD) | 30 | | ns |

Note: All time intervals are recorded in nanoseconds. HD refers to data provided by the system to the PATA Card.

Figure 6: Configuration Register (Attribute Memory) Write Timing



Common Memory Read Timing

| Cycle Time Mode | | 250 ns | | 120ns | | 100ns | | 80ns | | Unit |
|---------------------------------|---------------|--------|-----|-------|-----|-------|-----|------|-------|------|
| Item | Symbol | Min | Max | Min | Max | Min | Max | Min | Max | |
| Output Enable Access Time | ta(HOE) | | 125 | | 60 | | 50 | | 45 | ns |
| Output Disable Time from HOE# | tdis(HOE) | | 100 | | 60 | | 50 | | 45 | ns |
| Address Setup Time | tsu(HA) | 30 | | 15 | | 10 | | 10 | | ns |
| Address Hold Time | t th(HA) | 20 | | 15 | | 15 | | 10 | | ns |
| CEx# Setup before HOE# | tsu(CEx) | 0 | | 0 | | 0 | | 0 | | ns |
| CEx# Hold following HOE# | th(CEx) | 20 | | 15 | | 15 | | 10 | | ns |
| Wait Delay Falling from HOE# tv | tv(IORDY-HOE) | | 35 | | 35 | | 35 | | na[1] | ns |
| Data Setup for Wait Release | tv(IORDY) | | 0 | | 0 | | 0 | | na[1] | ns |

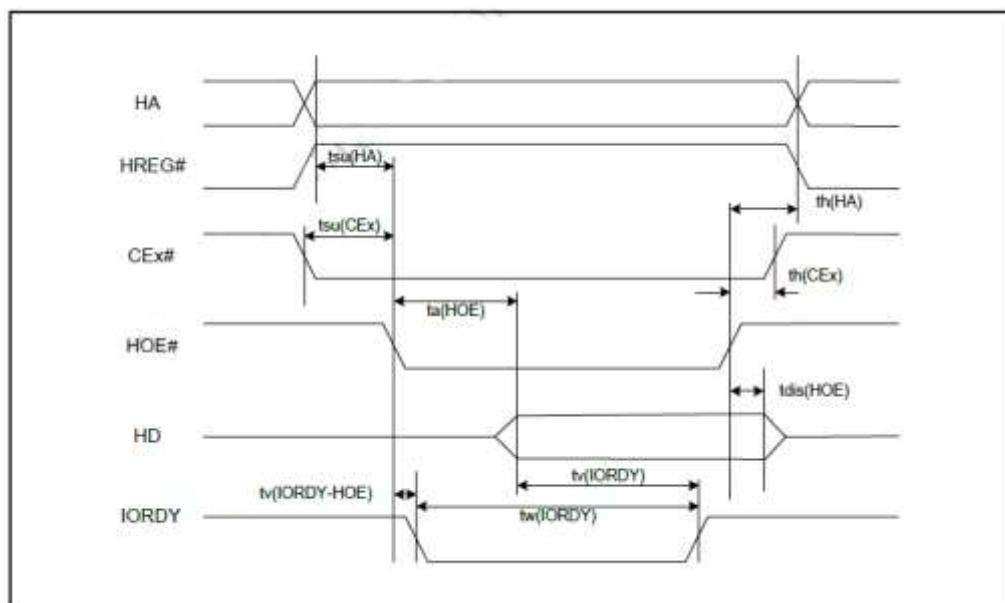
| | | | | | | | | | | |
|--------------------------------|-----------|--|-----|--|-----|--|-----|--|-------------------|----|
| Wait Width Time ^[2] | tw(IORDY) | | 350 | | 350 | | 350 | | na ^[1] | ns |
|--------------------------------|-----------|--|-----|--|-----|--|-----|--|-------------------|----|

Notes:

[1] IORDY is not supported in this mode.

[2] The maximum load on IORDY is 1 LSTTL with a 50 pF (40 pF below 120 nsec cycle time) total load. All time intervals are recorded in nanoseconds. HD refers to data provided by the PATA Card to the system. The IORDY signal can be ignored when the HOE# cycle-to-cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure (CIS). Although adhering to the PCMCIA specification of 12 μ s, the Wait Width time is intentionally lower in this specification.

Figure 7: Common Memory Read Timing



Common Memory Write Timing

| Cycle Time Mode | | 250 ns | | 120ns | | 100ns | | 80ns | | Unit |
|--------------------------|--------------|--------|-----|-------|-----|-------|-----|------|-----|------|
| Item | Symbol | Min | Max | Min | Max | Min | Max | Min | Max | |
| Data Setup before HWE# | tsu(HD-HWEH) | 80 | | 50 | | 40 | | 30 | | ns |
| Data Hold following HWE# | th(HD) | 30 | | 15 | | 10 | | 10 | | ns |
| HWE# Pulse Width | tw(HWE) | 150 | | 70 | | 60 | | 55 | | ns |
| Address Setup Time | tsu(HA) | 30 | | 15 | | 10 | | 10 | | ns |
| CEx# Setup before HWE# | tsu(CEx) | 0 | | 0 | | 0 | | 0 | | ns |
| Write Recovery Time | Trec (HWE) | 30 | | 15 | | 15 | | 15 | | ns |
| Address Hold Time | th(HA) | 20 | | 15 | | 15 | | 15 | | ns |
| CEx# Hold following HWE# | th(CEx) | 20 | | 15 | | 15 | | 10 | | ns |

| | | | | | | | | | | |
|--------------------------------|---------------|---|-----|---|-----|---|-----|-------|-------|----|
| Wait Delay Falling from HWE# | tv(IORDY-HWE) | | 35 | | 35 | | 35 | | na[1] | ns |
| HWE# High from Wait Release | Tv (IORDY) | 0 | | 0 | | 0 | | na[1] | | |
| Wait Width Time ^[2] | tw (IORDY) | | 350 | | 350 | | 350 | | na[1] | |

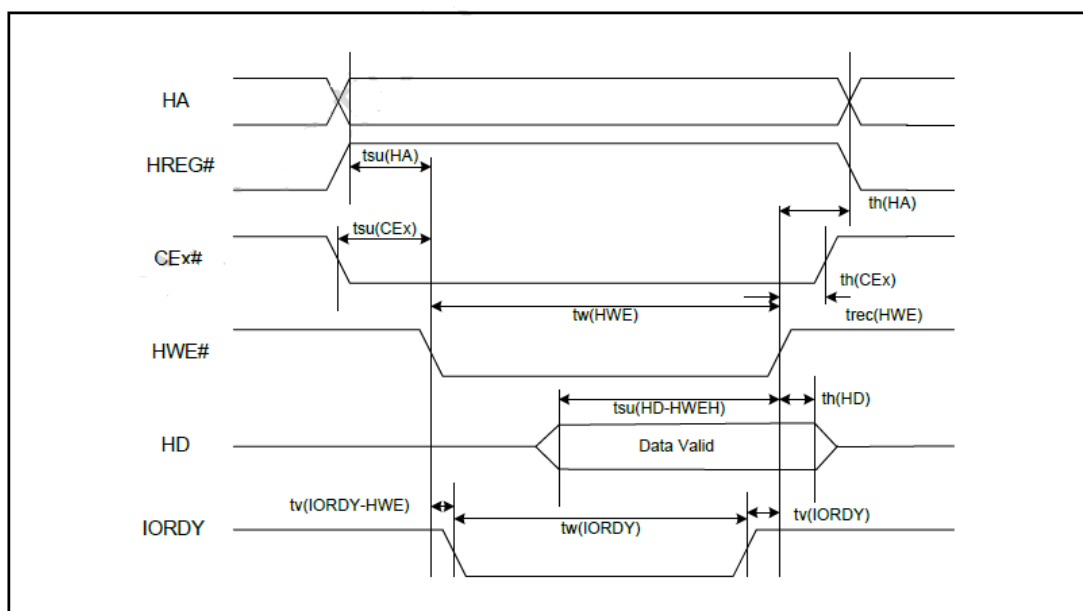
Notes:

[1] IORDY is not supported in this mode.

[2] The maximum load on IORDY is 1 LSTTL with a 50 pF (40 pF below 120 nsec Cycle Time) total load. All time intervals are recorded in nanoseconds. HD refers to data provided by the PATA Card to the system. The IORDY signal can be ignored when the HWE# cycle-to-cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure (CIS).

Although adhering to the PCMCIA specification of 12 μ s, the Wait Width time is intentionally lower in this specification.

Figure 8: Common Memory Write Timing



I/O Read Timing

| Cycle Time Mode | | 250 ns | | 120ns | | 100ns | | 80ns | | Unit |
|------------------------------|---------------|--------|-----|-------|-----|-------|-----|------|-----|------|
| Item | Symbol | Min | Max | Min | Max | Min | Max | Min | Max | |
| Data Delay after HIOE# | td(HIOE) | | 100 | | 50 | | 50 | | 45 | ns |
| Data Hold following HIOE# | th(HIOE) | 0 | | 5 | | 5 | | 5 | | ns |
| HIOE# Width Time | tw(HIOE) | 165 | | 70 | | 65 | | 55 | | ns |
| Address Setup before HIOE# | tsuHA (HIOE) | 70 | | 25 | | 25 | | 15 | | ns |
| Address Hold following HIOE# | thHA (HIOE) | 20 | | 10 | | 10 | | 10 | | ns |
| CEx# Setup before HIOE# | tsuCEX (HIOE) | 5 | | 5 | | 5 | | 5 | | ns |

| | | | | | | | | | | |
|----------------------------------|----------------|----|-----|----|-----|----|-----|----|-------|----|
| CEx# Hold following HIOE# | thCEx (HIOE) | 20 | | 10 | | 10 | | 10 | | ns |
| HREG# Setup before HIOE# | tsuHREG (HIOE) | 5 | | 5 | | 5 | | 5 | | ns |
| HREG# Hold following HIOE# | thHREG (HIOE) | 0 | | 0 | | 0 | | 0 | | ns |
| Wait Delay Falling from HIOE#[2] | tdIORDY (HIOE) | | 35 | | 35 | | 35 | | na[1] | |
| Data Delay from Wait Rising[2] | Td (IORDY) | | 0 | | 0 | | 0 | | na[1] | |
| Wait Width Time[2] | Tw (IORDY) | | 350 | | 350 | | 350 | | na[1] | |

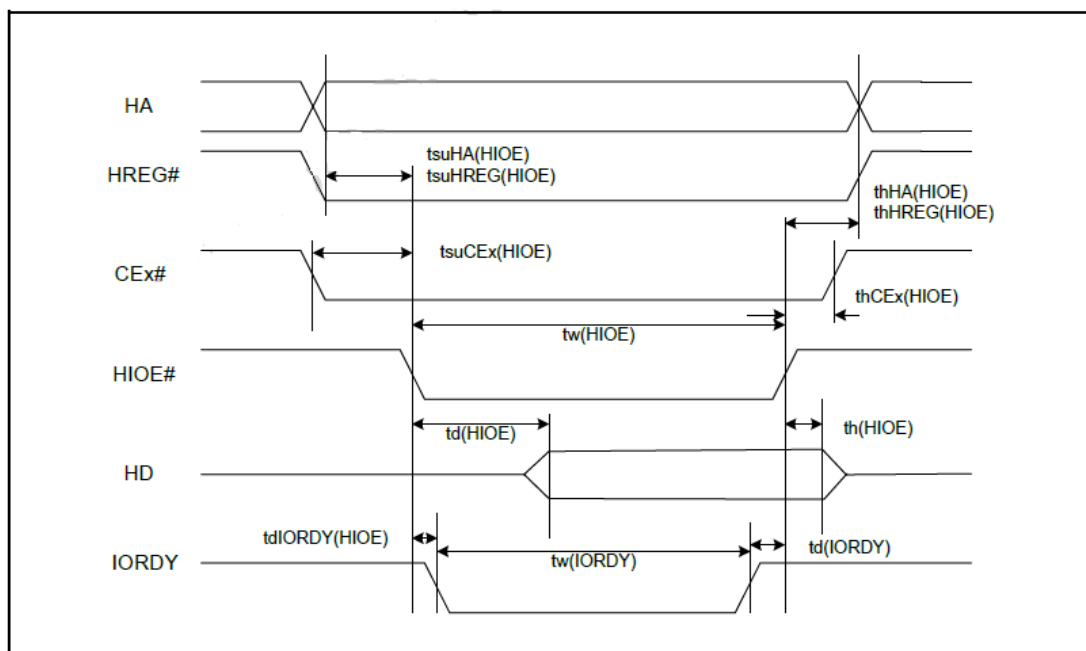
Notes:

[1] IORDY is not supported in this mode.

[2] Maximum load on IORDY is 1 LSTTL with a 50 pF (40 pF below 120 nsec cycle time) total load. All time intervals are recorded in nanoseconds. Although minimum time from IORDY high to HIOE# high is 0 nsec, the minimum HIOE# width is still met. HD refers to data provided by the PATA Card to the system.

Although adhering to the PCMCIA specification of 12 μ s, the Wait Width time is intentionally lower in this specification.

Figure 9: I/O Read Timing



I/O Write Timing

| Cycle Time Mode | | 250 ns | | 120ns | | 100ns | | 80ns | | Unit |
|-------------------------|-----------|--------|-----|-------|-----|-------|-----|------|-----|------|
| Item | Symbol | Min | Max | Min | Max | Min | Max | Min | Max | |
| Data Setup before HIOW# | tsu(HIOW) | 60 | | 20 | | 20 | | 15 | | ns |

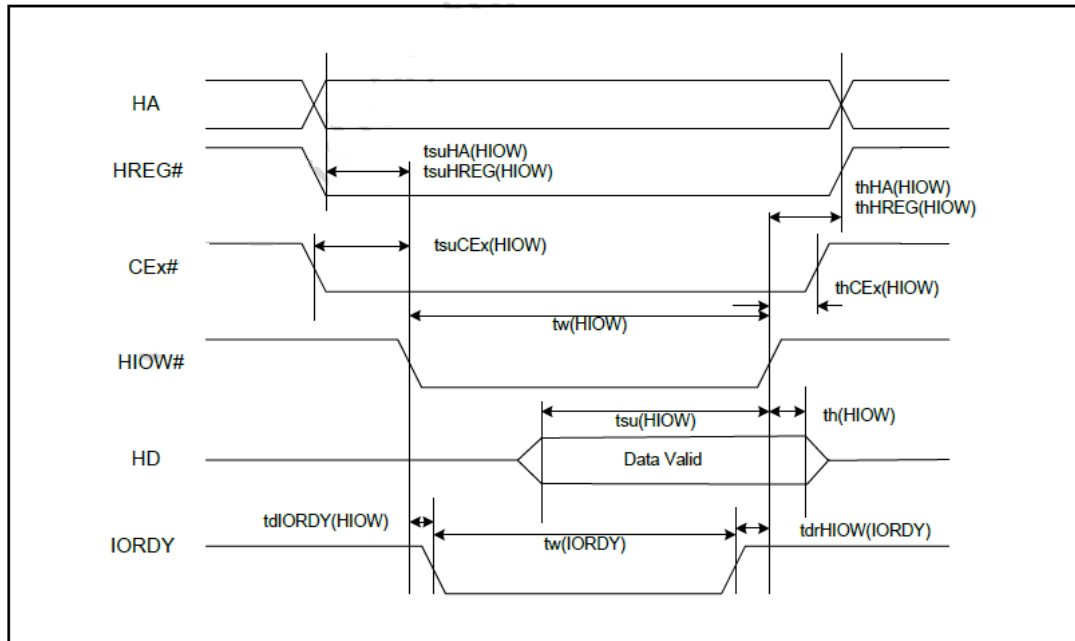
| | | | | | | | | | | |
|-------------------------------------|--------------------|-----|-----|----|-----|----|-----|-------------------|-------------------|----|
| Data Hold following HLOW# | th(HLOW) | 30 | | 10 | | 5 | | 5 | | ns |
| HLOW# Width Time | tw(HLOW) | 165 | | 70 | | 65 | | 55 | | ns |
| Address Setup before HLOW# | tsuHA (HLOW) | 70 | | 25 | | 25 | | 15 | | ns |
| Address Hold following HLOW# | thHA (HLOW) | 20 | | 20 | | 10 | | 10 | | ns |
| CEx# Setup before HLOW# | tsuCEX (HLOW) | 5 | | 5 | | 5 | | 5 | | ns |
| CEx# Hold following HLOW# | thCEX (HLOW) | 20 | | 20 | | 10 | | 10 | | ns |
| HREG# Setup before HLOW# | tsuHREG (HLOW) | 5 | | 5 | | 5 | | 5 | | ns |
| HREG# Hold following HLOW# | thHREG (HLOW) | 0 | | 0 | | 0 | | 0 | | ns |
| Wait Delay Falling from HLOW#[2] | tdIORDY (HLOW) | | 35 | | 35 | | 35 | | na _[1] | ns |
| HLOW# high from Wait high[2] | tdrHLOW (IORDY) | 0 | | 0 | | 0 | | na _[1] | | ns |
| Wait Width Time[2] | Tw (IORDY) | | 350 | | 350 | | 350 | | na _[1] | ns |

Notes:

[1] IORDY is not supported in this mode.

[2] The maximum load on IORDY is 1 LSTTL with a 50 pF (40 pF below 120 nsec cycle time) total load. All time intervals are recorded in nanoseconds. Although minimum time from IORDY high to HLOW# high is 0 nsec, the minimum HLOW# width is still met. HD refers to data provided by the PATA Card to the system. Although adhering to the PCMCIA specification of 12 μ s, the Wait Width time is intentionally lower in this specification.

Figure 10: I/O Write Timing



True IDE PIO Mode Read/Write Timing

| | Item | Mode 0 | Mode 1 | Mode 2 | Mode 3 | Mode 4 | Mode 5 | Mode 6 |
|-----|---|--------|--------|--------|--------|--------|-------------------|-------------------|
| t0 | Cycle time (Min.) ^[1] | 600 | 383 | 240 | 180 | 120 | 100 | 80 |
| t1 | Address valid to HIOE# / HIOW# setup (Min.) | 70 | 50 | 30 | 30 | 25 | 15 | 10 |
| t2 | HIOE# / HIOW# (Min.) ^[1] | 165 | 125 | 100 | 80 | 70 | 65 | 55 |
| t2 | HIOE# / HIOW# (Min.) Register (8-bit) ^[1] | 290 | 290 | 290 | 80 | 70 | 65 | 55 |
| t2i | HIOE# / HIOW# recovery time (Min.) ^[1] | - | - | - | 70 | 25 | 25 | 20 |
| t3 | HIOW# data setup (Min.) | 60 | 45 | 30 | 30 | 20 | 20 | 15 |
| t4 | HIOW# data hold (Min.) | 30 | 20 | 15 | 10 | 10 | 10 | 5 |
| t5 | HIOE# data setup (Min.) | 50 | 35 | 20 | 20 | 20 | 20 | 10 |
| t6 | HIOE# data hold (Min.) | 5 | 5 | 5 | 5 | 5 | 5 | 5 |
| t6Z | HIOE# data tristate (Max.) ^[2] | 30 | 30 | 30 | 30 | 30 | 30 | 20 |
| t7 | Address valid to IOCS16# assertion (Max.) ^[4] | 90 | 50 | 40 | n/a | n/a | n/a | n/a |
| t8 | Address valid to IOCS16# released (Max.) ^[4] | 60 | 45 | 30 | n/a | n/a | n/a | n/a |
| t9 | HIOE# / HIOW# to address valid hold | 20 | 15 | 10 | 10 | 10 | 10 | 10 |
| tRD | Read Data valid to IORDY active (Min.), if IORDY initially low after tA | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| tA | IORDY Setup time ^[3] | 35 | 35 | 35 | 35 | 35 | na ^[5] | na ^[5] |

| | | | | | | | | |
|----|-----------------------------------|------|------|------|------|------|-------------------|-------------------|
| tB | IORDY Pulse Width (Max.) | 1250 | 1250 | 1250 | 1250 | 1250 | na ^[5] | na ^[5] |
| tC | IORDY assertion to release (Max.) | 5 | 5 | 5 | 5 | 5 | na ^[5] | na ^[5] |

Notes: All timings are in nanoseconds. The maximum load on IOCS16# is 1 LSTTL with a 50 pF (40 pF below 120 nsec cycle time) total load. All time intervals are recorded in nanoseconds. Although minimum time from IORDY high to HIOE# high is 0 nsec, the minimum HIOE# width is still met.

[1] Where t0 denotes the minimum total cycle time; t2 represents the minimum command active time; t2i is the minimum command recovery time or command inactive time. Actual cycle time equals the sum of actual command active time and actual command inactive time. The three timing requirements for t0, t2, and t2i are met. The minimum total cycle time requirement is greater than the sum of t2 and t2i, implying that a host implementation can extend either or both t2 or t2i to ensure that t0 is equal to or greater than the value reported in the device's identity data. A PATA Card implementation supports any legal host implementation.

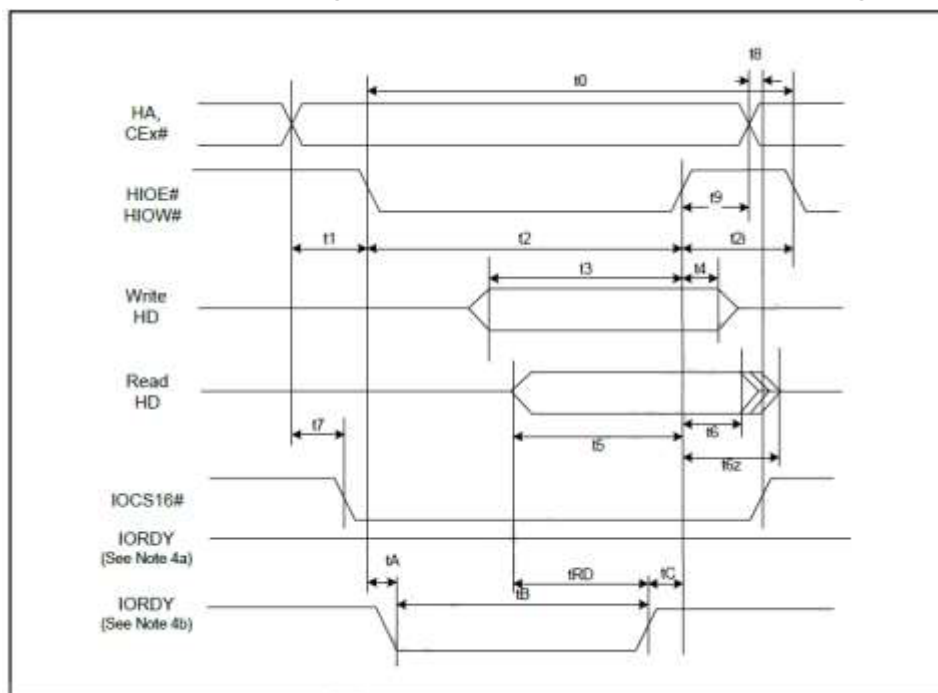
[2] This parameter specifies the time from the negation edge of the HIOE# to the time that the PATA Card (tri-state) no longer drives the data bus.

[3] The delay originates from HIOE# or HIOW# activation until the state of IORDY is first sampled. If IORDY is inactive, the host waits until IORDY is active before the PIO cycle is completed. When the PATA Storage Card is not driving IORDY, which is negated at tA after HIOE# or HIOW# activation, then t5 is met and tRD is inapplicable. When the PATA Card is driving IORDY, which is negated at the time tA after HIOE# or HIOW# activation, then tRD is met and t5 is inapplicable.

[4] Both t7 and t8 apply to modes 0, 1, and 2 only. For other modes, this signal is invalid.

[5] IORDY is not supported in this mode.

Figure 11: True IDE Mode Read/Write Timing



Notes:

1. Device address comprises CE1#, CE2#, and HA[2:0].

2. Data comprises HD[15:0] (16-bit) or HD[7:0] (8-bit).
3. IOCS16# is shown for PIO modes 0, 1, and 2. For other modes, this signal is ignored.
4. The negation of IORDY by the device is used to lengthen the PIO cycle. Whether the cycle is to be extended is determined by the host after tA from the assertion of HIOE# or HIOW#. The assertion and negation of IORDY is described in the following three cases.
 - (a) The device never negates IORDY: No wait is generated.
 - (b) Device drives IORDY low before tA: a wait is generated. The cycle is completed after IORDY is reasserted. For cycles in which a wait is generated and HIOE# is asserted, the device places read data on D15-D00 for tRD before IORDY is asserted.

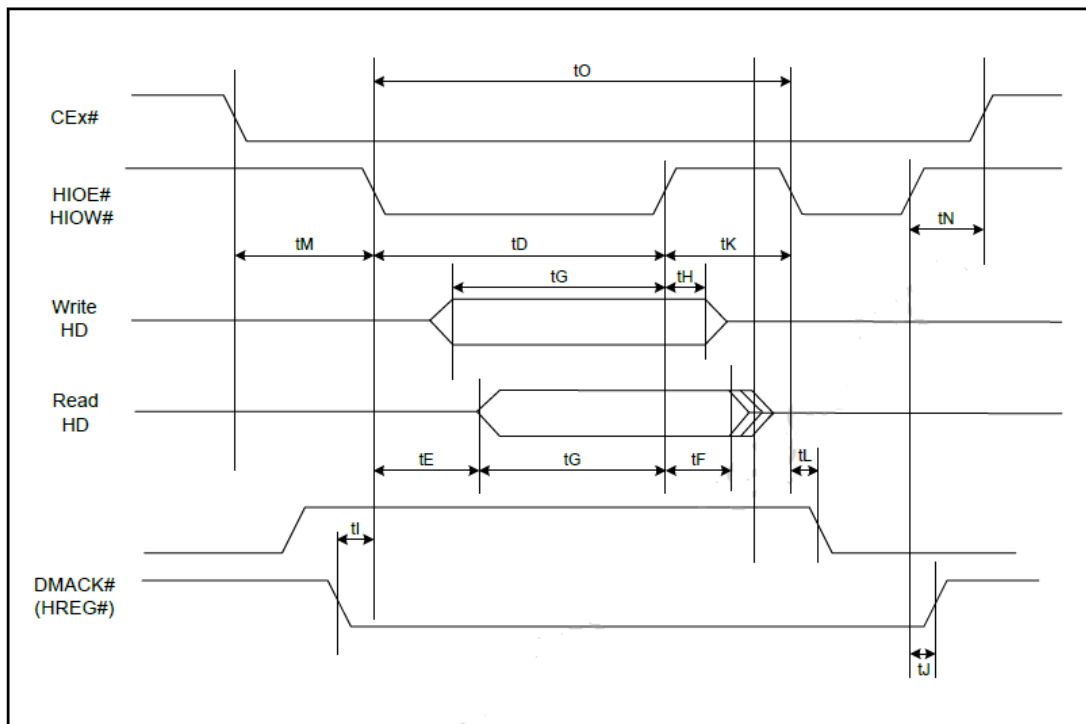
True IDE Multiword DMA Mode Read/Write Timing

| | Item | Mode 0 | Mode1 | Mode 2 | Mode3 | Mode 4 | Unit | Note |
|-----|--------------------------------------|--------|-------|--------|-------|--------|------|------|
| tO | Cycle time (Min.) | 480 | 150 | 120 | 100 | 80 | ns | [1] |
| tD | HIOE# / HIOW# asserted width (Min.) | 215 | 80 | 70 | 65 | 55 | ns | [1] |
| tE | HIOE# data access (Max.) | 150 | 60 | 50 | 50 | 45 | ns | |
| tF | HIOE# data hold (Min.) | 5 | 5 | 5 | 5 | 5 | ns | |
| tG | HIOE# / HIOW# data setup (Min.) | 100 | 30 | 20 | 15 | 10 | ns | |
| tH | HIOW# data hold (Min.) | 20 | 15 | 10 | 5 | 5 | ns | |
| tI | HREG# to HIOE# / HIOW# setup (Min.) | 0 | 0 | 0 | 0 | 0 | ns | |
| tJ | HIOE# / HIO50W# to HREG# hold (Min.) | 20 | 5 | 5 | 5 | 5 | ns | |
| tKR | HIOE# negated width (Min.) | 50 | 50 | 25 | 25 | 20 | ns | [1] |
| tKW | HIOW# 30negated width (Min.) | 215 | 50 | 25 | 25 | 20 | ns | [1] |
| tLR | HIOE# to DMARQ delay (Max.) | 120 | 40 | 35 | 35 | 35 | ns | |
| tLW | HIOW# to DMARQ delay (Max.) | 40 | 40 | 35 | 35 | 35 | ns | |
| tM | CEX# valid to HIOE# / HIOW# | 50 | 30 | 25 | 10 | 5 | ns | |
| tN | CEX# hold | 15 | 10 | 10 | 10 | 10 | ns | |

Note:

[1] Where tO is the minimum total cycle time and tD is minimum command active time, whereas tKR and tKW are minimum command recovery time or command inactive time for input and output cycles, respectively. Actual cycle time equals the sum of actual command active time and actual command inactive time. The three timing requirements of tO, i.e. tD, tKR, and tKW, must be met. The minimum total cycle time requirement exceeds the sum of tD and tKR or tKW for input and output cycles, respectively, implying that a host implementation can extend either or both tD and tKR or tKW as deemed necessary to ensure that tO equals or exceeds the value reported in the device's identity data.

Figure 12: True IDE Multiword DMA Mode Read/Write Timing



Notes:

1. If a card cannot sustain continuous, minimum cycle time DMA transfers, it may negate DMARQ during the time from the start of a DMA transfer cycle (to suspend DMA transfers in progress) and reassertion of the signal at a relatively later time to continue DMA transfer operations.
2. The host may negate this signal to suspend the DMA transfer in progress.

Ultra DMA Signal Usage in Each Interface Mode

| Signal | Type | (Non UDMA MEM MODE) | PC CARD MEM MODE UDMA | PC CARD IO MODE UDMA | TRUE IDE MODE UDMA |
|----------|--------|------------------------|--|--|--|
| DMARQ | Output | (INPACK#) | DMARQ# | DMARQ# | DMARQ |
| HREG# | Input | (REG#) | DMACK# | DMACK | DMACK# |
| HIOW# | Input | (IOWR#) | STOP _[1] | STOP _[1] | STOP _[1] |
| HIOE# | Input | (IORD#) | HDMARDY#(R) _{[1][2]} HSTROBE(W) _{[1][3][4]} | HDMARDY#(R) _{[1][2]} HSTROBE(W) _{[1][3][4]} | HDMARDY#(R) _{[1][2]} HSTROBE(W) _{[1][3][4]} |
| IORDY | Output | (WAIT#) | DDMARDY#(W) _{[1][3]} DSTROBE(R) _{[1][2][4]} | DDMARDY#(W) _{[1][3]} DSTROBE(R) _{[1][2][4]} | DDMARDY#(W) _{[1][3]} DSTROBE(R) _{[1][2][4]} |
| HD[15:0] | Bidir | (D[15:00]) | D[15:00] | D[15:00] | D[15:00] |
| HA[10:0] | Input | (A[10:00]) | A[10:00] | A[10:00] | A[02:00] _[5] |
| CSEL# | Input | (CSEL#) | CSEL# | CSEL# | CSEL# |
| HIRQ | Output | (READY) | READY | INTRQ# | INTRQ |
| CE1# | Input | (CE1#) | CE1# | CE1# | CS0# |
| CE2# | | (CE2#) | CE2# | CE2# | CS1# |

Notes:

- [1] UDMA interpretation of this signal is valid only during an Ultra DMA data burst.
- [2] UDMA interpretation of this signal is valid only during an Ultra DMA data burst during a DMA Read command.

[3] UDMA interpretation of this signal is valid only during an Ultra DMA data burst during a DMA Write command.

[4] HSTROBE and DSTROBE signals are active on both rising and falling edges.

[5] Address lines 03-10 are not used in the True IDE mode.

Ultra DMA Data Burst Timing Requirements

| Name | UDMA Mode 0 | | UDMA Mode 1 | | UDMA Mode 2 | | UDMA Mode3 | | UDMA Mode 4 | | UDMA Mode 5 | | UDMA Mode 6 | | UDMA Mode 7 | | Measure Location (see Note[2]) |
|----------------------|-------------|-----|-------------|-----|-------------|-----|------------|-----|-------------|-----|-------------|-----|-------------|-----|-------------|-----|-----------------------------------|
| | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| t _{2CYCTYP} | 240 | | 160 | | 120 | | 90 | | 60 | | 40 | | 30 | | 24 | | Sender |
| t _{CYC} | 112 | | 73 | | 54 | | 39 | | 25 | | 16.8 | | 13.0 | | 10 | | Note[3] |
| t _{2CYC} | 230 | | 153 | | 115 | | 86 | | 57 | | 38 | | 29 | | 23 | | Sender |
| t _{DS} | 15.0 | | 10.0 | | 7.0 | | 7.0 | | 5.0 | | 4.0 | | 2.6 | | 2.5 | | Recipient |
| t _{DH} | 5.0 | | 5.0 | | 5.0 | | 5.0 | | 5.0 | | 4.6 | | 3.5 | | 2.9 | | Recipient |
| t _{DVS} | 70.0 | | 48.0 | | 31.0 | | 20 | | 6.7 | | 4.8 | | 4.0 | | 2.9 | | Sender |
| t _{DVH} | 6.2 | | 6.2 | | 6.2 | | 6.2 | | 6.2 | | 4.8 | | 4.0 | | 3.2 | | Sender |
| t _{CS} | 15.0 | | 10.0 | | 7.0 | | 7.0 | | 5.0 | | 5.0 | | 5.0 | | 5.0 | | Device |
| t _{CH} | 5.0 | | 5.0 | | 5.0 | | 5.0 | | 5.0 | | 5.0 | | 5.0 | | 5.0 | | Device |
| t _{CVS} | 70.0 | | 48.0 | | 31.0 | | 20 | | 6.7 | | 10.0 | | 10.0 | | 10.0 | | Host |
| t _{CVH} | 6.2 | | 6.2 | | 6.2 | | 6.2 | | 6.2 | | 10.0 | | 10.0 | | 10.0 | | Host |
| t _{ZFS} | 0 | | 0 | | 0 | | 0 | | 0 | | 35 | | 25 | | 15.0 | | Device |
| t _{DZFS} | 70.0 | | 48.0 | | 31.0 | | 20 | | 6.7 | | 25 | | 17.5 | | 10.5 | | Sender |
| t _{FS} | | 230 | | 200 | | 170 | | 130 | | 120 | | 90 | | 80 | | 70 | Device |
| t _{LI} | 0 | 150 | 0 | 150 | 0 | 150 | 0 | 100 | 0 | 100 | 0 | 75 | 0 | 60 | | 50 | Note[4] |
| t _{MLI} | 20 | | 20 | | 20 | | 20 | | 20 | | 20 | | 20 | | 20 | | Host |
| t _{UI} | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | Host |
| t _{AZ} | | 10 | | 10 | | 10 | | 10 | | 10 | | 10 | | 10 | | 10 | Note[5] |
| t _{ZA} | 20 | | 20 | | 20 | | 20 | | 20 | | 20 | | 20 | | 20 | | Host |
| t _{AD} | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | Device |
| t _{ENV} | 20 | 70 | 20 | 70 | 20 | 70 | 20 | 55 | 20 | 55 | 20 | 50 | 20 | 50 | 20 | 50 | Host |
| t _{RFS} | | 75 | | 70 | | 60 | | 60 | | 60 | | 50 | | 50 | | 50 | Sender |
| t _{RP} | 160 | | 125 | | 100 | | 100 | | 100 | | 85 | | 85 | | 85 | | Host |
| t _{ORDYZ} | | 20 | | 20 | | 20 | | 20 | | 20 | | 20 | | 20 | | 20 | Device |
| t _{ZORDY} | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | Device |
| t _{ACK} | 20 | | 20 | | 20 | | 20 | | 20 | | 20 | | 20 | | 20 | | Host |
| t _{SS} | 50 | | 50 | | 50 | | 50 | | 50 | | 50 | | 50 | | 50 | | Sender |

Notes: All timings in ns:

[1] All timing measurement switching points (low to high and high to low) are taken at 1.5V.

[2] All signal transitions for a timing parameter are determined at the connector specified in the measurement location column. For instance, for the case of t_{RFS} , both STROBE and DMARDY# transitions are determined by the sender's connector.

[3] Parameter t_{CYC} is determined at the connector of the recipient farthest from the sender.

[4] Parameter t_{LI} is determined at the connector of a sender or recipient responding to an incoming transition from the recipient or sender, respectively. Both incoming signal and outgoing response are determined at the same connector.

[5] Parameter t_{AZ} is determined at the connector of a sender or recipient driving the bus, and must release the bus to allow for a bus turnaround.

[6] Table 25 lists the AC Timing requirements: Ultra DMA AC Signal Requirements.

Ultra DMA Data Burst Timing Descriptions

| Name | Comment | Note |
|---------------|---|--------|
| $t_{2CYCTYP}$ | Typical sustained average two cycle time | |
| t_{CYC} | Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge) | |
| t_{2CYC} | Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE) | [2][5] |
| t_{DS} | Data setup time at recipient (from data valid until STROBE edge) | [2][5] |
| t_{DH} | Data hold time at recipient (from STROBE edge until data may become invalid) | [3] |
| t_{DVS} | Data valid setup time at sender (from data valid until STROBE edge) | [3] |
| t_{DVH} | Data valid hold time at sender (from STROBE edge until data may become invalid) | [2] |
| t_{CS} | CRC word setup time at device | [2] |
| t_{CH} | CRC word hold time at device | [3] |
| t_{CVS} | CRC word valid setup time at host (from CRC valid until DMACK(##) negation) | [3] |
| t_{CVH} | CRC word valid hold time at sender (from DMACK(##) negation until CRC may become invalid) | |
| t_{ZFS} | Time from STROBE output released-to-driving until the first transition of critical timing. | |
| t_{DZFS} | Time from data output released-to-driving until the first transition of critical timing. | |
| t_{FS} | First STROBE time (for device to first negate DSTROBE from STOP during a data in burst) | [1] |
| t_{LI} | Limited interlock time | [1] |
| t_{MLI} | Interlock time with minimum | [1] |
| t_{UI} | Unlimited interlock time | |
| t_{AZ} | Maximum time allowed for output drivers to release (from asserted or negated) | |
| t_{ZAH} | Minimum delay time required for output | |
| t_{ZAD} | drivers to assert or negate (from released) | |

| | | |
|---------|---|--------|
| tENV | Envelope time (from DMACK(#) to STOP and HDMARDY# during data in burst initiation and from DMACK(#) to STOP during data out burst initiation) | |
| tRFS | Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of DMARDY#) | |
| tRP | Ready-to-pause time (that recipient shall wait to pause after negating DMARDY#) | |
| tIORDYZ | Maximum time before releasing IORDY | [6] |
| tZIORDY | Minimum time before driving IORDY | [4][6] |
| tACK | Setup and hold times for DMACK(#) (before assertion or negation) | |
| tSS | Time from STROBE edge to negation of DMARQ(#) or assertion of STOP (when sender terminates a burst) | |

Notes:

[1] Parameters t_{UI}, t_{MLI} (in Figure 16: Ultra DMA Data-In Burst Device Termination Timing and Figure 17: Ultra DMA Data-In Burst Host Termination Timing), and t_{LI} represent sender-to-recipient or recipient-to-sender interlocks, i.e., one agent (sender or recipient) is waiting for the other agent to respond with a signal before proceeding. Parameter t_{UI} denotes an unlimited interlock that has no maximum time value; t_{MLI} represents a limited time-out that has a defined minimum; t_{LI} is a limited time-out that has a defined maximum.

[2] The 80-conductor cabling is required to meet setup (t_{DS}, t_{CS}) and hold (t_{DH}, t_{CH}) times in modes exceeding 2.

[3] Timing for t_{DVS}, t_{DVH}, t_{CVS}, and t_{CVH} must be met for lumped capacitive loads of 15 and 40 pF at the connector where the data and STROBE signals have the same capacitive load value. Due to cable reflections, these timing measurements are invalid in a system functioning normally.

[4] For all timing modes, parameter t_{ZIORDY} may be greater than t_{ENV} since the host has a pull-up on IORDY giving it a known state when released.

[5] Parameters t_{DS} and t_{DH} for mode 5 are defined for a recipient at the end of a cable only in a configuration that has a single device located at the cable end. This configuration can result in t_{DS} and t_{DH} for mode 5 at the middle connector having minimum values of 3.0 and 3.9 ns, respectively.

[6] The parameters are applied to True IDE mode operation only.

Ultra DMA Sender and Recipient IC Timing Requirements

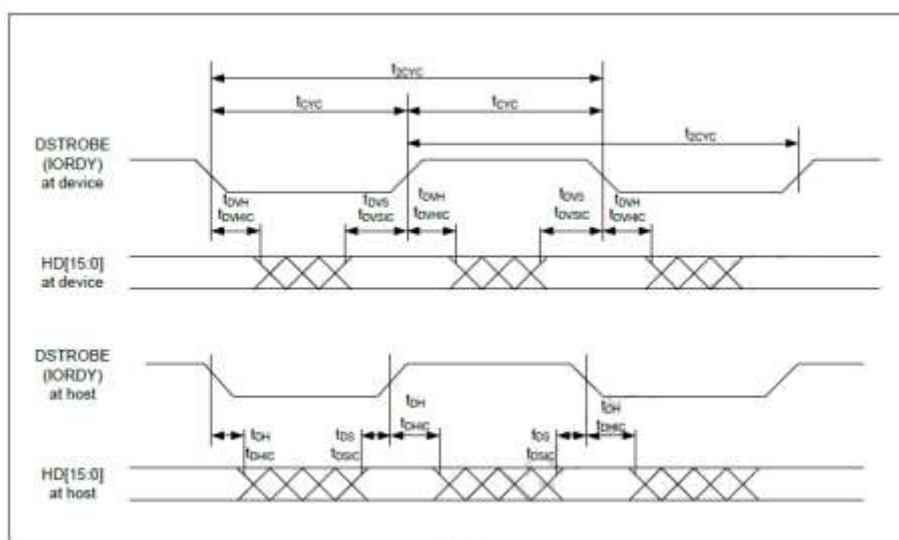
| Name | UDMA Mode 0 | | UDMA Mode 1 | | UDMA Mode 2 | | UDMA Mode3 | | UDMA Mode 4 | | UDMA Mode 5 | | UDMA Mode 6 | | UDMA Mode 7 | | Unit |
|--------------------|---|-----|-------------|-----|-------------|-----|------------|-----|-------------|-----|-------------|-----|-------------|-----|-------------|-----|------|
| | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| t _{DSIC} | 14.7 | | 9.7 | | 6.8 | | 6.8 | | 4.8 | | 2.3 | | 2.3 | | 2.3 | | ns |
| t _{DHIC} | 4.8 | | 4.8 | | 4.8 | | 4.8 | | 4.8 | | 2.8 | | 2.8 | | 2.8 | | ns |
| t _{DVSIC} | 72.9 | | 50.9 | | 33.9 | | 22.6 | | 9.5 | | 6.0 | | 5.2 | | 3.7 | | ns |
| t _{DVHIC} | 9.0 | | 9.0 | | 9.0 | | 9.0 | | 9.5 | | 6.0 | | 5.2 | | 3.7 | | ns |
| t _{DSIC} | Recipient IC data setup time (from data valid until STROBE edge) (see Note[2]) | | | | | | | | | | | | | | | | ns |
| t _{DHIC} | Recipient IC data hold time (from STROBE edge until data may become invalid) (see Note[2]) | | | | | | | | | | | | | | | | ns |
| t _{DVSIC} | Sender IC data valid setup time (from data valid until STROBE edge) (see Note[3]) | | | | | | | | | | | | | | | | ns |
| t _{DVHIC} | Sender IC data valid hold time (from STROBE edge until data may become invalid) (see Note[3]) | | | | | | | | | | | | | | | | ns |

Notes:

[1] All timing switching point measurements (low to high and high to low) are taken at 1.5V.

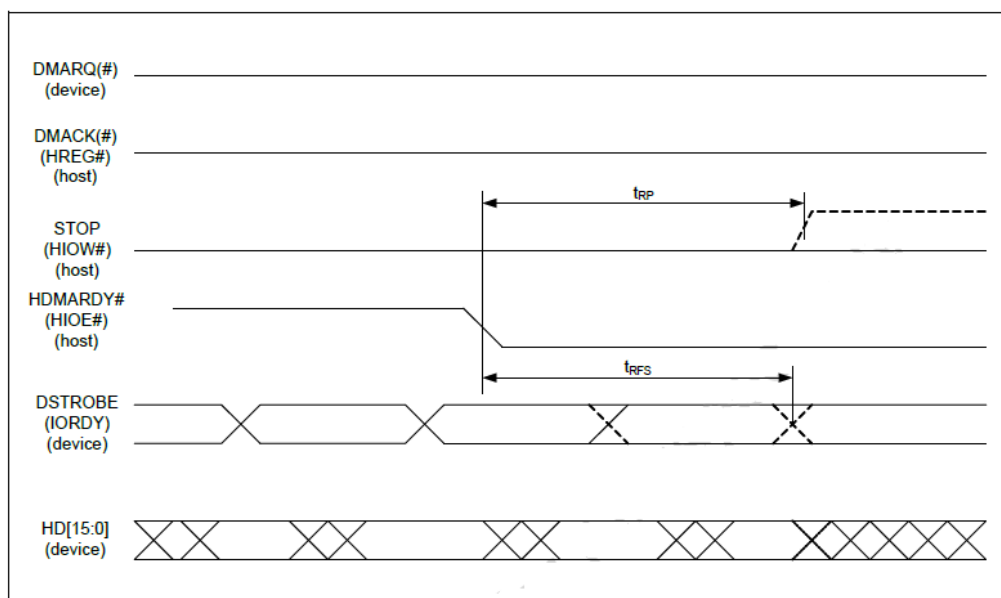
2. The definitions for the IORDY:DDMARDY#:DSTROBE, HIOE#: HDMARDY#: HSTROBE and HIOW#: STOP signal lines are not in effect until DMARQ(#) and DMACK(#) are asserted. Notably, HA[2:0], CS0# and CS1# are True IDE mode signal definitions, and HA[10:0], CE1# and CE2# are PC Card mode signals. The Bus polarity of DMACK(#) and DMARQ(#) is based on the active interface mode.

Figure 14: Sustained Ultra DMA Data-In Burst Timing



Note: HD[15:0] and IORDY signals are shown at both the host and device to emphasize that neither cable settling time nor cable propagation delay allow data signals to be considered stable at the host until after they are driven by the device.

Figure 15: Ultra DMA Data-In Burst Host Pause Timing

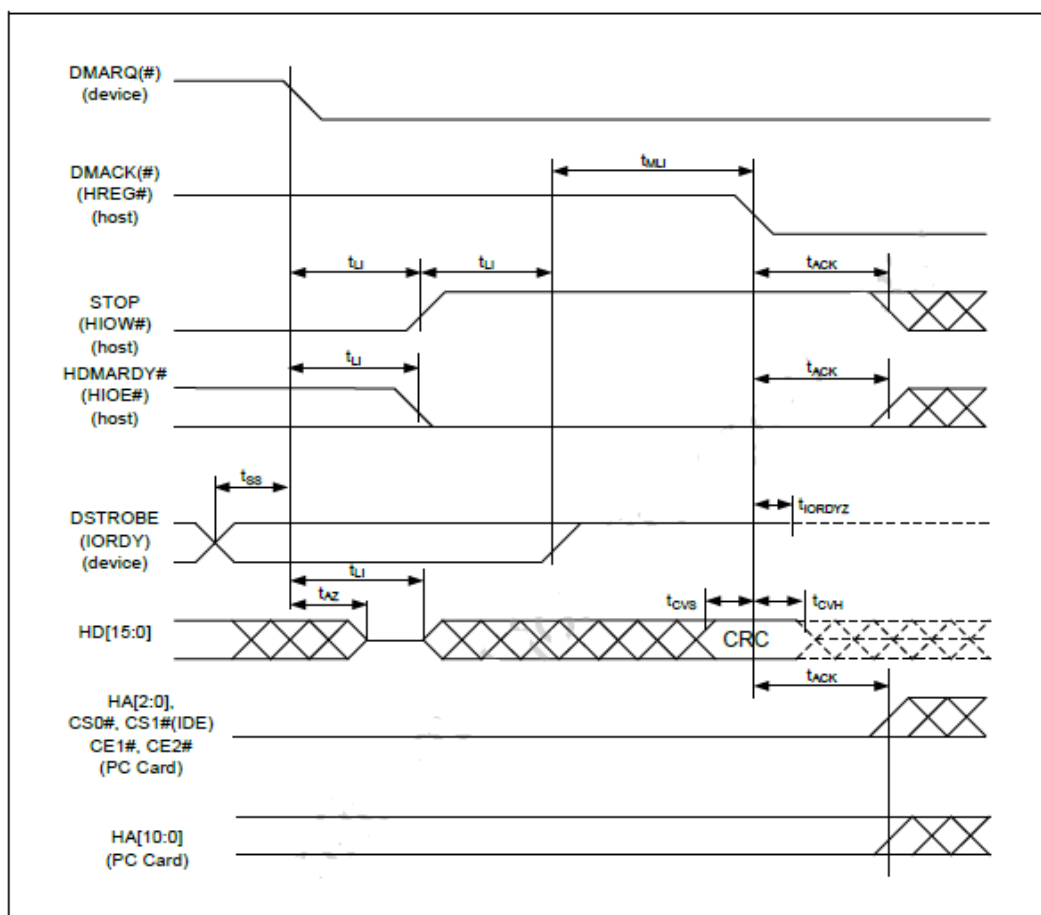


Notes:

1. All waveforms in this diagram are shown with the asserted state high. Negative true signals are inverted on the bus relative to the diagram.
2. The host can implement STOP to request termination of the Ultra DMA data burst at a time no sooner than when tRP after HDMARDY# is negated.

3. After negating HDMARDY#, the host may receive zero, 1, 2, or 3 additional data words from the device.
4. Bus polarities of the DMARQ(#) and DMACK(#) signals are dependent on the active interface mode.

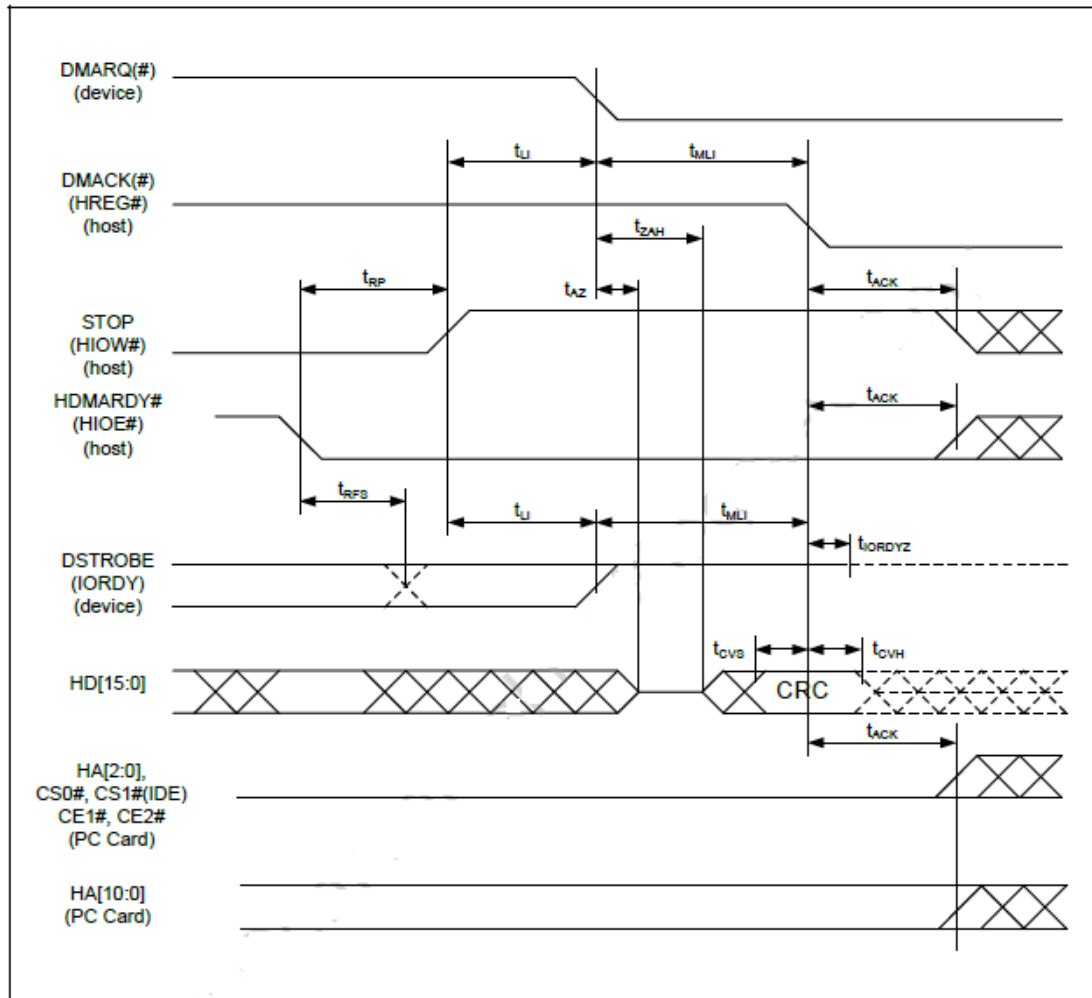
Figure 16: Ultra DMA Data-In Burst Device Termination Timing



Notes:

1. All waveforms in this diagram are shown with the asserted state high. Negative true signals are inverted on the bus relative to the diagram.
2. Definitions for STOP, HDMARDY#, and DSTROBE signal lines are no longer in effect once DMARQ(#) and DMACK(#) are negated. The HA[2:0], CS0# and CS1# are True IDE mode signal definitions. HA[10:0], CE1# and CE2# are PC Card mode signals. Bus polarities of DMARQ(#) and DMACK(#) are dependent on the active interface mode.

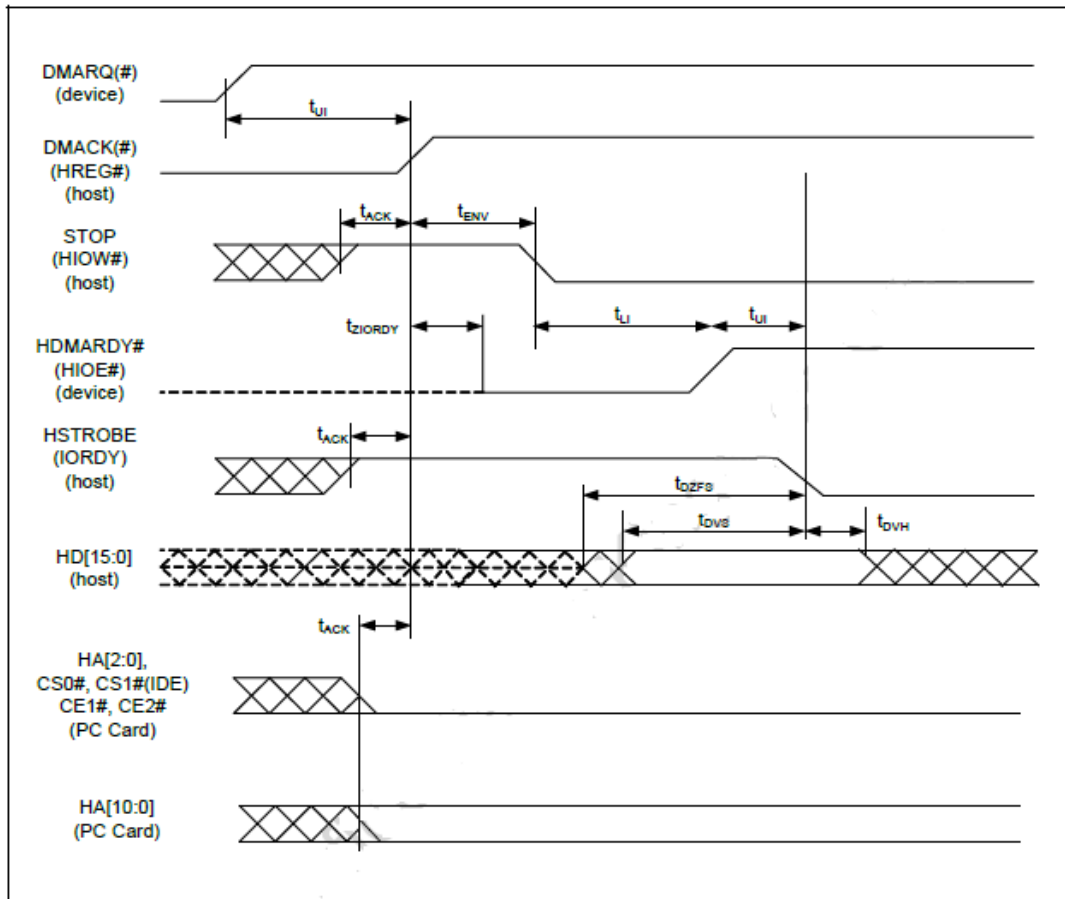
Figure 17: Ultra DMA Data-In Burst Host Termination Timing



Notes:

1. All waveforms in this diagram are shown with the asserted state high. Negative true signals are inverted on the bus relative to the diagram.
2. Definitions for STOP, HDMARDY#, and DSTROBE signal lines are no longer in effect once DMARQ(##) and DMACK(##) are negated. The HA[2:0], CS0# and CS1# are True IDE mode signal definitions. The HA[10:0], CE1# and CE2# are PC Card mode signal definitions. Bus polarities of DMARQ(##) and DMACK(##) are dependent on the active interface mode.

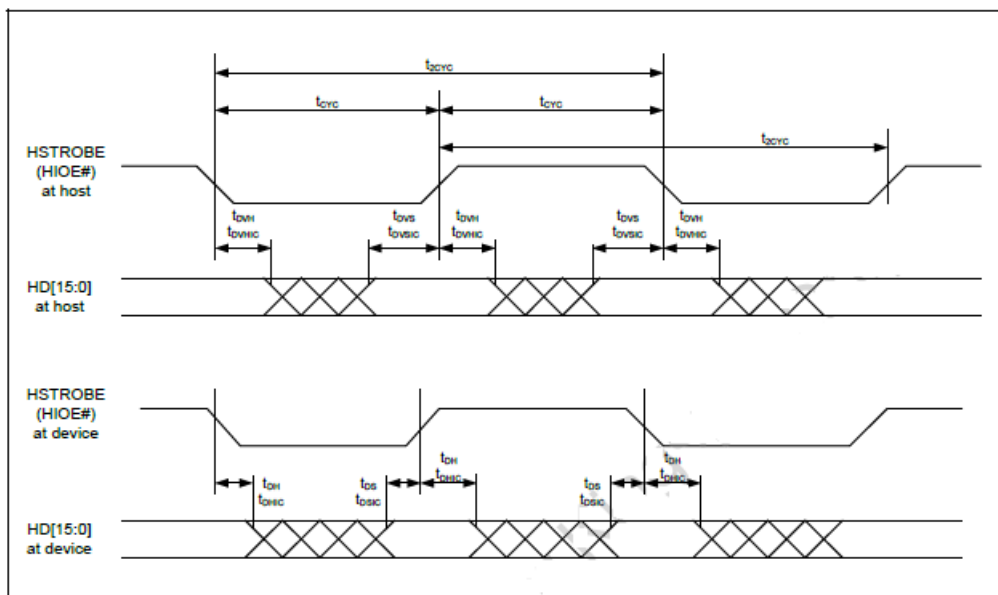
Figure 18: Ultra DMA Data-Out Burst Initiation Timing



Notes:

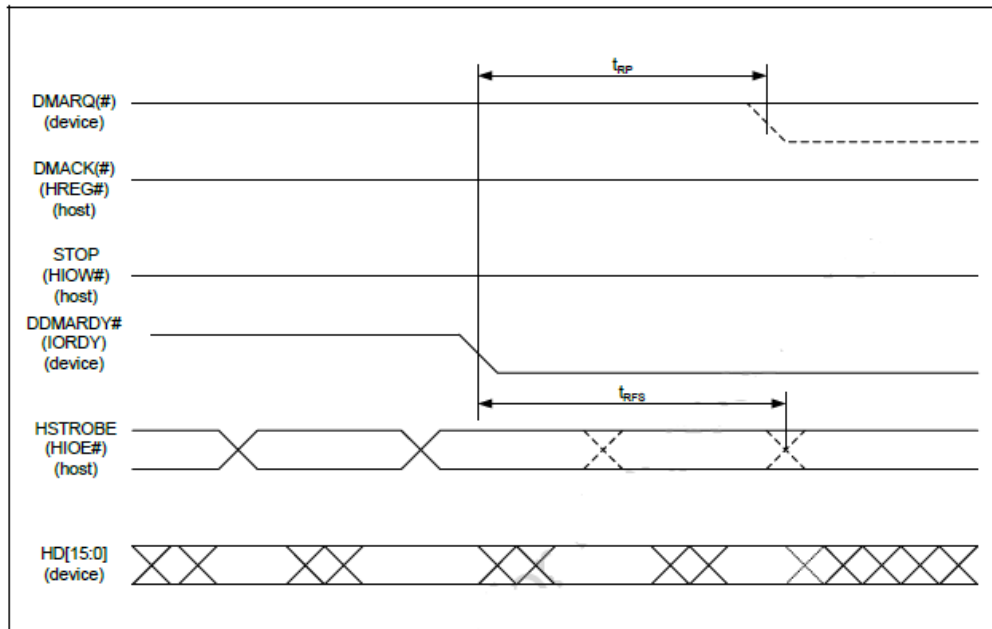
1. All waveforms in this diagram are shown with the asserted state high.
2. Negative true signals are inverted on the bus relative to the diagram.
- 3 Definitions for STOP, DDMARDY#, and HSTROBE signal lines are not in effect until the DMARQ(#) and DMACK(#) are asserted. The HA[2:0], CS0# and CS1# are True IDE mode signal definitions. 4. The HA[10:0], CE1# and CE2# are PC Card mode signal definitions. Bus polarities of DMARQ(#) and DMACK(#) are dependent on the active interface mode.

Figure 19: Sustained Ultra DMA Data-Out Burst Timing



Note: Data (HD[15:0]) and HSTROBE signals are shown at both the device and host to emphasize that neither cable settling time nor cable propagation delay allow for data signals to be considered stable at the device until after they are driven by a host.

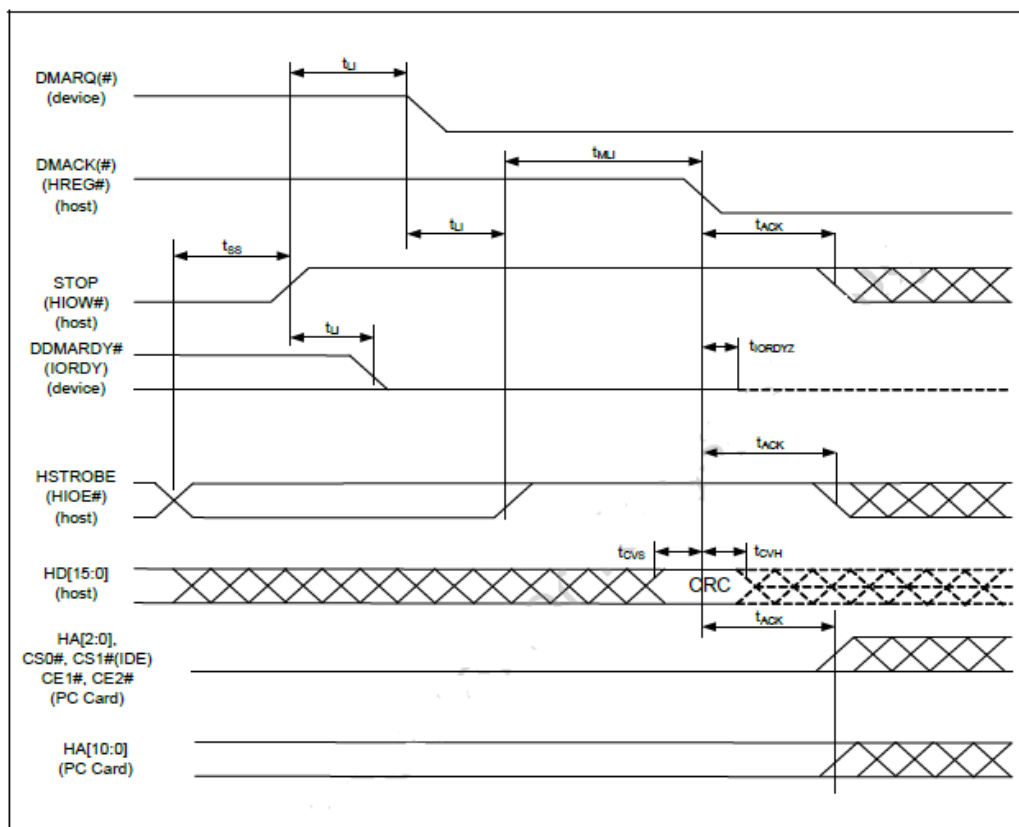
Figure 20: Ultra DMA Data-Out Burst Device Pause Timing



Notes:

1. All waveforms in this diagram are shown with the asserted state high. Negative true signals are inverted on the bus relative to the diagram. The device can negate DMARQ(##) when requesting termination of the Ultra DMA data burst no sooner than t_{RP} after DDMARDY## is negated.
2. After negating DDMARDY##, the device may receive zero, 1, 2, or 3 additional data words from the host. The bus polarities of DMARQ(##) and DMACK(##) are dependent on the active interface mode.

Figure 21: Ultra DMA Data-Out Burst Device Termination Timing



Notes:

1. All waveforms in this diagram are shown with the asserted state high. Negative true signals are inverted on the bus relative to the diagram.
2. Definitions for the STOP, DDMARDY#, and HSTROBE signal lines are no longer in effect once DMARQ(#) and DMACK(#) are negated. The HA[2:0], CS0# and CS1# are True IDE mode signal definitions. The HA[10:0], CE1# and CE2# are PC Card mode signal definitions. Bus polarities of DMARQ(#) and DMACK(#) are dependent on the active interface mode.

4.4. Flash Interface AC Characteristics

Flash Interface AC Timing Parameters for Command / Address

| Symbol | Parameter | Timing | | Unit |
|--------|-------------------|--------------------------|-------------------------|------|
| | | Disable Flash CMD Extend | Enable Flash CMD Extend | |
| tCLS | CLE Setup Time | 2 | 4 | tCK |
| tCLH | CLE Hold Time | 1 | 2 | tCK |
| tALS | ALE Setup Time | 2 | 4 | tCK |
| tALH | ALE Hold Time | 1 | 2 | tCK |
| tWP | WE Pulse Width | 1 | 2 | tCK |
| tDS | Data Setup Time | 1 | 3 | tCK |
| tDH | Data Hold Time | 1 | 1 | tCK |
| tWC | Write Cycle Time | 2 | 4 | tCK |
| tWH | WE High Hold Time | 1 | 2 | tCK |
| tWP | WE Low Hold Time | 1 | 2 | tCK |

| Symbol | Parameter | Timing | Unit |
|--------|-------------------|--------|------|
| tWP | WE Pulse Width | 0.5 | tCK |
| tDS | Data Setup Time | 0.75 | tCK |
| tDH | Data Hold Time | 0.25 | tCK |
| tWC | Write Cycle Time | 1 | tCK |
| tWH | WE High Hold Time | 0.5 | tCK |
| tWP | WE Low Hold Time | 0.5 | tCK |
| tRC | Read Cycle Time | 1 | tCK |
| tRP | RE Pulse Width | 0.5 | tCK |
| tREH | RE High Hold Time | 0.5 | tCK |

Figure 23: Command Latch Cycle

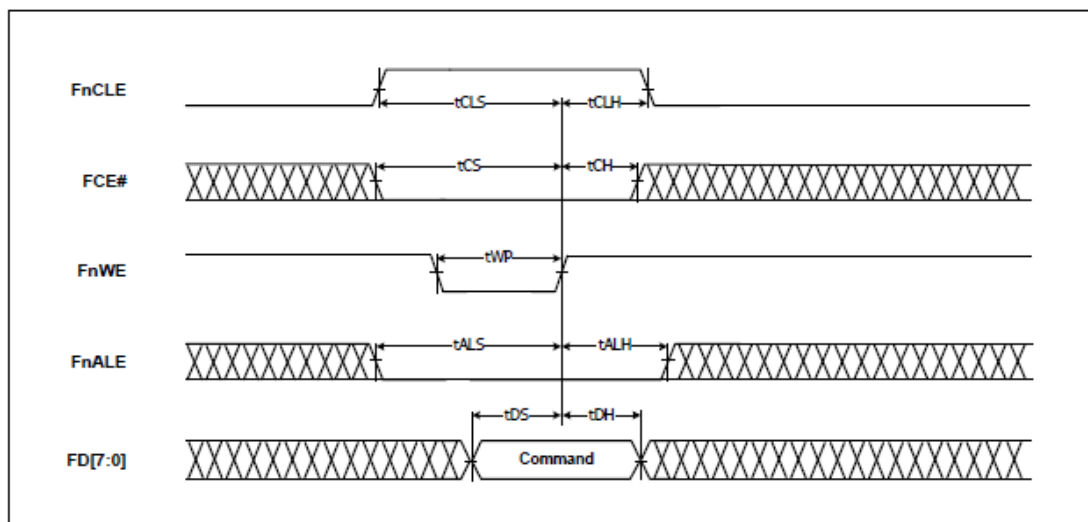


Figure 24: Address Latch Cycle

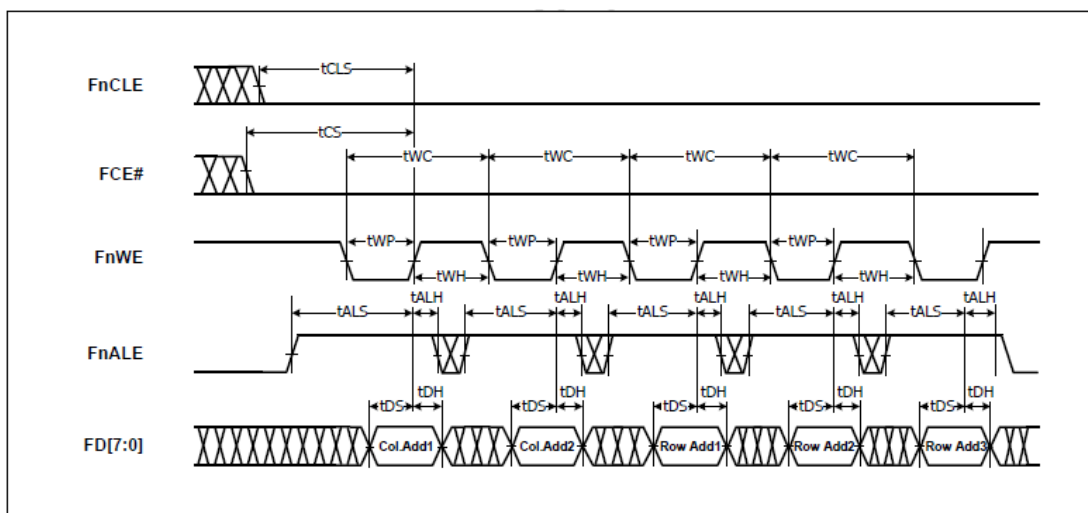
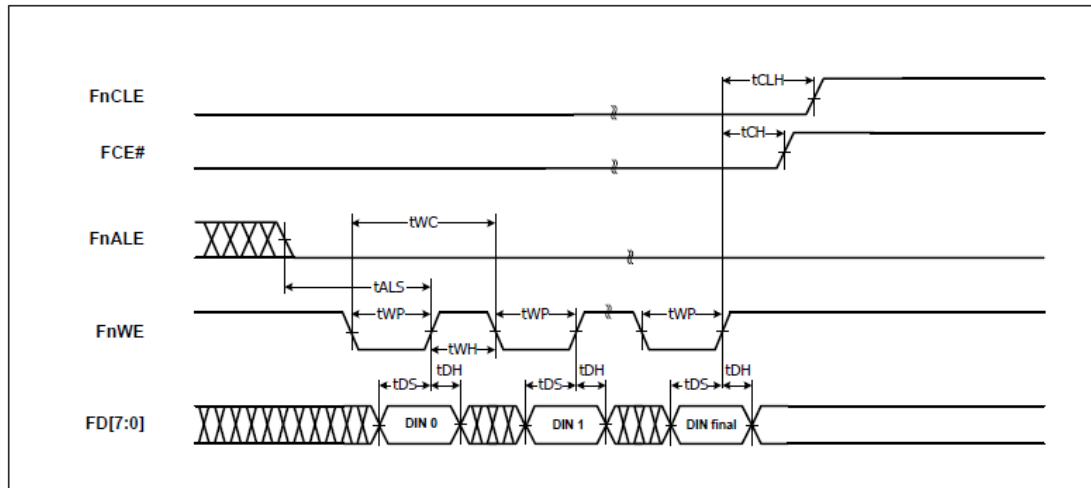


Figure 25: Input Data Latch Cycle



4.5. Power Consumption (typical)

Operation (Read/Write): 110mA/90mA (UDMA6)

Idle: 5mA

Sleep (Partial/Slumber): 5mA/7mA (typ. /max.)



5. Reliability Specification

5.1. Wear-leveling

| Item | Features |
|-----------------------|-------------------------------|
| Operating Temperature | -40°C to +85°C |
| Storage Temperature | -50°C to +95°C |
| Humidity | 5-95% |
| Vibration | 20G(7-2000HZ) |
| Shock | 2,000G(@0.3ms half sine wave) |

Renice X5 2.5" IDE SSD support both static and dynamic wear-leveling. These two algorithms guarantee all type of flash memory at same level of erase cycles to improve lifetime limitation of NAND based storage

5.2. Endurance

Write endurance: >8 years @ 100GB write/ day (8GB SLC)

Read endurance: unlimited

5.3. H/W ECC for NAND Flash

Hardware BCH ECC capable of correcting errors up to 72-bit/1KB

5.4. MTBF

MTBF (Mean Time between Failures) of Renice X5 2.5" PATA IDE SSD: 3,000,000 hours Data retention at 25°C of Renice SSD: >10 years

5.5. Over voltage and inrush current protection

The over voltage and inrush current protection mechanism of Renice X5 2.5" PATA IDE SSD is to deploy a protect circuitry on Device Power In. Once the current or voltage is exceeded, it will be pulled down to the normal value in very short time to protect the drive.



6. Software Interface

Renice X5 2.5" PATA IDE SSD supports the SMART (Self-Monitoring, Analysis and Reporting Technology) command set and defines some vendor-specific data to report spare/bad block numbers. Detailed SMART commands and data structure will be updated in a later Data Sheet version.

6.1. SMART Feature Set

Renice X5 2.5" PATA IDE SSD supports the SMART (Self-Monitoring, Analysis and Reporting Technology) command set and defines some vendor-specific data to report spare/bad block numbers in each memory management unit.

SMART Feature Register Values

| Value | Command | Value | Command |
|-------|----------------------------|-------|--------------------------|
| D0h | Read Data | D5h | Reserved |
| D1h | Read Attribute Threshold | D6h | Reserve |
| D2h | Enable/Disable Autosave | D8h | Enable SMART Operations |
| D3h | Save Attribute Values | D9h | Disable SMART Operations |
| D4h | Execute OFF-LINE Immediate | DAh | Return Status |

6.2. SMART Data Structure

The following 512 bytes make up the device SMART data structure. Users can obtain the data using the "Read Data" command (D0h).

SMART Data Structure

| Byte | F / V | Description |
|---------|-------|---|
| 0 - 1 | X | Revision code |
| 2 - 361 | X | Vendor specific (see 4.2.2) |
| 362 | V | Off-line data collection status |
| 263 | X | Self-test execution status byte |
| 364-365 | V | Total time in seconds to complete off-line data collection activity |
| 366 | X | Vendor specific |
| 367 | F | Off-line data collection capability |
| 368-369 | F | SMART capability |

| | | |
|---------|---|--|
| 370 | F | Error logging capability • 7-1 Reserved • 0 1 = Device error logging supported |
| 371 | X | Vendor specific |
| 372 | F | Short self-test routine recommended polling time (in minutes) |
| 373 | F | Extended self-test routine recommended polling time (in minutes) |
| 374 | F | Conveyance self-test routine recommended polling time (in minutes) |
| 375-385 | R | Reserved |
| 386-395 | F | Firmware Version/Date Code |
| 396-399 | R | Reserved |
| 400-406 | F | 'Chips information' |
| 407-511 | R | Reserved |

Notes:

1. F = content (byte) is fixed and does not change.
2. V = content (byte) is variable and may change depending on the state of the device or the commands executed by the device.
3. X = content (byte) is vendor specific and may be fixed or variable.
4. R = content (byte) is reserved and shall be zero.

6.3. SMART Attributes

The following table defines the vendor specific data in byte 2 to 361 of the 512-byte SMART data.

SMART Data Vendor-Specific Attributes

| Attribute ID (hex) | Raw Attribute Value | | | | | | Attribute Name |
|--------------------|---------------------|-----|----|-----|----|----|---------------------------------|
| 01 | LSB | MSB | 00 | 00 | 00 | 00 | Read error rate |
| 05 | LSB | MSB | 00 | 00 | 00 | 00 | Reallocated sector count |
| 0C | LSB | MSB | 00 | 00 | 00 | 00 | Power cycle count |
| A1 | LSB | MSB | 00 | 00 | 00 | 00 | Number of valid spare block |
| A2 | LSB | MSB | 00 | 00 | 00 | 00 | Number of child pair |
| A3 | LSB | MSB | 00 | 00 | 00 | 00 | Number of initial invalid block |
| A4 | LSB | | | MSB | 00 | 00 | Number of total erase count |
| A5 | LSB | | | MSB | 00 | 00 | Maximum erase count |
| A6 | LSB | | | MSB | 00 | 00 | Minimum erase count |
| A7 | LSB | | | MSB | 00 | 00 | Average erase count |
| C0 | LSB | | | MSB | 00 | 00 | Power-off retract count |

| | | | | | | | |
|----|-----|-----|----|----|----|-----|---|
| C7 | LSB | MSB | 00 | 00 | 00 | 00 | UDMA CRC error count |
| F1 | LSB | | | | | MSB | Total LBAs written (each write unit = 32MB) |
| F2 | LSB | | | | | MSB | Total LBAs read (each read unit = 32MB) |

7. PATA Host ID table

The Identify Device command enables the host to receive parameter information from the Renice X5 2.5" PATA IDE SSD. This command has the same protocol as the Read Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in the following Table.

ID Table Information

| Word Address | Default Value | Total Bytes | Data Field Type Information |
|--------------|---------------|-------------|---|
| 0 | 044Ah | 2 | General configuration |
| 1 | XXXXh | 2 | Default number of cylinders |
| 2 | 0000h | 2 | Reserved |
| 3 | 00XXh | 2 | Default number of heads |
| 4 | 0000h | 2 | Obsolete |
| 5 | 0240h | 2 | Obsolete |
| 6 | XXXXh | 2 | Default number of sectors per track |
| 7-8 | XXXXh | 4 | Number of sectors per card (Word 7 = MSW, Word 8 = LSW) |
| 9 | 0000h | 2 | Obsolete |
| 10-19 | XXXXh | 20 | Serial number in ASCII (Right justified) |
| 20 | 0002h | 2 | Obsolete |
| 21 | 0002h | 2 | Obsolete |
| 22 | 0004h | 2 | Obsolete |
| 23-26 | XXXXh | 8 | Firmware revision in ASCII. Big Endian Byte Order in Word |
| 27-46 | XXXXh | 40 | Model number in ASCII (Left justified). Big Endian Byte Order in Word |
| 47 | 8001h | 2 | Maximum number of sectors on Read/Write Multiple command |
| 48 | 0000h | 2 | Reserved |
| 49 | 0F00h | 2 | Capabilities |
| 50 | 0000h | 2 | Capabilities |
| 51 | 0200h | 2 | PIO data transfer cycle timing mode |
| 52 | 0000h | 2 | Obsolete |
| 53 | 0007h | 2 | Field validity |
| 54 | XXXXh | 2 | Current numbers of cylinders |
| 55 | XXXXh | 2 | Current numbers of heads |
| 56 | XXXXh | 2 | Current sectors per track |
| 57-58 | XXXXh | 4 | Current capacity in sectors (LBAs) (Word 57 = LSW, Word 58 = MSW) |
| 59 | 0000h | 2 | Multiple sector setting |
| 60-61 | XXXXh | 4 | Total number of sectors addressable in LBA Mode |
| 62 | 0000h | 2 | Reserved |
| 63 | 0007h | 2 | Multiword DMA transfer. In PCMCIA mode this value shall be 0h. |
| 64 | 0003h | 2 | Advanced PIO modes supported |

| | | | |
|---------|-------------------------|-----|--|
| 65 | 0078h | 2 | Minimum Multiword DMA transfer cycle time per word. In PCMCIA mode this value shall be 0h. |
| 66 | 0078h | 2 | Recommended Multiword DMA transfer cycle time. In PCMCIA mode this value shall be 0h. |
| 67 | 0078h | 2 | Minimum PIO transfer cycle time without flow control |
| 68 | 0078h | 2 | Minimum PIO transfer cycle time with IORDY flow control |
| 69-79 | 0000h | 22 | Reserved |
| 80 | 0100h | 4 | Major version number (ATAPI-8) |
| 81 | 0000h | | Minor version number |
| 82 | 7028h | 2 | Command sets supported 0 |
| 83 | 5000h | 2 | Command sets supported 1 |
| 84 | 4000h | 2 | Command sets supported 2 |
| 85 | 0000h | 2 | Command sets enabled 0 |
| 86 | 0000h | 2 | Command sets enabled 1 |
| 87 | 0000h | 2 | Command sets enabled 2 |
| 88 | 007Fh | 2 | Ultra DMA mode supported and selected |
| 89 | 0000h | 2 | Time required for Security erase unit completion |
| 90 | 0000h | 2 | Time required for Enhanced security erase unit completion |
| 91 | 0000h | 2 | Current Advanced power management value |
| 92 | 0000h | 2 | Master Password revision code |
| 93 | 604Fh 6F00h 603Fh | 2 | . Hardware reset result (Master) . Hardware reset result (Slave) . Hardware reset result (Master w/ slave present) |
| 94-127 | 0000h | 68 | Reserved |
| 128 | 0000h | 2 | Security status |
| 129-159 | 0000h | 62 | Vendor unique bytes |
| 160 | 0000h | 2 | Power requirement description |
| 161 | 0000h | 2 | Reserved |
| 162 | 0000h | 2 | Key management schemes supported |
| 163 | 0000h | 2 | Advanced True IDE Timing Mode Capability and Setting |
| 164 | 0000h | 2 | Advanced PCMCIA I/O and Memory Timing Mode Capability and Setting |
| 165-175 | 0000h | 22 | Reserved |
| 176-255 | 0000h | 160 | Reserved |

8. Ordering Information

Valid Combinations

| Capacities/Flash type | Industrial Temp |
|-----------------------|-----------------|
| 16GB/MLC | RIM016-PX52 |
| 32GB/MLC | RIM032- PX52 |
| 64GB/MLC | RIM064- PX52 |
| 128GB/MLC | RIM128- PX52 |
| 8GB/SLC | RIS008- PX52 |
| 16GB/SLC | RIS016- PX52 |
| 32GB/SLC | RIS032- PX52 |
| 64GB/SLC | RIS064- PX52 |
| 128GB/SLC | RIS128- PX52 |



9. Product Part Number Naming Rule

R I S 064 - P X5 2

Renice

2.5" Form Factor

Temp Range

X5 Series

I: Industrial

Flash Type:

M: MLC

PATA IDE

Interface S: SLC

Capacities:

008: 8GB

016: 16GB

032: 32GB

064: 64GB

128: 128GB