## Appendix B

# **ASCII Character Codes**

Hex code	ASCII character	Hex Code	ASCII character	Hex code	ASCII character	Hex code	ASCII character
00	NUL	20	SP	40	@	60	
01	SOH	21	!	41	A	61	a
02	STX	22	"	42	В	62	b
03	ETX	23	#	43	C	63	C
04	EOT	24	\$	44	D	64	d
05	ENQ	25	%	45	E	65	e
06	ACK	26	&	46	F	66	f
07	BEL	27	,	47	G	67	g
08	BS	28	(	48	H	68	h
09	HT	29	)	49	I	69	i
0A	LF	2A	*	4A	J	6A	j
0B	VT	2B	+	4B	K	6B	k
0C	FF	2C	,	4C	L	6C	1
0D	CR	2D	_	4D	M	6D	m
0E	SO	2E		4E	N	6Ę	n
0F	SI	2F	1	4F	0	6F	O
10	DLE	30	0	50	P	70	P
11	DC1	31	1	51	Q	71	q
12	DC2	32	2	52	R	72	r
13	DC3	33	3	53	S	73	S
14	DC4	34	4	54	T	74	t
	NAK	35	5	55	U	75	u
15	SYN	36	6	56	V	76	· V
16	ETB	37	7	57	W	77	W
17	CAN	38	8	58	X	78	x
18	EM	39	9	59	Y	79	У
19	SUB	3A .		5A	Z	7A	Z
1A	ESC	3B		5B	[	7B	1
1B		3C	. <	5C	1	7C	
1C	FS	3D	=	5D		7D	
1D	GS RS	3E	>	5E	^	7E	DEL
1E	US	3F	?	. 5F	-	7F	DEL.
1F	03	0.					

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	Farmet	Opcode	Effect	Notes
Mnemonic	Format		$A \leftarrow (A) + (mm+2)$	
ADD m	3/4	18	$F \leftarrow (F) + (mm+5)$	XF
ADDF m	3/4	58	$r2 \leftarrow (r2) + (r1)$	X
ADDR r1,r2	2	90	$A \leftarrow (A) \& (mm+2)$	
AND m	3/4	40		X
CLEAR r1	2	B4	$r1 \leftarrow 0$	C
COMP m	3/4	28	(A): (mm+2)	XFC
COMPF m	3/4	88	(F): (mm+5)	ХС
COMPR r1,r2	2	A0	(r1): (r2)	7 (
DIV m	3/4	24	$A \leftarrow (A) / (mm+2)$	VE
DIVF m	3/4	64	$F \leftarrow (F) / (mm+5)$	
DIVR r1,r2	2	9C	$r2 \leftarrow (r2) / (r1)$	X
FIX	1	C4	$A \leftarrow (F)$ [convert to integer]	XF
FLOAT	1 000	CO	$F \leftarrow (A)$ [convert to floating]	XF
HIO	1 1 111) -	F4	Halt I/O channel number (A)	PX
J m	3/4	3C	(A) specifies that the $m \to 2q$	
JEQ m	3/4	30	PC ← m if CC set to = bba ls a	
JGT m	3/4	34	PC ← m if CC set to >	
JLT m	3/4	38	$PC \leftarrow m \text{ if } CC \text{ set to } \leq 200 \text{ m}$	
JSUB m	3/4	48	$L \leftarrow (PC); PC \leftarrow m$	
LDA m	3/4	00	$A \leftarrow (mm+2)$	
LDB m	3/4	68	$B \leftarrow (mm+2)$	X
LDCH m	3/4	50	A [rightmost byte] $\leftarrow$ (m)	
LDF m	3/4	70		XF
LDL m	3/4	08	L ← (mm+2)	
LDS m	3/4	6C	$S \leftarrow (mm+2)$	X
LDT m	3/4	74	$T \leftarrow (mm+2)$	X
LDX m	3/4	04	$X \leftarrow (mm+2)$	
LPS m	3/4	D0	Load processor status from information beginning at address m (see Section 6.2.1)	PX
MUL m	3/4	20	$A \leftarrow (A) * (mm+2)$	

Mnemonic	Format	Opcode	Effect	Notes
MULF m	3/4	60	F ← (F) * (mm+5)	XF
MULR r1, r2	2	98	$r2 \leftarrow (r2) * (r1)$	X
NORM	1	C8	$F \leftarrow (F)$ [normalized]	XF
OR m	3/4	44	$A \leftarrow (A) \mid (mm+2)$	im-Si
RD m	3/4	D8	A [rightmost byte] ← data	P
RMO r1,r2	2	AC	from device specified by (m) $r2 \leftarrow (r1)$	X
RSUB	3/4	4C	PC ← (L)	m ety
SHIFTL r1,n	2	A4	$r1 \leftarrow (r1)$ ; left circular shift n bits. {In assembled instruction, $r2 = n-1$ }	X
SHIFTR r1,n	2	A8	$r1 \leftarrow (r1)$ ; right shift n bits, with vacated bit positions set equal to leftmost bit of (r1). {In assembled instruction, $r2 = n-1$ }	X
SIO	1	F0	Start I/O channel number (A); address of channel program is given by (S)	PX
SSK m	3/4	EC	Protection key for address m $\leftarrow$ (A) (see Section 6.2.4)	PX
STA m	3/4	0C	mm+2 ← (A)	
STB m	3/4	78	mm+2 ← (B)	X
STCH m	3/4	54	$m \leftarrow (A)$ [rightmost byte]	
STF m	3/4	80	mm+5 ← (F)	ΧF
STI m	3/4	D4	Interval timer value ← (mm+2) (see Section 6.2.1)	PX
STL m	3/4	14	mm+2 ← (L)	
STS m	3/4	7C	mm+2 ← (S)	X
STSW m	3/4	E8	mm+2 ← (SW)	P
STT m	3/4	84	mm+2 ← (T)	X
STX m	3/4	10	mm+2 ← (X)	
SUB m	3/4	1C	$A \leftarrow (A) - (mm+2)$	VE
SUBF m	3/4	5C	$F \leftarrow (F) - (mm+5)$	XF

Mnemonic	Format	Opcode	Effect	Notes
SUBR r1,r2	2	94	$r2 \leftarrow (r2) - (r1)$	X
SVC n	2	В0	Generate SVC interrupt. {In assembled instruction, $r1 = n$ }	X
TD m	3/4	E0	Test device specified by (m)	P C
TIO	1	F8	Test I/O channel number (A)	PX C
TIX m	3/4	2C	$X \leftarrow (X) + 1; (X): (mm+2)$	C
TIXR r1	2	B8	$X \leftarrow (X) + 1; (X): (r1)$	X C
WD m	3/4	DC	Device specified by $(m) \leftarrow (A)$ [rightmost byte]	P

### **Instruction Formats**

## Format 1 (1 byte):

8 op

### Format 2 (2 bytes):

8	4	4
ор	rı	r2

### Format 3 (3 bytes):

6	1	1	1	1	1	1	(d) -> 2+m12n
ор	n	i	x	b	р	е	right (A) disp

## Format 4 (4 bytes):

6	1	1	1	1	1	1	20
ор	n	i	x	Ь	р	е	address