Ncore Perf Counter Architecture Specification

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ARTERIS® NCORE PERF COUNTER ARCHITECTURE SPECIFICATION

Release Information

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Product Status

The information in this document is ***Preliminary***.

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Preface

This preface introduces the Arteris® Network-on-Chip Hierarchical Coherency Engine Architecture Specification.

About this document

This technical document is for the Arteris Network-on-Chip Hierarchical Coherency Engine Architecture. It describes the subsystems and their function along with the system's interactions with the external subsystems. It also provides reference documentation and contains programming details for registers.

Product revision status

TBD

Intended audience

This manual is for system designers, system integrators, and programmers who are designing or programming a System-on-Chip (SoC) that uses or intend to use the Arteris Network-on-Chip Hierarchical Coherency System (ANoC-HCS).

Using this document

TBD

Glossary

The Arteris© Glossary is a list of terms used in Arteris© documentation, together with definitions for those terms. The Arteris© Glossary does not contain terms that are industry standard unless the Arteris© meaning differs from the generally accepted meaning.

Typographic conventions

italic

Introduces special terminology, denotes cross-references, and citations.

bold

Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.

monospace

Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.

monospace italic

Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name. monospace italic Denotes arguments to monospace text where the argument is to be replaced by a specific value. monospace bold Denotes language keywords when used outside example code.

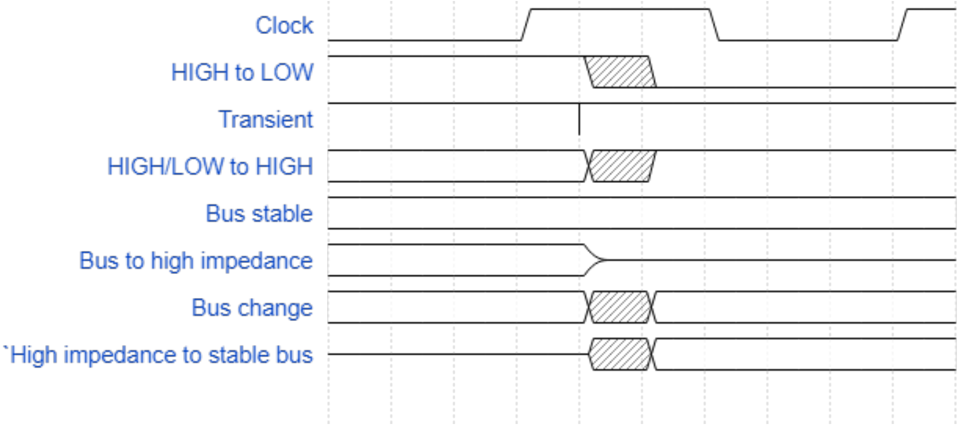
SMALL CAPITALS

Used in body text for a few terms that have specific technical meanings, that are defined in the Arteris® Glossary. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.

Timing diagrams

The following figure explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.



Signals

The signal conventions are:

Signal level

The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW. Asserted means:

- HIGH for active-HIGH signals.
- LOW for active-LOW signals.

Lowercase n

At the start or end of a signal name denotes an active-LOW signal.

Additional reading

This book contains information that is specific to this product. See the following documents for other relevant information.

History of the World II, Mel Brooks.

1 Introduction

This specification describes the performance counter architecture for Ncore.

A performance counter unit must be implemented in each Ncore unit i.e. AIUs, DCEs, DMIs, DIIs and DVE. This document goes over the architecture details and parameters of this unit and different events that are reported. The performance counter unit is not an optional unit and must always be present.

1.1 Parameters

A new unit level parameter is introduced. This parameter is passed to all Ncore units, it is shown in Table 1.

Name: nPerfCounters **Type:** Int **Visibility:** None

	Architecture		**Release**		**Default**
	Min	*Max*	*Min*	*Max*	
Value	4	16	4	8	4
Constraint	Only two valid values are supported 4 and 8				
Customer Description	Number of performance counters per Ncore unit				
Engineering Description					

Table 1 nPerfCounters Parameter

1.2 Detailed Description

The performance counter unit can track and report upto 31 events. The Ncore unit instantiating the performance unit specifies the events. These events maybe single bit or multi bit events and are specified in 1.4 section. The performance counter unit can be configured to implement either 4 or 8 counters.

Each counter is implemented as a 64 bit counter that is capable of counting upto 2 events at a time with following counter modes.

1. **Normal count**: In this mode the counter counts both the events together, if both the events are asserted then it is counted as two, if one event is asserted then it is counted as one
2. **AND count**: In this mode the counter counts one if both the events are asserted.
3. **XOR count**: In this mode the counter counts one only if one event is asserted and the other is de asserted.
4. **Instantaneous count:** In this mode the counter provides the instantaneous value of the multi bit event as is.

The counter reports count via 2 registers one is a 32-bit count register that reports lower 32 bits and another configurable register which supports

1. Capturing the upper 32 bits of the count

2. Used as an accumulation register for IIR filter.
3. Use as max/saturation value for accumulation events

1.3 Register Definition

Different registers supported by the performance counter unit are described below. A set of registers exist per counter configuration i.e. each Ncore unit can either have 4 or 8 set of registers

1.3.1 Counter Value Register (xCNTVR)

Bits	Name	Access	Reset	Description
31:0	Count value	R/W	0x0	Count value lower bits 31:0

1.3.2 Counter Saturation Register (xCNTSR)

Bits	Name	Access	Reset	Description
31:0	Count saturation value	R/W	0x0	Can be configured as follows: 1. Capture upper count value of 63:31 2. Use as IIR filter bits 3. Use as max/saturation value for accumulation events

1.3.3 Counter Control Register (CNTCR)

Bits	Name	Access	Reset	Description
0	Count Enable	R/W	0x0	Write one to enable counting
1	Count Clear	WSC	0x0	Write one to clear the counter (both CNTVR and CNTSR)
2	Interrupt Enable	R/W	0x0	Write one to enable rollover or overflow interrupt (gets ORed with correctable error interrupt)
3	Rollover/Overflow status	RO	0x0	One indicates overflow, sticky bit clears by clearing the counter
6:4	Conter control	R/W	0x0	000 – Normal count 001 – AND count 010 – XOR count 011 – Instantaneous count (used for multi bit events like Active OTT entries) 100 to 111 – reserved
9:7	SSR count	R/W	0x0	000 – Clear CNTSR (value of CNTSR is always zero) 001 – Capture upper 63:31 count in CNTSR 010 – use CNTSR as IIR filter (currently used only for active TT count)

				011 – use CNTSR as max/saturation value (currently used only for CHI AIU interleave count) 100 to 111 reserved
12:10	Filter select	R/W	0x0	Low pass filter coefficients (IIR filter) 000 – 0 001 – ½ 010 – ¼ 011 – 1/8 100 – 1/16 101 – 1/32 110 – 1/64 111 – 1/128
15:13	Minimum stall period	R/W	0x0	Value is 2 ^ (minimum stall period) clock cycles valid range is 0 to 7
16:21	Count event second	R/W	0x0	Select the second count event (must be different from Count event first), value of zero is not valid
22:23	Reserved			
24:29	Count event first	R/W	0x0	Select the first count event, value of zero is not valid
31:30	Reserved			

1.4 Performance events

1.4.1 CAIU Performance events

Event #	Width	Name	Description
1	1	SMI 0 Tx Stall event	Counts every cycle when valid is set and ready is low
2	1	SMI 1 Tx Stall event	Counts every cycle when valid is set and ready is low
3	1	SMI 2 Tx Stall event	Counts every cycle when valid is set and ready is low
4		Reserved	
5	1	SMI 0 Rx Stall event	Counts every cycle when valid is set and ready is low
6	1	SMI 1 Rx Stall event	Counts every cycle when valid is set and ready is low
7	1	SMI 2 Rx Stall event	Counts every cycle when valid is set and ready is low
8		Reserved	
9	1	ACE AW stall event	Counts every cycle when valid is set and ready is low (Does not apply to CHI AIU)
10	1	ACE W stall event	Counts every cycle when valid is set and ready is low (Does not apply to CHI AIU)
11	1	ACE B stall event	Counts every cycle when valid is set and ready is low (Does not apply to CHI AIU)
12	1	ACE AR stall event	Counts every cycle when valid is set and ready is low (Does not apply to CHI AIU)
13	1	ACE R stall event	Counts every cycle when valid is set and ready is low (Does not apply to CHI AIU)

14	1	ACE AC stall event	Counts every cycle when valid is set and ready is low (Does not apply to CHI AIU)
15	1	ACE CD stall event	Counts every cycle when valid is set and ready is low (Does not apply to CHI AIU)
16	1	ACE CR stall event	Counts every cycle when valid is set and ready is low (Does not apply to CHI AIU)
17		Reserved	
18		Reserved	
19		Reserved	
20	8	Active OTT entries	Number of active OTT entries
21		Reserved	
22	3	Captured SMI packets	Number of SMI packets Captured
23	3	Dropped SMI packets	Number of SMI packets dropped
24	1	Address Collisions	Count number of address collisions on incoming transactions
25	3	Interleaved Data	Count max number of active interleaved data transactions
26	1	Agent event counter	Counts number of events triggered by the native agent
27	1	Noc evet counter	Counts number of events triggered by the Noc
28		Reserved	
29		Reserved	
30	1	Div 16 counter	Divide by 16 free running counter
31	1	Number of QoS starvations	Number of times QoS starvations occurred

1.4.2 NCAIU Performance events

Event #	Width	Name	Description
1	1	SMI 0 Tx Stall event	Counts every cycle when valid is set and ready is low
2	1	SMI 1 Tx Stall event	Counts every cycle when valid is set and ready is low
3	1	SMI 2 Tx Stall event	Counts every cycle when valid is set and ready is low
4		Reserved	
5	1	SMI 0 Rx Stall event	Counts every cycle when valid is set and ready is low
6	1	SMI 1 Rx Stall event	Counts every cycle when valid is set and ready is low
7	1	SMI 2 Rx Stall event	Counts every cycle when valid is set and ready is low
8		Reserved	
9	1	ACE-Lite/AXI AW stall event	Counts every cycle when valid is set and ready is low
10	1	ACE-Lite/AXI W stall event	Counts every cycle when valid is set and ready is low
11	1	ACE-Lite/AXI B stall event	Counts every cycle when valid is set and ready is low
12	1	ACE-Lite/AXI AR stall event	Counts every cycle when valid is set and ready is low
13	1	ACE-Lite/AXI R stall event	Counts every cycle when valid is set and ready is low
14		Reserved	
15		Reserved	
16		Reserved	

17		Reserved	
18		Reserved	
19		Reserved	
20	8	Active OTT entries	Number of active OTT entries
21		Reserved	
22	3	Captured SMI packets	Number of SMI packets Captured
23	3	Dropped SMI packets	Number of SMI packets dropped
24	1	Address Collisions	Count number of address collisions on incoming transactions
25		Reserved	
26	1	Agent event counter	Counts number of events triggered by the native agent
27	1	Noc evet counter	Counts number of events triggered by the Noc
28		Reserved	
29		Reserved	
30	1	Div 16 counter	Divide by 16 free running counter
31	1	Number of QoS starvations	Number of times QoS starvations occurred

1.4.3 Proxy Performance events

Event #	Width	Name	Description
1	1	Cache read hit	
2	1	Cache write hit	
3	1	Cache snoop hit	
4	1	Cache eviction	
5	1	Cache no ways to allocate	
6	1	Cache fill stall	
7	1	Cache read stall	
8	1	Cache write stall	
9	1	Cache replay	
10	1	Cache read miss	
11	1	Cache write miss	
12	1	Cache snoop miss	
13		Reserved	
14		Reserved	
15		Reserved	
16		Reserved	
17		Reserved	
18		Reserved	
19		Reserved	
20		Reserved	
21		Reserved	
22		Reserved	
23		Reserved	
24		Reserved	

25		Reserved	
26		Reserved	
27		Reserved	
28		Reserved	
29		Reserved	
30		Reserved	
31		Reserved	

1.4.4 DMI Performance events

Event #	Width	Name	Description
1	1	SMI 0 Tx Stall event	Counts every cycle when valid is set and ready is low
2	1	SMI 1 Tx Stall event	Counts every cycle when valid is set and ready is low
3	1	SMI 2 Tx Stall event	Counts every cycle when valid is set and ready is low
4	1	SMI 3 Tx Stall event	Counts every cycle when valid is set and ready is low
5	1	SMI 0 Rx Stall event	Counts every cycle when valid is set and ready is low
6	1	SMI 1 Rx Stall event	Counts every cycle when valid is set and ready is low
7	1	SMI 2 Rx Stall event	Counts every cycle when valid is set and ready is low
8	1	SMI 3 Rx Stall event	Counts every cycle when valid is set and ready is low
9	1	AXI AW stall event	Counts every cycle when valid is set and ready is low
10	1	AXI W stall event	Counts every cycle when valid is set and ready is low
11	1	AXI B stall event	Counts every cycle when valid is set and ready is low
12	1	AXI AR stall event	Counts every cycle when valid is set and ready is low
13	1	AXI R stall event	Counts every cycle when valid is set and ready is low
14		Reserved	
15		Reserved	
16		Reserved	
17		Reserved	
18		Reserved	
19		Reserved	
20	8	Active WTT entries	Number of active WTT entries
21	8	Active RTT entries	Number of active RTT entries
22	4	Captured SMI packets	Number of SMI packets Captured
23	4	Dropped SMI packets	Number of SMI packets dropped
24	1	Address Collisions	Count number of address collisions on incoming transactions
25	1	Number of Merge events	Count number of DtwMergeMrds
26	1	Number of system visible Txn	Count number of system visible transactions
27		Reserved	
28		Reserved	
29		Reserved	
30	1	Div 16 counter	Divide by 16 free running counter
31	1	Number of QoS starvations	Number of times QoS starvations occurred

1.4.5 SMC Performance events

Event #	Width	Name	Description
1	1	Cache read hit	
2	1	Cache write hit	
3	1	Cache CMO hit	Operations like cleanInvlidate etc
4	1	Cache eviction	
5	1	Cache no ways to allocate	
6	1	Cache fill stall	
7	1	Cache read stall	
8	1	Cache write stall	
9	1	Cache replay	
10	1	Cache read miss	
11	1	Cache write miss	
12	1	Cache CMO miss	
13		Reserved	
14		Reserved	
15		Reserved	
16		Reserved	
17		Reserved	
18		Reserved	
19		Reserved	
20		Reserved	
21		Reserved	
22		Reserved	
23		Reserved	
24		Reserved	
25		Reserved	
26		Reserved	
27		Reserved	
28		Reserved	
29		Reserved	
30		Reserved	
31		Reserved	

1.4.6 DII Performance events

Event #	Width	Name	Description
1	1	SMI 0 Tx Stall event	Counts every cycle when valid is set and ready is low
2	1	SMI 1 Tx Stall event	Counts every cycle when valid is set and ready is low
3	1	SMI 2 Tx Stall event	Counts every cycle when valid is set and ready is low
4		Reserved	
5	1	SMI 0 Rx Stall event	Counts every cycle when valid is set and ready is low

6	1	SMI 1 Rx Stall event	Counts every cycle when valid is set and ready is low
7	1	SMI 2 Rx Stall event	Counts every cycle when valid is set and ready is low
8		Reserved	
9	1	AXI AW stall event	Counts every cycle when valid is set and ready is low
10	1	AXI W stall event	Counts every cycle when valid is set and ready is low
11	1	AXI B stall event	Counts every cycle when valid is set and ready is low
12	1	AXI AR stall event	Counts every cycle when valid is set and ready is low
13	1	AXI R stall event	Counts every cycle when valid is set and ready is low
14		Reserved	
15		Reserved	
16		Reserved	
17		Reserved	
18		Reserved	
19		Reserved	
20	8	Active WTT entries	Number of active WTT entries
21	8	Active RTT entries	Number of active RTT entries
22	3	Captured SMI packets	Number of SMI packets Captured
23	3	Dropped SMI packets	Number of SMI packets dropped
24	1	Address Collisions	Count number of address collisions on incoming transactions
25		Reserved	
26		Reserved	
27		Reserved	
28		Reserved	
29		Reserved	
30	1	Div 16 counter	Divide by 16 free running counter
31		Reserved	

1.4.7 DCE Performance events

Event #	Width	Name	Description
1	1	SMI 0 Tx Stall event	Counts every cycle when valid is set and ready is low
2	1	SMI 1 Tx Stall event	Counts every cycle when valid is set and ready is low
3	1	SMI 2 Tx Stall event	Counts every cycle when valid is set and ready is low
4		Reserved	
5	1	SMI 0 Rx Stall event	Counts every cycle when valid is set and ready is low
4	1	SMI 1 Rx Stall event	Counts every cycle when valid is set and ready is low
7	1	SMI 2 Rx Stall event	Counts every cycle when valid is set and ready is low
8		Reserved	
9		Reserved	
10		Reserved	
11		Reserved	
12		Reserved	
13		Reserved	

14		Reserved	
15		Reserved	
16		Reserved	
17		Reserved	
18		Reserved	
19		Reserved	
20	8	Active ATT entries	Number of active ATT entries
21		Reserved	
22		Reserved	
23		Reserved	
24	1	Address Collisions	Count number of address collisions on incoming transactions
25	1	SF hit	Snoop filter hit (either owner or sharer) count
26	1	SF miss	Snoop filter miss (neither owner nor sharer) count
27	1	SF recall	Snoop filter recall transaction count
28	1	Snoop rsp miss	Snoop response reports miss
29	1	Snoop rsp Owner transfer	Snoop response Ownership transfer
30	1	Div 16 counter	Divide by 16 free running counter
31	1	Number of QoS Starvations	Number of times QoS starvations occurred

1.4.8 DVE Performance events

Event #	Width	Name	Description
1	1	SMI 0 Tx Stall event	Counts every cycle when valid is set and ready is low
2	1	SMI 1 Tx Stall event	Counts every cycle when valid is set and ready is low
3	1	SMI 2 Tx Stall event	Counts every cycle when valid is set and ready is low
4		Reserved	
5	1	SMI 0 Rx Stall event	Counts every cycle when valid is set and ready is low
4	1	SMI 1 Rx Stall event	Counts every cycle when valid is set and ready is low
7	1	SMI 2 Rx Stall event	Counts every cycle when valid is set and ready is low
8		Reserved	
9		Reserved	
10		Reserved	
11		Reserved	
12		Reserved	
13		Reserved	
14		Reserved	
15		Reserved	
16		Reserved	
17		Reserved	
18		Reserved	
19		Reserved	

20	8	Active STT entries	Number of active STT entries
21		Reserved	
22	1	Captured DtwDbgReq packets	Number of DtwDbg packets captured
23	1	Dropped DtwDbgReq packets	Number of DtwDbg packets dropped
24		Reserved	
25		Reserved	
26		Reserved	
27		Reserved	
28		Reserved	
29		Reserved	
30	1	Div 16 counter	Divide by 16 free running counter
31		Reserved	

2 Opens

Questions/Feedback/Need to discuss:

3 Glossary

Arteris

A NoC Company

NCore3

A coherent NoC provided by Arteris with AMBA interfaces and built-in caches.

4 Notes

Notes ……