Ncore CSR access update Architecture Specification

Release: 1.0

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ARTERIS® NCORE CSR ACCESS UPDATE ARCHITECTURE SPECIFICATION

Release Information

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Product Status

The information in this document is ***Preliminary***.

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http://www.arteris.com

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Preface

This preface introduces the Arteris® Network-on-Chip Hierarchical Coherency Engine Architecture Specification.

About this document

This technical document is for the Arteris Network-on-Chip Hierarchical Coherency Engine Architecture. It describes the subsystems and their function along with the system's interactions with the external subsystems. It also provides reference documentation and contains programming details for registers.

Product revision status

TBD

Intended audience

This manual is for system designers, system integrators, and programmers who are designing or programming a System-on-Chip (SoC) that uses or intend to use the Arteris Network-on-Chip Hierarchical Coherency System (ANoC-HCS).

Using this document

TBD

Glossary

The Arteris© Glossary is a list of terms used in Arteris© documentation, together with definitions for those terms. The Arteris© Glossary does not contain terms that are industry standard unless the Arteris© meaning differs from the generally accepted meaning.

Typographic conventions

italic

Introduces special terminology, denotes cross-references, and citations.

bold

Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.

monospace

Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.

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monospace italic

Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name. monospace italic Denotes arguments to monospace text where the argument is to be replaced by a specific value. monospace bold Denotes language keywords when used outside example code.

SMALL CAPITALS

Used in body text for a few terms that have specific technical meanings, that are defined in the Arteris® Glossary. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.

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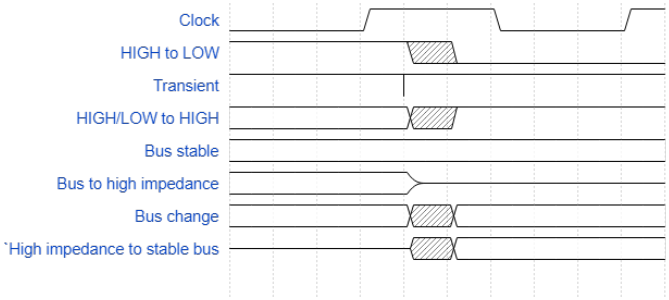
Timing diagrams

The following figure explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.



Signals

The signal conventions are:

Signal level

The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW. Asserted means:

- HIGH for active-HIGH signals.
- LOW for active-LOW signals.

Lowercase n

At the start or end of a signal name denotes an active-LOW signal.

Additional reading

This book contains information that is specific to this product. See the following documents for other relevant information.

History of the World II, Mel Brooks.

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Introduction

This specification describes changes to be made to improve CSR access from security perspective

1.1 Parameters

A new unit level parameter that applies to all AIUs is introduced; it is shown in Table 1.

Name: fnCsrAccess **Type:** Boolean **Visibility:** User

	Architecture	Release	Default
	Valid values	*Valid Values*	
Value	True, False	False	False
Constraint	Should be true on at-least one AIU. Always false on coherent AXI NCAIU where ncMode parameter is set to false		
Customer Description	Enables CSR access via this AIU		
Engineering Description			

TABLE 1 FNCSRACESS PARAMETER

1.2 Detailed Description

A new NRSAR register is added this register has a valid field that is set based on fnCsrAccess parameter. If the parameter is true then the valid field resets to 1 if the parameter is false then the valid field resets to 0. Hardware should use this valid field to qualify a transaction hit to the CSR address space. When valid is not set this will likely result in no BAR hit error.

Note: xNRSBHR and xNRSBLR should not be visible to customer and scope set to Engg or register condition changed to 0

1.2.1 Ncore register space attribute register (xNRSAR)

Bits	Name	Access	Reset	Description
30:0	Reserved	RO	0x0	
31	NRS valid	R/W	fnCsrAccess	Set high to enable CSR access via this AIU (This field must be RO for AIUs where the fnCsrAccess parameter is set and R/W where fnCsrAccess parameter is not set)

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Glossary

Arteris

A NoC Company

NCore3

A coherent NoC provided by Arteris with AMBA interfaces and built-in caches.

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Notes

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