Ncore Proxy Cache update Architecture Specification

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Release Information

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0.5	MK	Update tables with sharer promotion	09/09/2021
0.6	MK	Corrected typo of DT[0] and DT [1]	09/21/2021
0.7	MK	Update after review Added clarification to non-coherent transactions Added clarification on UP filed for table 4 description	11/10/2021
0.8	MK	Updated Non-Coherent access state updates and eviction (update command control)	11/22/2021
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Product Status

The information in this document is ***Preliminary***.

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Preface

This preface introduces the Arteris® Network-on-Chip Hierarchical Coherency Engine Architecture Specification.

About this document

This technical document is for the Arteris Network-on-Chip Hierarchical Coherency Engine Architecture. It describes the subsystems and their function along with the system's interactions with the external subsystems. It also provides reference documentation and contains programming details for registers.

Product revision status

TBD

Intended audience

This manual is for system designers, system integrators, and programmers who are designing or programming a System-on-Chip (SoC) that uses or intend to use the Arteris Network-on-Chip Hierarchical Coherency System (AnoC-HCS).

Using this document

TBD

Glossary

The Arteris© Glossary is a list of terms used in Arteris© documentation, together with definitions for those terms. The Arteris© Glossary does not contain terms that are industry standard unless the Arteris© meaning differs from the generally accepted meaning.

Typographic conventions

italic

Introduces special terminology, denotes cross-references, and citations.

Bold

Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.

Monospace

Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.

Monospace italic

Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name. monospace italic Denotes arguments to monospace text where the argument is to be replaced by a specific value. Monospace bold Denotes language keywords when used outside example code.

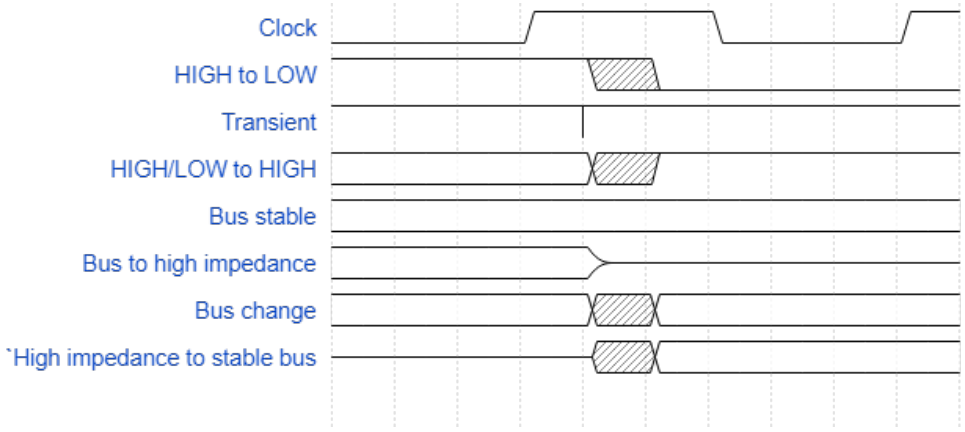
SMALL CAPITALS

Used in body text for a few terms that have specific technical meanings, that are defined in the Arteris® Glossary. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.

Timing diagrams

The following figure explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.



Signals

The signal conventions are:

Signal level

The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW. Asserted means:

- HIGH for active-HIGH signals.
- LOW for active-LOW signals.

Lowercase n

At the start or end of a signal name denotes an active-LOW signal.

Additional reading

This book contains information that is specific to this product. See the following documents for other relevant information.

History of the World II, Mel Brooks.

1 Introduction

This specification describes the changes to caching model of Ncore proxy cache. Two changes are covered in this document.

1. Ownership transfer
2. Pseudo exclusive proxy cache

The general caching model stays as is, which is MOESI

1.1 Parameters

No new parameters are introduced but the NcMode parameter is deprecated in this release.

Name: NCMode **Type:** Int **Visibility:** Deprecated

	Architecture		**Release**		**Default**
	Min	*Max*	*Min*	*Max*	
Value	0	1	0	1	0
Constraint	Applies only to AXI interface Must be set for to '0' i.e., coherent mode when Proxy cache is enabled Else can be either '1' or '0'				
Customer Description					
Engineering Description	Applies to AXI interface only '0' for coherent mode '1' for non-coherent mode				

TABLE 1 NC-MODE PARAMETER

1.2 Proxy cache allocation and visibility policies

Proxy cache allocation policy is controlled only by AxCache value of the transaction. Table 2 gives details on how proxy cache allocates transactions and sets visibility attributes based on AxCache values. If a cache line is allocated in the cache, then the concerto command going out on SMI must go with allocation attribute set to no allocate i.e. 0.

AxCache	Allocation	Visibility	Notes
0000	No	Late (system)	Device Non-bufferable[a, b]
0001	No	Early	Device bufferable[a, b]
0010	No	Late (system)	Normal Non-cacheable, Non-bufferable[b]
0011	No	Early	Normal Non-cacheable, Bufferable[b]
0110	Yes(R)/No(W)	Early	Write through no allocate / read allocate
0111	Yes(R)/No(W)	Early	Write back no allocate / read allocate
1010	No(R)/Yes(W)	Early	Write through write allocate
1011	No(R)/Yes(W)	Early	Write back write allocate
1110	Yes	Early	Write through read & write allocate
1111	Yes	Early	Write back read and write allocate

Note:

a. It is illegal to send Device type transactions to an address range mapped to normal memory.

b. It is not recommended to send non-cacheable transactions to an address range mapped to coherent (normal) memory. Sending non-cacheable transactions to cacheable address space breaks memory consistence.

Ncore 3.4 will not report an error, but correct behavior will not be guaranteed. Future versions of Ncore may report an error.

TABLE 2 CACHE ALLOCATION & VISIBILITY

1.3 Transactions native to concerto

This section goes over how native transactions are translated to concerto transactions after proxy cache look up. Table 3 shows different cache look up actions. Note that in this table "X" denotes don't care. **SZ** denotes size of the transaction which can be partial (ptl) or full. **CS** denotes current state of the cache which can be SC (shared clean), SD (shared dirty or owned), UC (unique clean) and UD (unique dirty). **AP** denotes allocation policy where NA is no allocate and AL allocate, this is determined based on Table 2. **NS** denotes possible next state of the cache after the transaction finishes. **Conc Msg** specifies the message to be issued into the Ncore system.

Transaction	SZ	CS	AP	NS	Conc msg	Notes
Read	X	IX	NA	IX	CmdRdNITC	Miss no allocate (no cache case)
			AL	SC/SD/UC/UD	CmdRdVld	Miss allocate
		SC	X	-	-	Cache hit
		SD	X	-	-	Cache hit
		UD	X	-	-	Cache hit
		UC	X	-	-	Cache hit
Write	Ptl	IX	NA	IX	CmdWrUnqPtl	Miss no allocate (no cache case)
			AL	UD	CmdRdUnq	Miss allocate
		SC	X	UD	CmdRdUnq	Cache hit upgrade
		SD	X	UD	CmdRdUnq	Cache hit upgrade, drop data if SD is not lost in the interim and just upgrade to UD. (Data could be form memory and thus stale)
		UC	X	UD	-	Cache hit
		UD	X	UD	-	Cache hit
	Full	IX	NA	IX	CmdWrUnqFull	Miss no allocate (no cache case)
			AL	UD	CmdMkUnq	Miss allocate
		SC	X	UD	CmdMkUnq	Cache hit upgrade
		SD	X	UD	CmdMkUnq	Cache hit upgrade
		UD	X	UD	-	Cache hit
		UC	X	UD	-	Cache hit

TABLE 3 CACHE LOOKUP ACTIONS

For Write Ptl cache hit upgrade cases, current states SC or SD issues CmdRdUnq instead of CmdClnUnq. This is done to avoid the creation of UCE and UDP state, in the case where an intervening snoop invalidates the SC and SD state.

If a cache is not present, then the native commands are mapped to concerto commands using the row where allocation (AP) policy AP is NA and the nest state (NS) is IX

1.3.1 Non-Coherent transactions

The updated proxy cache must support access to DII, these transactions are non-coherent. Native read and write transactions hitting DII/DMI GPRS with NC bit set are simply translated to CmdRdNc and CmdWrNc respectively.

NcMode parameter will be deprecated and only the GPRS configuration will be honored.

Cache allocation and look up is followed based on AxCache bits for the transaction. Partial Miss allocate cases must be converted to no allocate case for non-coherent transactions. Non-coherent cache lookup actions are shown in Table 4. Note that final state transition for allocating read is always UC and on write is UD. This is done to make sure dirty write data is evicted back to the memory; the read data does not need to be evicted back to the memory if it is clean. This architecture does not grantee coherency/consistency if software mixes coherent and non-coherent transactions within the same address space without taking proper precautions.

Transaction	SZ	CS	AP	NS	Conc msg	Notes
Read	Ptl	IX	NA	IX	CmdRdNc	Miss no allocate (no cache case)
			AL	IX	CmdRdNc	Partial allocate converted no allocate on miss
		SC	X	-	-	Cache hit
		SD	X	-	-	Cache hit
		UD	X	-	-	Cache hit
		UC	X	-	-	Cache hit
	Full	IX	NA	IX	CmdRdNc	Miss no allocate (no cache case)
			AL	UC	CmdRdNc	Miss allocate
		SC	X	-	-	Cache hit
		SD	X	-	-	Cache hit
		UD	X	-	-	Cache hit
		UC	X	-	-	Cache hit
Write	Ptl	IX	NA	IX	CmdWrNcPtl	Miss no allocate (no cache case)
			AL	IX	CmdWrNcPtl	Partial allocate converted no allocate on miss
		SC	X	UD	-	Cache hit
		SD	X	UD	-	Cache hit
		UC	X	UD	-	Cache hit
		UD	X	UD	-	Cache hit
	Full	IX	NA	IX	CmdWrNcFull	Miss no allocate (no cache case)
			AL	UD	-	Miss allocate
		SC	X	UD	-	Cache hit
		SD	X	UD	-	Cache hit
		UD	X	UD	-	Cache hit
		UC	X	UD	-	Cache hit

TABLE 4 NON-COHERENT CACHE LOOKUP ACTIONS

Evictions of non-coherent transactions allocated to proxy cache do not need update commands to be sent to DCE, if they are sent, it results in extra command traffic on the network and does not have functional impact. Coherent transactions allocated to proxy cache do need update commands to be sent to DCE, they help in reducing snoop traffic by updating the snoop filter at the expense of extra command traffic on the network, if they are not sent then it may result in more snoop traffic in the network.

A CSR control bit must be implemented in the cache control register to enable/disable update commands to DCE. This bit must affect update commands in general irrespective of the original allocating transaction is coherent or non-coherent.

1.4 Proxy cache state transitions

Proxy cache state transitions are detailed in this section. Table 5 gives details of state transition at the proxy cache when a DTR is received from the Ncore system. Table 6 gives details of state transition based on the snoop received at the proxy cache. This table also gives details regarding different DtrReq and DtwReq that may be issued. The UP column refers to unique presence, here "X" means don't care, "Y" means a UP value of 11 with a match on MPF3 field or UP value of 01 and "N" means UP value of 11 with no match on MPF3 field. Currently UP values of 00 and 10 are reserved, they can be treated as "N" case but DCE should not be sending them out and are illegal for this release. Cases that are not mentioned in the table are not legal.

Transaction	CS	DtrReq	NS	Notes
Read	IX	DtrDataInv	IX	Data not cached
		DtrDataSCln	SC	
		DtrDataSDty	SD	
		DtrDataUCln	UC	
		DtrDataUDty	UD	
Write partial	IX/SC/SD	DtrDataUCln or DtrDataUDty	UD	Merge partial data and cache
Write full	IX/SC/SD	X	UD	Replace data with write data

TABLE 5 PROXY CACHE DTRREQ STATE TRANSITION

SnpReq	CS	NS	UP	RV	RS	DC	DT[1]	DT[0]	DtrReq	DtwReq
SnpClnDtr	IX	IX	X	0	0	0	0	0	-	-
	SC	SC	N	1	1	0	0	0	-	-
	SC	SC	Y	1	1	0	1	0	DtrDataSCln	-
	SD	SD	Y	1	0	0	1	0	DtrDataSCln	-

SnpReq	CS	NS	UP	RV	RS	DC	DT[1]	DT[0]	DtrReq	DtwReq
	UC	SC	Y	1	1	0	1	0	DtrDataSCln	-
	UD	SD	Y	1	0	0	1	0	DtrDataSCln	-
SnpNoSDInt	IX	IX	X	0	0	0	0	0	-	-
	SC	SC	N	1	1	0	0	0	-	-
	SC	SC	Y	1	1	0	1	0	DtrDataSCln	-
	SD	SD	Y	1	0	0	1	0	DtrDataSCln	-
	UC	SC	Y	1	1	0	1	0	DtrDataSCln	-
	UD	SD	Y	1	0	0	1	0	DtrDataSCln	-
SnpVldDtr	IX	IX	X	0	0	0	0	0	-	-
	SC	SC	N	1	1	0	0	0	-	-
	SC	SC	Y	1	1	0	1	0	DtrDataSCln	-
	SD	SC	Y	1	1	1	1	0	DtrDataSDty	-
	UC	SC	Y	1	1	1	1	0	DtrDataSCln	-
	UD	SC	Y	1	1	1	1	0	DtrDataSDty	-
SnpInvDtr	IX	IX	X	0	0	0	0	0	-	-
	SC	IX	N	0	0	0	0	0	-	-
	SC	IX	Y	0	0	0/1[a]	0/1[a]	0/1[b]	If (UP = 01) DtrDataUCln	If (UP =11) DtwDataCln
	SD	IX	Y	0	0	0/1[a]	0/1[a]	0/1[b]	If (UP = 01) DtrDataUDty	If(UP=11) DtwDataDty
	UC	IX	Y	0	0	1	1	0	DtrDataUCln	-
	UD	IX	Y	0	0	1	1	0	DtrDataUDty	-
SnpNitc	IX	IX	X	0	0	0	0	0	-	-
	SC	SC	N	1	1	0	0	0	-	-
	SC	SC	Y	1	1	0	1	0	If (TOF=CHI/AXI) DtrDataInv else DtrDataSCln	-
	SD	SD	Y	1	0	0	1	0	If (TOF=CHI/AXI) DtrDataInv else DtrDataSCln	-
	UC	UC	Y	1	0	0	1	0	DtrDataInv	-
	UD	UD	Y	1	0	0	1	0	DtrDataInv	-
SnpNitcCI	IX	IX	X	0	0	0	0	0	-	-
	SC	IX	N	0	0	0	0	0	-	-
	SC	IX	Y	0	0	0	1	0	DtrDataInv	-
	SD	IX	Y	0	0	0	1	1	DtrDataInv	DtwDataDty

SnpReq	CS	NS	UP	RV	RS	DC	DT[1]	DT[0]	DtrReq	DtwReq
	UC	IX	Y	0	0	0	1	0	DtrDataInv	-
	UD	IX	Y	0	0	0	1	1	DtrDataInv	DtwDataDty
SnpNitcMI	IX	IX	X	0	0	0	0	0	-	-
	SC	IX	N	0	0	0	0	0	-	-
	SC	IX	Y	0	0	0	1	0	DtrDataInv	-
	SD	IX	Y	0	0	0	1	0	DtrDataInv	-
	UC	IX	Y	0	0	0	1	0	DtrDataInv	-
	UD	IX	Y	0	0	0	1	0	DtrDataInv	-
SnpClnDtw	IX	IX	X	0	0	0	0	0	-	-
	SC	SC	X	1	1	0	0	0	-	-
	SD	SC	X	1	1	0	0	1	-	DtwDataDty
	UC	UC	X	1	0	0	0	0	-	-
	UD	UC	X	1	0	0	0	1	-	DtwDataDty
SnpInvDtw / SnpUnqStsh / SnpStshUnq	IX	IX	X	0	0	0	0	0	-	-
	SC	IX	X	0	0	0	0	0	-	-
	SD	IX	X	0	0	0	0	1	-	DtwDataDty
	UC	IX	X	0	0	0	0	0	-	-
	UD	IX	X	0	0	0	0	1	-	DtwDataDty
SnpInv/SnpInvStsh	X	IX	X	0	0	0	0	0	-	-
SnpStshShd	IX	IX	X	0	0	0	0	0	-	-
	SC	SC	X	1	1	0	0	0	-	-
	SD	SD	X	1	0	0	0	1	-	DtwDataDty
	UC	SC	X	1	1	0	0	0	-	-
	UD	SD	X	1	0	0	0	1	-	DtwDataDty

TABLE 6 CACHE SNPREQ STATE TRANSITIONS

Notes:

a. Set if UP == 01
b. Set if UP ==11 and target matches

2 Opens

Questions/Feedback/Need to discuss:

3 Glossary

Arteris

A NoC Company

NCore3

A coherent NoC provided by Arteris with AMBA interfaces and built-in caches.

4 Notes

Notes ……