Ncore Supplemental Architecture Specification

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ARTERIS® NCORE SUPPLEMENTAL ARCHITECTURE SPECIFICATION

Release Information

Version	*Editor*	*Change*	*Date*
0.5	MK	Initial Document	06/17/2022
0.6	MK	Updated Burst restrictions	06/24/2022
0.7	MK	Added a parameter to disable AXI interleaving Added Debug and BIST disable description	08/11/2022
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Product Status

The information in this document is ***Preliminary***.

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Preface

This preface introduces the Arteris® Network-on-Chip Hierarchical Coherency Engine Architecture Specification.

About this document

This technical document is for the Arteris Network-on-Chip Hierarchical Coherency Engine Architecture. It describes the subsystems and their function along with the system's interactions with the external subsystems. It also provides reference documentation and contains programming details for registers.

Product revision status

TBD

Intended audience

This manual is for system designers, system integrators, and programmers who are designing or programming a System-on-Chip (SoC) that uses or intend to use the Arteris Network-on-Chip Hierarchical Coherency System (AnoC-HCS).

Using this document

TBD

Glossary

The Arteris© Glossary is a list of terms used in Arteris© documentation, together with definitions for those terms. The Arteris© Glossary does not contain terms that are industry standard unless the Arteris© meaning differs from the generally accepted meaning.

Typographic conventions

italic

Introduces special terminology, denotes cross-references, and citations.

Bold

Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.

Monospace

Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.

Monospace italic

Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name. monospace italic Denotes arguments to monospace text where the argument is to be replaced by a specific value. Monospace bold Denotes language keywords when used outside example code.

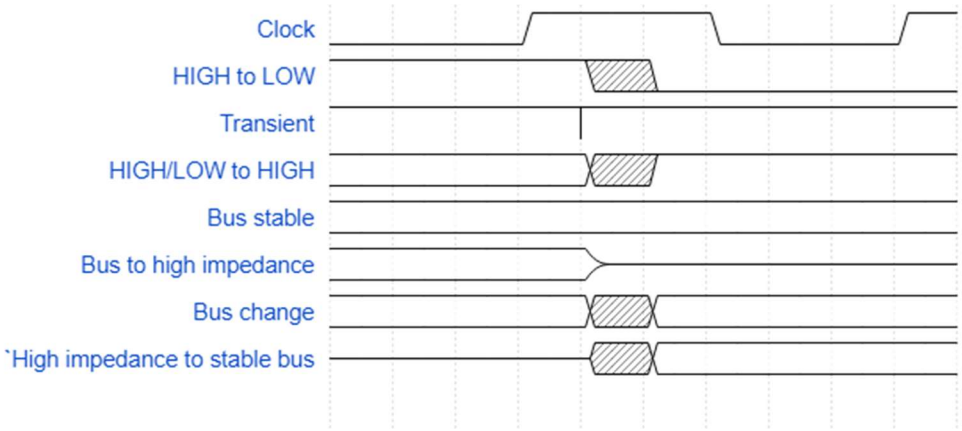
SMALL CAPITALS

Used in body text for a few terms that have specific technical meanings, that are defined in the Arteris® Glossary. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.

Timing diagrams

The following figure explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.



Signals

The signal conventions are:

Signal level

The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW. Asserted means:

- HIGH for active-HIGH signals.
- LOW for active-LOW signals.

Lowercase n

At the start or end of a signal name denotes an active-LOW signal.

Additional reading

This book contains information that is specific to this product. See the following documents for other relevant information.

History of the World II, Mel Brooks.

1 Introduction

This is a supplemental specification to override, missing or incorrect miscellaneous items in the original Ncore 3.0 architecture specification, concerto messaging protocol specification and parameter specification. Note that this document does not cover all items and some functionality and features are covered in their own specific additional documents like Ncore error architecture document.

1.1 Parameters

Following new parameters have been introduced, parameters related to features which have their own arch document are included in that specific document.

Name: fnDisableRdInterleave **Type:** Int **Visibility:** user Settable

	Architecture		Release		Default
	Min	*Max*	*Min*	*Max*	
Value	0	1	0	1	0
Constraint					
Customer Description	When set disables read data interleaving across different AXI IDs				
Engineering Description	When set disables read data interleaving across different AXI IDs. This parameter applies to NCAIU with AXI, ACE-Lite and ACE-Lite E ports				

TABLE 1 FNDISABLERDINTERLEAVE PARAMETER

Name: fnDebugAPBEnable **Type:** Int **Visibility:** user Settable

	Architecture		Release		Default
	Min	*Max*	*Min*	*Max*	
Value	0	1	0	1	1
Constraint					
Customer Description	When set enables an APB slave port on the CSR network. This port is expected to be used for on chip debug purposes only.				
Engineering Description	When set enables an APB slave port on the CSR network. This port is expected to be used for on chip debug purposes only.				

TABLE 2 FNDEBUGAPBENABLE PARAMETER

Name: fnDisableResiliencyBistDebugPin **Type:** Int **Visibility:** user Settable

	Architecture		Release		Default
	Min	*Max*	*Min*	*Max*	
Value	0	1	0	1	0
Constraint					
Customer Description	When set removes BIST and trace & debug disable pin.				
Engineering Description	When set removes BIST and trace & debug disable pin.				

TABLE 3 FNDISABLERESILIENCYBISTDEBUGPIN PARAMETER

1.2 Burst limitations

Ncore 3.x has following burst limitation at AIU with native interfaces AXI, ACE-Lite, ACE-Lite E and ACE.

- Narrow bursts are limited to only a single beat
- Fixed bursts are not supported
- Wrap non modifiable burst which cross 64-byte boundary are not supported

1.3 Barrier Support

Nore 3.x does not support barriers on any Native interfaces. The connected agent is expected to not issue them into Ncore. If they are issued Ncore behavior is undefined.

1.4 Atomics Support

Ncore 3.x supports only cacheable coherent and non-coherent atomics to normal memory connected below a DMI. Ncore does not support atomic transactions to non-cacheable device memory or cacheable normal memory below a DII.

1.5 RL field definition for concerto messages

The RL field (response level) specifies when and if the target of the message is expected to issue a response. Mapping of different values of RL are specified in Table 4.

RL value	Description
0x0	The initiator of the message does not expect a response
0x1	The initiator of the message expects a response, the target may send the response as soon as it gets the message acknowledging that the message is received. The response here may be used as credit return in which case it may be delayed till the credit can be freed.
0x2	The initiator of the message expects a response, the target may send the response after completing protocol level activities restricted to that message. Protocol level activity here may include cache look up and or getting a response from the native interface.
0x3	The initiator of the message expects a response, the target may send the response only after completion of any dependent concerto messages. Here completion of a dependent message includes receiving any expected response for all dependent messages

TABLE 4 RM FIELD VALUE ENCODING

Different messages have this field set as follows

- CmdReq this field is always set as 0x01 except for CMO CmdReq with VZ set as 1 and UpdReq where it is set as 0x2
- SnpReq this field is always set as 0x02
- MrdReq this field is set based on the originating command or CmType as shown in Table 5

Command type	RL value	Description

Regular read command MrdRdCln, MrdRdWSCln, MrdRdWUCln, MrdRdWU, and MrdRdWInv	0x1	MrdRsp must be issued by DMI as soon as possible, this represents a credit return
Cache maintenance operations MrdCln, MrdInv, and MrdFlush	0x2	MrdRsp must be issued after the cache is looked up and any dependent write transaction finishes on the native interface.
Stash once command MrdRdCln	0x3	MrdRsp must be issued only after the resultant DtrReq completes i.e., DtrRsp is recived

TABLE 5 MEMORY READ REQUEST RL FIELD

- RbrReq this field is set to 0x2
- RbuReq this field is set to 0x2
- DtwReq this field is set as shown in Table 6

DtwReq Type	RL field value
All DtwMrgMrd	0x3
All DtwReq	0x2

TABLE 6 DATA TRANSFER WRITE REQUEST RL FIELD VALUES

- DtwRsp this field is set 0x0 (Probably needs to be deprecated from DtwRsp)
- DtwDbgReq this field is set to 0x1
- DtwDbgRsp this field is set 0x0 (Probably needs to be deprecated from DtwDbgRsp)

1.6 Debug and BIST disable pin

Resiliency requirements require that Ncore IP provide a pin that can disable enablement of BIST and debug & trace feature via CSRs. The user of the Ncore IP may decide to use this pin as an Effuse, pin on the chip or route it to a secure register.

This pin “<prefix>_en _debug_bist” must be present only when resiliency is enabled via the resiliency enable parameter.

Internal to Ncore the pin must be routed to all CAIUs, NACIUs, DMIs, DIIs and FSC. Note that this pin is not propagated to DCE.

1.7 Debug APB port

To enable debug of a hung Ncore system a slave APB port must be added to the CSR network that can access all the Ncore CSRs. At top level this port signals must be “<prefix>_debug_apb_<rest of the signal name>”.

Following APB port restrictions apply

- Fixed data bus width 32 bits
- Fixed address bus width of 20 bits
- Fixed access size of 4 bytes
- All access are 4 byte aligned.

This port is expected to be used for debug only, if same register is accessed concurrently via this debug APB port and the internal Ncore CSR accesses then the effect on the CSR is undefined. Ncore does not guarantee any ordering between the two access.

1.8 Non-Coherent Exclusive Transactions Support

In IO-AIU with proxy cache configuration, the address used for non-coherent exclusive transactions can only be non-cacheable. In other words, the GPRAR NC bit must be 1, and the AxCache[3:2] == 0. Therefore, the transaction will never hit proxy cache and go straight to DMI and utilize exclusive monitor inside DMI to return correct exclusive status (EXOK/EXFAIL) back to the IO-AIU then to the original requester.

1.9 Coherent Transactions Constraint

In IO-AIU with ACE/ACE_Lite/ACE_LiteDVM master, add a constraint "the total size of coherent transactions must be equal or smaller than the cacheline size of the system. In addition, the transaction CAN NOT cross cacheline boundary, in other words, the transaction MUST fall into a single cacheline only". The IO-AIU DO NOT collect response from multiple cacheline to determine the final response back to the initiating master.

2 Opens

Questions/Feedback/Need to discuss:

3 Glossary

Arteris

A NoC Company

NCore3

A coherent NoC provided by Arteris with AMBA interfaces and built-in caches.

4 Notes

Notes ……