Ncore QoS Improvement Architecture Specification

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Release Information

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Product Status

The information in this document is ***Preliminary***.

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Preface

This preface introduces the Arteris® Network-on-Chip Hierarchical Coherency Engine Architecture Specification.

About this document

This technical document is for the Arteris Network-on-Chip Hierarchical Coherency Engine Architecture. It describes the subsystems and their function along with the system's interactions with the external subsystems. It also provides reference documentation and contains programming details for registers.

Product revision status

TBD

Intended audience

This manual is for system designers, system integrators, and programmers who are designing or programming a System-on-Chip (SoC) that uses or intend to use the Arteris Network-on-Chip Hierarchical Coherency System (AnoC-HCS).

Using this document

TBD

Glossary

The Arteris© Glossary is a list of terms used in Arteris© documentation, together with definitions for those terms. The Arteris© Glossary does not contain terms that are industry standard unless the Arteris© meaning differs from the generally accepted meaning.

Typographic conventions

italic

Introduces special terminology, denotes cross-references, and citations.

Bold

Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.

Monospace

Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.

Monospace italic

Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name. monospace italic Denotes arguments to monospace text where the argument is to be replaced by a specific value. Monospace bold Denotes language keywords when used outside example code.

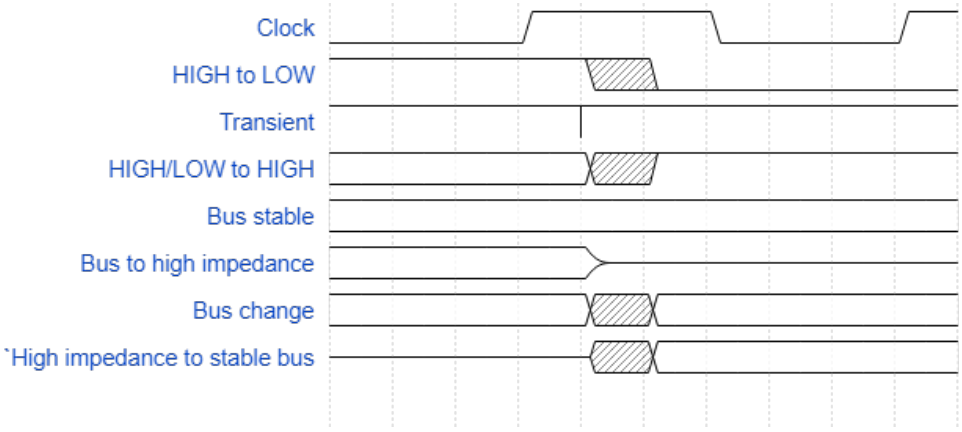
SMALL CAPITALS

Used in body text for a few terms that have specific technical meanings, that are defined in the Arteris® Glossary. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.

Timing diagrams

The following figure explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.



Signals

The signal conventions are:

Signal level

The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW. Asserted means:

- HIGH for active-HIGH signals.
- LOW for active-LOW signals.

Lowercase n

At the start or end of a signal name denotes an active-LOW signal.

Additional reading

This book contains information that is specific to this product. See the following documents for other relevant information.

History of the World II, Mel Brooks.

1 Introduction

This specification describes the changes to improve Ncore QoS support. Needed changes are within DMI only. The purpose of these changes is to work around AXI head of line blocking issue. Expected top level view of DMI and DMC (Dram Memory Controller) connectivity is shown in Figure 1. The customer/user of Ncore is expected to develop the

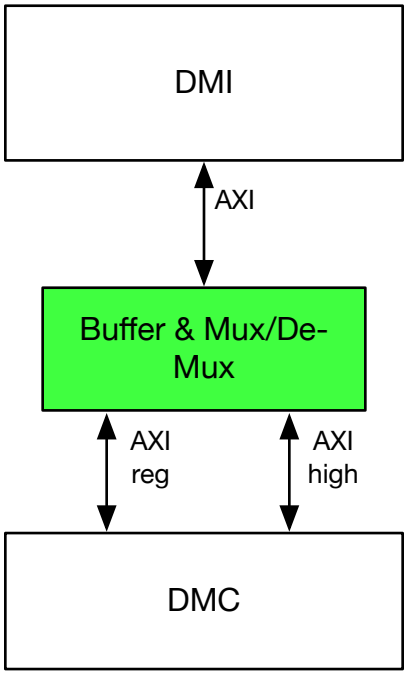


FIGURE 1 DMI AND DMC CONNECTIVITY

Following assumptions apply in this use case

1. The DMC used has 2 AXI ports one for regular traffic shown as “AXI reg” and another for high priority or real time traffic shown as “AXI high”
2. The user or customer develops “Buffer & Mux/De-Mux” block

The “Buffer & mux/de-mux” block consists of simple logic where it has a buffer that is larger than the DMC’s AXI reg port buffer. The mux/de-mux logic is responsible for routing the high priority or real time traffic to DMC’s AXI high, while all other traffic is routed to DMC’s AXI reg port. The buffer being larger than the buffer DMC’s AXI reg port buffer grantees that high priority traffic does not see head of line blocking.

The changes in DMI are needed to make sure DMI has reserved resources and provides an unblocked path for real time traffic.

1.1 Parameters

Three new DMI level parameter is introduced. These parameters are:

Name: DmiQoSThVal **Type:** Int **Visibility:** User Settable

	Architecture		Release		Default
	Min	*Max*	*Min*	*Max*	
Value	1	15	1	15	8
Constraint	This parameter is available only when QoS is enabled				
Customer Description	DMI QoS threshold value. Traffic with QoS equal to or above this value are considered as high priority hard real time traffic				
Engineering Description					

TABLE 1 DMIQOSTHVAL PARAMETER

Name: nDmiWttQoSRsv **Type:** Int **Visibility:** User Settable

	Architecture		Release		Default
	Min	*Max*	*Min*	*Max*	
Value	1	64	1	32	1
Constraint	This parameter is available only when QoS is enabled Maximum acceptable value must be minimum of WTT size -1 or size of DMI non-coherent write data buffer or Coherent write data buffer. • Non-Coherent write data buffer is represented by DMI RB credits. • Coherent write data buffer is represented by number of connected DCEs multiplied by DCE RB credits per DMI. Max value = minimum of (Max WTT size -1, DMI Rb Credits -1, DCE RB Credits-1 * number of connected DCEs) Example: WTT size = **16** DMI RB credits = **24** (non-Coherent write data buffer size) DCE RB credits = 4 and number of DCEs connected to DMI = 2. This gives the coherent write data buffer size of 4*2 = **8** As of the three numbers Coherent write data buffer size of **8** is smallest then maximum possible value is **8-1 = 7**				
Customer Description	WTT entries in DMI reserved for high priority hard real time traffic				
Engineering Description					

TABLE 2 NDMIWTTQOSRSV PARAMETER

Name: nDmiRttQoSRsv **Type:** Int **Visibility:** User Settable

	Architecture		Release		Default
	Min	*Max*	*Min*	*Max*	
Value	1	64	1	32	1
Constraint	This parameter is available only when QoS is enabled Maximum acceptable value must be RTT size -1				
Customer Description	RTT entries in DMI reserved for high priority hard real time traffic				
Engineering Description					

TABLE 3 NDMIRTTQOSRSV PARAMETER

1.2 Changes in DMI

Needed changes in DMI are shown in Figure 2. This change involves implementing a feedback loop from DMI egress AXI port i.e. both RTT/WTT to the SMI ingress skid buffers. RTT and WTT must reserve certain number of entries for high priority real time traffic. The number of reserved entries in RTT and WTT are defined by nDmiRttQoSRsv and nDmiWttQoSRsv parameters respectively. QoS threshold value for high priority real time traffic is defined by the parameter DmiQoSThVal. These three values can be changed at boot time via a CSR.

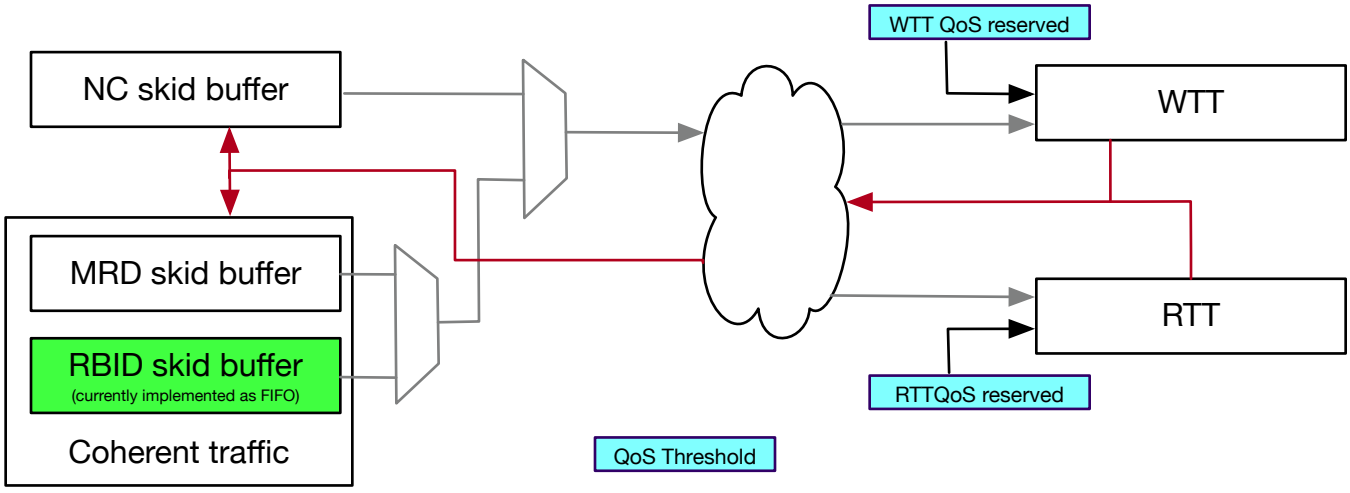


FIGURE 2 DMI QOS FEEDBACK LOOP

During runtime when WTT/RTT have only reserved entries left they individually give feedback to the skid buffers to send only high priority real time traffic. As this feedback is provided individually the skid buffer is responsible to respond individually for either read or write traffic i.e. at any given time only one or both RTT/WTT can push back regular traffic and the skid buffer should handle them separately.

Once regular entries free up in RTT/WTT then the feedback is removed, and regular traffic can start making forward progress. The feedback path is shown with red arrows. Note that the current implementation of coherent writes in DMI is in FIFO order this will need to be changed to a priority-based skid buffer.

The user or customer is expected to size the WTT/RTT and reserved entries with some margins to account for pipeline delays. The micro-arch is expected to provide DMI pipeline delay between Skid buffer and the WTT/RTT.

The skid buffer starvation logic should ignore the reserved entries feedback and push starved entries through.

1.3 Register Definition

The threshold and reservation values are implemented in a single register as shown below:

Bits	Name	Access	Reset	Description
7:0	WttQoSRsv	R/W	nDmiWttQoSRsv	WTT entries in DMI reserved for high priority hard real time traffic (recommended to be same as RttQoSRsv)
15:8	RttQoSRsv	R/W	nDmiRttQoSRsv	RTT entries in DMI reserved for high priority hard real time traffic (recommended to be same as WttQoSRsv)
29:16	Reserved	-	-	-
31:28	QoSThVal	R/W	DmiQoSThVal	DMI QoS threshold value. Traffic with QoS equal to or above this value are considered as high priority hard real time traffic

2 Opens

Questions/Feedback/Need to discuss:

3 Glossary

Arteris

A NoC Company

NCore3

A coherent NoC provided by Arteris with AMBA interfaces and built-in caches.

4 Notes

Notes ……