

Ncore System Architecture Specification

Product release: 3.7

Revision: 1.10, September 26, 2025

ARTERIS® NCORE SYSTEM ARCHITECTURE SPECIFICATION

Copyright © 2024-2025 Arteris® or its affiliates. All rights reserved.

Release Information

Version	Editor	Change	Date
1.10	HL	<ul style="list-style-type: none"> Updated section 12.2.1 and Figure 12-1 accordingly per requested in [CONC-17734] Updated section 13.4.3 and clarified on how a cache write hit with update is counted a cache write miss per identified in [CONC-17930] 	9/26/2025
1.09	HL	<ul style="list-style-type: none"> Corrected a typo in Table 6-6 as identified in [CONC-17696] Removed previous section 4.14.5 and 4.14.6 because these two sections simply repeat what AMBA AXI version H.c on ordering definitions and corresponding handling based on the recent team reviews while fixing NXP order related bugs <ul style="list-style-type: none"> Updated Table 5-14 in section 5.4.7 with the addition of section 5.4.7.1 to restrict the supported combinations among policy and ReadID/WriteID setting Further cleaned up the ordering handling in PCAIU as described in section 4.14.5 In section 8.1.2.1, clarified detection enable bit needs to be set so a corresponding uncorrectable error interrupt can be observable as identified in [CONC-17585] Corrected the flow diagram Figure 4-4 per identified in [CONC-17610] 	8/27/2025
1.08	HL	<ul style="list-style-type: none"> Made CAIU always set VZ to be 1 when a request with No Order mode is selected even with an early acknowledge (EWA) is set in the native command request to address the bugs identified in NXP design as identified and discussed in [CONC-17461]. Corresponding updates are described in section 1.2.8 and Figure 4-27. 	8/20/2025
1.07	HL	<ul style="list-style-type: none"> Updated and aligned parity error handling in section 8.12 per discussed in [CONC-17253] 	6/9/2025
1.06	HL	<ul style="list-style-type: none"> Maded Cache_Stash_Trasanctions peroprty no required for PCAIU configuration as explained in [CONC-17146] and [CONC-17155] Made ACE5-Lite explicit as one of the native interfaces to support for OWO in section 4.14 per requested in [CONC-17146] 	5/18/2025
1.05	HL	<ul style="list-style-type: none"> Removed previous Figure 4-31 since Synopsys has updated its PCIe Gen6 controller architecture. Previous diagram is not accurate to reflect the proper system view Expanded interface check_type error list for both AXI/ACE/ACE5-Lite etc. and CHI-B/E in Table 8-12 to accommodate check_type error for AC channel, RACK and WACK per requested in [CONC-17137] Changed IOAIUp configuration as PCAIU per described in [MAES-8134] 	5/14/2025
1.03	HL	<ul style="list-style-type: none"> Fixed errors and discrepancy in self review 	5/7/2025

Version	Editor	Change	Date
		<ul style="list-style-type: none"> ○ Corrected Figure 5-10 and Error! Reference source not found. on the definition of NSX and NC subfields of GPRAR register ● Updated and corrected DCE interleaving supports identified in the recent non-power-of 2 interleaving architectural review of Ncore 3.8 <ul style="list-style-type: none"> ○ Corrected Figure 5-4, Figure 5-5, and Figure 5-11 ● Further clarified invalidating snoop handling in section 8.6 per discussed in [NCOR-760] and [CONC-16847] based on ARM support ticket No. 03506229 ● Merged in non-coherent Exclusive support per identified in [CONC-13774] <ul style="list-style-type: none"> ○ Added section 4.12.3.1 to merge in DII exclusive support ○ Added section 4.12.3.2 to merge in DMI exclusive support ● Cleaned up AMBA AXI/ACE specification reference throughout the entire specification to be version H.c per clarification required in [CONC-17032] since the differences between version H and H.c are mainly typo corrections and terminology updates <ul style="list-style-type: none"> ○ Checked CHI specification reference to be consistent with version B and E.c throughout the entire specification. 	
1.02	HL	<ul style="list-style-type: none"> ● Added two new flow diagrams Figure 4-25 and Figure 4-26 to show how an Evict is handled by a CHI or an ACE processor as per discussed in [CONC-16846] ● Clarified further in section 4.14.2 on the limitations of Atomic support of PCIe in section per discussed and identified in [CONC-16890] ● Added more clarification in section 4.14.3.1 to further clarify on how Atomic transaction for coherent accesses per discussed in [CONC-16965] ● Added more clarification in section 4.14.3.2 to futher clarify the ordering point condition for Atomic transaction for non-coherent accesses per discussed in [CONC-16962] ● Updated error handling in section 8.6 for Non_Data_ERROR received for a CHI agent per identified in [NCOR-760] and [CONC-16847] ● Added the missing “interface checker error” as an uncorrectable error to IOAIU in Table 8-15 per identified in [CONC-16861] 	4/25/2025
1.01	HL	<ul style="list-style-type: none"> ● Further confirmed WRAP transaction usage added in version 0.79 and stated that wrap transaction is still required to support because it is used in Atomics transactions ● Updated Figure 4-31 and Error! Reference source not found. based on the latest data books version 6.30a released from Synopsys in March 2025 	3/31/2025

Version	Editor	Change	Date
1.00	HL	<ul style="list-style-type: none"> Set the release version to 1.00 to sync up with product release Added a foot note in section 14.1.3 to clarify that the interleaving configuration is applicable to both regular memory spaces and the boot space per discussed in [CONC-15334] Fixed an error in Table 9-4 particular for check_2 as reported in [CONC-16568] 	3/20/2025
0.80	HL	<ul style="list-style-type: none"> Updated the error reporting for Atomic transactions based on ARM recommendation in section 8.6 per discussed in [CONC-12609] Corrected and clarified on the system event enabling, handling and usage in section 6.3 per discussed in [CONC-16572] Added a new flow diagram as illustrated in Figure 4-17 Write Stash Partial Accept Flow when the Target Cache was in Invalid State just to make the flow diagrams more complete Removed a redundant Figure 4-7 and corresponding descriptions since it is the same as that of Figure 4-4 Read with snoop data per identified in [CONC-16514] Corrected DVE RPN assignment offset in Table 5-1: RP assignment to Ncore Components per identified in [CONC-16514] Updated Table 9-4: BIST FSM to align with Table 1 of FSC micro-architecture version 1.0 per described in [CONC-16568] 	2/28/2025
0.79	HL	<ul style="list-style-type: none"> Also added clarifications in section 10.4 on how Q-channel correlates with “external’ clock-gating option discussed in [CONC-16396] Added Figure 4-32 in section 4.14.2 to show how asynchronous and data width adapters are connected for an PCAIU configuration per discussed in [CONC-16396] Clarified WRAP transaction usage of the OWO support in section Updated the constraint/limitation for ACE in section 2.2.2 of Ncore per described in [CONC-15999] Updated and merged in opcodes used in trace in section 12.2.1.6 and section 12.2.1.7 per identified in [CONC-15183] Fixed a few reference errors and typos in the specification 	1/31/2025
0.78	HL	<ul style="list-style-type: none"> Merged in an earlier update in Figure 4-34 and Figure 4-35. Updated the corresponding descriptions in section 4.14.3.1 per aligned in [CONC-15687] to remove UPDReq in the coherent write flow and per notified later by [CONC-16216] Further updated and completed the review feedback per identified in [CONC-16120] <ul style="list-style-type: none"> On supported interfaces in section 1.2.7 On supported DVM versions and their corresponding properties in Table 1-2: DVM version support 	12/30/2024
0.77	HL	<ul style="list-style-type: none"> Updated Table 1-2: DVM version support for Ncore 3.7 [CONC-16120] 	12/20/2024

Version	Editor	Change	Date
		<ul style="list-style-type: none"> Updated the list of supported interface in section 2.2.3 per identified in [CONC-16120] Replaced ACE-Lite E by ACE5-Lite per identified in [CONC-16120] <ul style="list-style-type: none"> In section 1.2.1 Compliance In section 2.3.1 Multi Ported NCAIU In Figure 2-2 Multi ported NCAIU In section 4.6 System Cache Table 8-14 CmStatus to Native interface mapping Figure 12-1 Trace and Debug Overview Corrected a typo in Figure 5-9 from RFAR to RTAR per identified in [CONC-16016] 	
0.76	HL	<ul style="list-style-type: none"> Updated Table 1-3 and Table 1-4 for relevant PRDs and TSRs with Benard Bonardi's helps Updated Table 9-3 in section 9.4 and relevant descriptions on Mission and Latent fault handling per discussed in [CONC-15867] and [CONC-15700]. Also updated Figure 9-6 to be in-sync with what we have implemented in Ncore Removed deprecated PCIe handling section since it is totally obsolete 	11/27/2024
0.75	HL	<ul style="list-style-type: none"> Updated Table 4-39 to reflect the property driven approach for DVM handling per described in [CONC-14944] 	11/15/2024
0.74	HL/BH	<ul style="list-style-type: none"> Added asynchronous clock domain crossing supports for both CHI interface and PCAIU in section 1.2.2 per described in [CONC-15496] Updated to not support clock gater for SRAM in section 10.3 as per described in [CONC-15496] Added the Interface Checker Error codes for AXI/ACE/ACE-Lite/ACE-LiteDVM for IOAIU in Table 8-12 per requested in [CONC-15471] and [CONC-15496] Took out check_type support for AXI4, ACE and ACE-Lite and added AXI5 after the group discussion held on September 27, 2024 by following ARM property driven approach Added error handling for skid buffer if it is implemented with SRAM as identified and requested in [CONC-15488] <ul style="list-style-type: none"> Updated Table 8-11 with two new correctable error types related to skid buffer if implemented in SRAM Updated Table 8-12 with two new un-correctable error type related to skid buffer if implemented in SRAM Corrected a couple of typos in section 4.14.3 and in Figure 4-35 per identified in [CONC-15551] Added and clarified the following CSR registers per identified in [CONC-15409] <ul style="list-style-type: none"> Added a new section 4.4.5 with eight tables from Table 4-10 to Table 4-17 for the CSR registers related to proxy cache functionalities 	10/4/2024

Version	Editor	Change	Date
		<ul style="list-style-type: none"> ○ Added a new section 4.6.1 with seventeen tables from Table 4-18 to Table 4-33 for system memory cache operations and control ○ Added a new section 5.3.1 with two tables from Table 5-7 to Table 5-8 for memory interleaving configurations ○ Added a new section 5.4.6.1 with three tables from Table 5-9 to Table 5-11 for address translation and relocation configurations ○ Added a new section 5.5 with three tables from Table 5-15 to Table 5-17 for boot region address definition ○ Added two tables from Table 6-7 to Table 6-8 for the system event handshake time-out control ○ Added Table 7-2 for QoS control ○ Added Table 8-17 for time out error control ○ Added Table 8-18 for SysCo time out error control ○ Added Table 14-1 and Table 14-2 for coherency attached transition and control ○ Added Table 14-3 for the control of snoop enable of DCE/DVE ● Added captions for the tables from Table 8-1 to Table 8-12 for the ease of future tracking and updates. Re-generated all the indexes for table of contents, table of figures and table of tables to reset baselines for future updates 	
0.73	HL	<p>The following updates are sync-up updates from 3.6.x</p> <ul style="list-style-type: none"> ● Added the missing handling on SnpStshShd and made it as a non-invalidating snoop in section 8.6 after a group discussion with the design team and made necessary updates per discussed in [CONC-15335] ● Corrected SnpStshUnq from an invalidating snoop to be a non-invalidating snoop in section 8.6 in the same group discussion with the design team per discussed in [CONC-15335] ● Corrected transaction flow diagrams Figure 4-4, Figure 4-22 and Figure 4-23 as per described in [CONC-15514] 	9/26/2024
0.72	HL	<p>The following updates are sync-up updates from 3.6.x</p> <ul style="list-style-type: none"> ● Added section 4.15 to clarify and define Ncore handling on Stash target is Not identified and Illegal Stash target per discussed in [CONC-15363], [CONC-15364] and [CONC-14819] ● Added a new diagram Figure 4-15 to show the write stash flow with no stash target is identified as per requested in [CONC-15363] ● Added a new diagram Figure 4-21 to show the read stash flow with no stash target is identified but cache line is cached per requested in [CONC-15364] 	9/20/2024
0.71	HL	UPDATED <ul style="list-style-type: none"> ● Table 4-39 to remove ACE support on DVM v8.1 per described in [CONC-14944] 	9/13/2024

Version	Editor	Change	Date
		<ul style="list-style-type: none"> Updated Table 6-6 to make event interface configurable for CHI and ACE to be consistent with the current implementation and parameter specification per identified in [CONC-15265] Updated the following in section 2.6 per feedback received from Jean Philippe Loison and Ashley Stevens: <ul style="list-style-type: none"> Clarified the difference between a partition and a tile Further clarified the criteria to validate a tile and its replica Updated Figure 2-4 to include external IPs such as a CPU etc. can be also included in a tile as long as they satisfy the criteria of tiling 	
0.70	HL	<ul style="list-style-type: none"> Based on an internal review with Brian Huang, updated the following in section 4.14: <ul style="list-style-type: none"> Updated Error! Reference source not found. to add a missing connection from an IOAIU to the DVE Updated Figure 4-34 to comply CCMP state nomenclature and to identify the two phases in the same diagram Cleaned up Figure 4-35 to highlight out of order execution is allowed in the first phase and corrected that RBRreq is not needed for a MakeUnique transaction 	9/4/2024
0.60	HL	<ul style="list-style-type: none"> Based on the group review held on August 25, 2024, the following updates are made to tiling support in section 2.6: <ul style="list-style-type: none"> Added a new diagram to show how Type-C tiles look like Added more clarifications to explain how a tile candidate can be validated as a tile or not Added subsection 2.6.6 to clarify the support scope for the first release of Ncore 3.7 Updated async and data width gasket usage in section 4.14 based on the agreement made on group discussion with both Maestro software and design team on August 30, 2024. Added the necessary description to support the removal of clock gater for the SRAM/memory instantiations across Ncore in section 10.3 per requested in [CONC-14362] 	8/30/2024
0.56	HL	<ul style="list-style-type: none"> Added no multi-port support for PCAIU configuration based on the group review feedback received on August 15, 2024 Updated and modified section 2.6 to further define the supports for tiling per requested in [NCOR-560][NCORPM-70] based on 2nd architectural review held on August 14, 2024 	8/16/2024
0.53	HL	<ul style="list-style-type: none"> Added section 9.6.1 to enable protection for AXI, ACE, ACE-LITE, ACE5-LITE and ACE-LITEDVM interfaces per requested in [NCOR-605] Added section 9.6.2 to enable protection for CHI-B interface per requested in [NCOR-543] 	8/12/2024

Version	Editor	Change	Date
		<ul style="list-style-type: none"> Updated and modified based on group view comments received on August 7th 2024, as reflected by the change bars Updated and modified section 4.14 based group review comments received on August 2nd 2024, as reflected by the change bars Updated and modified section 2.6 to further define the supports for tiling per requested in [NCOR-560][NCORPM-70] 	
0.52	HL	<ul style="list-style-type: none"> Updated FSC related registers in both Table 9-5 and Table 9-6 in section 9.5.3 to support as many as 160 error inputs and increase support on DMI units from 8 to 32 per requested in [CONC-12816] Added section 2.6 to describe the supports for tiling per requested in [NCOR-560][NCORPM-70] Modified multiple places in section 4.14 based on 2nd round of review comments from JeanPhilippe Loison on July 26 2024, as reflected by the change bars 	7/30/2024
0.51	HL	<ul style="list-style-type: none"> Updated in Table 4-34 to support WriteEvictOrEvict always with Evict rather than report an error with a potential to hang the transaction as per described in [CONC-14946] Revised and updated section 4.14 based on Eric Taylor's and Jean Philippe Loison's review comments marked by change bars Added back a missed update when system architecture specification version 0.7 was merged with supplement system architecture version 0.79. Updated accordingly in section 4.8.1.2 on how stash works per discussed in [CONC-13156], [CONC-14058] and [CONC-14033] Added section 2.4.2 to describe Mesh topology support and limitations per requested in [NCORPM-69] Added section 4.11.2.1.1 to support the usage of SRAM for the Overflow FIFO of the Skid Buffer per requested in [NCOR-249][NCORPM-118] 	7/25/2024
0.50	HL	<p>Added Ordered Write Observation feature support:</p> <ul style="list-style-type: none"> Updated section 2.2.3 to add a new configuration for PCAIU Completely updated section 4.14 with the system overview, up-to-date details of the 3rd party IP and ordering requirements per requested in [CONC-14926][NCORE-549][NCORPM-71]. Kept the older version for reference <p style="text-align: center;">CLARIFIED NCORE 3 CAPABILITIES WITH DIFFERENT VERSIONS OF DVM SUPPORTS IN</p> <ul style="list-style-type: none"> Table 4-39 per described in [CONC-14944] Clarified and cleaned up message type and different NCAIU configuration options in Table 3-12 per described in [CONC-14944] 	7/16/2024

Version	Editor	Change	Date
HL	Hao Luan		
BH	Brian Huang		
Xx	Whoever else edited this document		
		Blue colored text represents new features in Ncore 3.7 till they are finalized	

Confidential Proprietary Notice

This document is CONFIDENTIAL AND PROPRIETARY to Arteris, Inc. or its applicable subsidiary or affiliate (collectively or as applicable, "Arteris" or "Arteris IP"), and any use by you is subject to the terms of the agreement between you and Arteris IP or the terms of the agreement between you and the party authorized by Arteris IP to disclose this document to you.

This document is also protected by copyright and other related rights and the practice or implementation of the information contained in this document may be protected by one or more patents or pending patent applications. No part of this document may be reproduced in any form by any means without the express prior written permission of Arteris IP. **No license, express or implied, by estoppel or otherwise to any intellectual property rights is granted by this document unless specifically stated. You are prohibited from altering or deleting this notice from any use by you of this document.**

Your access to the information in this document is conditional upon your acceptance that you will not use or permit others to use the information: (i) for the purposes of determining whether implementations infringe any third party patents; (ii) for developing technology or products which avoid any of Arteris IP's intellectual property; or (iii) as a reference for modifying existing patents or patent applications or creating any continuation, continuation in part, or extension of existing patents or patent applications; or (iv) for generating data for publication or disclosure to third parties, which compares the performance or functionality of the Arteris IP technology described in this document with any other products created by you or a third party, without obtaining Arteris IP's prior written consent.

THIS DOCUMENT IS PROVIDED "AS IS". ARTERIS IP PROVIDES NO REPRESENTATIONS AND NO WARRANTIES, EXPRESS, IMPLIED OR STATUTORY, INCLUDING, WITHOUT LIMITATION, THE IMPLIED WARRANTIES OF MERCHANTABILITY, SATISFACTORY QUALITY, NON-INFRINGEMENT OR FITNESS FOR A PARTICULAR PURPOSE WITH RESPECT TO THE DOCUMENT. For the avoidance of doubt, Arteris IP makes no representation with respect to, and has undertaken no analysis to identify or understand the scope and content of, third party patents, copyrights, trade secrets, or other rights. This document may include technical inaccuracies or typographical errors. Arteris IP makes no representations or warranties against the risk or presence of same.

TO THE EXTENT NOT PROHIBITED BY LAW, IN NO EVENT WILL ARTERIS IP BE LIABLE FOR ANY DAMAGES, INCLUDING WITHOUT LIMITATION ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, PUNITIVE, OR CONSEQUENTIAL DAMAGES, HOWEVER CAUSED AND REGARDLESS OF THE THEORY OF LIABILITY, ARISING OUT OF ANY USE OF THIS DOCUMENT, EVEN IF ARTERIS HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

This document consists solely of commercial items. You shall be solely responsible for ensuring that any use, duplication or disclosure of this document complies fully with any relevant export laws and regulations to assure that this document or any portion thereof is not exported, directly or indirectly, in violation of such export laws. Use of the word "partner" in reference to Arteris IP's customers is not intended to create or refer to any partnership relationship with any other company. Arteris IP may

make changes to this document at any time and without notice. If any of the provisions contained in these terms conflict with any of the provisions of any click through or signed written agreement covering this document with Arteris IP, then the click-through or signed written agreement prevails over and supersedes the conflicting provisions of these terms. This document may be translated into other languages for convenience, and you agree that if there is any conflict between the English version of this document and any translation, the terms of the English version of the agreement shall prevail.

The Arteris IP name and corporate logo, and words marked with [®] or [™] are registered trademarks or trademarks of Arteris (or its subsidiaries) in the US and/or elsewhere. All rights reserved. Other brands and names mentioned in this document may be the trademarks of their respective owners. Please follow Arteris IP's trademark usage guidelines, available from Arteris IP upon request by emailing to contracts@arteris.com.

Copyright © 2020 Arteris Inc. or its applicable subsidiary or affiliate. All rights reserved.

Confidentiality Status

This document is Confidential and Proprietary. This document may only be used and distributed in accordance with the terms of the agreement entered into by Arteris IP and the party that Arteris IP delivered this document to.

Product Status

The information in this document is **Preliminary**.

Web Address

<http://www.arteris.com>

Table of Contents

I	Introduction.....	30
1.1	About	30
1.2	Features	31
1.2.1	Compliance	31
1.2.2	Ncore features	35
1.2.3	System/Chassis level features.....	36
1.2.4	List of features added to NCore version 3.2	36
1.2.5	List of features added to NCore version 3.4.....	37
1.2.6	List of features added to NCore version 3.6.....	37
1.2.7	List of key features added to NCore version 3.7.x	37
1.2.8	Known limitations in NCore version 3.7.1.....	38
1.3	Requirements	38
2	Ncore System description.....	42
2.1	Terminology.....	42
2.2	Ncore units	43
2.2.1	Agent Interface Unit (AIU)	43
2.2.2	Coherent-Agent Interface Units (C-AIU)	44
2.2.3	Non-Coherent Agents'- Agent Interface Units (NC-AIU also called IO-AIU)	44
2.2.4	Multi ported NCAIU	45
2.2.5	Distributed Coherency Engine (DCE)	46
2.2.6	Distributed Memory Interface (DMI)	46
2.2.7	Distributed IO Interface (DII)	47
2.2.8	Distributed Virtual Memory System Engine (DVE)	48
2.2.9	Global Register Block (GRB)	48
2.3	Ncore System organization.....	48
2.3.1	Multi-ported NCAIU description	50
2.4	Topology options.....	53
2.4.1	Crossbar	53
2.4.2	Mesh	53
2.5	Engineering version ID	53
2.6	Tiling	54
2.6.1	Methodology.....	54
2.6.2	Different types of Tiling	55
2.6.3	Criteria to create a tile	56

2.6.4	Handling of a tile(s) inside of an Ncore	57
2.6.5	Exceptions.....	57
2.6.6	Expected usage and limitations of support	58
3	Transport layer	58
3.1	Legato transport description.....	59
3.1.1	Attachment of Ncore units to CTF	61
3.1.2	Structure of the Terminal Block.....	62
3.2	Ncore Messaging over CTF	63
3.2.1	CCMP Message Formats.....	63
3.2.2	Concerto C Message Header.....	64
3.2.3	Packetized delivery of Concerto C messages.....	66
3.2.4	Formats of Concerto C Messages	66
3.3	CTF Messaging Interface	66
3.3.1	Transmission of Concerto C messages over CTF	67
3.3.2	SMI Interface signals	67
3.3.3	Mapping Messages to SMI fields	69
3.4	Ncore CDTI Network	70
3.4.1	CDTI Blocks.....	71
3.4.2	Mapping CDTI to SMI field	76
3.4.3	Mapping CDTI to ATP field.....	77
3.4.4	CDTI Connectivity	77
3.4.5	Connectivity mapping	77
3.4.6	Connectivity Optimization.....	82
3.5	Ncore CSTI Network	88
3.5.1	CSTI Blocks.....	88
3.6	Addressing in CTFs.....	88
3.6.1	Fabric Unit Identification	88
3.6.2	Message Target Identification.....	89
3.6.3	Message Initiator Identification	90
4	Protocol Layer.....	91
4.1	Introduction.....	91
4.2	Storage Classification	92
4.3	Coherency protocol features	93
4.3.1	Cacheline states	93
4.3.2	Supported coherency protocol classes	94
4.3.3	Elements of Coherency Management	94

4.4 Proxy cache	95
4.4.1 Proxy cache allocation and visibility policies.....	96
4.4.2 Transactions native to concerto	96
4.4.3 Proxy cache state transitions.....	98
4.4.4 Sharer promotion	101
4.4.5 Relevant CSR registers with proxy cache	103
4.5 Read data interleaving mode	105
4.5.1 Proxy cache	106
4.5.2 IOAIU.....	106
4.5.3 DMI.....	106
4.6 System cache	106
4.6.1 Relevant CSR registers.....	108
4.7 Transaction flows	111
4.7.1 Non-Coherent transactions	112
4.7.2 Coherent Read and CMO transactions	114
4.7.3 Coherent write transactions	120
4.7.4 Coherent atomic transactions	123
4.7.5 Stash transactions	124
4.7.6 Prefetch transactions	132
4.7.7 Evict transactions	133
4.7.8 Late response for a non-coherent write targets a Dll with an EWA attribute	134
4.8 CHI-E support	135
4.8.1 CHI-E Request bus.....	135
4.8.2 CHI-E Data bus	138
4.9 Response bus	138
4.10 DVM support	138
4.11 End to end credit.....	139
4.11.1 Previous Skid buffer architecture	140
4.11.2 Skid buffer optimization.....	142
4.11.3 Software Support (Maestro)	146
4.12 Exclusive monitor	146
4.12.1 Coherent Exclusive support	146
4.12.2 CHI-E Exclusive transaction support	148
4.12.3 Non coherent exclusive support.....	148
4.13 Constraint of Mixed Coherent and Non-coherent Transactions	152
4.14 PCI Express support and acceleration	152

4.14.1	The system view of PCIe acceleration	152
4.14.2	Assumptions and limitations	153
4.14.3	Function descriptions of the PCAIU configuration.....	158
4.14.4	Relevant PCIe information.....	163
4.14.5	Ordering Considerations.....	165
4.14.6	PCIe support forward looking architectural recommendations	167
4.15	Special handlings of cache stashing	167
4.15.1	Stash target not identified	168
4.15.2	Illegal Stash target	168
5	Addressing and Memory Regions	170
5.1	Ncore Register Space	170
5.1.1	Global Register Block (GRB)	171
5.1.2	Ncore CSR access security	175
5.2	General Purpose Address Space	176
5.3	Interleaving	177
5.3.1	Relevant CSR registers.....	177
5.4	Instance and Set Selection	178
5.4.1	Directory Interleaving	179
5.4.2	Snoop Filter, System Memory Cache and Proxy Cache	180
5.4.3	Distributed Memory Interface Selection	180
5.4.4	Distributed Coherency Engine Selection	181
5.4.5	Address hashing SecSubRows	181
5.4.6	Address Space Compaction	182
5.4.7	Definition of a Memory Address Map	185
5.5	Boot Region Address Space	188
6	System messages.....	190
6.1	SYSSreq and SYSSrsp Messages	190
6.1.1	SysReq Commands.....	193
6.1.2	Command CMStatus.....	193
6.2	SysCoReq Implementation	194
6.2.1	System Architecture	195
6.2.2	Attach/Detach Protocol.....	196
6.2.3	SysCo Engine at Initiator Agent.....	197
6.2.4	SysCo Engine at Coherency Agent.....	199
6.3	Event Propagation	201
6.3.1	Event Messaging Architecture	202

6.3.2	Event Sender	204
6.3.3	Event Receiver.....	205
6.3.4	Event Broadcaster	208
7	Quality of service (QoS)	210
7.1	Fields related with QoS	210
7.2	Starvation Avoidance	211
7.3	Starvation Detection:	211
7.3.1	Starvation Handling:	212
7.4	NCore 3 Unit Functionalities	212
7.4.1	IOAIU.....	212
7.4.2	CHI_AIU.....	212
7.4.3	DCE.....	213
7.4.4	DVE	213
7.4.5	DMI.....	213
8	Error handling.....	215
8.1	Error registers.....	216
8.1.1	Correctable Error Registers	216
8.1.2	Uncorrectable Error Registers	218
8.1.3	Error Type and Information Summary	221
8.2	Native Interface Error Response Logging and Interrupt.....	224
8.3	Transport Error Logging and Interrupt	227
8.4	Resiliency Related Error Logging and Interrupt.....	227
8.5	Address Decode, Software Programming and Configuration Error Logging and Interrupt	232
8.6	CCMP Completion	233
8.7	Data Poisoning.....	237
8.8	Timeout Error.....	238
8.9	Sys event and SysCo Errors	238
8.10	Unsupported Message Type	239
8.11	Error Reporting in CMStatus.....	239
8.12	Interface Checker Error	239

8.13 CHI-E transaction error handling.....	239
9 Functional Safety.....	241
9.1 Functional Safety Features	242
9.2 Fault Checker	246
9.2.1 Architecture of fault checker used for duplicated units	246
9.3 Detectable internal fault conditions	248
9.3.1 SRAM protection	249
9.3.2 Transport protection	249
9.3.3 CSR register protection	250
9.3.4 Correctable Error Threshold	250
9.3.5 Memories	250
9.4 Mission and Latent Fault Causes	250
9.5 Functional Safety Controller.....	251
9.5.1 Feature List	251
9.5.2 BIST FSM	252
9.5.3 Registers	254
9.6 Protections to the native interfaces	257
9.6.1 Odd parity check protection to NCAIU supported interfaces	257
9.6.2 Odd parity check protection to CHI-B interface.....	258
10 Power and Clock.....	259
10.1 Synchronization	260
10.2 Power Gating	260
10.3 Clock Gating.....	260
10.4 Q channel.....	261
11 Security	262
11.1 Non-secure bit of transactions	262
11.2 Non secure attribute of memory regions	263
11.3 Background: New Security states	264
12 Trace and Debug	265
12.1 Register offset.....	265
12.2 Detailed Description	265

12.2.1	Trace Trigger	266
12.2.2	Trace Capture	269
12.2.3	Trace Accumulate.....	272
12.3	Debug and BIST disable pin	273
12.4	Debug APB port	273
12.4.1	APB4 PPORT Usage Clarifications.....	274
13	Performance Monitoring	275
13.1	Parameters	275
13.2	Detailed Description	275
13.3	Register Definition.....	276
13.3.1	Counter Value Register (xCNTVR).....	276
13.3.2	Counter Saturation Register (xCNTSR)	276
13.3.3	Counter Control Register (xCNTCR)	276
13.3.4	BW Counter Filter Register (xBCNTFR)	277
13.4	Performance events.....	277
13.4.1	CAIU Performance events	277
13.4.2	NCAIU Performance events	278
13.4.3	Proxy Performance events.....	279
13.4.4	DMI Performance events	280
13.4.5	SMC Performance events.....	281
13.4.6	DII Performance events.....	282
13.4.7	DVE Performance events.....	283
13.5	Master Trigger	284
13.6	Bandwidth Counters.....	285
13.7	Latency Histogram Counters	286
14	System Software Guidelines	289
14.1	Reset and Initialization	289
14.1.1	Boot/Initialization.....	289
14.1.2	Ncore Component Discovery	290
14.1.3	Address space configuration	290
14.1.4	Error Detection and Reporting configuration	291
14.1.5	Proxy cache configuration	291
14.1.6	SMC configuration	291
14.1.7	Scratchpad configuration.....	292
14.1.8	CAIU Coherence transition mechanism	292

14.1.9 Snoop enabling configuration	293
14.2 Q channel clock gating sequence.....	294
15 PPA	295
15.1 Performance goals.....	295
15.2 Timing goals	296
15.3 Slow SRAM.....	296
16 Glossary.....	297
17 Document References	298
17.1 Supported standards and specifications	298
17.2 Relevant documents and specifications	298

Table of Figures

Figure 1-1 ANoc-HCS Block diagram	30
Figure 2-1 System Overview.....	50
Figure 2-2 Multi ported NCAIU.....	51
Figure 2-3 Multi-Ported NCAIU Wrapper	52
Figure 2-4 High Level View of Tiling.....	54
Figure 2-5 A Typical Type-C Tile Example Based on A Mesh Topology.....	56
Figure 3-1 Terminal block to terminal block path through the CTF	61
Figure 3-2 A CTF network offering multiple terminal blocks for connecting units.....	61
Figure 3-3 Ncore unit-to-unit path via the CTF	62
Figure 3-4 Structures of TX and RX Terminal Blocks.	63
Figure 3-5 Concerto C Message headers	65
Figure 3-6 TX and RX SMI interfaces.....	67
Figure 3-7 TX and RX SMI interfaces.....	67
Figure 3-8: CCMP communication through the CDTI	71
Figure 3-9: Internal Structure of WidthAdapter	74
Figure 3-10: Internal Structure of Rate Adapter	75
Figure 3-11: WidthAdapter with RateAdaptation.....	76
Figure 3-12: AIU to AIU connectivity	86
Figure 4-1: NC read transaction flow	112
Figure 4-2 NC write transaction flow	113
Figure 4-3 Non-coherent atomic transaction flow.....	114
Figure 4-4 Read with snoop data	115
Figure 4-5 Read with DMI data	116
Figure 4-6 Read Clean with snoop data	117
Figure 4-7 Clean with dirty snoop data	118
Figure 4-8 Invalidate transaction flow.....	119
Figure 4-9 Read when the Cache owner is in the unique partial state.....	120
Figure 4-10 Write unique transaction flow	121
Figure 4-11 CHI Coherent write transaction flow.....	122
Figure 4-12 ACE write back transaction flow	122
Figure 4-13 Coherent atomic transaction	123
Figure 4-14 Write stash full accept transaction flow.....	124
Figure 4-15 Write stash When The Stash Target Is Not Identified.....	125
Figure 4-16 Write stash decline transaction flow	126
Figure 4-17 Write Stash Partial Accept Flow when the Target Cache was in Invalid State	127
Figure 4-18 Write stash partial accept flow.....	128
Figure 4-19 Read stash decline flow.....	129
Figure 4-20 Read stash When The target Is Not Identified And The Cache Line Is Not Cached .	130

Figure 4-21 Read stash When The target Is Not Identified And The Cache Line Is Cached	130
Figure 4-22 Read stash accept flow with A Peer Cache Has Partial Dirty Data	131
Figure 4-23 Read stash accept flow with A Peer Agent Has a Clean Copy of the Cache line ...	132
Figure 4-24 Prefetch transaction flow	133
Figure 4-25 Evict Flow of A CHI-B/E based Processor	133
Figure 4-26 Evict Flow of An ACE-based Processor	134
Figure 4-27 Handling of A Non-coherent Write Targets A Dll with No Order and EWA Attribute .	135
Figure 4-28: Skid Buffer Overview	140
Figure 4-29: Skid Buffer as function of Depth	141
Figure 4-30: Skid Buffer Partitioning	142
Figure 4-31: The System View of PCIe Acceleration with One PCIe Interface	153
Figure 4-32: How Asynchronous and Datawidth Adapters are Connected	156
Figure 4-33: The Write Data Stream of a PCIe Transaction	159
Figure 4-34: THE TWO-PHASE FLOW CHART	160
Figure 4-35: THE TWO-PHASE FLOW TO HANDLE THE WRITE TRAFFIC TO THE COHERENT REGIONS	161
Figure 4-36: THE HANDLING FLOW OF NON-COHERENT WRITE TRAFFIC	162
Figure 5-1: NRS Structure	170
Figure 5-2: Address bit mapping	171
Figure 5-3 MIGS Options (Examples)	177
Figure 5-4: Memory and Directory Interleaving	179
Figure 5-5: Directory Interleaving	180
Figure 5-6: Memory Interleaving Group Register	181
Figure 5-7: Address Space Compaction	183
Figure 5-8: Matching Input address to ATR descriptor	183
Figure 5-9: Relocation to new Base Address	184
Figure 5-10: Layout of GP Address Space Descriptor	185
Figure 5-11: Example Address Map	188
Figure 6-1: SysCo Top Level Architecture	195
Figure 6-2: SysCo Flow	196
Figure 6-3: SysCo State Machine	198
Figure 6-4: Event Messaging	202
Figure 6-5: Event Sender - Interfaces	204
Figure 6-6: Event Sender FSM	205
Figure 6-7: Event Receiver Interface	205
Figure 6-8: Event Receiver Architecture	206
Figure 6-9: Event Receiver State Machine	207
Figure 6-10: Event Broadcaster Interface	208
Figure 6-11:Broadcaster FSM	209
Figure 7-1 DMI and DMC Connectivity	214
Figure 7-2 DMI Feedback Loop	215
Figure 9-1: Ncore 3 protection system level view	241
Figure 9-2a to 9-2c: New Wrapper configurations supported	243

Figure 9-3: Full Duplication applied	243
Figure 9-4: Optimized configuration for ASIL B.....	244
Figure 9-5: Ncore Unit View	245
Figure 9-6: Fault Checker UNIT	246
Figure 9-7: Fault Checker ND Unit	248
Figure 9-8: FSC top level block diagram.....	251
Figure 10-1 Power and Clock, Parent Child Relationship	260
Figure 10-2 Q channel PMA top-level view	261
Figure 12-1 Trace and Debug Overview	266
Figure 12-2 Trace DTW data build format.....	270
Figure 12-3 Counter sync feedback loop.....	271
Figure 12-4 Trace format.....	272
Figure 13-1 Latency Histogram block.....	287

Table of Tables

Table 1-1: CHI Evolution	33
Table 1-2: DVM version support	34
Table 1-3: LINKS TO SECTIONS THAT CAPTURE THE TECHNICAL ANSWERS TO THE PRDs	38
Table 1-4: LINKS TO SECTIONS THAT CAPTURE THE TECHNICAL ANSWERS TO THE TSRs.....	41
Table 3-1 SMI message NDP signals.....	68
Table 3-2 SMI message DP signals	69
Table 3-3: Insertion Rules for adapters	72
Table 3-4: SMI to Concerto Message Mapping	76
Table 3-5: ATP signal in the network	77
Table 3-6: System Control and Data Network Mapping	78
Table 3-7:Connectivity mapping.....	79
Table 3-8: CN0 TX RX Connectivity Map.....	80
Table 3-9: CN1 TX RX Connectivity Map.....	80
Table 3-10: CN2 TX RX Connectivity Map.....	80
Table 3-11: CN3 TX RX Connectivity Map.....	81
Table 3-12: DN TX RX Connectivity Map	81
Table 3-13: AIU DCE interleaving example.....	83
Table 4-1:Subset of protocol classes	94
Table 4-2: Cache allocation & visibility.....	96
Table 4-3: Cache lookup actions	96
Table 4-4: Non-coherent cache lookup actions	97
Table 4-5: Proxy cache DtrReq state transition.....	98
Table 4-6: Cache SnpReq state transitions.....	99
Table 4-7: Unique presence field	101
Table 4-8: DCE UP and MPF3 filed setting.....	102
Table 4-9: AIU UP action.....	103
Table 4-10 : Proxy Cache Transaction Control Register (xPCTCR)	103
Table 4-11 : Proxy Cache Transaction Activity Register (xPCTAR).....	104
Table 4-12 : Proxy Cache Initialization Status Register (xPCISR)	104
Table 4-13 : Proxy Cache Maintenance Control Register (xPCMCR)	104
Table 4-14 : Proxy Cache Maintenance Activity Register (xPCMAR)	105
Table 4-15 : Proxy Cache Maintenance Location Register 0 (xPCMLR0).....	105
Table 4-16 : Proxy Cache Maintenance Location Register 1 (xPCMLR1).....	105
Table 4-17 : Proxy Cache Maintenance Data Register (xPCMDR)	105
Table 4-18 : System Memory Cache Transaction Control Register (xSMCTCR)	108
Table 4-19 : System Memory Cache Transaction Activity Register (xSMCTAR)	108
Table 4-20 : System Memory Cache Allocation Policy Registe (xSMCAPR).....	108
Table 4-21 : System Memory Cache Initialization Status Register (xSMCISR).....	109
Table 4-22 : System Memory Cache Maintenance Control Register (xSMCMCR)	109

Table 4-23 : System Memory Cache Maintenance Activity Register (xSMCMAR)	109
Table 4-24 : System Memory Cache Maintenance Location Register 0 (xSMCMLR0)	109
Table 4-25 : System Memory Cache Maintenance Location Register 1 (xSMCMLR1)	110
Table 4-26 : System Memory Cache Maintenance Data Register (xSMCMDR)	110
Table 4-27 : System Memory Cache Scratchpad Base Address Register 0 (xSMCSPBR0)	110
Table 4-28 : System Memory Cache Scratchpad Base Address Register 1 (xSMCSPBR1)	110
Table 4-29 : System Memory Cache Scratchpad Configuration Register 0 (xSMCSPCR0).....	110
Table 4-30 : System Memory Cache Scratchpad Configuration Register 1 (xSMCSPCR1).....	111
Table 4-31: System Memory Cache Way Partitioning Control Register 0 (xSMCWPCR0).....	111
Table 4-32 : System Memory Cache Way Partitioning Control Register 1 (xSMCWPCR1).....	111
Table 4-33 : System Memory Cache Information Register (xSMCIFR)	111
Table 4-34:CHI-E request mapping.....	136
Table 4-35:Command request fields	137
Table 4-36:Snoop request fields	137
Table 4-37: Data Fields	138
Table 4-38: Responses fields	138
Table 4-39 DVM version capability	139
Table 4-40: Credit control field format	144
Table 4-41: Skid buffer size info register format	145
Table 4-42: CHI E Exclusive request mapping	148
Table 4-43: Monitor Update Required in a DII	150
Table 4-44: SMStatus Depending on The Success or Failure of the Exclusive Transaction	150
Table 4-45: Monitor Updates Required in A DMI.....	151
Table 4-43: AXI5 Features Supported by Synopsys Controller	157
Table 4-44: Supported PCIe Atomic Operations for A PCAIU.....	157
Table 4-45: ACE Lite Transactions – 3rd Party PCIe IP.....	157
Table 4-46: PCIe Ordering Rules Summary	163
Table 4-47: Expected PCIe Transaction to AXI mapping	164
Table 5-1: RP assignment to Ncore Components.....	171
Table 5-2: Coherent Subsystem Snoop Filter Identification Register	172
Table 5-3: NRR Identification Register	173
Table 5-4: Engineering ID Register	173
Table 5-5: NRR Unit Census Register	174
Table 5-6: NRR Subsystem Identification Register	174
Table 5-7 : Active Memory Interleave Group Register (xAMIGR)	177
Table 5-8 : Memory Interleave Function Select Register (xMIFSR)	178
Table 5-9 : Address Translation Enable Register (xATER)	184
Table 5-10 : Reallocate From Address Register (xRFAR)	184
Table 5-11 : Reallocate To Address Register (xRTAR)	184
Table 5-12: Aperture Base Registers	185
Table 5-13: Aperture High Registers.....	185
Table 5-14: Aperture Attribute Register.....	185

Table 5-15 : Boot Region Base Address Low Register (xBRBLR)	189
Table 5-16 : Boot Region Base High Address Register (xRBHHR)	189
Table 5-17 : Boot Region Attribute Register (xBRAR)	189
Table 6-1: Overview Ncore 3.0 Messaging	190
Table 6-2: SysReq Command Layout	191
Table 6-3: SysRsp Response Layout	192
Table 6-4: SysReq Command Operation Payload	193
Table 6-5: SysCmd and SysRsp Command status Field encoding	193
Table 6-6: Event Messaging Interfaces - Sources and Destinations	203
Table 6-7 : System Event Protocol Timeout Control Register (xSEPTOCR)	204
Table 6-8 : Event Handshake Timeout Control Register (xEHTOCR)	204
Table 7-1: System Parameters for QoS configuration.....	210
Table 7-2 : QoS Control register (xQOSCR).....	212
Table 7-3: DMI parameters for QoS configuration.....	214
Table 8-1: The Definition of the Correctable Error Control Register.....	216
Table 8-2: The Definition of the Correctable Error Status Register.....	216
Table 8-3: The Definition of the Correctable Error Location Register 0	217
Table 8-4: The Definition of the Correctable Error Location Register 1	217
Table 8-5: The Definition of the Correctable Error Status Alias Register	218
Table 8-6: The Definition of the Correctable Resiliency Threshold Register.....	218
Table 8-7: The Definition of the Uncorrectable Error Detect Register	218
Table 8-8: The Definition of the Uncorrectable Error Interrupt Register.....	219
Table 8-9: The Definition of the Uncorrectable Error Status Register	220
Table 8-10: The Definition of the Uncorrectable Error Status Alias Register	220
Table 8-11: The Definition of the Correctable Error Type and Information Register	221
Table 8-12: The Definition of the Uncorrectable Error Type and Information Register	221
Table 8-13: Native interface to CmStatus mapping	225
Table 8-14 CmStatus to Native interface mapping	226
Table 8-15 Uncorrectable Errors	227
Table 8-16 Correctable Errors	230
Table 8-17 : Timeout Control Register (xTOCR)	238
Table 8-18 : System Coherency Protocol Timeout Control Register (xSCPTOCR)	238
Table 9-1: Functional Safety Support.....	242
Table 9-2:Unit Errors.....	248
Table 9-3: Mission _Fault and Latent_Fault Signals Outputs Values.....	250
Table 9-4: BIST FSM	253
Table 9-5: Register's Address Map.....	254
Table 9-6: Register Overview.....	255
Table 9-7:FSCLFX Register Bit Assignment	255
Table 9-8: FSCMFX Register Bit Assignment.....	255
Table 9-9: FSCCETHFX Register Bit Assignment	255
Table 9-10: FSCBISTCR Bit Assignment	256

Table 9-11: FSCBISTAR Bit Assignment.....	256
Table 9-12: FSCERR Bit Assignment	257
Table 11-1: Trustzone implementation in each unit.....	262
Table 12-1: DtwRsp cm_status description	270
Table 12-2: Increment value examples.....	271
Table 14-1 : Transaction Activity Register (xTAR):.....	292
Table 14-2 : Transaction Control Register (xTCR):	293
Table 14-3 : Snoop Enable register (xSER)	293

Preface

This preface introduces the Arteris® Network-on-Chip Hierarchical Coherency Engine Architecture Specification.

About this document

This technical document is for the Arteris Network-on-Chip Hierarchical Coherency Engine Architecture. It describes the subsystems and their function along with the system's interactions with the external subsystems. It also provides reference documentation and contains programming details for registers.

Product revision status

TBD

Intended audience

This manual is for system designers, system integrators, and programmers who are designing or programming a System-on-Chip (SoC) that uses or intend to use the Arteris Network-on-Chip Hierarchical Coherency System (ANoC-HCS).

Using this document

TBD

Glossary

The Arteris® Glossary is a list of terms used in Arteris® documentation, together with definitions for those terms. The Arteris® Glossary does not contain terms that are industry standard unless the Arteris® meaning differs from the generally accepted meaning.

Typographic conventions

italic

Introduces special terminology, denotes cross-references, and citations.

bold

Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.

`monospace`

Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.

monospace italic

Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name. *monospace italic* Denotes arguments to monospace text where the argument is to be replaced by a specific value. *monospace bold* Denotes language keywords when used outside example code.

SMALL CAPITALS

Used in body text for a few terms that have specific technical meanings, that are defined in the Arteris® Glossary. For example, **IMPLEMENTATION DEFINED**, **IMPLEMENTATION SPECIFIC**, **UNKNOWN**, and **UNPREDICTABLE**.

Timing diagrams

The following figure explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.



Signals

The signal conventions are:

Signal level

The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW.

Asserted means:

- HIGH for active-HIGH signals.
- LOW for active-LOW signals.

Lowercase n

At the start or end of a signal name denotes an active-LOW signal.

1 Introduction

3 This chapter provides an overview of the Arteris Network-On-Chip Hierarchical Coherency Engine and its features.

6 1.1 About

9 The Arteris Network-On-Chip Hierarchical Coherency System (ANoC-HCS) is a high-performance, scalable, coherent NoC. It supports all types of traffics, including cache coherent, I/O coherent, and non-coherent traffic. It includes a transport layer and provides full state of the art cache coherency protocol layer to connect heterogeneous compute or IO nodes.

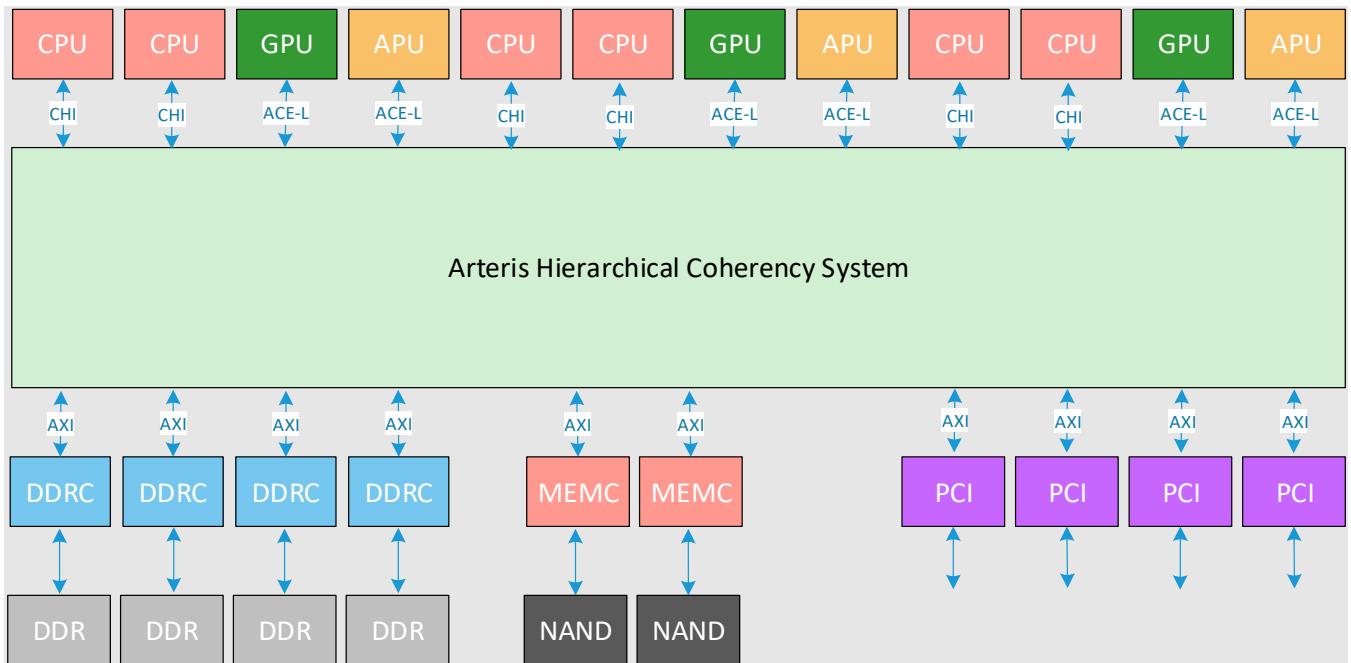


FIGURE 1-1 ANoC-HCS BLOCK DIAGRAM

15 The NoC is composed of various components, the cache protocol layer units are called Concerto units and the transport layer is also called CDN for control and data network. The NoC is highly configurable and the selected components depend of the SoC requirements.

18

1.2 Features

1.2.1 Compliance

21 Ncore 3.6 is compliant with the following interface standards, coherency architecture and related functionality.

It provides a native interface with CHI Protocol: Ncore 3.6 supports Arm AMBA 5 CHI Issue B and issue E¹ implementing the base features plus the following:

- 24
 - Distributed Virtual Memory (DVM) transactions
 - Exclusive transactions
 - Far Atomic operations
 - 27
 - Cache-stashing for data locality
 - Direct data transfer for latency
 - Separate Read Data and Comp Responses for direct memory transfer (DMT)
 - 30
 - Combined CompAck with WriteData
 - Data width option 128/256 bits
 - Up to 32 User bits (RSVDC field as User Placeholder)

33 does not support the following features:

- 36
 - Retry mechanism
 - Write stashes
 - CHI data check
 - Eviction of clean lines
 - Barrier transactions
 - 39
 - Big Endian support

Ncore 3.6 targets in particular the support of Arm V9a processors. For this purpose, Ncore 3.6 shall be functionally compatible implementing the required options of CHI-E protocol.

- 42
 - The following CHI-E features are supported:
 - o Emulation of new commands
 - o Emulation of combined commands
 - o Emulation of state change exclusives
 - The following CHI-E features are not supported:
 - o data source information
 - o stash group support
 - o persistence group support
 - o DBID order support

¹ CHI E refers to AMBA CHI Issue-E.c Specification

- 51
 - split transaction support
 - DVM updates (v8.4 and v8.5) – invalidate TLB by address range
 - MTE
- 54
 - MPAM

CHI-A support is deprecated in Ncore 3.6.

A mixed system with CHI-B and CHI-E is supported using Ncore 3.6.

- 57 The evolution of CHI features up to version E is shown in Table 1-1.

	A → B	B → C	C → D	D → E
Performance/ Protocol	<ul style="list-style-type: none"> ○ Retry Transaction ○ Forwarding Snoops ○ CleanSharedPersist ○ Data Stashing ○ Prefetch Req ○ Far atomics 	<ul style="list-style-type: none"> ○ Response after first Data packet ○ Separate Data-Only & Non-Data Response ○ Combined CompAck with WriteData ○ Persistent CMO 	<ul style="list-style-type: none"> ○ Persistent CMO with two-part response ○ Deep Persistent Cache Maintenance ○ OWO for WriteNoSnp 	<ul style="list-style-type: none"> ○ MakeReadUnique ○ Write with optional data ○ Write Zero with no data ○ Two-part Stash transactions ○ SnpQuery ○ DBIDRespReqOrd ○ Direct Write-data transfer ○ Combined Write and CMO ○ Combined Write and PCMO ○ MakeReadUnique with Exclusive access ○ SnpPreferUnique & SnpPreferUniqueFwd ○ Permitted Fwd-snoops to be handled as non-fwd snoop ○ Enhance Exclusive Read Transactions ○ SLC replacement hint <p>Responses</p> <ul style="list-style-type: none"> ○ StashDoneResp ○ CompStashDoneResp ○ CompCMOResp ○ TagMatchResp
Interface Changes			<ul style="list-style-type: none"> ○ Increased TXID width to 10 bits ○ Data Source Indication 	<ul style="list-style-type: none"> ○ Increased TXID width to 12 bits ○ Request Channel 7 bits (New transactions) ○ RSP Channel OpCode 5 bits (New Responses) ○ DBID increased to 12 bits (More buffers) ○ Multiple CHI interfaces per block ○ Replicating channels on single interfaces
ARM Architecture	<ul style="list-style-type: none"> ○ Armv8.1-A Large System Extensions ○ Improved virtualization ○ 52-bit physical address space 	<ul style="list-style-type: none"> ○ DVM enhancements (Arm v8.2) Change in Prefetch semantics (TgtID must be 0) 	<ul style="list-style-type: none"> ○ ICache Invalidation broadcast signal (DVM) ○ MPAM support added ○ CBusy (feedback for QoS) 	<ul style="list-style-type: none"> ○ MTE Support ○ DVM updates (v8.4 and v8.5) – invalidate TLB by address range ○ StashGroupID ○ TagGroupID

	A → B	B → C	C → D	D → E
RAS	<ul style="list-style-type: none"> ○ Data Poisoning ○ Data Check ○ Enables common error signaling, logging, and reporting 		<ul style="list-style-type: none"> ○ Persistance GroupID ○ Interface Parity 	

TABLE 1-1: CHI EVOLUTION

60 **It provides a native interface with AXI4/ACE/ACE-Lite/ACE5-Lite Protocols:** Ncore 3.6 supports Arm AMBA® AXI4 and ACE Protocol Specification issue E², implementing the following options:

- Data width option 64/128/256 bits
- Up to 32 User bits (User Placeholder)

63 does not support the following features

- Untranslated transaction identifiers
- Non-secure Access identifier
- Near Atomic transactions
- Barrier transactions
- Persist CMO write transactions
- Big Endian support
- burst limitation with native interfaces AXI, ACE-Lite, ACE5-Lite and ACE.
 - Narrow bursts are limited to only a single beat
 - Fixed bursts are not supported
 - Wrap non modifiable burst which cross 64-byte boundary are not supported
- ACE5-Lite StashOnceShared and StashOnceUnique are not supported for non-shareable domain
- ACE5-Lite data check and poison is not supported
- ACE5-Lite user loop-back is not supported
- ACE5-Lite low power signaling is not supported
- ACE5-Lite device and non-cacheable atomics are not supported

72 **With Distributed Virtual Memory:** Ncore 3 supports Arm's Distributed Virtual Memory architecture(DVMv8), including support for System MMUs (SMMUs), both Table Look-aside Buffer Unit (TBU) and Translation Control Unit (TCU). Ncore 3 does not perform conversion between DVMv8 and DVMv7 messages. As a result, if a system includes coherent agents capable of issuing DVMv8 transactions and coherent agents capable of receiving DVMv7 transactions, a bridge to translate DVMv8 transactions to DVMv7 transactions must be implemented. See the "Conversion from DVMv8 to DVMv7 format" section in the ACE specification for additional information. gives

² ACE5-Lite refers to AMBA AXI and ACE Protocol Specification TO (ARM IHI 0022H.c ID 12621)

⁸⁷ Table 1-2 lists the DVM versions and the corresponding architecture. A component that supports a specific version also support earlier version. The lowest common denominator is supported in the system.

TABLE 1-2: DVM VERSION SUPPORT

DVM version	Architecture	Corresponding ARM Supported Property	Supported Ncore 3 versions
7.xx	Armv7	N/A	3.0, 3.2, 3.4
8.0	Armv7 v8a	DVM_v8	3.0, 3.2, 3.4, 3.6, 3.7
8.1	Armv7 v8.1	DVM_v8.1	
8.2		No ARM supported DVM property	
8.3	Armv7 v8.3a, v9a	No ARM supported DVM property	
8.4	Armv7 v8.4, v9.0, v9.1	DVM_v8.4	3.6, 3.7
9.2	Armv7 v9.2	DVM_v9.2	

⁹⁰ **With Arm TrustZone:** Ncore 3 supports the Arm TrustZone technical security model by handling the security bit when the TrustZone is enable on the interface. It supports Arm TrustZone technology specification used by some Arm processors that run secure and non-secure operating system on the same core. Indeed, the secure vs. ⁹³ non-secure indication is propagated and stored throughout the Ncore 3 system.

⁹⁶ **With Arm access permission:** Ncore 3 supports legacy access permission signals. AxPROT[0] and AxPROT[2] are passed through within Ncore 3 for masters with AXI, ACE-Lite, ACE5-Lite, and ACE. In the case of CHI masters, the signal is tied off.

⁹⁹ **With Arm Q-channel:** Ncore 3 implements power management features with two levels of clock-gating and ARM Q-channel support. The implementation shall comply with the AMBA® Low Power Interface Specification issue C while the P-channel is not supported. The two levels of clock gating are configurable. The first level of clock gating shall turn on and off local clock and it can be enabled during the synthesis while the second level of clock gating shall turn on and off the clock for an entire unit and it can be enabled during the configuration creation via a parameter.

Ncore 3.6 support APB issue 4.

105 1.2.2 Ncore features

- Ncore 3 supports simultaneous coherent inter-operation of ACE based and CHI-based processors or accelerators via front-end interfaces units with its proprietary messaging protocol Concerto revision C
- Ncore 3 provides a generic memory interface via DMI unit
- Ncore 3 provides a generic interface to peripheral via DII unit
- Ncore 3 provides an optional system memory cache with the following functionalities:
 - Atomic Engine to perform atomic operations
 - Enhanced and flexible caching policies
 - Per-way SRAM mode for data arrays
 - Per-source way-reservation for allocation of data
- Ncore 3 supports an optional proxy cache at interface units for AXI, ACE-Lite and ACE5-Lite
- Ncore 3 provides Microarchitecture enhancements to fully support Producer-Consumer ordering across the system, offering optimized PCIe compatibility.
- Ncore 3 provides an efficient and high-performance transport interconnection (called Legato) for carrying Concerto C messages:
 - Low latency and high bandwidth
 - Deadlock-free routing of protocol messages
- Ncore 3 provides End-to-End Credit Management
- Ncore 3 also provides a dedicated transport interconnection solution for accessing Configuration and Status Registers in the system
- Ncore 3 provides a flexible address map facility
 - To enable the implementation of a “single system image” covering all storage spaces in the system
 - To access both coherent and non-coherent regions in the system
 - To support multiple non-contiguous address ranges, including those accessed non-coherently, to be mapped to a single memory controller
 - To offer optional programmable registers to specify the map, which enable the possibility to implement the system address map at run time.
 - To allow the physical address space to be packed to a smaller footprint allowing use of fewer address bits and reducing board space occupied by memory devices
- Support for System Event and Coherency Messaging
- Ncore 3 provides Quality of Service with up to 8 levels (QoS)
- Ncore 3 also provides a customized configuration option for a complete³ RISC-V based system:
 - Completely disabled DVM function throughout the Ncore

³ Complete implies that ALL processors that are connected to an Ncore are RISC-V based

141

- A new parameter will be introduced in Maestro configuration to disable DVM function and does not reserve any DVM related credits such as DVM snoop credits across all Ncore units
 - Once this parameter is enabled, an Ncore doesn't expect to see any DVM related transactions and it might have unexpected behavior if any DVM transaction is injected into the Ncore
- Mesh topology is supported with a maximum limit of 25 nodes
 - Ncore supports asynchronous clock domain crossing for CHI interface and PCAIU configuration

144

147

1.2.3 System/Chassis level features

Ncore 3 provides system/chassis level functionalities.

150 **Trace and debug:** Ncore 3 provides debug and trace features to allow to the customer to capture the Ncore 3 internal transactions. The functionalities below are supported:

- 1. Label: Identify and select transactions based on a set criterion like address, target etc.
- 2. Order: Identify temporal ordering of transactions, using a time stamp.
- 3. Capture: Take a snapshot of the labeled transaction.
- 4. Aggregate and access: Accumulate all captured transactions at a central location and provide SW access.
- 5. Analysis: Software is required to access the captured information and analyze it.

153 The debug and trace registers data shall be readable even if the system is hanged: a debug APB port is implemented to enable an alternate way to access all the Ncore 3 configuration and status registers.

159 **Performance monitoring:** Ncore 3 implements a performance monitoring framework and capabilities such as performance counters to determine the system performances. Performance counter units shall be added to the functional units (DCE, DVE, IOAIU, CHIAIU, DMI, DII blocks) and support tracking and reporting up to 31 events.

1.2.4 List of features added to NCore version 3.2

165

- Resiliency Enhancements:
 - Concerto mux enhancement: Adding missing bits into ECC calculation
 - Memory address protection
- CSTI network enhancement:
 - Limit CSTI access from CDTI initiator
- Processor Event support:
 - SysCo/SysAck messages
- Performance enhanced for PCIe traffic

168

171

1.2.5 List of features added to NCore version 3.4

- 174 - Support for security and coherency based on GPRS
 - o Security extension for the security level required to access GPR address regions
 - o GPRS Access through single CAIU
 - o Secure CSR update
- 177 - NCAIU capabilities:
 - o Multiport NCAIU support
 - o No interleaving on NCAIU data response
 - o NCAIU interleaving only at 64B boundaries
 - o NCAIU with proxy cache non-coherent access support
- 180 - Proxy cache capabilities:
 - o Owner transfer
 - o Sharer promotion
- 183 - DMI:
 - o WTT/RTT threshold available for better QoS
 - o Optional Read data interleaving support
- 189 - Performance statistics enhancement
 - o Periodic static collecting & reporting infra structure
 - o Transport layer optimization
 - o Periodic proxy cache statistics
 - o Filter statistics
- 192

1.2.6 List of features added to NCore version 3.6

- 195 - Support for CHI-E
- Support for non-coherent exclusive
- 198 - Support for slow SRAM

1.2.7 List of key features added to NCore version 3.7.x

- 201 - Added support on AXI5 and ACE5 interfaces
- Ordered Write Observation (OWO) to accelerate PCIe traffic
 - o Details are described in section 4.14
- 204 - Support mesh topology
 - o Details are described in section 2.4.2
- Skid buffer overflow buffer area optimization with the usage of SRAM
 - o Details are described in section 4.11.2.1.1
- Added odd parity check for AMBA 5 AXI, ACE5, ACE5-Lite, ACE5-LITEDvm interfaces
 - o Details are described in section 9.6.1
- 210 - Added odd parity check for CHI-B interface

- Details are described in section 9.6.2

1.2.8 Known limitations in NCore version 3.7.1

- 213 - For the non-coherent writes issued from a CAIU that target to a DII, when they are set as in “No Order” mode and with an EWA attribute, late responses are always enforced for those transactions where Vz is always set for those command requests when they leave a CAIU as shown in Figure 4-27
- 216 ○ It implies that a DII needs to pass on the EWA attribute to the downstream subordinate or an interconnect
- 219 - Start to limit the supported combinations among policy and ReadID/WriteID values as described in section 5.4.7.1

1.3 Requirements

TABLE 1-3: LINKS TO SECTIONS THAT CAPTURE THE TECHNICAL ANSWERS TO THE PRDs

PRD name	Link to section
NCR37-PRD-267 CHI Protocol Support	Compliance
NCR37-PRD-268 AXI4/ACE4/ACE5-Lite AIU Support	Compliance
NCR37-PRD-245 AXI AIU with Proxy Cache	Proxy cache
NCR37-PRD-246 DII and internal non-coherent connectivity	Distributed IO Interface (DII)
NCR37-PRD-225 Support of Flexible Coherent Memory Map	General Purpose Address Space
NCR37-PRD-224 System Clock target Frequency of 1.6GHz	Timing goals
NCR37-PRD-282 Power Management features	Power and Clock
NCR37-PRD-288 Debug and Trace Features	Trace and Debug
NCR37-PRD-290 Performance Monitoring Feature	Performance Monitoring
NCR37-PRD-226 System Memory Cache Capabilities into Ncore	System cache
NCR37-PRD-247 Read Data Forwarding into Ncore	Transaction flows
NCR37-PRD-275 Support for different data widths	Topology options Width Adapters
NCR37-PRD-294 Separate Data and Virtual Address Table Coherency	Distributed Virtual Memory System Engine (DVE)
NCR37-PRD-279 Ncore Security features	Security
NCR37-PRD-296 Optimized Coherent Interconnect Transport Fabric aka Legato	Legato transport description
NCR37-PRD-243 Distributed Memory Interface unit (DMI)	Distributed Memory Interface (DMI)
NCR37-PRD-244 QoS support in Ncore	Quality of service (QoS)
NCR37-PRD-297 Increase CAIU, IOAIU & DMI outstanding transactions amount	Performance goals
NCR37-PRD-271 PCIe ordering changes	PCI Express support
NCR37-PRD-287 Coherency requests support for power down	Attach/Detach Protocol
NCR37-PRD-277 Exclusive events reporting	Event Messaging Architecture
NCR37-PRD-298 Error handling feature enhancement	Error handling
NCR37-PRD-278 Increase of CHI-AIU and AXI-AIU units user bit limit	Compliance
NCR37-PRD-300 SRAM address protection	SRAM protection
NCR37-PRD-299 Limiting CSR access to one unit	Ncore CSTI Network
NCR37-PRD-233 Proxy cache AXI AIU interleaving only at 64 Byte boundaries	Read data interleaving mode

PRD name	Link to section
NCR37-PRD-234 Proxy cache support for owner transfer	Owner ship transfer
NCR37-PRD-235 Proxy cache support for sharer promotion	Sharer promotion
NCR37-PRD-236 AXI AIU with proxy cache non-coherent access support.	Proxy cache
NCR37-PRD-237 Multi-ported AXI AIU implementation support	Multi-ported NCAIU description
NCR37-PRD-238 Support for DMI WTT/RTT threshold	DMI Threshold support
NCR37-PRD-292 Support for performance monitors	Performance events
NCR37-PRD-239 No interleaving on AXI AIU data responses	Read data interleaving mode
NCR37-PRD-281 Support for security and coherency based on configuration register bit values	Definition of a Memory Address Map
NCR37-PRD-265 Connectivity interleaving	Removing connectivity
NCR37-PRD-264 Software credit management and skid buffer optimization	End to end credit
NCR37-PRD-241 Read/ Write dependency downstream the SMC to be removed to comply with standard	Read data interleaving mode
NCR37-PRD-266 Width and Rate adapter updates	CDTI Blocks
NCR37-PRD-242 Clock Domain Crossing on SMI and APB interfaces	Adapters automated insertion support
NCR37-PRD-273 CHI issue E compliance	CHI-E support
NCR37-PRD-276 Non-Coherent Exclusive monitor support	Non coherent exclusive support
NCR37-PRD-301 System Clock target Frequency of 1.6GHz or 1.3GHz in case of automotive project.	Timing goals
NCR37-PRD-302 Support event messaging as per arm spec for CHI + Ace/ ACE5-Lite	Event Messaging Architecture
NCR37-PRD-303 Hashing support	Address hashing SecSubRows
NCR37-PRD-304 Replacement policy for SMC, Proxy-cache and Snoop Filter	System cache
NCR37-PRD-305 Design for Functional Safety enhancements	Functional Safety Features
NCR37-PRD-306 APB issue 4 support	Compliance
NCR37-PRD-307 CCMP bandwidth enhancement	CDTI Connectivity
NCR37-PRD-323 Ncore Product Version register update	Refer to section 5.1.1.6
NCR37-PRD-324 Write Data to be forwarded downstream the DMI AXI	DMI microarchitecture
NCR37-PRD-325 Product design and Engineering processes shall comply with ISO-26262 standard requirements	Not Applicable
NCR37-PRD-326 AXI ID generation based on address bits	Refer to DII Micro architecture specification
NCR37-PRD-328 FMEDA export for custom automotive configuration	Not Applicable
NCR37-PRD-330 Ncore 3 mesh topology support	Refer to section 2.4.2
NCR37-PRD-331 Ordered Write Observation (OWO) support	Refer to section 4.14
NCR37-PRD-332 Ncore 3 support for arm plus RISC-V processors and Server market	Refer to section 1.2.1 and 1.2.2
NCR37-PRD-333 Subchip reuse support	Refer to section 2.6

225

TABLE 1-4: LINKS TO SECTIONS THAT CAPTURE THE TECHNICAL ANSWERS TO THE TSRs

TSR ID	Description	Link to section
NCR37-TSR-57 NCR37-TSR-58 NCR37-TSR-59 NCR37-TSR-72 NCR37-TSR-73 NCR37-TSR-74	Memory, Transport and External interface ECC and parity logic shall be testable with a coverage $\geq 90\%$	Functional Safety
NCR37-TSR-65 NCR37-TSR-66 NCR37-TSR-67 NCR37-TSR-68 NCR37-TSR-69 NCR37-TSR-70	Snoop Filter, Proxy Cache and System Level Cache memories address and data shall be protected by Parity	SRAM protection
NCR37-TSR-47 NCR37-TSR-48 NCR37-TSR-50 NCR37-TSR-51 NCR37-TSR-54 NCR37-TSR-55	Snoop Filter, Proxy Cache and System Level Cache memories address and data shall be protected by ECC	SRAM protection
NCR37-TSR-83	Lock Steps Latent	Functional Safety
NCR37-TSR-85	Timeout Latent	Detectable internal fault conditions
NCR37-TSR-45 NCR37-TSR-60 NCR37-TSR-46 NCR37-TSR-61 NCR37-TSR-49 NCR37-TSR-62 NCR37-TSR-52 NCR37-TSR-63 NCR37-TSR-77 NCR37-TSR-79	Functional unit shall be duplicated and output continuously compared	Functional Safety Controller
NCR37-TSR-64 NCR37-TSR-71	Transaction internally exchanged between agents or between agents and external associated units shall be protected by using parity	Transport protection
NCR37-TSR-53 NCR37-TSR-56	Transaction internally exchanged between agents or between agents and external associated units shall be protected by using ECC	Transport protection

TSR ID	Description	Link to section
NCR37-TSR-75	Configuration Registers Readback	Ncore CSTI Network
NCR37-TSR-76	Configuration Registers Protection	CSR register protection
NCR37-TSR-78	TP Timeout	Transport protection
NCR37-TSR-82	Fault Reporting Logic	Fault Checker
NCR37-TSR-84	Fault Reporting BIST	Fault Checker
NCR37-TSR-80	Debug & Trace, BIST and APB port shall be isolated to be protected against unattended activation	Debug and BIST disable pin
NCR37-TSR-81		
NCR37-TSR-87		

2 Ncore System description

228 An Ncore 3 system is comprised of a collection of specialized, parameterizable, and configurable soft digital function blocks, connected via a fabric providing a light-weight transport protocol.

This chapter describes the structure of an Ncore 3 system.

231 2.1 Terminology

234 To provide coherency and other storage access services to the components of an SoC, an Ncore 3 system implements a proprietary protocol, called **Concerto C Messaging Protocol (CCMP)**. This protocol is implemented via a set of messages exchanged between the various specialized function blocks that are the components of the Ncore 3 system. These blocks are called the Ncore 3 units.

237 Certain of Ncore 3 units, in addition to being connected to other Ncore 3 units also embody one or more additional interfaces to which components in the SoC, referred to as “external agents,” may connect to access the services of the Ncore 3 system. An external device that can originate a request, such as a storage access, into the Ncore 3 system is referred to as a “requester agent,” an “initiator agent,” or simply, an “agent.” An external device to which an Ncore 3 unit might transmit a request is referred to as a “target device,” or simply a “target.”

243 An agent or target device is expected to have one or more “native” interfaces by which it and the Ncore 3 system communicate with each other. A single native interface may be comprised of multiple transmit or receive sub-interfaces (from the point of view of the device). Associated with a native interface is the “native protocol,” which describes the rules of exchange of information over the interface. A unit of communication exchanged over the native interface is referred to as a “transaction.”

249 A single request transaction from an external agent translates into a sequence of CCMP messages internal to the Ncore 3 system plus additional transactions on external interfaces, as necessary.

CCMP messages are carried over an underlying light-weight, packetized transport interconnect, called the **Concerto Transport Fabric (CTF)**. The interconnection fabric itself is oblivious of the message contents and their semantics. The transport fabric and all the Concerto C units connected via this fabric are henceforth referred to in this document as the **Concerto C Protocol Domain**. The protocol domain represents the totality of hardware elements that participate in the CCMP, both in terms of transporting its messages and of taking action based on them, thus being subject to CCMP semantics. When reference is specifically in relation to coherency, the protocol domain is also referred to as the **coherency domain**.

Storage in an SoC is classified either as **system memory** or **peripheral storage**. System memory refers to the general-purpose bulk memory, often implemented via DDR DRAM or SRAM in modern computer systems, used to store program code and data. Ncore 3 system enables access to system memory via specialized interfaces and ensures maintenance of coherence for those accesses when so demanded. Peripheral storage, on the other hand, is storage in the system that includes peripheral device based storage, particularly such as control and status registers. Because of its nature, coherency protocols cannot be applied to such type of storage.

Peripheral storage also is subject to different access ordering rules than coherent storage. For this reason, in Ncore 3, peripheral storage is accessed via a separate specialized interface.

Although this interface also supports connectivity to SRAMs and DDR DRAM, data residing in them cannot be accessed coherently.

2.2 Ncore units

The following is the list of types of Ncore 3 units and a short description of the function each type serves.

2.2.1 Agent Interface Unit (AIU)

AIUs offer means of connecting request originating agents into an Ncore 3 system. An AIU externally connects to an agent via an industry standard native interface. Internal to the Ncore 3 system, it connects to multiple other Ncore 3 units.

An AIU's primary purpose is for protocol translation from agent's native to Concerto C. The unit communicates with the external agent using its native protocol. The AIU embodies all the necessary functionality to support the native protocol. A request transaction causes the AIU to initiate a Concerto C message sequence to realize the semantic intent of the transaction.

An AIU can handle both coherent and non-coherent accesses to system memory and non-coherent accesses to peripheral storage.

285 Each AIU implements the System Address Map specified for the SoC. There can be more than one type
of AIU in an Ncore 3 system.

2.2.2 Coherent-Agent Interface Units (C-AIU)

288 Ncore 3 offers C-AIUs to connect coherent agents into the system, typically individual processor or
processor clusters, which include internal cache hierarchies. Each C-AIU offers one native interface to
which an agent can be attached. A C-AIU supports one of the following three types of interfaces:

- 291 • ACE: ACE-AIU offers an ACE native interface to connect compatible processors and processor
clusters which include coherency-capable cache hierarchies into the Ncore 3 coherency
system.
- 294 ○ Ncore doesn't support a ReadOnce transaction that crosses a cache line boundary
- 297 • CHI-B: CHI-B-AIU offers a CHI-B native interface to connect compatible processors or processor
clusters which include coherency-capable cache hierarchies into the Ncore 3 coherency
system.
- 300 • CHI-E: CHI-E-AIU offers a CHI-E native interface to connect compatible processors or processor
clusters which include coherency-capable cache hierarchies into the Ncore 3 coherency
system.

For maintaining coherency over caches internal to the agent, a C-AIU is equipped with logic to snoop
the agent via its native interface.

303 A C-AIU can handle both coherent and non-coherent accesses to system memory and to peripheral
storage that might be issued by its agent.

2.2.3 Non-Coherent Agents'- Agent Interface Units (NC-AIU also called IO-AIU)

306 Ncore 3 offers AIUs to connect non-cache coherent agents, i.e., those that either don't have internal
caches or have internal caches but whose contents are not required to be maintained coherent with
respect to the backing store. This type of devices is also referred to herein as peripheral or IO devices.
309 Thus, the AIU that support such devices is referred to as an NC-AIU or IO-AIU. A single NC-AIU can
provide connectivity into the system to one or more peripheral or IO agents.

312 Each NC-AIU offers one native interface to which an agent can be attached. An NC-AIU supports one of
the following types of interfaces:

- 315 • AXI-4: AXI-AIU offers an AXI-4 native interface to connect to one or more non-coherent agents.
- Can be configured with OWO (Ordered_Write_Observation property) -PCAIU for PCIe
traffic acceleration
- AXI-5: AXI-AIU offers an AXI-5 native interface to connect one non-coherent agent

- 318 ○ Can be configured With OWO (Ordered_Write_Observation property) -PCAIU for PCIe
traffic acceleration

- 321 ● ACE-Lite:ACE-Lite-AIU offers an ACE-Lite native interface to connect to one or more non-coherent agents.
- 321 ● ACE5-Lite:ACE5-Lite-AIU offers an ACE5-Lite native interface to connect to one or more non-coherent agents.

324 While the peripherals or IO agents themselves are non-cache coherent, their accesses may pass through a System Memory Management Unit block (SMMU), which authenticates and translates requests initiated by agents. The SMMUs may cache copies of the address translation entries that are stored in the main memory of the system. As such, these copies may be required to be maintained coherent using a special coherency protocol that is usually part of the main cache coherency protocol of the system. Maintaining copies of these translation entries involves snooping the SMMUs via the same interface by which the peripheral devices connect into the system. ACE-Lite and ACE5-Lite interfaces and their associated protocols have this functionality, which the corresponding NC-AIUs also enable.

333 During the run time, a NC-AIU can be configured with a CSR to adjust the read or write reservations for the OTT to balance the traffic so to improve the overall performance.

336 An NCAIU with an AXI interface may also be configured to include a proxy cache that can enable non-coherent accelerators to enable more efficient cache coherent data exchanges with native coherent agents, details are described in section 4.4.

339 To further accelerate PCIe traffic for the data center related applications, a customized configuration of NC-AIU can be selected during the Ncore build time to improve the support and sustain the throughput for PCIe generation 5 and beyond. Details are described in section 4.14.

342 ACE5-Lite interface can be configured as an ACE5-LiteDVM interface and only as a bidirectional agent, which can generate and receive DVM messages. Also, the address width must be 44 bits or bigger to support ARM DVM v8.4 features.

There can be zero or more NC-AIU units of each type in an Ncore 3 system. Different configuration might have different timing and area impacts such as the following:

- 345 ● The area of a NC-AIU with a proxy cache can be much bigger than one without it. Also, the maximum running frequency can be lower for a NC-AIU with a proxy cache configuration.
- 345 ● The area of a NC-AIU with an ACE interface can be bigger than one with an AXI interface.

348 2.2.4 Multi ported NCAIU

351 Multi ported NCAIU can have multiple identical native interfaces in power of 2s and a single SMI protocol transport connection (the number of SMI ports are determined by number of networks in the system). The Ncore 3 system sees the multi ported NCAIU as a single Ncore 3 unit. Following limitation applies to multi ported NCAIU:

- 354
- DVMs are not supported.
 - Each port is address interleaved and must be identical.
 - Individual powering down of ports is not supported.
 - Proxy cache supports a max size of 1MB per port

357 It is architected as a wrapper around a single NCAIU core that is replicated.

2.2.5 Distributed Coherency Engine (DCE)

Cacheline copies are kept coherent by one or more **Distributed Coherence Engine Units (DCEs)**.

360 Each cacheline address is associated with a single DCE, known as the **Home DCE** for that cacheline address. The Home DCE acts as the point of serialization for, and enforces coherence on, the given cacheline address. The **serialization point** refers to the point at which coherent accesses from all agents to a given address are serialized, establishing a **coherence order** for that address.

363
366 In a system configured with multiple DCEs, cacheline address are distributed across the DCEs using an *implementation-defined* mapping function, e.g. address bit interleaving or hashing, that routes coherent memory accesses to the appropriate Home DCE based on the cacheline address. Address interleaving can help reduce average utilization and thereby improve coherent access throughput in the system.

369 A DCE may implement a system directory partition for tracking and managing the contents of caching agent caches with respect to the addresses associated with the DCE. This allows the snoop messages to be sent to only the necessary AIUs. In theory, a directory may also be configured without a directory, effectively “broadcasting” snoop messages to all caching agents (Hybrid directory and broadcast configurations may also be possible). NCore 3 does not support broadcast configurations.

372
375 Unlike an AIU, a DCE does not connect to an external agent, and thus does not carry an external interface.

378 There can be one or more DCE units in an Ncore 3 system. If coherent accesses are being made in an Ncore 3 system, however, at least one DCE unit must be present in the system.

2.2.6 Distributed Memory Interface (DMI)

In a Concerto-based system, **system memory** is assumed to behave as “normal” storage in that a write to a given memory location updates the value stored at that location and a read from a memory location returns the last value written to that memory location. Furthermore, performing an access to system memory does not have side-effects.

384 Typically, system memory resides in off-chip DRAM storage, commonly in DDR memory devices, or in SRAMs that might be on- or off-chip.

387

In Ncore 3, system memory can be accessed **coherently**. Coherency is maintained on the basis of a cacheline, which is a contiguous block of a power-of-two number of bytes that is uniquely identified by a **cacheline address**, which is a system memory address aligned to the size, in bytes, of a cacheline.

390

Note that regions of system memory can also be accessed non-coherently.

System memory may be treated as being **cacheable**, meaning an agent may buffer a copy of a cacheline, or a **cacheline copy**, in its cache.

393

In Concerto C, system memory may only be accessed via the Ncore 3 unit called, **Distributed Memory Interface Unit (DMIU)**.

396

Note that any system memory reached via a DMI is within the Coherency Domain of the CCMP.

There can be one or more DMI units per Ncore 3 system.

Multiple DMIs can be accessed in an address interleaved manner.

399

The DMI block offers an AXI interface to connect to a memory controller. The width of this AXI bus is parameterizable.

ADMI may optionally contain a cache, called **System Memory Cache (SMC)**, that acts as the last-level cache in-line to memory. Being in-line to the memory controller, the SMC can help reduce Read latency and improve delivered bandwidth.

402

The SMC offers an option to include an **Atomic Engine (AE)**. The AE supports the **Far Atomic Operations (FAOs)** defined in CHI-B and ACE5-Lite interface architectures. Thus, in Ncore 3 FAOs are supported for all locations in *system memory* connected via the DMI.

405

The DMI also contains logic to remap addresses referenced in Concerto C messages to physical addresses that may allow **address compaction** on the AXI bus.

2.2.7 Distributed IO Interface (DII)

408

Besides system memory, a system can have additional storage that cannot be, or doesn't need to be, maintained coherently. Configuration and status registers in the system's peripheral devices are an example of this category. These registers can have side effects under Reads or Writes. Consequently, they cannot be prefetched as part of a cacheline. Such storage, thus, must be treated as being **non-cacheable**, and therefore also **non-coherent**. Peripheral device based buffers and peripheral SRAMs are other examples of this category. These may be well-behaved, allowing them to be accessed as **cacheable** but **non-coherent** storage.

414

In Ncore 3, this category of storage, labeled herein generally as **peripheral device storage**, is accessed via a unit called **Distributed IO Interface (DII)**.

417

Coherency is not supported for any storage that is accessed via a DII. However, if it is well-behaved, such as SRAM, it can be accessed as being cacheable. There can be multiple DII units in an Ncore 3 system.

420

The DII block offers an AXI interface to connect to IO devices. The width of this AXI bus is parameterizable. The DII also contains logic to remap addresses referenced in Concerto C messages to physical addresses that may allow **address compaction** on the AXI bus. Ncore 3 should have at least one SysDII, which is special DII connecting with CSR network.

423

Just like application processes, peripheral devices cannot always be trusted as being free of malicious or erroneous behavior. And so, their accesses must be screened via MMUs akin to those that are used inside processors. These MMUs used to authenticate IO accesses into coherency domain are called IO MMUs (IOMMU) or System MMUs (SMMUs).

426

It is also advantageous, and common practice, for processor MMUs and SMMU to use the same page tables stored in system memory. When this is done, an SMMU's contents must be maintained consistent with those of a processor's MMU. This is achieved in Ncore 3 via a hardware function block called **Distributed Virtual Memory Management Engine (DVE)**.

432

There can be at most one DVE in the Ncore 3 system. Please note that the number of credits are depends on the number of masters that can issue DVMops and the number of outstanding DVMops each master can issue.

435

Currently, the number of snoop credits are fixed at 8 so that the number of STT entries are fixed at 4. STT entries are partitioned to be regular and reserved. The number of reserved STT entry is fixed at 1. The reserved STT entry is only for non-sync DVMop bypass. The maximum number of Sync DVMop in regular STT entries is 3 (this can be controlled by CSR to be 1).

438

DVE include a module to capture traces from other units. Also, it would be connected to the user's device driver to deliver captured data through APB interface.

2.2.9 Global Register Block (GRB)

441

Global Register Block (GRB) connects only to the CSR network and hosts system identification registers.

Please refer to section 5.1.1 for more details.

444

2.3 Ncore System organization

447

The Architectural system Overview with different concerto units is shown in Figure 2-1. The figure depicts one or more instances of the various types of AIUs discussed above connected to the Concerto Transport Fabric.

450

The coherent processors or accelerators or clusters thereof are connected individually via a native interface offered by ACE, CHI-B, or CHI-E AIU. One or more non-coherent agents, typically peripheral devices that don't possess coherent cache hierarchies and carry interfaces such as AXI, may optionally

453 be first connected via an external network to concentrate their traffic, and then be connected to an AXI-
 AIU. This traffic may optionally be intercepted by an SMMU before getting to the AIU. The SMMUs may
 456 optionally interface with an ACE-Lite or an ACE5-Lite AIU, depending on the desired functionality. ACE5-
 Lite interfaces enable peripherals to perform stashing and Far Atomic operations. The fabric is
 460 comprised of one or more independent transport networks that carry Concerto C message traffic that is
 generated in response to coherent and non-coherent accesses along with other types of transactions
 issued by agents to the AIUs. The connectivity capabilities, performance parameters, physical
 464 placement, and topology of these networks are customizable per the needs of the SoC.

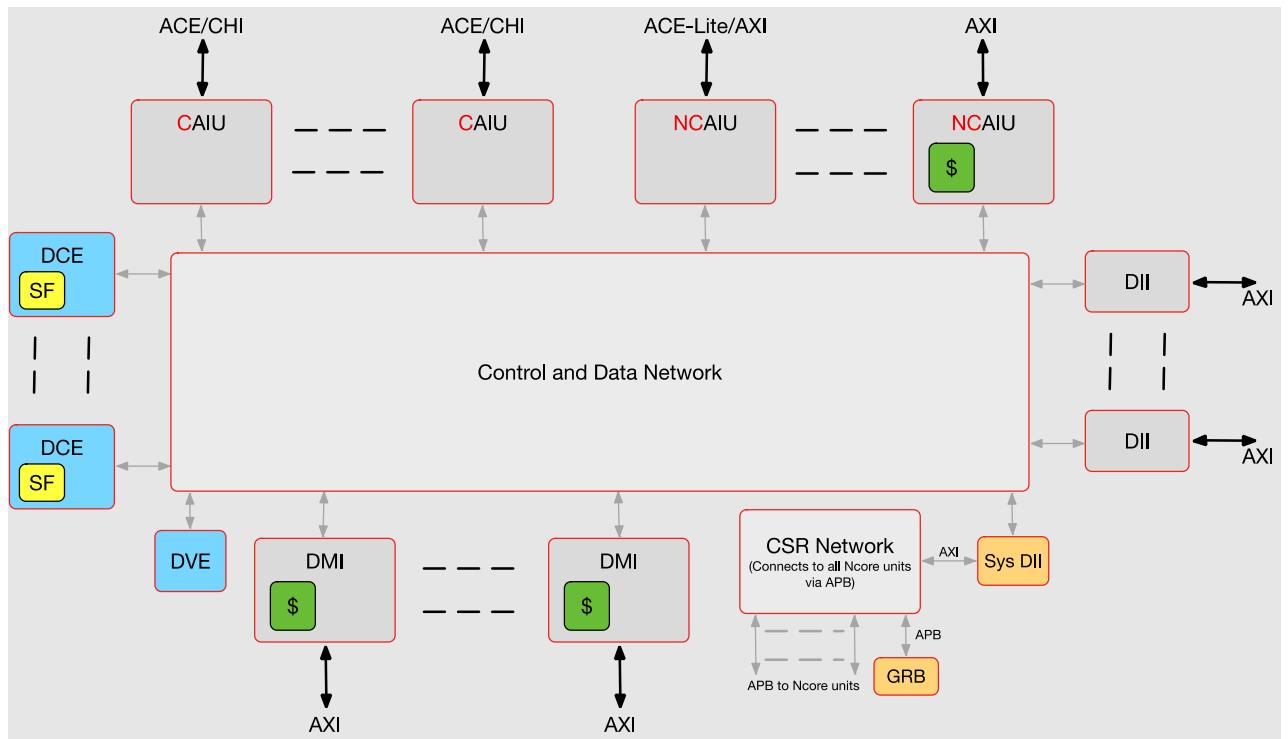
462 The target of an agent's transaction could be system memory or peripheral storage. System memory is accessed via one or more DMI units. System memory address ranges can be interleaved across sets of DMIs.

465 One or more DII units are used to access all peripheral storage in the system.

468 The Ncore 3 system supports the ARM DVM architecture operations including required interactions with the SMMUs in an SoC. The DVE unit coordinates the execution of the DVM protocol.

A concerto unit can expose up to three different main interface types, they are classified as

- Native interface: this is for communication with other standard interface IPs
- SMI: this is for concerto protocol communication
- APB: this is for control and status register (CSR) communication



471

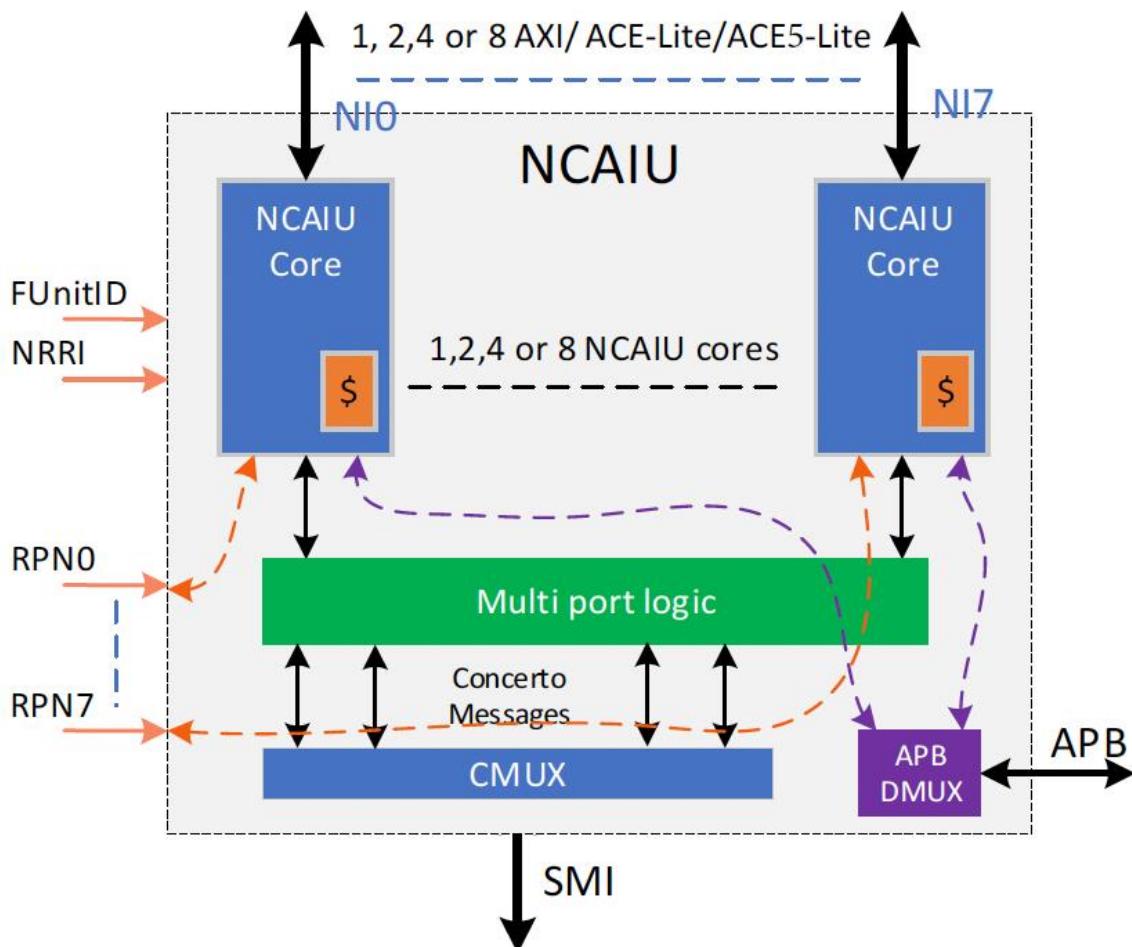
FIGURE 2-1 SYSTEM OVERVIEW

For the sake of brevity, the Figure 2-1 is simplified and does not show complete details of the CSR network and APB connections to all concerto units.

474 2.3.1 Multi-ported NCAIU description

The Top-level block diagram of a multi ported NCAIU is shown in Figure 2-2. As can be see, it is architected as a wrapper around a single NCAIU core that is replicated. The native interface (which can be AXI, ACE-Lite or ACE5-Lite) and NCAIU Core are replicated based on the parameter nNativeInterfacePorts. The multiport logic is responsible to make the NCAIU cores look like a single NCAIU to the CMUX (concerto mux), and in turn to the rest of the Ncore 3 system. The APB demux manages the APB connectivity to access each NCAIU core. See section 5.1 for more detail on Ncore 3 register region. The orange input ports are tie offs; note that there is:

- one identifier FUnit ID
- one Ncore register region identifier (NRRI)
- separate register page number (RPNs) depending on the number of ports.



486

FIGURE 2-2 MULTI PORTED NCAIU

All NCAIU Cores must be identical. Parameters that are constrained based on the number of ports must
489 be divided by the number of ports (nNativeInterfacePorts) before they are passed to the NCAIU core.
The Native interface ports and the NCAIU cores are address interleaved based on the parameter
492 aNcaiuIntvFunc. Depending on the implementation, address bits used for interleaving may or may not
be present (stored) within NCAIU cores, in either case they are expected to be present on the native
interface and the SMI interface.

Outgoing messages must have unique message ID. Ideally this message ID is nothing but the OTT index,
495 as there are multiple NCAIU cores the message ID will need to be extended by appending NCAIU core
identification bits at MSB. These bits are nothing but ordinal numbers identifying the NCAIU core,
example for a 4-port NCAIU it will be 2 bits 00, 01, 10 and 11. Depending on the implementation either
498 the NCAIU core can append the unique identifier bits or just append Zeros which may be replaced by
the unique identifier bits within the Multiport logic.

The Multiport logic block is mainly responsible for muxing and demuxing concerto messages between
501 the NCAIU cores and the CMUX. The outgoing messages are muxed out based on the type of Concerto
message. Incoming Concerto messages are demuxed based on the MSB bits of the message ID within
504 the Concerto message, exception to this rule is the SnpReq message which is demuxed based on the
interleaved address bits.

2.3.1.1 CSR address space and access support

Each NCAIU core supports one register page number RPN, this translates to up to 8 RPNs per multi-
507 ported NCAIU depending on number of ports configured. All the RPNs of a single multiport NCAIU must
be contiguous and within a single NRRI. All configured RPNs (NCAIU cores) must be accessed via a
single APB port, an APB demux is used to support only one APB port on the multi-ported NCAIU.

510 Note: SW changes may be needed to support more than 4K address space per APB on the CSR network.

2.3.1.2 Trace and Debug Support

Each NCAIU core will implement its own trace trigger block and CSRs. The trace capture block will have
513 to be implemented within the Multiport logic and must be controlled via CSRs in the first NCAIU core.
To keep the NCAIU cores identical all of them will implement the trace capture registers.

516 **2.3.1.3 High transport BW support**

519 To support higher BW on the SMI ports software will need to implement a special wrapper. This wrapper will instantiate 2 multi-ported NCAIUs as shown in Figure 2-3.

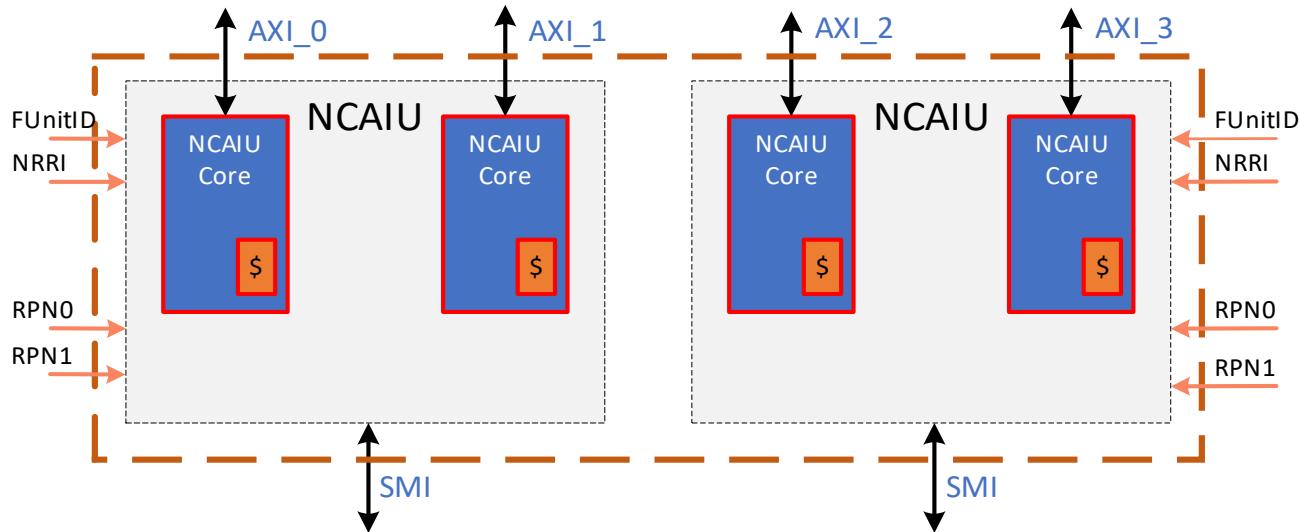


FIGURE 2-3 MULTI-PORTED NCAIU WRAPPER

522 2.4 Topology options

The transport layer offers the flexibility to create optimized topologies to find the best tradeoffs for each SoC configuration.

525 The list of data width options for each unit is the following:

- CHI AIU interface data width options: 128/256 bits
- ACE/AXI/ACE-Lite AIU interface data width options - 64/128/256
- 528 ○ DII interface data width selection - 64/128/256
- DMI interface data width selection - 128/256

As a reminder, the SMI interface width matches the corresponding ATP interface width because Ncore 3.4 supports header parallel style. All the data widths combinations shall be verified.

531 Ncore 3 does not impose restrictions on the choice of topologies but helps to ensure that the outcome is correct and efficient. It shall detect protocol and routing deadlocks.

534 2.4.1 Crossbar

This topology can be represented by multiple level of switches connected one after another between Ncore agents and Ncore targets such as DMIs or DIIs. The routing paths are calculated and checked in Maestro during 537 the build time. The number of layers between the agents and targets are calculated based on the connectivity among them, overall address map and respective address region assigned to each target.

2.4.2 Mesh

540 2.4.2.1 Methodology and flow

Mesh topology can be supported with the addition of sym_ibuf_switch as described in section 3.4.1.2. The X-Y routing scheme will be employed for the routing for a mesh topology. Please note that X represents the 543 horizontal/row as one observes in the Maestro GUI and Y represents the vertical/column in the same GUI.

2.4.2.2 Limitations and constraints

Ncore can only support of maximum 25 nodes for any mesh topology. And any configuration with any 546 permutation of X^*Y^4 is less or equal to 25 are valid and supported.

2.5 Engineering version ID

549

⁴ The multiplication of the size of both horizontal and vertical dimension of a mesh topology

552

The Engineering Version Identifier is a concatenation of two fields: {MPFHash[18:0], CHIP_ID[12:0]}. The CHIP_ID is obtained from a license file and the MPFHash is the last 19 bits obtained from the 128bit MD5 Hash."

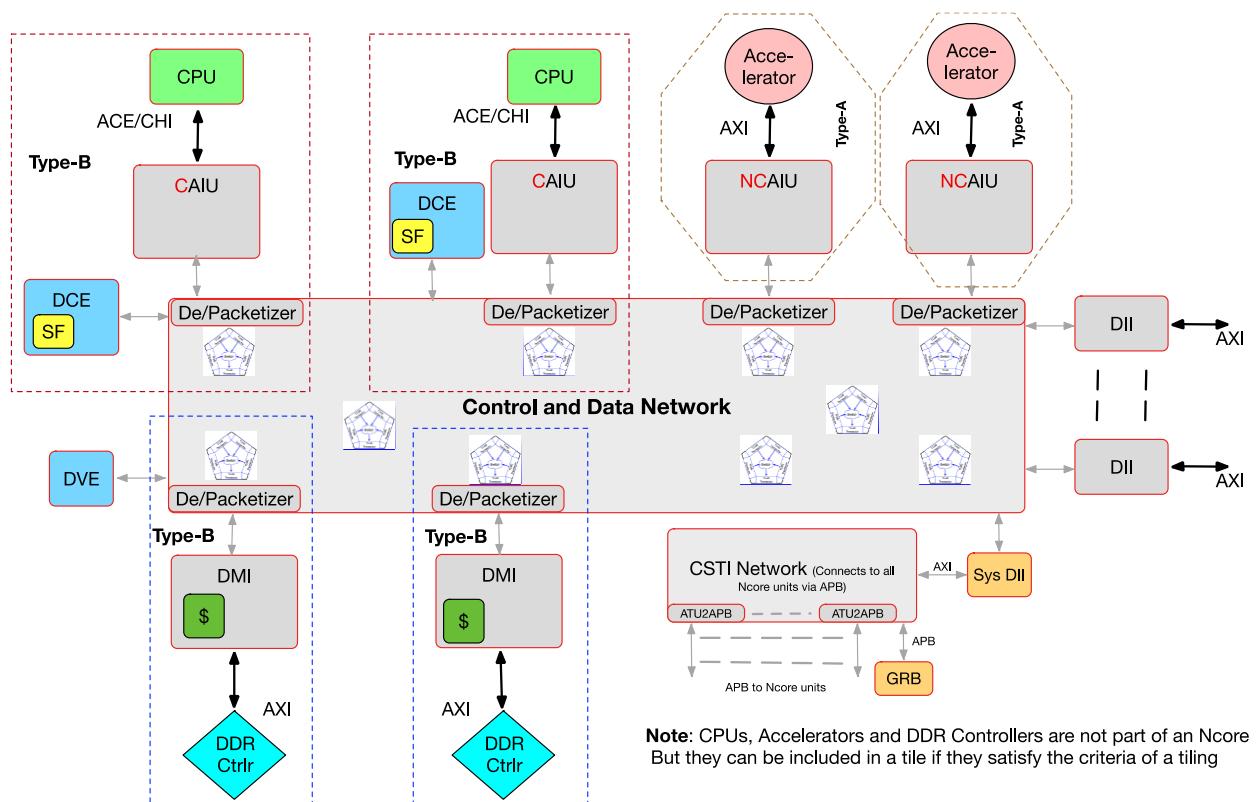
The Engineering ID Register (ENGIDR) is described in section 5.1.1.4.

2.6 Tiling

555

2.6.1 Methodology

558



561

FIGURE 2-4 HIGH LEVEL VIEW OF TILING

As shown in Figure 2-4, tiling is supported to encourage re-use of physical design work for any Ncore unit, a few different types of Ncore units or a partition consists of different type of Ncore units. By enabling this feature, an Ncore configuration can be divided and conquered with a few groups/partitions for the ease of physical design, which enables a hierarchical flow to facilitate a much smoother implementation experience. It helps to produce predictable Quality of Result throughout the design execution and lead to a shorter time to market schedule.

Please note that a partition is simply a group consists of one or more Ncore units, zero or more switches etc., but a tile is a partition that can be replicated and re-used from RTL to physical design.

2.6.2 Different types of Tiling

The following list summarizes different types of tiling:

- A. Any Ncore unit such as C-AIU, NC-AIU, DCE etc.; or any component of CDTI or CSTI such as a switch, a packetizer or a de-parcketizer etc.. For example, the NC-AIU embedded in the brown hexagon shape shown in Figure 2-4 is a typical representation of a Type-A tile
- B. A partition/group that consists of same set of Ncore unit(s) along with its(their) associated CDTI/CSTI component(s) as shown inside of the rectangles circled by the red and blue dashed lines as shown in Figure 2-4
- C. A hierarchical tile which consists of any Ncore unit(s), or any type-A or type-B of tiles, or the combinations of the two as shown inside the hexagon shape in purple color in Figure 2-5

In any Ncore implementation, one can have none, any single type of tile or combinations of any two or more tiles.

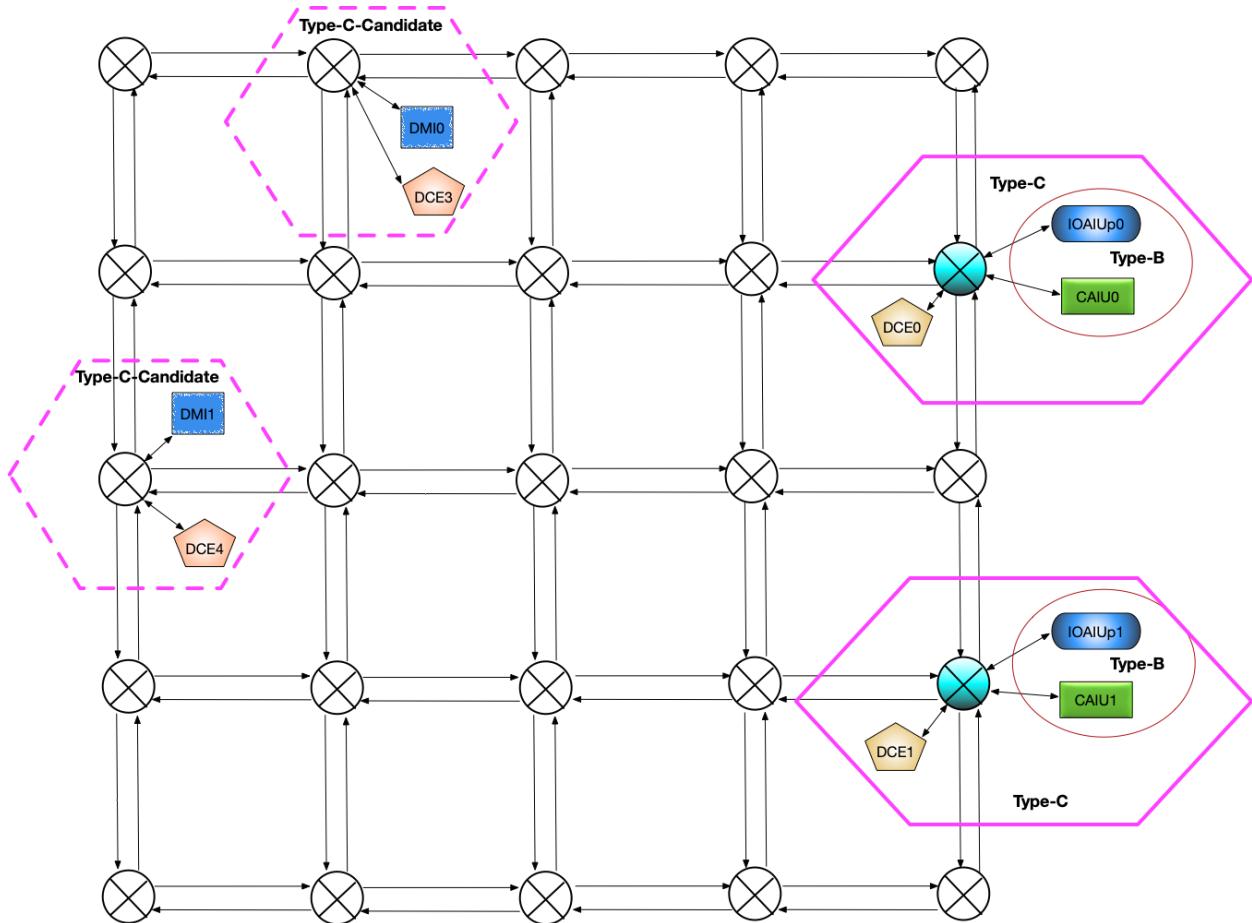


FIGURE 2-5 A TYPICAL TYPE-C TILE EXAMPLE BASED ON A MESH TOPOLOGY

2.6.3 Criteria to create a tile

585 To create a tile, there are at least **two or more** functional units/components that represent the following characteristics:

- 588 • Same Ncore unit functions
- For a group of switches used in CDTI/CSTI between the master tile and its replica(s), they should be graph isomorphic, and be equivalent from logical and timing perspectives or they obey the following equivalent rules:
 - 591 ○ Same type of the switch
 - Same number of ingress/egress ports
 - Same number of pipeline stages
 - 594 ○ Same routing between any ingress port to any egress port
 - Same number of latencies between any ingress port to any egress port
 - Same number of connections between this switch to the one(s) in front of it (if any)
 - 597 ○ Same number of connections between this switch to the one(s) behind of it (if any)
- Same input and output interface protocol along with the same bus width

- Same clocks and resets, and associated handlings
- 600 • Same timing constraints observed
- Same power management functions and interface such Q channel interface and associated handshake logic
- 603 • Same silicon orientation of the physical block/sub chip etc.. A tile can be re-used if it is flipped horizontally or vertically, but might not be re-used if it is rotated 90 or 270 degrees depends on the technology used for manufacture

606 2.6.4 Handling of a tile(s) inside of an Ncore

As described in section 2.6.3, for any specific tile, all the tiles are the same inside out. We must distinguish them by a tile ID, which needs to be available at the tile boundary. Depends on what kind of type is used, the tile ID 609 can be represented differently as the following:

- For type A tiles,
 - All Ncore units can be uniquified by their corresponding FUnitIDs
 - All Ncore units with maximum 8-bit wide FUnitID
 - The width of FUnitID will be the ceiling of $\log_2(\text{number of ncore units})$
 - Packetizer can be uniquified by the concatenation of {FUnitID, PortID}, so the downstream 615 routing tables can be indexed properly
 - PortID is fixed at zero at this point, but it is reserved for future expansion
 - ATU2APB can be uniquified by the nodeID
- 618 • For type B tiles,
 - The tiles can be uniquified by the concatenation of all FUnitIDs inside of a tile. The sequence of 621 the FUnitIDs concatenation is the same as FUnitIDs are numbered, which is described in section 3.6.1.
 - It will be {CAIUs → NC-AIUs → DCEs → DMIs → DIIs → Packetizers → ATU2APBs}
 - CHI-B CAIUs → CHI-E CAIUs
 - ACE-IOAIUs → ACE-Lite IOAIUs → ACE-LiteDVM IOAIUs → AXI4 IOAIUs
 - Packetizers go by the order the Ncore Units they are associated with
 - ATU2APBs go by the order the Ncore Units they are associated with
 - 627 • For type C tiles,
 - The tiles can be uniquified by the concatenation of the IDs with the following sequence
 - {[Any type A tile(s)] → [Any type B tile(s)] → [Any type C tile(s)]}
 - If there are multiple type B/C tiles, the type B/C tile has the Ncore unit(s) rank ahead in the sequence defined in section 3.6.1 take precedence in the concatenation

633

2.6.5 Exceptions

636 The following functionalities or units are not considered for tiling:

- DVE – Distributed Virtual memory system Engine
- Function Safety Controller
- Power management master functionalities
- Trace and debug
- Sys DII

639 642 Also, some signals/wirings need to be treated separately such as:

- Interrupts
- System events to DVE
- Functional Safety signals

2.6.6 Expected usage and limitations of support

648 The expected usage of tiling at this point is the end user to identify the tile candidates in Maestro, Maestro runs the checks to make sure the criteria discussed in section 2.6.3 are all satisfied. Maestro doesn't attempt to change the topology nor the type of switch to make any tile candidates become tiles but only validates 651 candidates are feasible or not to become tiles.

As shown in Figure 2-5, the two Type-C tile candidates on the right side can be validated as tiles because all criteria listed in section 2.6.3. However, the two candidates shown in the top edge and left edge are not tiles.

654 Because the switch used in top edge tile candidate has the connections at east, west and south directions versus the switch in the tile candidate located in the left edge has the connections at north, south and east directions even though the same type of switch with the same number of ingress and egress ports are used in both places.

657

660 3 Transport layer

Ncore 3 uses two types of transport interconnect: the Control and Status Transport Interconnect (CSTI) 663 and the Control and Data Transport Interconnect (CDTI).

CSTI is the service interconnect for configuration and status register access to all Ncore 3 components. CDTI is the main protocol interconnect.

666 Ncore 3 components generate different set of control and data messages as described in Concerto
protocol specification. These messages are mapped to one data network and at least two control
669 network, these networks are referred together as CDTI. Separation of different messages onto
independent transport resources avoids dependency loops inside the transport that would otherwise
have deadlock issues and may also improve performance.

672 The number of control networks are determined based on floor plan and throughput requirements.
Control network width is determined based on system address width and other protocol control
information that needs to flow on it. Data network supports three width options, 64, 128, and 256 bit.
These options can be mixed and matched within a single data network.

675 For a single native request, Ncore 3 protocol issues multiple control messages and most likely a single
data message. Depending on the width of the data network, one or more control network can be chosen
678 to achieve the required throughput. For example, If the data network is 256 bits, a cache line read will
consume 2 data network cycles. In this case to achieve maximum throughput three control networks
must be used. This ensures the number of control network cycles required will be within the 2 data
network cycles. Currently, Ncore 3 supports the following two options:

- 681
- Three networks, one data and two control networks, one for requests and another for responses
 - Four networks, one data and three control networks, one for requests, another for responses
684 and lastly a dedicated network for messages between DCEs and DMIs.

3.1 Legato transport description

687 Ncore 3 units are interconnected via an underlying interconnection fabric, called Legato. It relies on the
Concerto Transport Fabric (CTF). The CTF provides the transportation service for the CCMP messages.
Each individual network is built out of communication components: switches, adapters, pipeline
registers, and terminal blocks.

690 The components are connected amongst themselves via point-to-point, unidirectional links.

A network component may have multiple ports. Each port connects to exactly one link. A port is called an
ingress port if the link connected to it points toward the component; it is called an **egress port** if the link
693 connected to it points away from the component.

696 A component may have “primary” ports and “secondary” ports. Primary ports, ingress and egress, are
defined to be the ones that are used for communicating information across the component during the
normal operation of the network. It is assumed that secondary ports, ingress and egress, are strictly
used for orthogonal and supplementary functions such as error reporting, component status inquiry,
etc. A primary ingress port is considered to be connected to a primary egress port, if the component
699 allows a message to travel from the said ingress port to the said egress port.

702

A link connects two network components. It connects an egress port on one component to an ingress port of another component. Information on the link travels over the link from the egress port to the ingress port, which is also the direction a message flows over the link. The direction of information flow over a link is the direction indicated for that link. Thus, a link can only be “traversed” in the direction the information can flow over it. The two said network components are considered to be “connected” via the said directed link between them.

705

A **link** is a set of wires, perhaps punctuated by electrical buffers to help power the transmission of signals. It is used to transmit information from one of the pair of components it connects to the other. The link also includes signals that travel in the opposite direction that are used to control the flow of said information. In a graphical representation, the direction of the link indicates the direction of the flow of information over the link.

708

711

A path from network component A to network component B exists if there exists an alternating sequence of components and links, such that a message can travel from A to B. If this is true, component A is considered to be “connected” to component B via the path.

714

717

A single path defines a rudimentary CTF network. If two paths share a network component, they both belong to the CTF network that contains all the components and links used by those two paths. If a path shares a component of a CTF network, the path and the components used by it also belong to the said CTF network.

If a path does not share a component with a network, it does not belong to the said network.

720

Note that by definition, paths are unidirectional. A path from A to B does not necessarily guarantee a path from B to A.

723

A message enters a network via one **terminal block** and exits it via another **terminal block**. The terminal blocks are *directional*. A unit connects to a **Transmit (TX)** terminal block to send a message into the network, and it connects to a **Receive (RX)** terminal block to receive a message from the network. Figure 3-1 shows a path from a TX terminal block to an RX terminal block via a CTF network.

726

A CTF network, thus, is a collection of network components, and links connecting them, such that it provides paths from one defined set of terminal blocks to another defined set of terminal blocks. Figure 3-2 shows a CTF network offering multiple TX and RX terminal blocks to which an end-point units can connect to transmit and receive messages.

729

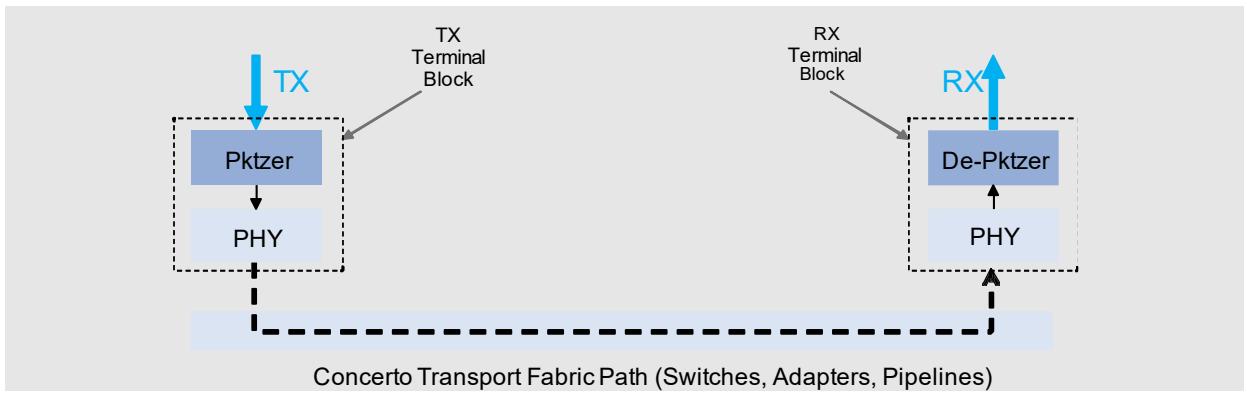
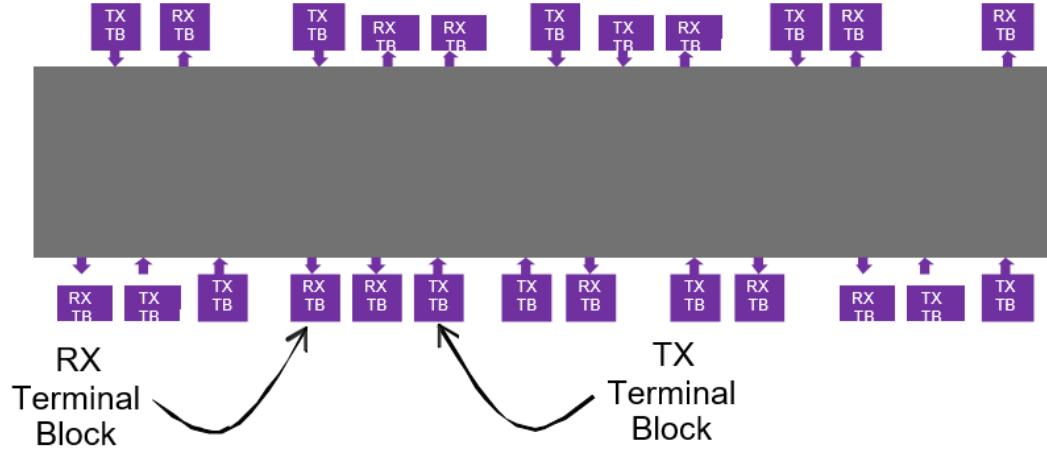


FIGURE 3-1 TERMINAL BLOCK TO TERMINAL BLOCK PATH THROUGH THE CTF



732

FIGURE 3-2 A CTF NETWORK OFFERING MULTIPLE TERMINAL BLOCKS FOR CONNECTING UNITS

A CTF network, in general, may offer more than one path between two terminal blocks.

735

A given CTF network is characterized by the subset of types of messages it carries. In general, a given physical path in a network may be used to carry multiple types of Concerto C Protocol messages. Distinct CTF networks carry distinct subsets of CCMP message types.

738

3.1.1 Attachment of Ncore units to CTF

Ncore 3 units use a CTF network to send or receive messages from other Ncore 3 units.

741

Figure 3-3 shows the connectivity between the Ncore 3 units and a CTF network. As can be seen, the sending Ncore 3 unit attaches to the TX terminal block of the CTF and the receiving Ncore 3 unit attaches to the RX terminal block.

744

An Ncore 3 unit A can send a message to another Ncore 3 unit B if a path exists from the *TX terminal block* to which A is connected to the *RX terminal block* to which B is connected.

A single terminal block, TX or RX, is used to connect to any single CTF network.

In general, an Ncore 3 unit may connect into a given CTF network via one or more TX and/or RX terminal blocks.
747

An Ncore 3 unit may also connect into multiple CTF networks. However, sets of terminal blocks used by an Ncore 3 unit to connect into distinct networks are distinct.

The interfaces between an Ncore 3 units and CTF terminal blocks are defined in detail in section 3.3.
750

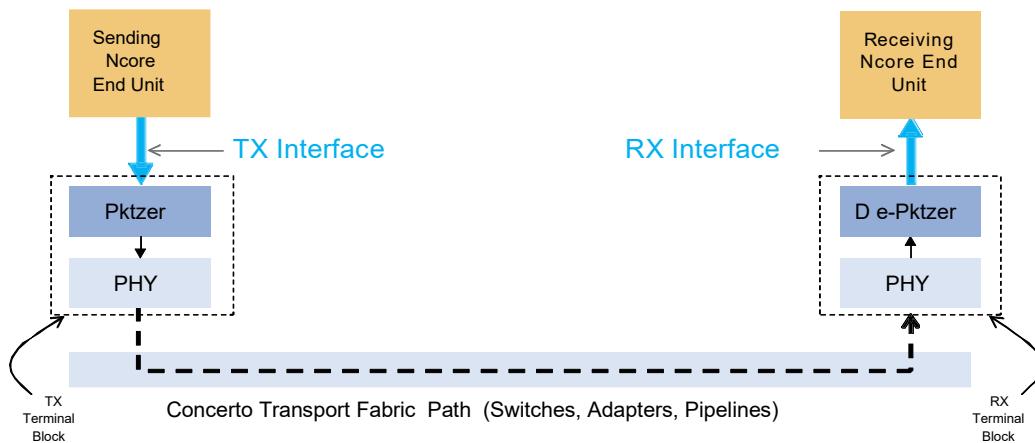


FIGURE 3-3 NCORE UNIT-TO-UNIT PATH VIA THE CTF

753 3.1.2 Structure of the Terminal Block

A **terminal block** connects on one side to another CTF network component via a link. On the other side, it offers a standardized interface to which an Ncore 3 unit is connected. The terminal block offers a **Transmit interface (TX)** to the Ncore 3 unit if the network link attached to the block points away from it. The terminal block offers a **Receive interface (RX)** to the Ncore 3 unit if the network link attached to the block points towards it. A terminal block thus represents an extremity, an end, or a “terminal” for the transport interconnects and the **ATP protocol domain**. The domain is entered at a TX terminal block and exited at an RX terminal block. The Ncore 3 units that attach to the terminal blocks are thus referred to as **end-units** or **terminal-units** of the CTF networks.
756
759

Figure 3-4 (a) shows a diagram of the functionality of a Transmit Terminal block. It performs the following functions:
762

- **Interface Logic:** Accepts a message from the Ncore 3 unit with which it interfaces.
- **Route Calculation:** Calculates the Data-Link layer route to the target unit indicated in the message.
- This block may take into account the “Steering” field in the Concerto C Message Header in calculating the Route. It is not used in the current version of Ncore.
765
768

- 771
- **ATP Data-Link Packetization:** Creates a Data-Link layer packet from the message. Note that each Concerto C Message results in a single packet at the ATP DL layer.
 - This block may take into account the TTier field in the Concerto C Message Header to pick the virtual channel to use for transmitting the packet along its link. Virtual channels are not used in the current version of Ncore 3.

774

 - **ATP PHY TX Interface:** Transmits the packet into the CTF network via its link.

Figure 3-4 (b) shows the internal functionality of a receive terminal block. Performs the following functions:

- 777
- **ATP PHY RX Interface:** Accepts a Data-Link layer packet from its CTF link.
 - **ATP Data-Link De-Packetization:** Extracts the message from the ATP packet format to forward it to the end-unit attached at this TerminalBlock.
 - **Interface Logic:** Transmits the message to the Ncore 3 unit with which it interfaces.

780

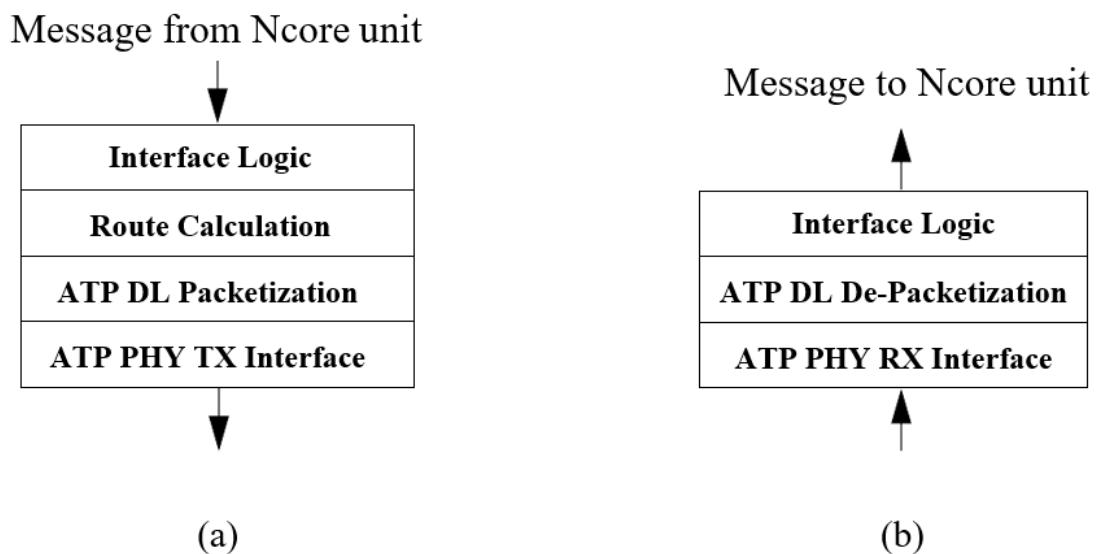


FIGURE 3-4 STRUCTURES OF TX AND RX TERMINAL BLOCKS.

783

3.2 Ncore Messaging over CTF

786

3.2.1 CCMP Message Formats

Two basic formats are used for CCMP messages:

- **A Data Message(DM)**

- 789 ○ In addition to command and/or control information, a data message carries data that may be read from or written into storage locations.

792 ● **A Non-Data Message(NDM)**

- 792 ○ A non-data message carries only command and/or control information

Below are shown formats of NDM and DM:

NDM = <Concerto C Message Header> + <Non-Data Payload>

795 DM = <Concerto C Message Header> + <Non-Data Payload> + <Data Payload> + <Auxiliary Payload>

Exchange of each message over an SMI is performed “atomically,” meaning that one message is delivered completely before the next is transmitted, for both NDM and DM.

798 An NDM is delivered wholly in a single clock cycle.

801 For a DM, the Data Payload is allowed to be transferred in multiple segments or beats, each of which must be a power of 2 number of double-words (64 bits). Thus, if the size of the beat is 2 double words (8 bytes), or 16 bytes, 64 bytes of data will be transferred in 4 beats.

804 In a DM, the <Concerto C Message Header>, <Non-Data Payload>, and the first beat of <Data Payload> are all transmitted during the first cycle of DM transfer, and the remaining beats of data are transmitted during subsequent cycles.

In general, a data payload beat may also include auxiliary information payload, as shown above. This auxiliary information is on a per double word basis and is present for each double word in the beat.

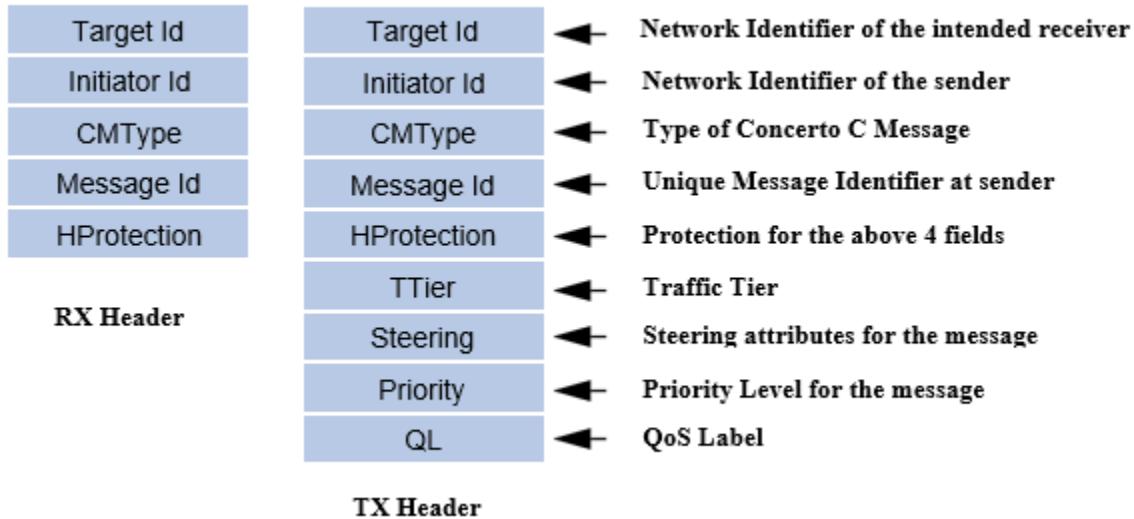
807 Typically, per double word, the following information is included:

- DW Byte Enables
- DW Protection bits
- DWId
- Poison
- User bits

813 The auxiliary bits for the data beat are right-appended to data beat.

3.2.2 Concerto C Message Header

816 All Concerto C messages have a common set of fields at their start. This set forms the common header for all Ncore C messages. Although the width of the fields can change from one Ncore 3 instance to the next, the order of fields is fixed as shown in Figure 3-5, giving all message a common header format.



819

FIGURE 3-5 CONCERTO C MESSAGE HEADERS

Target Id, Initiator Id, CMType, Message Id, and HProtection are fields that are carried end-to-end by the message, and hence appear in the TX and RX headers in Figure 3-5.

There are other fields in the TX header that are not intended to be carried end-to-end, but are included in the header. It is via these fields that the Ncore 3 unit at the interface makes specific service requests of the transport service. The purpose of these fields is specified below:

- **TTier:** Traffic Tier. This field is used for deadlock avoidance purpose. Each type of Concerto C message is associated with an architected TTier value. Multiple types of messages may have the same TTier value.
- The transport network maps a TTier value to a virtual channel for each of the links over which the message is carried through the network. For a given message type, the virtual channel chosen can be different at different links. However, the following rule must be satisfied to ensure freedom for deadlocks.

Deadlock Prevention Rule: A message carrying a value V for TTier must not be permanently blocked by a message carrying a value greater than V. Satisfaction of this rule in the interconnect is mandatory to prevent deadlocks. Minimum value for this field is 0. Thus, messages with TTier = 0 must not be blocked by any message with TTier > 0. This field is not intended to be treated as a Quality of Service attribute.

- **Steering:** This field influences the determination of the route taken by the message to reach its target. It is not used in the current Ncore 3 implementation.
- **Priority:** A higher priority message is given preference over a lower priority message in determining passage across network components.

- **QL:** QoS Label. This field is used to enable bandwidth provisioning and requirements. It is not used in the current Ncore 3 implementation.

843 The widths of the fields in the header and individual message types are build-time constants that are known to all Ncore 3 units. The widths of the fields in the message header are also passed into the terminal block. This enables the terminal block to correctly access these fields when it receives the message over the SMI.

846 Other fields in the message, which constitute the “body” of the message are not visible to the transport facility.

849 Similarly, the Ncore 3 unit receiving a message is able to identify and access all the fields in the header. Once it accesses the CMType field, it knows what type of message it has received.

That in turn allows the receiving unit to interpret all the fields of the message.

852 3.2.3 Packetized delivery of Concerto C messages

855 The exact delivery format of Concerto C message is outside the scope of this architecture. The only requirement placed by this architecture is that for multi-PHIT delivery of messages, the Concerto C Message header is replicated for each PHIT of transmission.

3.2.4 Formats of Concerto C Messages

Majority of Concerto C Message use the NDM format.

858 3.2.4.1 DMs

The following CCMP messages use DM format: DTR, DTW, DTWMrgMRD

3.2.4.2 NDMs

861 The following CCMP messages use NDM format:

CMDreq, SNPreq, MRDreq, HNTreq, STRreq, RBRreq, UPDreq, CCMDrsp, NCMDrsp, SNPrsp, DTWrsp, DTRrsp, HNTrsp, MRDrsp, STRrsp, UPDrsp, RBRrsp, CMPrsp, CMErsp, and TRErsp.

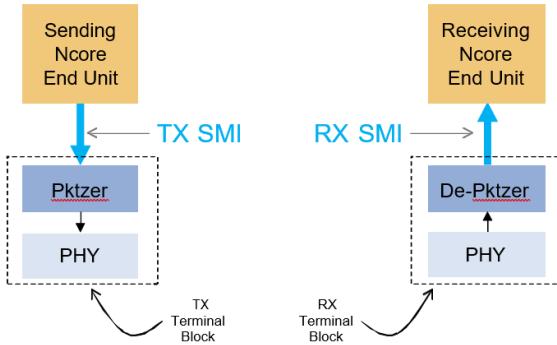
864 3.3 CTF Messaging Interface

An Ncore 3 unit and a CTF terminal block communicate via standardized interfaces, called the **Symphony Message Interface (SMI)**, across which the two blocks exchange messages.

867 An SMI can be of **TX** or **RX** kind, named with reference to the Ncore 3 unit which shares it with a *Terminal Blocks* of the CTX. These two interfaces are shown in Figure 3-6.

870 The SMI is defined to be a synchronous interface, and any resynchronization to another clock is done outside the SMI interface.

The messages exchanged across the SMIs are Concerto C Messaging Protocol messages.

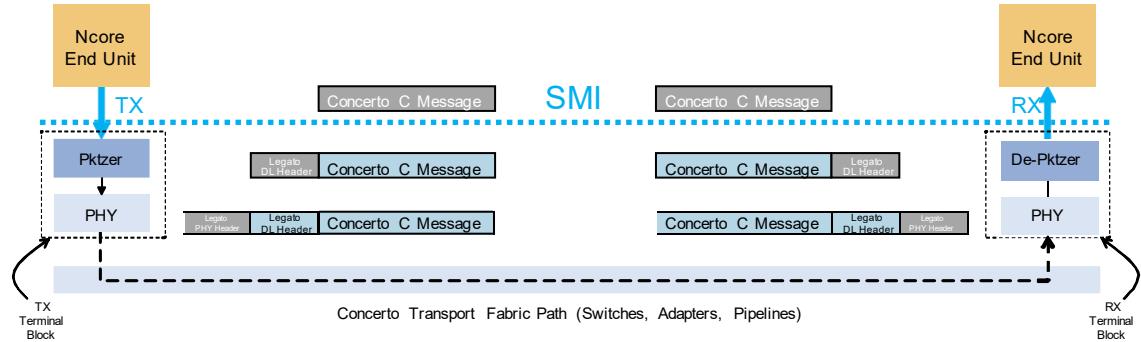


873

FIGURE 3-6 TX AND RX SMI INTERFACES

3.3.1 Transmission of Concerto C messages over CTF

As shown in the Figure 3-7, after receiving a message from the Ncore 3 unit over the TX SMI, the transmit terminal block packetizes the message and transmits it via its link into the CTF network. On the other side, a receive terminal block receives a packet from its link, extracts the message from it, and transmits it to the Ncore 3 unit connected via the RX SMI.



879

FIGURE 3-7 TX AND RX SMI INTERFACES

3.3.2 SMI Interface signals

SMI is message passing interface that transfers messages with or without data.

- Flow control for SMI message is based on valid-ready handshake. If both valid (by master) and ready (by slave) are asserted the transfer takes place. The ready may or may not be asserted in absence of valid.
- There is a separate flow control for the SMI data payload interface (dp_ *). The flow control for data payload is independent from the SMI message flow control though there will be some implementation dependencies (like – SMI packetizer will not accept SMI data payload transfer without the corresponding SMI message transfer).

888

- Flow control can be per VC (valid-ready per VC), with only 1 VC transfer accepted per cycle (only 1 ready asserted). The VC selection can change per cycle. VC is not used in Ncore 3.
- 891 Messages per flow/VC are not interleaved. The next message does not start before the current message finishes.
- 894 SMI can be with or without data payload interface (parameterized). Even with SMI data payload interface, a given message can have no data payload (dp_present set to 0 in SMI message).
- 897 SMI message can include non-data payload, which is handled like just another message field
- All SMI fields are parameterized, and can be optimized out based on configuration
- The SMI message length is an optional field for legato. The data payload uses last indicator to indicate the end of the data and thus makes length field optional for those messages (can be used for length error check).
- 900 Route can be generated by path lookup using {target ID, steer}, and so either route or steer (with target ID) is defined for a given interface. Steer is not used in Ncore 3.

903 Restrictions/Assumptions:

1. SMI master must not present DP (smi_dp_valid) before presenting the corresponding SMI message/NDP (smi_valid).
2. SMI slave must not hold off acknowledging the SMI message/NDP (smi_ready not asserted) while wanting to accept all the DP beats first.

SMI message interface signals are described below in Table 3-1.

909 The SMI Interface is a hierarchical interface broken into two interfaces:

- 1) Non-Data Payload
- 2) Data Payload

912 The two sub interfaces shall have the following names:

- 1) ndp_*
- 2) dp_*

915 TABLE 3-1 SMI MESSAGE NDP SIGNALS

Signal Name	Description
ndp_msg_valid	message valid
ndp_msg_ready	message ready
ndp_targ_id	Target ID
ndp_src_id	Source ID
ndp_steer	Steer (for route lookup, along with target ID).
ndp_msg_tier	Tier
ndp_msg_qos	QoS
ndp_msg_pri	Priority

ndp_ndp_len	Non-data payload length in bits
ndp_ndp	Non-data payload
ndp_dp_present	1: Data payload present, 0: no Data payload
ndp_msg_id	message ID
ndp_msg_type	message type
ndp_msg_user	User defined signals
ndp_msg_err	Message error/status

TABLE 3-2 SMI MESSAGE DP SIGNALS

Signal Name	Description
dp_valid	data valid
dp_ready	data ready
dp_last	data last
dp_data	Data payload
dp_user	User defined signals (for Ncore it maps to: BE + AUX)

918

3.3.3 Mapping Messages to SMI fields

This section specifies how CCMP message contents are mapped onto SMI fields at the TX SMI and 921 appear on the SMI fields at the RX SMI.

3.3.3.1 NDM TX

For an NDM, the entire NDM is mapped bit 0-aligned into the NDPayload field of the TX SMI interface. 924 That is,

$$\text{TX_SMI.NDPayload} \Leftarrow \langle\text{Concerto C Message Header}\rangle + \langle\text{Non-Data Payload}\rangle \text{ (left aligned)}$$

The message header, being at the beginning of Concerto C message is always located at the start of the 927 NDPayload field of the SMI, TX.

3.3.3.2 NDM RX

At the RX SMI interface, the whole NDM is wholly extracted left-aligned from the NDPayload field of the 930 SMI interface.

$$\langle\text{Concerto C Message Header}\rangle + \langle\text{Non-Data Payload}\rangle \Leftarrow \text{RX_SMI.NDPayload} \text{ (left aligned extraction)}$$

The message header, being at the beginning of Concerto C message is always located at the start of the 933 NDPayload field of the SMI, RX.

3.3.3.3 DM TX

For a DM, the Message Header and the Non-Data Payload portions of the DM are mapped left-aligned 936 into the NDPayload field of the TX SMI interface. That is,

$$\text{TX_SMI.NDPayload} \Leftarrow \langle\text{Concerto C Message Header}\rangle + \langle\text{Non-Data Payload}\rangle \text{ (left aligned)}$$

939 The message header, being at the beginning of Concerto C message is always located at the start of the

NDPayload field of the SMI, TX.

The Data Payload portion of DM is mapped into the DPayload field of the TX SMI, on a per beat basis.
That is,

942 TX_SMI.DPayload \Leftarrow <DM.Data Payload>

Note: It is required that the number of DWs supported in the TX_SMI match that for the DM being transmitted over it.

945 The Auxiliary Payload portion of DM is mapped into the DPAux field of the TX SMI, on a per beat basis.
That is,

TX.SMI.DPAux \Leftarrow <DM.Auxiliary Payload>

948 3.3.3.4 DM RX

At the RX SMI interface, the Message Header and the Non-Data Payload portions of the DM is extracted left-aligned from the NDPayload field of the SMI interface.

951 <Concerto C Message Header> + <Non-Data Payload> \Leftarrow RX_SMI.NDPayload (left aligned extraction)

The message header, being at the beginning of Concerto C message is always located at the start of the NDPayload field of the SMI, RX.

954 The Data Payload portion of DM is extracted from the DPayload field of the RX SMI, on a per beat basis.
That is,

<DM.Data Payload> \Leftarrow RX_SMI.DPayload

957 **Note:** It is required that the number of DWs supported in the TX_SMI match that for the DM being received over it.

960 The Auxiliary Payload portion of DM is extracted from the DPAux field of the RX SMI, on a per beat basis.
That is,

<DM.Auxiliary Payload> \Leftarrow RX.SMI.DPAux

3.4 Ncore CDTI Network

963

The CDTI provides the transportation service for the CCMP messages. The CDTI may be comprised of one or more independent networks or interconnects, and individual network is built out of communication components: switches, adapters, and terminal blocks.

966

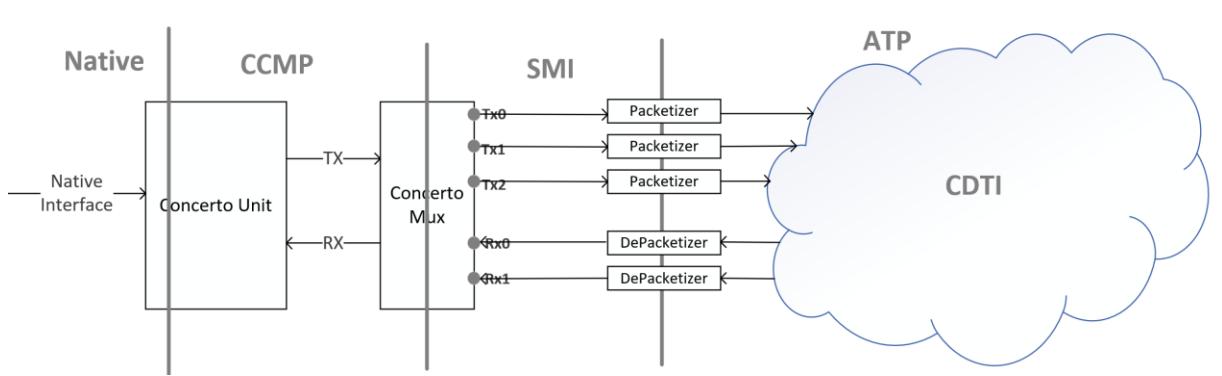


FIGURE 3-8: CCMP COMMUNICATION THROUGH THE CDTI

969

Concerto_Mux is playing an important role as a terminal between CCMP and ATP:

972

- Protocol conversion from CCMP to SMI
- Network mapping: CCMP includes large number of message types, and these will be delivered into ATP using different network considering performance and deadlock avoidance. The example in Figure 3-8 shows message mapping into three Tx networks and two Rx networks.
- ECC/Party check is implemented
- Transport error is detected, and the results will be added at CMStatus.

975

Transport error is detected only when Resiliency is enabled. SMI (Symphony Message Interface) is messaging interface that transfers messages with or without data (Ndp_, Dp_). Information that is needed to determine the route of the packets from Source to the Destination in the CDTI is added at this layer. This layer is also responsible for traffic management across the fabric.

978

NOTE: Flow control of SMI message is based on valid-ready handshakes.

981

NOTE: The SMI is defined to be synchronous interface, and any resynchronization to another clock is done outside the SMI interface (In CDTI).

984

Packetizer and Depacketizer are format/framing of packets/flits for actual transmission of control and data bits over the CDTI networks. (ATP) Legato components are based on this ATP protocol.

3.4.1 CDTI Blocks

987

There are four types of blocks used in the networks of the CDTI: switches, pipe, clock and width adapters. For the detailed configuration capability of the Adapters, refer NCore 3 parameter specification.

990

3.4.1.1 Adapters automated insertion support

Maestro shall support automated insertion of width adapters. When source and destination of a network segment have different width, the decision shall be based on:

- 993
- $nInputWidth = \{switch, FUnit\} transmitter.width$
 - $nOutputWidth = \{switch, FUnit\} receiver.width$

996 The automatically generated WidthAdapter shall be customer configurable by changing the default settings of the following parameters:

- $nDepth$ (default = 0) to configure additional buffer stages
- $boolPipelined$ (default = false)

999 Maestro shall support user configurable insertion and removal of RateAdapters

- UI shall provide a means to select a network connection between two FUnits or an FUnit and a switch

1002 The manually inserted RateAdapter shall be configurable by UI

- $nDepth$ (default = TxnSize) to configure buffer stages
- $nDepth$ shall be derived from the network segment where the user chose to insert the adapter
- When a user attempts to insert a rate adapter on a segment connecting a WidthAdapter output to a receiver, Maestro shall offer to parametrize the widthAdapter to increase depth instead (do we need a forced override to insert a RateAdapter?)
- When a user attempts to insert a rate adapter in front of a WidthAdapter, Maestro shall issue a warning, this is useless and only adds latency, recommend parametrizing the width adapter instead
- Future versions of the RateAdapter may support different clock domains for input and output ports

1014 TABLE 3-3: INSERTION RULES FOR ADAPTERS

	Input < Output	Input = Output	Input > Output	Description
Type	Width Adapter	Rate Adapter	Width/Rate Adapter	Adapter type depends on the interface configuration
Rule	Automatic Insertion	Insertion by User Input	Automatic Insertion	When input and output do not have the same width, a Width Adapter will be required
Configurability	Automatic <ul style="list-style-type: none"> • Insertion = Yes • $nInputWidth$ • $nOutputWidth$ 	Automatic <ul style="list-style-type: none"> • Insertion = No 	Automatic <ul style="list-style-type: none"> • Insertion = Yes • $nInputWidth$ • $nOutputWidth$ 	
	User <ul style="list-style-type: none"> • $boolPipelined$ • $nDepth^1$ 	User <ul style="list-style-type: none"> • Insertion • $nWidth$ • $nDepth$ • $boolPipelined$ 	User <ul style="list-style-type: none"> • $boolPipelined$ • $nDepth^1$ 	
nDepth	Automatic $1 \times nInputWidth$ $+ 1 \times nOutputWidth$		Automatic $\geq 1 \times nInputWidth$	Automatic insertion will always use the minimum size required for the functionality

	Input < Output	Input = Output	Input > Output	Description
	User + n x nOutputWidth	User parameter based on rate difference $\geq n \times nWidth$	User + n x nOutputWidth	User may configure additional storage in Maestro's UI
Notes:	1. Optional, additional buffer stages for rate adaptation			

3.4.1.2 Switches

- 1017 Ncore 3 supports sym_switch, sym_buf_switch and sym_ibuf_switch
- Sym_switch: This is a worm hole switch that provides no buffering or pipelining at all in the switch. There is a check put in that looks for logic loops between sym_switches because of cycles in the topology. These cycles can be broken with a sym_pipe_adapter.
 - Sym_buf_switch: Buffered switches are switches that at a minimum buffer at the input of the switch but can also buffer in various places along the data path.
 - Sym_ibuf_switch: It is same as sym_buf_switch with the addition of a pipe stage added between every input to output combination
 - This type of switch is required for the implementation of mesh topology
 - All switches support path pruning.
 - Ncore 3 is only using round-robin arbitration policy.

1029 **3.4.1.3 Clock Adapters**

- sym_async_adapter: This is a unidirectional adapter that sits between two ATP links that run off different clocks. The two clocks can be edge aligned or not. It is also being used for power domain control. Users can change the buffer depth of this async adapter. Also, user could configure the depth of synchronizer using system parameter.
- chi_async_adapter: This is a unidirectional adapter that sits between CHI interfaces that run off different clocks. The buffer depth is calculated referring the credit of chi-interface. User could configure the depth of synchronizer using system parameter.
- sym_rate_adapter: A rate adapter is a unidirectional adapter that sits between two ATP links that run off different clocks and the ATP link's clock entering the block is slower than the ATP link's clock exiting the block. The purpose of the rate adapter is to eliminate bubbles in a packet on the fast side of the adapter.

1041

3.4.1.4 Pipe adapters

- sym_pipe_adapter: The pipe adapter is a unidirectional adapter that places storage along an ATP link and can be used as a pipe stage or FIFO. The ATP links going in and going out have identical definitions. User could configure the size of this pipe adapter. Also, sym_pipe_adapter has two modes: circular and FIFO. They're functionally equivalent but

1047 affect timing and power. Circular is lower power but has worse timing on the output. Default
should be circular.

1050 3.4.1.5 Width Adapters

Ncore 3 architecture supports different widths of networks between agents (64, 128, 256 bits).

Connections between receivers and transmitters with different widths require a WidthAdapter.

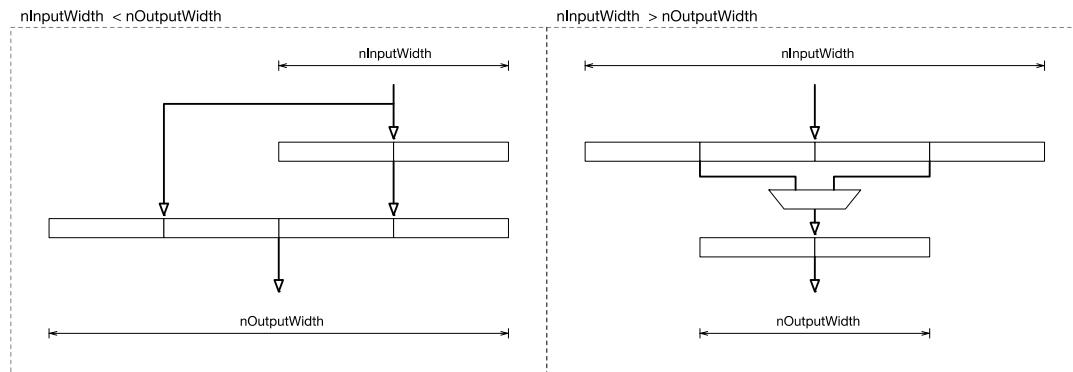
1053 A WidthAdapter converts a sequence of phits belonging to a packet arriving from a narrow interface to
the wide interface.

This avoids using only part of the wide output interface's bandwidth, which would propagate
1056 downstream. A WidthAdapter will assemble a wider phit by storing:

- at least one phit entry of the width of the outgoing port
- one entry with the difference in width between the input and the output port

1059 A WidthAdapter will introduce additional latency m:

- $m = (\text{nOutputWidth}/\text{nInputWidth}) + \text{ord}(\text{boolPipeline})$ If pipelining enabled



1062 FIGURE 3-9: INTERNAL STRUCTURE OF WIDTHADAPTER

A WidthAdapter will introduce additional bubbles into the down stream traffic.

1065 A WidthAdapter converting from wide interface to narrow interface may use a single wide entry to hold
a phit while breaking it down into a stream of consecutive, narrow phits.

A WidthAdapter shall track up to 4 transactions and detect the boundary between packets having a
different TxnID

1068 3.4.1.6 Rate adapter

A RateAdapter will be used when a packet, consisting of multiple phits, may contain bubbles. The rate
adapter's function is, to aggregate temporally separated pieces/phits of a transaction and retransmit
1071 them as consecutive sequence to a downstream receiver. The Legato interconnect does not support

transmission of flits belonging to different transactions. Rate adapters may be used to level out fluctuations in input rate, even when the arrival rate \geq departure rate for a short time, at the cost of increased buffering.

- Rate adapters always have the same width on the input and the output port
- A rate adapter implements a FiFo-Queue where the first phit of a packet (flit) will not signal valid to the downstream receiver until the entire packet has been assembled in the queue.
- A rate adapter must implement sufficient storage to hold at least one full packet - n buffer entries organized as width bits
- number of entries $n = \text{txn_size}/\text{port_width}$

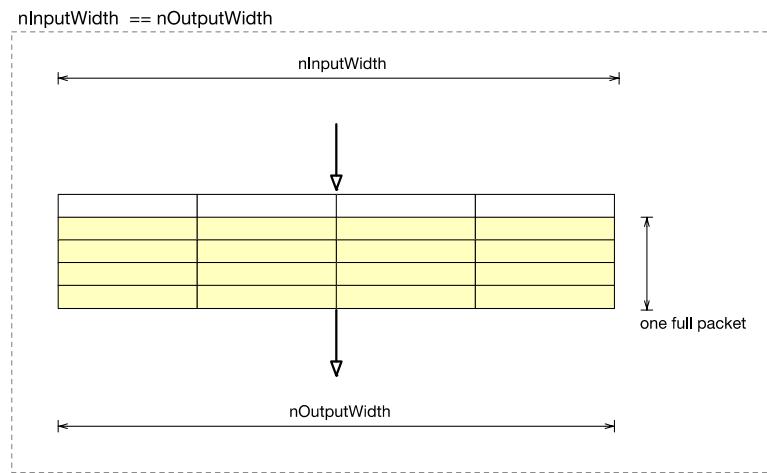


FIGURE 3-10: INTERNAL STRUCTURE OF RATE ADAPTER

Pipeline support shall be supported (improved timing), adding one additional storage entry of width bits to receive the first phit for the next transaction.

Additional entries may be specified if the designer desires to optimize bursty traffic in front of a congested switch. This will support more than a single transaction to be forwarded in an uninterrupted burst.

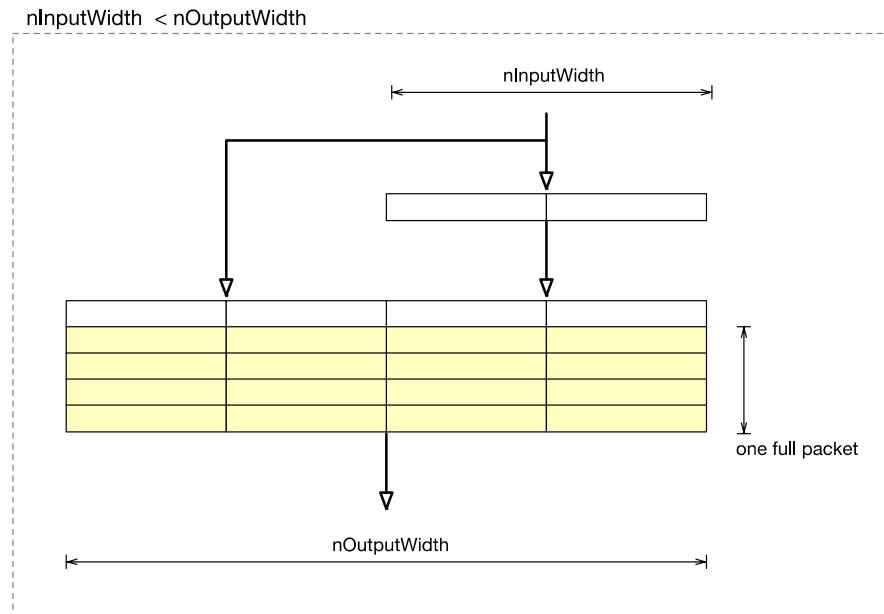
A rate adapter will introduce additional latency of m cycles:

- $m \geq \text{number of phits per transaction} + 1$

A width adapter shall track up to 4 transactions and detect the boundary between packets having a different TxnID.

3.4.1.7 Combined Width/Rate adapter

Figure 3-11 shows an example of a WidthAdapter that has been parametrized to add buffer stages.



1095

FIGURE 3-11: WIDTHADAPTER WITH RATEADAPTATION

3.4.2 Mapping CDTI to SMI field

1098

CDTI connects to other concerto units via a Symphony Messaging Interface (SMI), which encapsulates concerto messages as shown in Table 3-4.

TABLE 3-4: SMI TO CONCERTO MESSAGE MAPPING

SMI NDP Mapping	
SMI	Concerto Message
ndp_targ_id	{target_id, fPortId}
ndp_src_id	{initiator_id, fPortId}
ndp_steer	steering
ndp_msg_tier	t_tier
ndp_msg_qos	ql
ndp_pri	priority
ndp_len	wNdpBits parameter
ndp_ndp	See cpr/concMsg. This can include m_prot if SMI message protection is enabled. Note wMProt is based on the NDP width per message type.
ndp_dp_present	1 for DTWReq and DTRReq, otherwise 0
ndp_msg_id	message_id
ndp_msg_user	{Header protection bits (if enable SMI header protection) }
ndp_msg_err	0 (unused)
SMI DP Mapping	
SMI	Concerto Message
dp_last	last
dp_data	data
dp_user	NUM_DW_PER_BEAT x {dbad, dwid, dprot(if enable SMI data protection), be, user}

1101

3.4.3 Mapping CDTI to ATP field

Ncore 3 supports only Header Parallel packet style.

- Header Parallel means the first beat of a packet contains both header and data information and if subsequent data beats are needed, the following beats contain no header. The width of the ATP link in the header parallel style is set by the width of the header and width of the Data Phit. No Extra packetization latency added in this style.
 - The interface width is sum of header packet payload and data payload. That is, ATP interface width will match with SMI interface width.
 - This is mainly to maximize performance while spending more area.

The ATP link is defined by the following parameters:

- Maximum packet size.
- Flit Data Width
- Packet Style
- Header parallel (referred to as parallel)
- Header serial (referred to as serial)
- The below is ATP signals in the network.

TABLE 3-5: ATP SIGNAL IN THE NETWORK

Signal	I/O	Description	Width	Optional	Parametrizable	Note
Valid	O	1'b1 Indicates the present beat has valid data from master	Number of VCs	No	Yes	1 in NCore 3
Ready	I	1'b1 Indicates slave can accept beat this cycle	Number of VCs	No	Yes	1 in NCore3
First	O	1'b1 indicates first beat of packet.	1	No	No	
Last	O	1'b1 indicates last beat of packet.	1	No	No	
Bus	O	Contains the contents of the packet	Variable	No	Yes	
Pressure	O	The pressure of the present beat	Variable	Yes	Yes	Not in Core3
Prot	O	The protection bits of the output of the present beat	Variable	Yes	Yes	Not in Core3
Prob_b	I	The protection bits of the input of the present beat	Variable	Yes	Yes	Not in Core3

1119

3.4.4 CDTI Connectivity

The two next sections go over CDTI connectivity of different Ncore 3 units. The section 3.4.6 specifies how the connectivity must be optimized to take advantage of Ncore 3 unit and port interleaving commonality. Furthermore, it also specifies when certain connectivity can be removed by choice and how Ncore 3 units should report run time errors in these scenarios. The objective here is to optimize the network and remove any possible unused connectivity by the configuration.

1122

1125

3.4.5 Connectivity mapping

This section specifies the full connectivity mapping without any optimizations.

1128 CN0 is for control network 0, CN1 is for control network 1, CN2 is for control network 2, CN3 is for control network 3, and DN is for data network. The mapping for the control and data network in 4CN1DN configuration is shown in Table 3-6.

1131 3CN1DN configuration is achieved by combining CN1 and CN3

2CN1DN configuration is achieved by combining CN1 and CN2 and CN3

1CN1DN configuration is achieved by combining all the CNs

1134 Notes:

*1: if SysEventReceiver is instantiated in the unit: the unit is expected to receiver Inbound event messages, and requires Rx SysReq and Tx SysRsp

1137 *2: if SysEventSender is instantiated in the unit: the unit is expected to send outbound event messages, and requires Tx SysReq and Rx SysRsp

1140 TABLE 3-6: SYSTEM CONTROL AND DATA NETWORK MAPPING

Unit	Control Network 0 (CN0)		Control Network 1 (CN1)		Control Network 2 (CN2)		Control Network 3 (CN3)		Data Network (DN)	
	Tx Msg	Rx Msg	Tx Msg	Rx Msg	Tx Msg	Rx Msg	Tx Msg	Rx Msg	Tx Msg	Rx Msg
CAIU - CHI										
	CmdReq	StrReq	StrRsp	CmdRsp			DtrRsp	DtrRsp	DtwReq/ DtwDbgReq	DtrReq
	SysReq	SnpReq	SnpRsp	CmpRsp					DtwRsp/ DtwDbgRsp	DtrReq
		SysReq	SysRsp	SysRsp						
CAIU - ACE										
	CmdReq	StrReq	StrRsp	CmdRsp			DtrRsp	DtrRsp	DtwReq/ DtwDbgReq	DtrReq
	SysReq	SnpReq	SnpRsp	CmpRsp					DtwRsp/ DtwDbgRsp	DtrReq
	UpdReq	SysReq	SysRsp	SysRsp						
				UpdRsp						
NCAIU (ACE5-Lite with DVM)										
	CmdReq	StrReq	StrRsp	CmdRsp			DtrRsp		DtwReq/ DtwDbgReq	DtrReq
	SysReq	SnpReq	SnpRsp	SysRsp					DtwRsp/ DtwDbgRsp	
		SysReq(*1)	SysRsp(*1)	CmpRsp						
NCAIU (AXI with proxy cache)										
	CmdReq	StrReq	StrRsp	CmdRsp			DtrRsp	DtrRsp	DtwReq/ DtwDbgReq	DtrReq
	SysReq	SnpReq	SnpRsp	SysRsp					DtwRsp/ DtwDbgRsp	DtrReq
	UpdReq	SysReq	SysRsp	UpdRsp						
NCAIU (AXI without proxy cache/ACE-Lite/ACE5-Lite without DVM)										
	CmdReq	StrReq	StrRsp	CmdRsp			DtrRsp		DtwReq/ DtwDbgReq	DtrReq
	SysReq(*2)	SysReq(*1)	SysRsp(*1)	SysRsp(*2)					DtwRsp/ DtwDbgRsp	
DCE										
	StrReq	CmdReq	CmdRsp	SnpRsp	MrdReq	MrdRsp				
	SnpReq	SysReq	SysRsp	StrRsp	RbrReq	RbrRsp				
	SysReq	UpdReq	UpdRsp	SysRsp						

Unit	Control Network 0 (CN0)		Control Network 1 (CN1)		Control Network 2 (CN2)		Control Network 3 (CN3)		Data Network (DN)	
	Tx Msg	Rx Msg	Tx Msg	Rx Msg	Tx Msg	Rx Msg	Tx Msg	Rx Msg	Tx Msg	Rx Msg
DII										
	StrReq	CmdReq	CmdRsp	StrRsp			DtwRsp	DtwDbgRsp	DtrReq	DtwReq
	SysReq(*2)			SysRsp(*2)				DtrRsp	DtwDbgReq	
DMI										
	StrReq	CmdReq	CmdRsp	StrRsp	MrdRsp	MrdReq	DtwRsp	DtwDbgRsp	DtrReq	DtwReq
	SysReq(*2)			SysRsp(*2)	RbrRsp	RbrReq		DtrRsp	DtwDbgReq	
DVE										
	StrReq	CmdReq	CmdRsp	StrRsp			DtwRsp/ DtwDbgRsp			DtwReq/ DtwDbgReq
	SnpReq	SysReq	SysRsp	SnpRsp						
	SysReq		CmpRsp	SysRsp						

Connectivity between different Ncore 3 units is shown in Table 3-7:Connectivity mapping . The top row and the left most column specify the Ncore 3 unit names, the intersection point specifies the networks that connect the two units. Intersection points that are empty signifies that there are no connections between the corresponding units.

1143

TABLE 3-7:CONNECTIVITY MAPPING

	CAIU	NCAIU	DCE	DII	DMI	DVE
CAIU	DN CN3	DN CN3	CN0 CN1	CN0 CN1 CN3 DN	CN0 CN1 CN3 DN	CN0 CN1 CN3 DN
NCAIU	DN CN3	DN CN3	CN0 CN1	CN0 CN1 CN3 DN	CN0 CN1 CN3 DN	CN0 CN1 CN3 DN
DCE	CN0 CN1	CN0 CN1			CN2	CN0 CN1
DII	CN0 CN1 CN3 DN	CN0 CN1 CN3 DN				CN0 CN1
DMI	CN0 CN1 CN3 DN	CN0 CN1 CN3 DN	CN2			CN0 CN1
DVE	CN0 CN1 CN3 DN	CN0 CN1 CN3 DN	CN0 CN1	CN0 CN1	CN0 CN1	

1149

Detailed TX and RX connectivity between Ncore 3 units for different networks are shown in Table 3-8,

Table 3-9, Table 3-10, Table 3-11 and Table 3-12. The top row and the left most column specify the Ncore 3 unit names, the intersection point specifies the connectivity. The direction of connectivity is from column name perspective, i.e. the port names TX/RX specifies the connectivity on the column unit.

1152

TABLE 3-8: CN0 TX RX CONNECTIVITY MAP

	CAIU CHI	CAIU ACE	NCAIU AXI W Cache	NCAIU AXI No Cache	NCAIU ACE-Lite	NCAIU ACE5-Lite	DCE	DII	DMI	DVE
CAIU CHI							TX/RX	TX/RX	TX/RX	TX/RX
CAIU ACE							TX/RX	TX/RX	TX/RX	TX/RX
NCAIU AXI W Cache							TX/RX	TX/RX	TX/RX	TX/RX
NCAIU AXI No Cache							TX/RX	TX/RX	TX/RX	RX(*2)/TX(*1)
NCAIU ACE-Lite							TX/RX	TX/RX	TX/RX	RX(*2)/TX(*1) with DVM: TX/RX(*1)
NCAIU ACE5-Lite							TX/RX	TX/RX	TX/RX	RX(*2)/TX(*1) with DVM: TX/RX(*1)
DCE	TX/RX	TX/RX	TX/RX	TX/RX	TX/RX	TX/RX				RX
DII	TX/RX	TX/RX	TX/RX	TX/RX	TX/RX	TX/RX				RX(*2)
DMI	TX/RX	TX/RX	TX/RX	TX/RX	TX/RX	TX/RX				RX(*2)
DVE	TX/RX	TX/RX	TX/RX	TX(*2)/RX(*1)	TX(*2)/RX(*1) with DVM: TX/RX(*1)	TX(*2)/RX(*1) with DVM: TX/RX(*1)	TX	TX(*2)	TX(*2)	

1155

TABLE 3-9: CN1 TX RX CONNECTIVITY MAP

	CAIU CHI	CAIU ACE	NCAIU AXI W Cache	NCAIU AXI No Cache	NCAIU ACE-Lite	NCAIU ACE5-Lite	DCE	DII	DMI	DVE
CAIU CHI							TX/RX	TX/RX	TX/RX	TX/RX
CAIU ACE							TX/RX	TX/RX	TX/RX	TX/RX
NCAIU AXI W Cache							TX/RX	TX/RX	TX/RX	TX/RX
NCAIU AXI No Cache							TX/RX	TX/RX	TX/RX	RX(*1)/TX(*2) with DVM: RX(*1)/TX
NCAIU ACE-Lite							TX/RX	TX/RX	TX/RX	RX(*1)/TX(*2) with DVM: RX(*1)/TX
NCAIU ACE5-Lite							TX/RX	TX/RX	TX/RX	RX(*1)/TX(*2) with DVM: RX(*1)/TX
DCE	TX/RX	TX/RX	TX/RX	TX/RX	TX/RX	TX/RX				TX
DII	TX/RX	TX/RX	TX/RX	TX/RX	TX/RX	TX/RX				TX(*2)
DMI	TX/RX	TX/RX	TX/RX	TX/RX	TX/RX	TX/RX				TX(*2)
DVE	TX/RX	TX/RX	TX/RX	TX(*1)/RX(*2) with DVM: TX(*1)/RX	TX(*1)/RX(*2) with DVM: TX(*1)/RX	TX(*1)/RX(*2) with DVM: TX(*1)/RX	RX	RX(*2)	RX(*2)	

TABLE 3-10: CN2 TX RX CONNECTIVITY MAP

	CAIU CHI	CAIU ACE	NCAIU AXI W Cache	NCAIU AXI No Cache	NCAIU ACE-Lite	NCAIU ACE5-Lite	DCE	DII	DMI	DVE			
CAIU CHI													
CAIU ACE													
NCAIU AXI W Cache													
NCAIU AXI No Cache													
NCAIU ACE-Lite													
NCAIU ACE5-Lite													
DCE									TX/RX				
DII													
DMI						TX/RX							
DVE													

1158

TABLE 3-11: CN3 TX RX CONNECTIVITY MAP

	CAIU CHI	CAIU ACE	NCAIU AXI W Cache	NCAIU AXI No Cache	NCAIU ACE-Lite	NCAIU ACE5-Lite	DCE	DII	DMI	DVE			
CAIU CHI	TX/RX	TX/RX	TX/RX	TX	TX	TX/RX		TX/RX	TX/RX	TX			
CAIU ACE	TX/RX	TX/RX	TX/RX	TX	TX	TX		TX/RX	TX/RX	TX			
NCAIU AXI W Cache	TX/RX	TX/RX	TX/RX	TX	TX	TX		TX/RX	TX/RX	TX			
NCAIU AXI No Cache	RX	RX	RX							TX/RX	TX/RX	TX	
NCAIU ACE-Lite	RX	RX	RX							TX/RX	TX/RX	TX	
NCAIU ACE5-Lite	TX/RX	RX	RX							TX/RX	TX/RX	TX	
DCE													
DII	TX/RX	TX/RX	TX/RX	TX/RX	TX/RX	TX/RX							TX
DMI	TX/RX	TX/RX	TX/RX	TX/RX	TX/RX	TX/RX							TX
DVE	RX	RX	RX	RX	RX	RX			RX	RX			

1161

TABLE 3-12: DN TX RX CONNECTIVITY MAP

	CAIU CHI	CAIU ACE	NCAIU AXI W Cache	NCAIU AXI No Cache	NCAIU ACE-Lite	NCAIU ACE5-Lite	DCE	DII	DMI	DVE		
CAIU CHI	TX/RX	TX/RX	TX/RX	RX	RX	TX/RX				TX/RX	TX/RX	RX
CAIU ACE	TX/RX	TX/RX	TX/RX	TX/RX	RX	RX				TX/RX	TX/RX	RX
NCAIU AXI W Cache	TX/RX	TX/RX	TX/RX	TX/RX	RX	RX				TX/RX	TX/RX	RX
NCAIU AXI No Cache	TX	TX	TX	TX						TX/RX	TX/RX	RX

	CAIU CHI	CAIU ACE	NCAIU AXI W Cache	NCAIU AXI No Cache	NCAIU ACE-Lite	NCAIU ACE5-Lite	D C E	D I I	D M I	D V E
NCAIU ACE-Lite	TX	TX	TX					TX /R X	TX /R X	R X
NCAIU ACE5-Lite	TX/RX	TX	TX					TX /R X	TX /R X	R X
DCE										
DII	TX/RX	TX/RX	TX/RX	TX/RX	TX/RX	TX/RX				R X
DMI	TX/RX	TX/RX	TX/RX	TX/RX	TX/RX	TX/RX				R X
DVE	TX	TX	TX	TX	TX	TX		TX	TX	

3.4.6 Connectivity Optimization

1164

This section goes over connectivity optimizations that must be applied to remove connections from the full connectivity described in section 3.4.6.

1167

3.4.6.1 Removing connectivity

1170

Depending on the system requirements a customer may choose to design a system where only a subset of AIUs may talk to only a subset of DILs, this includes CSR configuration DIL. Following is required

SW requirements:

1173

- Provide GUI/TCL way to delete connections (all routes for all messages) between any AIUs and DILs with following restriction
 - If an AIU is specified as CSR access capable AIU where parameter fnCsrAccess is set, then the customer must not be able to delete connection to CSR configuration DIL
- Make sure the parameter hexAiuDilVec is set correctly once the connections are deleted

1176

HW requirements:

1179

- If a transaction gets decoded to a DIL to which the AIU is not connected based on port tie offs associated with parameters hexAiuDilVec; then report an error as address decode error with additional information as specified for error type code 0x7

1182

3.4.6.2 AIU – DCE Connectivity Optimization

1185 In cases where interleaving address bit commonality is present between an AIU group (AIU ports marked as interleaved) and DCE interleaving then the connection between them must be optimized.

- 1188
- If interleaving granularity is same and all address bits match, then optimization must be implemented i.e. connectivity becomes one to one
 - If interleaving granularity is same and necessarily all address bits do not match but at-least one or more bit at the same index match, then optimization must be implemented. The level optimization depends on number of address bits that match.
 - If interleaving granularity is same and all address bits do not match, then no optimization is required
- 1191

1194 Detailed examples for different combinations of 2-way and 4-way interleaving are shown in Table 3-13. In the example AIUs and DCEs are numbered as follows for 4-way interleaving

- 1197
- 00 → AIU0, DCE0
 - 01 → AIU1, DCE1
 - 10 → AIU2, DCE2
 - 11 → AIU3, DCE3
- 1200

1203

TABLE 3-13: AIU DCE INTERLEAVING EXAMPLE

Scenario	AIU interleaving address bits	DCE interleaving address bits	Optimization	Comment
2-way interleaved AIU and 2-Way interleaved DCE	X	X	AIU0 → DCE0 AIU1 → DCE1	One to one completely optimized connectivity
	X	Y	AIU0 → DCE0, DCE1 AIU1 → DCE0, DCE1	No optimization complete cross bar
4-way interleaved AIU and 4-way interleaved DCE	X, Y	X, Y	AIU0 → DCE0 AIU1 → DCE1 AIU2 → DCE2 AIU3 → DCE3	One to one completely optimized connectivity
	X, Y	X, A	AIU0 → DCE0, DCE1 AIU1 → DCE0, DCE1 AIU2 → DCE2, DCE3 AIU3 → DCE2, DCE3	Partially 1 to 2 optimized as the MSB bit is same and the LSB bit is not same
	X, Y	A, Y	AIU0 → DCE0, DCE2 AIU1 → DCE1, DCE3 AIU2 → DCE0, DCE2 AIU3 → DCE1, DCE3	Partially 1 to 2 optimized as the LSB bit is same and the MSB bit is not same
	X, Y	A, B	AIU0 → DCE0, DCE1, DCE2, DCE3 AIU1 → DCE0, DCE1, DCE2, DCE3 AIU2 → DCE0, DCE1, DCE2, DCE3 AIU3 → DCE0, DCE1, DCE2, DCE3	Complete cross bar, both bits are different.
	X	X, A	AIU0 → DCE0, DCE1 AIU1 → DCE2, DCE3	Partially 1 to 2 optimized as the MSB bit is same

Scenario	AIU interleaving address bits	DCE interleaving address bits	Optimization	Comment
2-way interleaved AIU and 4-Way interleaved DCE	X	A, X	AIU0 → DCE0, DCE2 AIU1 → DCE1, DCE3	Partially 1 to 2 optimized as the LSB bit is same
	X	A, B	AIU0 → DCE0, DCE1, DCE2, DCE3 AIU1 → DCE0, DCE1, DCE2, DCE3	No optimization complete cross bar
4-way interleaved AIU and 2-Way interleaved DCE	X, Y	X	AIU0 → DCE0 AIU1 → DCE0 AIU2 → DCE1 AIU3 → DCE1	2 to one optimization as the MSB bit matches
	X, Y	Y	AIU0 → DCE0 AIU1 → DCE1 AIU2 → DCE0 AIU3 → DCE1	2 to one optimization as the LSB bit matches
	X, Y	A	AIU0 → DCE0, DCE1 AIU1 → DCE0, DCE1 AIU2 → DCE0, DCE1 AIU3 → DCE0, DCE1	No optimization complete cross bar 1) only LSB bit matches 2) none of the bits match

1206

SW requirements:

- Make sure the parameter hexAiuDceVec is set correctly once the connections are optimized
- Compute nDceConnectedCas and nAiuConnectedDces

1209

HW requirements:

- If a transaction gets decoded to a DCE to which the AIU is not connected based on port tie offs associated with parameter hexAiuDceVec; then report an error as address decode error with additional information as specified for error type code 0x7

1212

3.4.6.3 AIU/DCE – DMI Connectivity Optimization

1215

In cases where interleaving address bit commonality is present between an AIU group (AIU ports marked as interleaved) / DCEs and DMI interleaving, then the connection between them must be optimized.

1218

- If interleaving granularity is same and all address bits match, then optimization must be implemented i.e. connectivity becomes one to one
- If interleaving granularity is same and necessarily all address bits do not match but at-least one or more bit at the same index match, then optimization must be implemented. The level optimization depends on number of address bits that match.
- If interleaving granularity is same and all address bits do not match, then no optimization is required

1221

In the case of DMI commonality must be considered across the different interleaving options specified, if there is an intersection then optimization can be done if not then no optimization applies.

1227

SW requirements:

- 1230
- Make sure the parameters hexAiuDceVec, hexAiuDmiVec and hexDceDmiVec are set correctly once the connections are optimized
 - Compute nDmiConnectedDces and nDceConnectedDmis

HW requirements

- 1233
- If a transaction gets decoded to a DCE/DMI to which the AIU/DCE is not connected based on port tie offs associated with parameters hexAiuDceVec, hexAiuDmiVec and hexDceDmiVec; then report an error as address decode error with additional information as specified for error type code 0x7
- 1236

3.4.6.4 AIU – AIU Connectivity Optimization

1239

In cases where interleaving address bit commonality is present between interleaved AIUs, then the connection between them must be optimized based on following:

- 1242
- AIUs within a single interleaved group must have all connectivity between them optimized.
 - AIUs across interleaved groups; if the interleaved address bit/s are not same for any two or more AIUs then all connectivity between these AIUs must be optimized. This is irrespective of the granularity of interleaving
- 1245

Detailed Example is shown in Figure 3-12.

1248

In group 0, AIU0 and AIU1 are 2 way interleaved with bit 7. As they are within a single group, they do not have any connectivity between them.

In group 1, AIU2, AIU3, AIU4 and AIU5 are 4 way interleaved with bit 7,8. As they are within a single group, they do not have any connectivity between them.

1251

As there is commonality between the two groups, connections are optimized as shown where AIU0 talks with AIU2 and AIU3 as they share the interleaving bit 7 with a value of 0, same applies between AIU1 and AIU4, AIU5.

1254

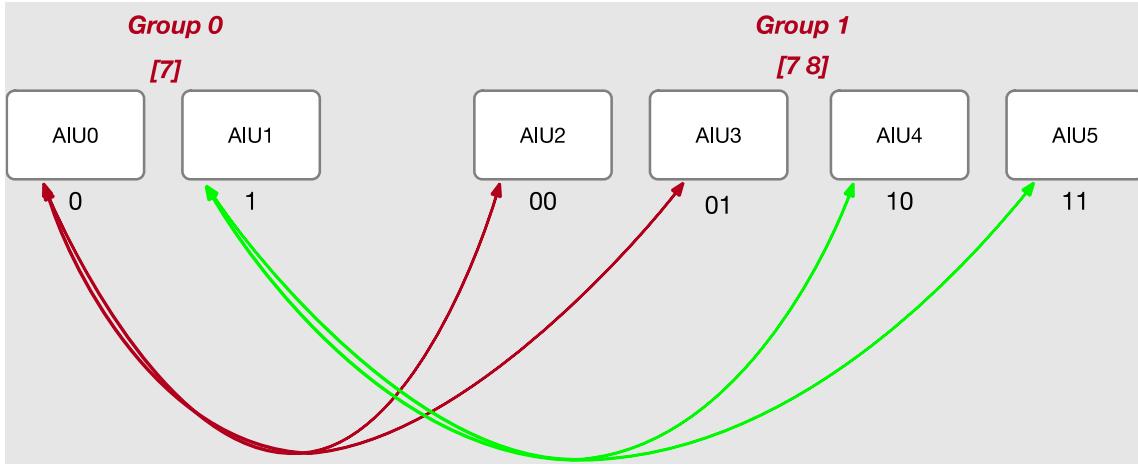
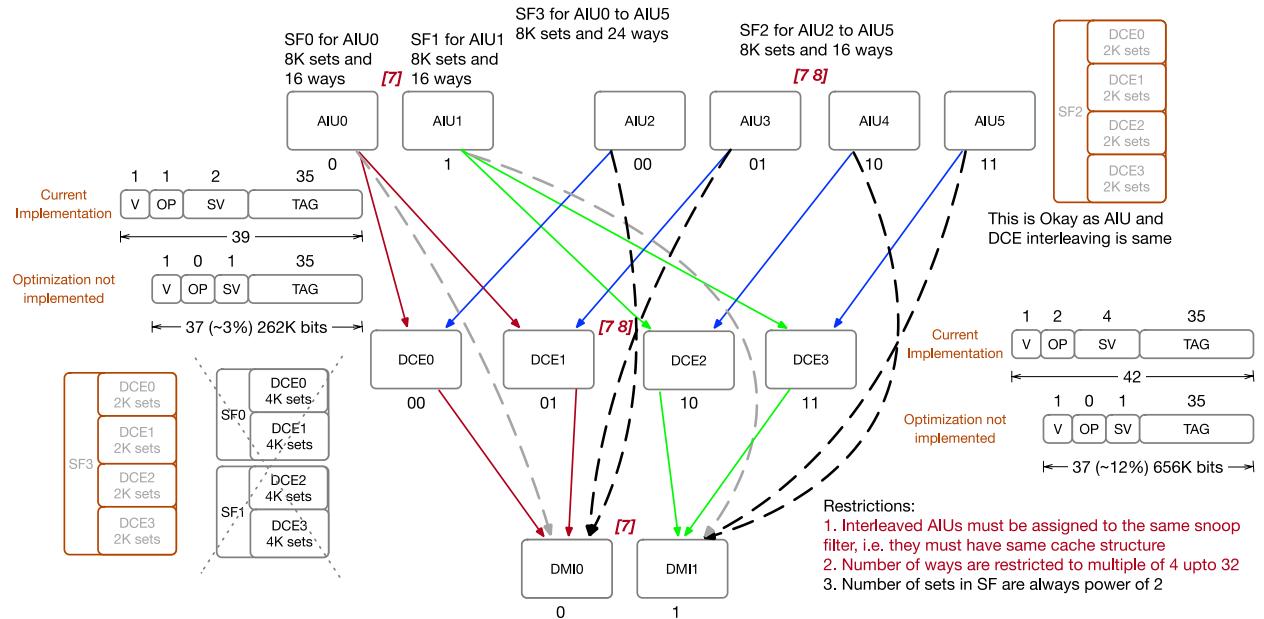


FIGURE 3-12: AIU TO AIU CONNECTIVITY

1257 3.4.6.5 Snoop filter optimizations

1260 The interleaving presents an opportunity to optimize snoop filter sharer vector. At this time these optimizations will not be implemented by Ncore 3, apart from following restrictions:

- 1263 1. Interleaved AIUs within a group must be assigned to the same Snoop filter. This restriction makes sense as it is expected that all agents connecting via interleaved ports within a group will have the same or shared cache structure.
2. Number of ways within a snoop filter must be limited to multiple of 4, with a max value of 32. This restriction is to reduce possible combinations.



3.4.6.6 Removing Rbu_rsp and Rbu_rsp from CN2

1269 In order to resolve the congestion of CN2 network in case of concurrent read and write and to improve the overall bandwidth of a Ncore 3 system, Rbu_req and Rbu_rsp messages are removed from CN2 network. The new architecture is described in the latest version of CCMP protocol specification.

1272

3.4.6.7 Credit Optimization

1275 This section goes over credit optimizations that must be implemented to compliment the connectivity optimizations. Credits in question here are build time defined credits specified for DCE i.e., nDceRbCredits and nAiuSnpCredits. Other credits do not get affected as they will be SW defined at run time. Credit parameter specification stays the same with following changes in software and hardware.

1278

SW changes:

- 1281
- nDceRbCredits are used to derive the coherent write buffer size in DMI. The size of this buffer must be limited to the sum of nDceRbCredits of only the DCEs that are connected to the DMI.
 - nAiuSnpCredits are used to derive the depth of the STT table (nSttCtrlEntries) in AIUs. The size of this STT table must be limited to sum of nAiuSnpCredits of only the DCEs that are connected to the AIU
- 1284

HW changes:

- 1287
- Implement RbCredit counters up to the number specified by the parameter nDceConnectedDmis. The offset value for Rb credits must be used from the DCE port tie off parameter hexDceDmiRbOffset.
 - Implement snoop credit counters up to the number specified by the parameter nDceConnectedCas. (This is optional, we can defer it to reduce RTL change, note that this change may help in timing)
- 1290

Note: AIUs have command credits counters, these can be optimized based on actual targets (DCEs, DMIs, DIIs) connected to the AIU.

1293

1296

3.5 Ncore CSTI Network

1299 The CSTI network is dedicated to access configuration, status and error registers in Ncore 3. It is composed of two sub networks:

1. Request network
2. Response network

1302 The CSTI network shall ensure that data written on configuration registers can be read back to confirm correct operation. It is required to implement safety measures.

1305 Similarly to CDTO network, the CSTI network implements parity or ECC checks.

3.5.1 CSTI Blocks

In addition to the four blocks listed in the CDTI network, the CSTI network adds two more blocks

1308 3.5.1.1 AXI initiator

There is one AXI initiator that is tied to a special DII unit using an AXI interface that is used to initiate all transactions into the CSTI.

1311 The AXI initiator has two ports into the CSTI network, an outgoing request port and an incoming response port.

The AXI initiator is 32 bits wide.

1314 3.5.1.2 APB target

The widths of all the CSTI blocks are fixed at 32 bits, which is a width that is not available in the CDTI network. Please refer to Legato section for details on these components.

1317 Every block in Ncore 3 that contains a register that can be read or written will have an APB port on it. The APB target block connects this port to the CSTI network. It converts requests from the AXI Initiator to APB transactions on the APB interface returns the responses to the AXI Initiator. All transactions generate responses, so when a write completes the APB Target sends a completion response back to the AXI initiator.

1323 The APB Target has two ports into the CSTI network, an incoming request port and an outgoing response port.

APB targets are 32 bits wide.

3.6 Addressing in CTFs

1326 3.6.1 Fabric Unit Identification

When an Ncore 3 unit sends a message to another Ncore 3 unit, the receiver of the message must be uniquely identified. For this purpose, each Ncore 3 unit in the Ncore 3 platform system is also identified by a *globally unique identifier* value called the **Fabric Unit Id (FUID)**. This unique identifier is used as part of the Initiator Id or Target Id in the header of a Concerto C message.

There is no specific requirement on the way the units are assigned identifiers.

1332

Example:

FUIDs in an Ncore 3 system are numbered from 0 to $(N-1)$, where N equals the total number of Ncore 3 units, and each unit, based on its type, is numbered within this name space as follows:

1335

- 0 to $(A-1)$: AIUs, where A equals the number of C-AIUs
- A to $(A+B-1)$: NC-AIUs, where B equals the number of NC-AIUs
- $(A+B)$ to $(A+B+D-1)$: DCEs, where D equals the number of DCEs
- $(A+B+D)$ to $(A+B+D+M-1)$: DMIs, where M equals the number of DMIs
- $(A+B+D+M)$ to $(A+B+D+M+I-1)$: DIIs, where I equals the number of DIIs
- $(A+B+D+M+I)$: DVE. An Ncore 3 system is expected to have 1 DVE.

1338

Note: $A+B+D+M+I+1$ equals N .

Primary input: Each Ncore 3 unit must implement the ability to receive its FUIDs as a primary input. Primary input means input using strap pins (tie-off signal), to get input value not at configuration time but at runtime. The main purpose of this is to support stamping.

1341

FUIDBase + FUNITOffset: As described earlier Ncore 3 could have more than one network. Also, we could stamp Ncore 3 network using FUIDs. In that case, to support unique ID to each Ncore 3 unit, we are using FUnitBase and FUIDOffset.

1344

- FUIDBase is FUID for each network.
- FUIDOffset is supplied as a parameter (or as a tie-off signals) to provide offset for the network to provide unique ID.

1347

NOTE: FUIDOffset = 0 in NCore 3

3.6.2 Message Target Identification

1353

An Ncore unit, in general, may connect to a given CDTI network via one or more terminal, TX and/or RX, and to one or more of CDTI networks, as necessary.

1356

The Target Id field in the header of the message must uniquely identify a destination RX terminal block within a CDTI network. To achieve that, the Target Id field is defined to be a concatenation of two subfields:

1359

- Target Unit Id: A unique identifier for the unit within the Ncore system. (FUnitId)
- Target Port Id: A unique identifier associated with the RX SMI interface of the said unit on which the message will be received. Target Port Ids are assigned integer values (0, 1, 2, 3, etc.) starting at 0. Thus, if a unit carries one or more RX SMIs, then there must be a Target Port Id of 0.

1362

If the unit attaches to a network via multiple RX SMIs, then the Target Port Id is used to disambiguate between those ports.

1365

The Target Port Id field is 0 or more bits long, as necessary. Its length is determined by the maximum of the minimum number of bits needed by any of the units connected to the network to uniquely identify all of its RX ports (= MAX (log₂(# RX ports for a network unit))). This length is applied to all the Target Ids for that network.

1368

Thus, for example, if a network has one unit with 2 RX ports, one with 3 RX ports, and all others with 1 RX port, the width of the Target Port Id field must be 2 bits, as needed by the unit with 3 RX ports.

3.6.3 Message Initiator Identification

1371

The message header also includes the Initiator Id. It is provided so that target unit can send a response message back to the initiator.

Like the Target Id, Initiator Id is also a concatenation of two sub-fields:

1374

- Initiator Unit Id: A unique identifier for the unit within the Ncore system.
- Initiator Port Id: A unique identifier associated with the TX SMI interface of the said unit on which the message is being transmitted.

1377

The Initiator Port Id field is 0 or more bits long, as necessary. Its length is determined by the maximum of the minimum number of bits needed by any of the units connected to the network to uniquely identify all of its TX ports (= MAX (log₂(# TX ports for a network unit))). This length is applied to all the Initiator Port Ids for that network.

1380

4 Protocol Layer

1383

In a shared memory multiprocessor containing caches, coherency support is necessary to ensure correctness of computations. In addition, co computation requires the enforcement of consistency among values of multiple data locations accessed. This chapter describes the support for coherency and consistency within an Ncore 3 system.

1386

4.1 Introduction

1389

SoCs include function blocks that initiate storage accesses. These function blocks are called **agents**. Agents can include **coherent agents** such as processors or processor clusters that incorporate cache hierarchies that must be kept coherent, as well as **non-coherent agents** that do not themselves hold copies of data that have to be kept coherent, but nonetheless may make coherent accesses to system memory and thereby do interact with coherent agents and access contents of their cache hierarchies. Both coherent and non-coherent⁵ agents can also make storage accesses that do not require enforcement of coherency, as well as other types of requests.

1392

SoC function blocks that don't initiate storage accesses but might receive storage accesses and might fulfill them are referred to as **target devices**.

1395

Ncore 3 enables implementations of cache coherency subsystems for SoCs that can support coherent accesses, as well as non-coherent accesses via them; latter to account particularly for providing efficient and full-function connectivity for agents that might use a common pathway to issue both types of accesses and for connecting devices, such as memory, that may be the targets for both types of accesses.

1401

Ncore 3 units implement a messaging protocol called the **Concerto C Messaging Protocol (CCMP)** to execute storage accesses and other requests, and their semantic actions.

1404

Only a subset of messages in CCMP and associated semantics are utilized in enforcement of coherency in Ncore 3. This subset is referred to as **Concerto Coherency Protocol (CCP)**.

1407

Agents in an SoC are connected via their **native interfaces** to **Agent Interface Units (AIUs)** in the Ncore 3 systems⁶. The agents make their requests over their native interface. The AIUs translate these into CCMP messages. These original messages result in subsequent messages being exchanged among appropriate NCore units.

1410

⁵ IO and peripheral devices are non-coherent devices.

⁶ For example, a processor may connect via CHI interface or a peripheral device might connect via an AXI interface.

All Ncore 3 units, AIUs, DCEs, DMIs, DIIs, and DVEs, participate in the CCMP are thus considered part of the **CCMP-domain**.

1413 Those units involved in the protocol activity related to coherency enforcement are also considered to be part of the **coherency-domain**. These typically include AIUs, DCEs, and DMIs.

1416 CCMP also supports maintenance of coherence among **MMU TLBs**. That coherency domain includes AIUs and the DVE.

4.2 Storage Classification

Ncore 3 categorizes the totality of storage within an SoC into two classes:

- 1419
- System memory, and
 - Peripheral storage

1422 Typically, system storage is implemented via Dynamic or Static RAM devices. Peripheral storage typically includes Control and Storage registers within peripheral devices, although it might include buffers and RAM devices.

1425 In a Concerto C based system, **system memory** refers to storage that is **well-behaved**.⁷ For such storage a write to a given memory location updates the value stored at that location and a read from a memory location returns the last value written to that memory location. Furthermore, performing an access to system memory does not have side-effects.

1428 **Peripheral storage** is not guaranteed to be well-behaved. As such, data values in such locations may not be persistent, e.g. two reads without an intervening write may not return the same value, or a read may not return the last value written. Additionally, a read or write access may cause side-effects.

1431 In Concerto C, coherency is enforced only on system memory locations, although these locations may also be accessed via Concerto C protocol without requiring that coherence be enforced during such accesses.

1434 System memory is divided into equal-sized data granules called **cachelines**, on which coherence is maintained. Each cacheline consists of a contiguous block of a power-of-two number of bytes and is uniquely identified by a **cacheline address**, which is a system memory address aligned to the size, in bytes, of a cacheline. An agent may buffer a copy of a cacheline, or a **cacheline copy**, in its cache.⁸

Memory accesses are classified relative to the size and alignment of a cacheline. A memory access that operates on all the bytes within a cacheline-aligned data granule is a **full-cacheline access**. A memory

⁷ Well-behaved storage is also referred to as “normal” storage.

⁸ Depending on the context, the term cacheline may refer to a container for data granule or the data granule itself.

1440 access that operates on a, possibly non-contiguous, subset of the bytes within a cacheline-aligned data granule is a **partial-cacheline access**. Finally, a memory access that operates on bytes in two or more cacheline-aligned data granules is classified as a **multiple-cacheline access**.

1443 Concerto C does not support multi-cache line accesses or those that span a cacheline address boundary. Ncore 3 supports 64-Byte cache lines.

4.3 Coherency protocol features

4.3.1 Cacheline states

1446 The data that can be kept coherent is located in system memory. CCP maintains coherency among copies of a cacheline in agent caches and its value in system memory ensuring that the latest value assigned to the data granule is never lost.

1449 The CCP allows a coherent agent to hold a partial cacheline, but for the sake of the coherency the protocol doesn't distinguish it from the agent holding a full copy of the cacheline.

1452 The CCP supports the following properties for cachelines in caches within an agent:

- **Invalid vs. Valid:** An **invalid** cacheline copy *must* not be accessed by a caching agent, while a **valid** cacheline copy may be accessed by a caching agent. A caching agent may consume cacheline data from a valid cacheline copy but may only modify cacheline data depending on the other properties of the cacheline copy.
- **Owned vs. Non-owned:** An **owned** cacheline copy is a valid cacheline copy that identifies an agent as the **cacheline owner**, who, depending on the other properties of the cacheline copy, is responsible for forwarding data in response to any snoop messages and for updating memory on a replacement. A **non-owned** cacheline copy is a valid cacheline copy that identifies an agent as a **cacheline sharer**, who has no responsibilities with respect to the protocol. There is at most one owned cacheline copy in the system at any time.
- **Shared vs. Unique:** A **shared** cacheline copy is a valid cacheline copy that may be valid in another agent's cache. A **unique** cacheline copy is a valid cacheline copy that *must* not be valid in any other agent's cache. A caching agent may modify cacheline data only if its copy of the cacheline is unique, and that modification may occur without any additional protocol transactions. There is at most one unique cacheline copy in the system at any time, and a unique cacheline copy implies the cacheline copy is also owned.
- **Clean vs. Dirty:** A **clean** cacheline copy is a valid cacheline copy that is consistent with respect to the latest copy of data, which may be present in either another agent's cache or system memory. A **dirty** cacheline copy is a valid cacheline copy that represents the latest copy of data and is known to be inconsistent with respect to system memory. Upon modifying a clean cacheline copy, a caching agent changes the state to dirty, and upon replacing a dirty cacheline copy, a caching agent must update memory. There is at most one dirty cacheline copy in the system at any time, and a dirty cacheline copy implies the cacheline copy is also owned.

1476 A cache line can be held in a cache in a state that is a combination of the above states. Examples are Shared-Clean, Unique-Clean, and Shared-Dirty.

A cacheline state may have another property when it is held in a cache.

- 1479 • **Empty vs. Partial vs. Full:** A cacheline may be held validly in a cache such that the cache hierarchy contains all of its bytes, only some of its bytes, or none.

1482 This state adds two more legal combination states of Unique-Clean-Empty, Unique-Dirty-Partial. These are not explicitly represented in Concerto C coherency protocol, but are supported effectively none-the-less by simply treating them as Unique-Clean and Unique-Dirty, respectively.

4.3.2 Supported coherency protocol classes

1485 Not all the 16 possible states based on the above state variables associated with a cache line are meaningful or legal within the CCP. But a large variety of well known coherency protocol classes, such as MESI, MOESI, etc. can be crafted by further restricting the possible legal states and transitions between them to smaller subsets. The following table shows the protocol created by limiting the set of permitted states to be a subset of legal states.

TABLE 4-1: SUBSET OF PROTOCOL CLASSES

Protocol Class	UD	UC	OD	OC
MSI	Yes	No	No	No
MFSI	Yes	No	No	Yes
MOSI	Yes	No	Yes	No
MOSIF	Yes	No	Yes	Yes
MESI/MEI	Yes	Yes	No	No
MESIF	Yes	Yes	No	Yes
MOESI	Yes	Yes	Yes	No

1491

4.3.3 Elements of Coherency Management

Cacheline copies are kept coherent by one or more **Distributed Coherence Enforcement Units (DCEs)**.

1494 Each cacheline address is associated with a single DCE, known as the **Home DCE** for that cacheline address. The Home DCE acts as the **point of serialization** for, and enforces coherence on, the given cacheline address. In a system configured with multiple DCEs, cacheline address are distributed across the DCEs using an Ncore-instance specific mapping function.

1500 Ncore 3 implements a **directory-based coherency protocol**. A DCE may implement a system **directory partition** for tracking and managing the contents of caching agent caches with respect to the addresses associated with the DCE. The directory can be configured to track the presence of a cacheline in various caches in the system as well as a specific cache which might hold the cacheline in an owner state.

When an AIU receives a coherent request from an agent, the AIU creates an appropriate CMDreq message and sends it to a DCE unit. The DCE unit consults the directory to determine which of the coherent agents must be snooped and sends the snoop messages to the corresponding AIUs.

The AIU receiving the snoops, snoop their coherent agents in turn and return their individual snoop responses. The DCE uses the responses to update its directory to reflect the new cache states.

The directory partition implemented by the DCE acts as a **snoop filter**, allowing the DCE to minimize the number of snoops that are sent out.

The CCMP primarily operates as a **Write-invalidate** style coherency protocol. Such a protocol requires that an update to a coherently maintained location by an agent results in invalidation of other copies of the cacheline that contains that location.

The CCMP also employs a **Write-Update** style coherency protocol to efficiently support **Write-stashing operations** that may be issued on ACE5-Lite and CHI-B native interfaces that allow data to be deposited directly into processor or system caches without first being written into memory.

4.4 Proxy cache

An NCAIU with an AXI interface may also be configured to instantiate a Proxy Cache that can satisfy native agent transaction from non-coherent agent.

Upon receiving a native agent transaction, an NCAIU configured with a proxy cache decode the memory type of the native agent transaction and breaks the native agent transaction into cacheline-sized cacheline transaction. Expressed on the AxCACHE signal, the memory type of the native agent transaction determines the visibility requirement of the cacheline transactions with respect to the proxy cache and memory. The proxy cache supports Normal Write-through (WT) and Normal Write-back (WB) memory types; however, Device and Non-Cacheable memory types are not supported. As a result, all native agent transactions received by an NCAIU configured with a proxy cache perform an IO cache lookup that determines whether or not the cache contains a copy of cache line.

This section describes the changes to caching model of Ncore proxy cache. Two changes are covered in this document.

1. Ownership transfer
2. Pseudo exclusive proxy cache

The general caching model stays as is, which is MOESI. No new parameters are introduced but the NcMode parameter is deprecated in this release. It must be set to 0 coherent mode when proxy cache is enabled.

4.4.1 Proxy cache allocation and visibility policies

Proxy cache allocation policy is controlled only by AxCache value of the transaction. Table 4-2 gives details on how proxy cache allocates transactions and sets visibility attributes based on AxCache values. If a cache line is allocated in the cache, then the concerto command going out on SMI must go with allocation attribute set to no allocate i.e. 0.

1539

TABLE 4-2: CACHE ALLOCATION & VISIBILITY

AxCache	Allocation	Visibility	Notes
0000	No	Late (system)	Device Non-bufferable
0001	No	Early	Device bufferable
0010	No	Late (system)	Normal Non-cacheable, Non-bufferable
0011	No	Early	Normal Non-cacheable, Bufferable
0110	Yes®/No(W)	Early	Write through no allocate / read allocate
0111	®(R)/No(W)	Early	Write back no allocate / read allocate
1010	No(R)/Yes(W)	Early	Write through write allocate
1011	No(R)/Yes(W)	Early	Write back write allocate
1110	Yes	Early	Write through read & write allocate
1111	Yes	Early	Write back read and write allocate

4.4.2 Transactions native to concerto

1542

This section goes over how native transactions are translated to concerto transactions after proxy cache look up. Table 4-3 shows different cache look up actions. Note that in Table 4-3 “X” denotes don’t care. **SZ** denotes size of the transaction which can be partial (ptl) or full. **CS** denotes current state of the cache which can be SC (shared clean), SD (shared dirty or owned), UC (unique clean) and UD (unique dirty). **AP** denotes allocation policy where NA is no allocate and AL allocate, this is determined based on Table 4-2. **NS** denotes possible next state of the cache after the transaction finishes. **Conc Msg** specifies the message to be issued into the Ncore system.

1545

1548

TABLE 4-3: CACHE LOOKUP ACTIONS

Transaction	SZ	CS	AP	NS	Conc msg	Notes
Read	X	IX	NA	IX	CmdRdNITC	Miss no allocate (no cache case)
			AL	SC/SD/UC/UD	CmdRdVld	Miss allocate
		SC	X	-	-	Cache hit
		SD	X	-	-	Cache hit
		UD	X	-	-	Cache hit
		UC	X	-	-	Cache hit
Write	Ptl	IX	NA	IX	CmdWrUnqPtl	Miss no allocate (no cache case)
			AL	UD	CmdRdUnq	Miss allocate
		SC	X	UD	CmdRdUnq	Cache hit upgrade
		SD	X	UD	CmdRdUnq	Cache hit upgrade, drop data if SD is not lost in the interim and just upgrade to UD. (Data could be from memory and thus stale)

Transaction	SZ	CS	AP	NS	Conc msg	Notes
		UC	X	UD	-	Cache hit
		UD	X	UD	-	Cache hit
	Full	IX	NA	IX	CmdWrUnqFull	Miss no allocate (no cache case)
			AL	UD	CmdMkUnq	Miss allocate
		SC	X	UD	CmdMkUnq	Cache hit upgrade
		SD	X	UD	CmdMkUnq	Cache hit upgrade
		UD	X	UD	-	Cache hit
		UC	X	UD	-	Cache hit

1551

For Write Ptl cache hit upgrade cases, current states SC or SD issues CmdRdUnq instead of CmdClnUnq.

This is done to avoid the creation of UCE and UDP state, in the case where an intervening snoop invalidates the SC and SD state.

1554

If a cache is not present, then the native commands are mapped to concerto commands using the row where allocation (AP) policy AP is NA and the next state (NS) is IX

1557

The updated proxy cache must support access to DII, these transactions are non-coherent. Native read and write transactions hitting DII/DMI GPRS with NC bit set are simply translated to CmdRdNc and CmdWrNc respectively.

1560

NcMode parameter will be deprecated and only the GPRS configuration will be honored.

Cache allocation and look up is followed based on AxCache bits for the transaction. Partial Miss allocate cases must be converted to no allocate case for non-coherent transactions. Non-coherent cache

1563

lookup actions are shown in Table 4-4. Note that final state transition for allocating read is always UC and on write is UD. This is done to make sure dirty write data is evicted back to the memory; the read data does not need to be evicted back to the memory if it is clean. This architecture does not guarantee coherency/consistency if software mixes coherent and non-coherent transactions within the same address space without taking proper precautions.

TABLE 4-4: NON-COHERENT CACHE LOOKUP ACTIONS

Transaction	SZ	CS	AP	NS	Conc msg	Notes
Read	Ptl	IX	NA	IX	CmdRdNc	Miss no allocate (no cache case)
			AL	IX	CmdRdNc	Partial allocate converted no allocate on miss
		SC	X	-	-	Cache hit
		SD	X	-	-	Cache hit
		UD	X	-	-	Cache hit
		UC	X	-	-	Cache hit
	Full	IX	NA	IX	CmdRdNc	Miss no allocate (no cache case)
			AL	UC	CmdRdNc	Miss allocate
		SC	X	-	-	Cache hit
		SD	X	-	-	Cache hit
		UD	X	-	-	Cache hit
		UC	X	-	-	Cache hit

Transaction	SZ	CS	AP	NS	Conc msg	Notes
Write	Ptl	IX	NA	IX	CmdWrNcPtl	Miss no allocate (no cache case)
			AL	IX	CmdWrNcPtl	Partial allocate converted no allocate on miss
		SC	X	UD	-	Cache hit
		SD	X	UD	-	Cache hit
		UC	X	UD	-	Cache hit
		UD	X	UD	-	Cache hit
	Full	IX	NA	IX	CmdWrNcFull	Miss no allocate (no cache case)
			AL	UD	-	Miss allocate
		SC	X	UD	-	Cache hit
		SD	X	UD	-	Cache hit
		UD	X	UD	-	Cache hit
		UC	X	UD	-	Cache hit

1569

Evictions of non-coherent transactions allocated to proxy cache do not need update commands to be sent to DCE, if they are sent, it results in extra command traffic on the network and does not have functional impact.

1572

Coherent transactions allocated to proxy cache do need update commands to be sent to DCE, they help in reducing snoop traffic by updating the snoop filter at the expense of extra command traffic on the network, if they are not sent then it may result in more snoop traffic in the network.

1575

A CSR control bit must be implemented in the cache control register to enable/disable update commands to DCE. This bit must affect update commands in general irrespective of the original allocating transaction is coherent or non-coherent.

1578

4.4.3 Proxy cache state transitions

1581

Proxy cache state transitions are detailed in this section. Table 4-5 gives details of state transition at the proxy cache when a DTR is received from the Ncore system. Table 4-6 gives details of state transition based on the snoop received at the proxy cache. Table 4-6 also gives details regarding different DtrReq and DtwReq that may be issued. The UP column refers to unique presence, here “X” means don’t care, “Y” means a UP value of 11 with a match on MPF3 field or UP value of 01 and “N” means UP value of 11 with no match on MPF3 field. Currently UP values of 00 and 10 are reserved, they can be treated as “N” case but DCE should not be sending them out and are illegal for this release. Cases that are not mentioned in the tables are not legal.

1584

1587

1590

TABLE 4-5: PROXY CACHE DTRREQ STATE TRANSITION

Transaction	CS	DtrReq	NS	Notes
Read	IX	DtrDataInv	IX	Data not cached
		DtrDataSCln	SC	
		DtrDataSDty	SD	

Transaction	CS	DtrReq	NS	Notes
		DtrDataUCln	UC	
		DtrDataUDty	UD	
Write partial	IX/SC/SD	DtrDataUCln or DtrDataUDty	UD	Merge partial data and cache
Write full	IX/SC/SD	X	UD	Replace data with write data

TABLE 4-6: CACHE SNPREQ STATE TRANSITIONS

SnpReq	CS	NS	UP	RV	RS	DC	DT[1]	DT[0]	DtrReq	DtwReq
SnpClnDtr	IX	IX	X	0	0	0	0	0	-	-
	SC	SC	N	1	1	0	0	0	-	-
	SC	SC	Y	1	1	0	1	0	DtrDataSCln	-
	SD	SD	Y	1	0	0	1	0	DtrDataSCln	-
	UC	SC	Y	1	1	0	1	0	DtrDataSCln	-
	UD	SD	Y	1	0	0	1	0	DtrDataSCln	-
SnpNoSDInt	IX	IX	X	0	0	0	0	0	-	-
	SC	SC	N	1	1	0	0	0	-	-
	SC	SC	Y	1	1	0	1	0	DtrDataSCln	-
	SD	SD	Y	1	0	0	1	0	DtrDataSCln	-
	UC	SC	Y	1	1	0	1	0	DtrDataSCln	-
	UD	SD	Y	1	0	0	1	0	DtrDataSCln	-
SnpVldDtr	IX	IX	X	0	0	0	0	0	-	-
	SC	SC	N	1	1	0	0	0	-	-
	SC	SC	Y	1	1	0	1	0	DtrDataSCln	-
	SD	SC	Y	1	1	1	1	0	DtrDataSDty	-
	UC	SC	Y	1	1	1	1	0	DtrDataSCln	-
	UD	SC	Y	1	1	1	1	0	DtrDataSDty	-
SnpInvDtr	IX	IX	X	0	0	0	0	0	-	-
	SC	IX	N	0	0	0	0	0	-	-
	SC	IX	Y	0	0	0/1 ^a	0/1 ^a	0/1 ^b	If (UP = 01) DtrDataUCln	If (UP = 11) DtwDataCln
	SD	IX	Y	0	0	0/1 ^a	0/1 ^a	0/1 ^b	If (UP = 01) DtrDataUDty	If(UP=11) DtwDataDty
	UC	IX	Y	0	0	1	1	0	DtrDataUCln	-
	UD	IX	Y	0	0	1	1	0	DtrDataUDty	-
SnpNitc	IX	IX	X	0	0	0	0	0	-	-
	SC	SC	N	1	1	0	0	0	-	-
	SC	SC	Y	1	1	0	1	0	If (TOF=CHI/AXI) DtrDataInv else DtrDataSCln	-

SnpReq	CS	NS	UP	RV	RS	DC	DT[1]	DT[0]	DtrReq	DtwReq
	SD	SD	Y	1	0	0	1	0	If (TOF=CHI/AXI) DtrDataInv else DtrDataSCln	-
	UC	UC	Y	1	0	0	1	0	DtrDataInv	-
	UD	UD	Y	1	0	0	1	0	DtrDataInv	-
SnpNitcCI	IX	IX	X	0	0	0	0	0	-	-
	SC	IX	N	0	0	0	0	0	-	-
	SC	IX	Y	0	0	0	1	0	DtrDataInv	-
	SD	IX	Y	0	0	0	1	1	DtrDataInv	DtwDataDty
	UC	IX	Y	0	0	0	1	0	DtrDataInv	-
	UD	IX	Y	0	0	0	1	1	DtrDataInv	DtwDataDty
SnpNitcMI	IX	IX	X	0	0	0	0	0	-	-
	SC	IX	N	0	0	0	0	0	-	-
	SC	IX	Y	0	0	0	1	0	DtrDataInv	-
	SD	IX	Y	0	0	0	1	0	DtrDataInv	-
	UC	IX	Y	0	0	0	1	0	DtrDataInv	-
	UD	IX	Y	0	0	0	1	0	DtrDataInv	-
SnpClnDtw	IX	IX	X	0	0	0	0	0	-	-
	SC	SC	X	1	1	0	0	0	-	-
	SD	SC	X	1	1	0	0	1	-	DtwDataDty
	UC	UC	X	1	0	0	0	0	-	-
	UD	UC	X	1	0	0	0	1	-	DtwDataDty
SnpInvDtw / SnpUnqStsh / SnpStshUnq	IX	IX	X	0	0	0	0	0	-	-
	SC	IX	X	0	0	0	0	0	-	-
	SD	IX	X	0	0	0	0	1	-	DtwDataDty
	UC	IX	X	0	0	0	0	0	-	-
	UD	IX	X	0	0	0	0	1	-	DtwDataDty
SnpInv/SnpInv vStsh	X	IX	X	0	0	0	0	0	-	-
SnpStshShd	IX	IX	X	0	0	0	0	0	-	-
	SC	SC	X	1	1	0	0	0	-	-
	SD	SD	X	1	0	0	0	1	-	DtwDataDty
	UC	SC	X	1	1	0	0	0	-	-
	UD	SD	X	1	0	0	0	1	-	DtwDataDty

1593

Notes:

- a. Set if UP == 01
- b. Set if UP ==11 and target matches

1596

4.4.4 Sharer promotion

The previous implementation of NCore (Ncore3.2) in certain scenarios read data from DMI/DRAM even when a copy of the cacheline is available in the cache upstream. This specifically happened when snoop filter ends up tracking a cacheline as only sharer and no owners. This section describes the changes implemented to promote one of the sharers as an owner for snooping and data retrieval purposes.

4.4.4.1 Unique Presence

This section goes over the unique presence field in snoop request messages Table 4-7 gives details of different encodings of the field.

TABLE 4-7: UNIQUE PRESENCE FIELD

UP	Name	Description
00	Reserved	future use for Null filters.
01	Unique Presence	This is the only copy in the system as per the Snoop filter. The snooping AIU maybe able to upgrade the Dtr type being issued to the requesting AIU
10	Reserved	Reserved
11	Unique Permission	The AIU identified in the MPF3 field is authorized to send DtrReq to the requesting AIU

4.4.4.1.1 UP = 00

This option maybe used in future for a null filter implementation where snoops are issued one at time i.e., the first caching agent's SnpReq must receive a SnpRsp before the next caching agent's SnpReq is issued. In this case any snooped AIU is authorized to issue a DtrReq. Depending on the type of request, DCE may stop issuing more SnpReq, if the Snooped AIU already sent out a DtrReq.

4.4.4.1.2 UP = 01

Unique Presence option maybe set only when one unique copy of the is cache line is present in the system. The snooped AIU in this case may upgrade the Dtr type to be issued from shared to unique. This is a legacy option that will be carried forward, benefit of this option is not quantified.

4.4.4.1.3 UP = 10

This option is reserved, with this new change in architecture the older functionality of this option is merged into UP = 11 option. This is done to simplify specification and design.

4.4.4.1.4 UP = 11

Unique Permission option is set to identify the AIU that is authorized to send the DtrReq. The Identified AIUs Funit ID is specified in the MPF3 field. If an owner is present in the system, then the owner is identified in the MPF3 field, if there are no owners and one or more sharers are present then one of the sharers is identified in the MPF3 field. The Snooped AIU is authorized to send the DtrReq if its own Funit ID matches the Funit ID in the MPF3 field of the SnpReq.

1626

4.4.4.2 DCE Details

Table 4-8 shows details on how the UP and MPF3 fields need to be set for different snoop request. X here denotes don't care, Implementation may set it zero or any random value.

TABLE 4-8: DCE UP AND MPF3 FILED SETTING

SnpReq	Condition	UP	MPF3	Notes
SnpClnDtr / SnpNoSDInt / SnpVldDtr /	Null filter	00	X	Future use
	Unique Owner/Sharer	01	X	AIU may upgrade to Unique Dtr
	Owner is identified Multiple sharers	11	Owner	
	Owner not identified Multiple Sharers	11	Find first Sharer	One of the sharer is promoted as owner
SnpInvDtr*	Null filter	00	X	Future use
	Unique Owner/Sharer	01	X	Issue DTR as per current spec of Snoop response map
	Owner is identified Multiple sharers	11	Owner	One owner and Multiple sharers are present in the system, issue DTW to DMI instead of DTR, In this case SnpRsp DC must be '0' and DT must be 2'b01
	Owner not identified Multiple Sharers	11	Find first Sharer	One of the sharers is promoted as owner, multiple sharers are present in the system, issue DTW to DMI instead of DTR , In this case SnpRsp DC must be '0' and DT must be 2'b01
SnpNitc / SnpNitcMI / SnpNitcCI	Null filter	00	X	Future use
	Unique Owner/Sharer	01	X	
	Owner is identified Multiple sharers	11	Owner	
	Owner not identified Multiple Sharers	11	Find first Sharer	One of the sharer is promoted as owner
SnpInvDtw / SnpClnDtw / SnpInv / SnpInvStsh / SnpUnqStsh / SnpStshUnq / SnpStshShd	Null filter	00	X	Future use
	Unique Owner/Sharer	01	X	AIU may do a DtwDataCln
	Owner is identified Multiple sharers	11	X	No DTR for this snoop so MPF3 is don't care
	Owner not identified Multiple Sharers	11	X	No sharer promotion in this case

*Currently DCE issues SnpInvDtw for Read Unique when there is more than one agent with the copy of

1632

CL. This will need to change so that DCE issues SnpInvDtr for all Read Unique cases with UP settings as specified in the Table 4-8 corresponding changes need to be made in AIUs. Motivation behind this

1635

change is to improve Read Unique performance when there is more than one copy of the CL in the system. The implementation of using SnpInvDtw may cause the DMI read when data is clean.

4.4.4.3 AIU Details

1638

Table 4-9 gives details on different actions the AIUs need to take based on the UP and MPF3 field in different SnpReq.

TABLE 4-9: AIU UP ACTION

SnpReq	UP	MPF3	CHI AIU RetToSrc	NCAIU with Proxy Cache	ACE AIU	Action
SnpClnDtr / SnpNoSDInt / SnpVldDtr / SnpInvDtr / SnpNitcMI / SnpNitcCI / SnpNitc	00	X	Not set	-	-	Future use
	01	X	Set	-	-	AIU may upgrade to Unique DtrReq based on the Snoop response mapping specification
	11	Match	Set	Provide data even if in SC state	Provide data if provided by the ACE agent	AIU must send out the appropriate DtrReq based on the snoop response mapping specification (for SnpInvDtr this may be a DTW based on Table 4-2)
	11	No Match	Not set	Do not provide data	Drop data if provided by the ACE agent	AIU must not send out the DtrReq
SnpInvDtw / SnpClnDtw / SnpInv / SnpUnqStsh / SnpStshUnq / SnpStshShd	00	X	Not set	-	-	Future use
	01	X	Not set	-	-	AIU may do a DtwDataCln based on the Snoop response mapping specification
	11	X	Not set	-	-	No DTR for this snoop
	11	X	Not set	-	-	No DTR for this snoop

1641

4.4.5 Relevant CSR registers with proxy cache

The following registers are related to the normal operations and controls associated with proxy cache

1644

functionalities.

TABLE 4-10 : PROXY CACHE TRANSACTION CONTROL REGISTER (xPCTCR)

Bit	Name	Description	Access	Reset Value
0	LookupEn	This bit enables proxy cache.	Read/Write	0x0
1	AllocEn	This bit enables allocation into proxy cache.	Read/Write	0x0
2	UpdateDis	This bit disables sending update commands for evictions.		
31:3	Rsvd	Reserved	Read Only	0x0

1647

TABLE 4-11 : PROXY CACHE TRANSACTION ACTIVITY REGISTER (xPCTAR)

Bit	Name	Description	Access	Reset Value
0	EvictActive	This bit is set when the unit is performing any proxy cache eviction activity and is cleared otherwise.	Read Only	0x0
1	AllocActive	This bit is set when the unit is performing any proxy cache allocation activity and is cleared otherwise.	Read Only	0x0
31:2	Rsvd	Reserved	Read Only	0x0

TABLE 4-12 : PROXY CACHE INITIALIZATION STATUS REGISTER (xPCISR)

Bit	Name	Description	Access	Reset Value
0	TagInitDone	This bit is set when PC tag initialization is done	Read Only	0x0
1	DataInitDone	This bit is set when PC data initialization is done	Read Only	0x0
31:2	Rsvd	Reserved	Read Only	0x0

1650

TABLE 4-13 : PROXY CACHE MAINTENANCE CONTROL REGISTER (xPCMCR)

Bit	Name	Description	Access	Reset Value
3:0	MntOp	This field encodes the cache maintenance operation to be performed: 0x0: Initialize all Entries 0x1-0x3: Reserved 0x4: Flush All Entries 0x5: Flush Entry at Set and Way 0x6: Flush Entry at Address 0x7: Flush Address Range 0x8: Flush Set Way Range 0x9-0xB: Reserved 0xC: Debug Read Entry at set, way, and word 0xD: Reserved 0xE: Debug Write Entry at set, way, and word 0xF: Reserved	Read/Write	0x0
15:4	Rsvd	Reserved	Read Only	0x0
21:16	ArrayID	This field selects the array on which the cache maintenance operation is to be performed: 0x00: Tag Array 0x01: Data Array 0x02-0x3F: Reserved	Read/Write	0x0
22	SecAttr	This bit indicates the value of the security attribute of the address for the cache maintenance operation is to be performed. If the cache maintenance operation does not operate on an address, the value of this bit should be zero.	Read/Write	0x0
31:23	Rsvd	Reserved	Read Only	0x0

1653

TABLE 4-14 : PROXY CACHE MAINTENANCE ACTIVITY REGISTER (xPCMAR)

Bit	Name	Description	Access	Reset Value
0	MntOpActv	This bit is set when any cache maintenance operation is in progress and is clear otherwise	Read/Write	0x0
31:2	Rsvd	Reserved	Read Only	0x0

TABLE 4-15 : PROXY CACHE MAINTENANCE LOCATION REGISTER 0 (xPCMLR0)

Bit	Name	Description	Access	Reset Value
19:0	MntSet	The field indicates the set on which the maintenance operation is to be performed.	Read/Write	0x0
25:20	MntWay	This field indicates the way on which the maintenance operation is to be performed.	Read/Write	0x0
31:26	MntWord	This field indicates the data word on which the maintenance operation is to be performed.	Read/Write	0x0

1656

TABLE 4-16 : PROXY CACHE MAINTENANCE LOCATION REGISTER 1 (xPCMLR1)

Bit	Name	Description	Access	Reset Value
15:0	MntAddr	This field contains the high-order address bits [53:38] of the byte address on which the maintenance operation is to be performed	Read/Write	0x0
31:16	MntRange	This field indicates the range for flush operations in number of cache lines. This field is used when doing flushes based on address or set/way range.	Read/Write	0x0

1659

TABLE 4-17 : PROXY CACHE MAINTENANCE DATA REGISTER (xPCMDR)

Bit	Name	Description	Access	Reset Value
31:0	MntData	This field contains the data resulting from a maintenance read operation or the data to be used for a maintenance write operation.	Read/Write	0x0

1662

4.5 Read data interleaving mode

Read data can be returned with data ‘beat’ interleaved. I.e., if the databus is less than a cacheline, which is always the case, two or more lines can be beat interleaved.

1665 4.5.1 Proxy cache

1668 The proxy cache shall support the mode when AXI AIU with proxy cache does not interleave read data below the cache line boundary of 64 Bytes. It is required for compatibility with agents which does not support interleaving. The mode may incur some performance penalty, since potential bubbles between the cacheline transfer beats are not filled.

1671 This mode is selectable by a configuration parameter NoCacheLineInterleave, please refer to the parameters specification for more detail on the parameter.

Read data can be returned with data interleaved for different AXIDs. This allows the agent databus to be fully utilized. However, not all agents can support return data interleaving for different AXIDs.

1674 4.5.2 IOAIU

Accordingly, a parameterized mode sets the IOAIU so read data is not interleaved for different AXIDs. This means that when a read request for a given AXID is sent, all the data for that AXID request must be transferred completely before data for another AXID can be returned to the IOAIU agent. The mode will be implemented by returning read data in agent request order. This mode will likely incur a performance penalty, since bubbles will likely occur on the return data bus.

1680 4.5.3 DMI

In DMI, if the native interface read interleaving is enabled, a read data buffer shall be instantiated. The read data buffer is sized with a number of cache lines wide entries matching the number of outstanding read transactions. The buffer will then never backpressure the native AXI R channel. It is required to remove the read/write dependency downstream the SMC to avoid deadlock.

4.6 System cache

1686

The system memory cache (SMC) allows DMI(s) to buffer cache lines and service requests without accessing next level of memory hierarchy. The SMC represents a lower-level cache in the memory hierarchy relative to those in the caching agents and NCAIU.

1689

SMC supports a three-state cache model, a cache line may either be in an **invalid** state (i.e., not present in the cache) or **clean** state (i.e., present and consistent with respect to the next level of the memory hierarchy) or **dirty** state (i.e., present and inconsistent with respect to the next level of the memory hierarchy). The capacity of the SMC is determined by specifying the number of sets and the degree of associativity (i.e. number of ways), and the product of both determines the number of cache lines that are buffered in the cache. The SMC can be configured as scratchpad. The SMC supports way partitioning.

Allocation policy

1698

SMC in general uses the native interface (CHI, ACE, ACE-Lite, ACE5-Lite & AXI) allocation hint to allocate to the cache. These hints can be overwritten by a configuration setting where following type of request may individually be disabled from allocation:

1701

- Write request with clean data
- Write request with dirty data
- All read request data
- All write request data
- Disable cache allocation for WriteUnique from CHI/ACE processors

1704

Allocating a new cache line may cause a valid cache line to be replaced based on a configurable replacement policy. The proxy cache will search for an invalid entry in the set to which the cache line maps. If an invalid entry exists, that entry is selected for the new cache line, but if an invalid entry does not exist, the cache selects a cache line for replacement using either a random policy or a not-recently-used policy (NRU). The random policy uses a pseudo-random pointer to choose a valid cache line for replacement, while the NRU policy tracks cache lines that have been recently used (i.e., recently accessed) and uses the pseudo-random pointer to choose a valid cache line for replacement from the set of cache lines that have not been recently used. The recently used status is reset once all entries in a set are deemed recently used.

1713

Also, the SMC allocates read depending on the memory attribute signals and originator (NCAIU with Proxy Cache yes or not).

1716

Way partitioning

1719

Way partitioning capability enables reservation of a portion of the cache for a single or multiple CAIUs/NCAIUs, for the purpose of brevity CAIU/NCAIU is referred to as AIU in this description. SMC can be configured to partition the cache on per way basis. Note that when a way is reserved, all the sets associated with that way will be reserved for the configured AIU. When way partitioning is enabled, all incoming request with configured AIUs will only allocate to the

1722

enabled way(s). No other AIUs requests will be able to allocate to the enabled way(s), furthermore all incoming requests will be able to hit on all the cache ways irrespective of the AIU it is from. Way partition can be configured via configuration and status registers. Portion of the cache reserved for single or multiple Agent identifiers (Agent = AIU)

1725

- Feature Build Time Enabled
 - Number of Agent IDs (register pairs)
- Boot time configured on a per way basis
 - Register Pair
 - Agent ID
 - Reserved ways for this Agent ID
- Partitioned Ways are reserved to Agent IDs for allocation

1731

1734

Scratchpad mode

Scratchpad can be thought of as a standalone, low latency memory which is separate from the cache. This memory can be direct mapped to a configurable address range. Accesses to this address range will be directed only to the scratchpad and will not be seen by the caching partition of SMC or the downstream memory.

SMC can be configured at initialization to partition part of the cache as scratchpad on a per way basis.

1737

Only contiguous ways starting from Way 0 can be configured as scratchpad.

The configuration is performed at boot time, and configured on a per way basis

4.6.1 Relevant CSR registers

1743

The following registers are employed for the normal operations and maintenance of system cache.

TABLE 4-18 : SYSTEM MEMORY CACHE TRANSACTION CONTROL REGISTER (xSMCTCR)

Bit	Name	Description	Access	Reset Value
0	LookupEn	This bit enables system memory cache.	Read/Write	0x0
1	AllocEn	This bit enables allocation into system memory cache.	Read/Write	0x0
31:2	Rsvd	Reserved	Read Only	0x0

1746

TABLE 4-19 : SYSTEM MEMORY CACHE TRANSACTION ACTIVITY REGISTER (xSMCTAR)

Bit	Name	Description	Access	Reset
0	EvictActive	This bit is set when the unit is performing any system memory cache eviction activity and is cleared otherwise.	Read/Write	0x0
1	AllocActive	This bit is set when the unit is performing any system memory cache allocation activity and is cleared otherwise.	Read/Write	0x0
31:2	Rsvd	Reserved	Read Only	0x0

TABLE 4-20 : SYSTEM MEMORY CACHE ALLOCATION POLICY REGISTE (xSMCAPR)

Bit	Name	Description	Access	Reset
0	TOFAllocDisable	This bit disables cache allocation for writeUnique from CHI/ACE processors	Read/Write	0x0
1	ClnWrAllocDisable	This bit disables cache allocation for clean writes	Read/Write	0x0
2	DtyWrAllocDisable	This bit disables cache allocation for dirty writes	Read/Write	0x0
3	RdAllocDisable	This bit disables cache allocation for reads	Read/Write	0x0
4	WrAllocDisable	This bit disables cache allocation for writes	Read/Write	0x0
31:5	Rsvd	Reserved	Read Only	0x0

1749

TABLE 4-21 : SYSTEM MEMORY CACHE INITIALIZATION STATUS REGISTER (xSMCISR)

Bit	Name	Description	Access	Reset
0	TagInitDone	This bit is set when SMC tag initialization is done	Read/Write	0x0
1	DataInitDone	This bit is set when SMC data initialization is done	Read/Write	0x0
31:2	Rsvd	Reserved	Read Only	0x0

1752

TABLE 4-22 : SYSTEM MEMORY CACHE MAINTENANCE CONTROL REGISTER (xSMCMCR)

Bit	Name	Description	Access	Reset
3:0	MntOp	This field encodes the cache maintenance operation to be performed: 0x0: Initialize all Entries 0x1-0x3: Reserved 0x4: Flush All Entries 0x5: Flush Entry at Set and Way 0x6: Flush Entry at Address 0x7: Flush Address Range 0x8: Flush Set Way Range 0x9-0xB: Reserved 0xC: Debug Read Entry at set, way, and word 0xD: Reserved 0xE: Debug Write Entry at set, way, and word 0xF: Reserved	Read/Write	0x0
15:4	Rsvd	Reserved	Read Only	0x0
21:16	ArrayID	This field selects the array on which the cache maintenance operation is to be performed: 0x00: Tag Array 0x01: Data Array 0x02-0x3F: Reserved		0x0
22	SecAttr	This bit indicates the value of the security attribute of the address for the cache maintenance operation is to be performed. If the cache maintenance operation does not operate on an address, the value of this bit should be zero.		0x0
31:23	Rsvd	Reserved	Read Only	0x0

TABLE 4-23 : SYSTEM MEMORY CACHE MAINTENANCE ACTIVITY REGISTER (xSMCMAR)

Bit	Name	Description	Access	Reset
0	MntOpActv	This bit is set when any cache maintenance operation is in progress and is clear otherwise	Read Only	0x0
31:2	Rsvd	Reserved	Read Only	0x0

1755

TABLE 4-24 : SYSTEM MEMORY CACHE MAINTENANCE LOCATION REGISTER 0 (xSMCMLR0)

Bit	Name	Description	Access	Reset

19:0	MntSet	The field indicates the set on which the maintenance operation is to be performed	Read/Write	0x0
25:20	MntWay	This field indicates the way on which the maintenance operation is to be performed.	Read/Write	0x0
31:26	MntWord	This field indicates the data word on which the maintenance operation is to be performed.	Read/Write	0x0

1758

TABLE 4-25 : SYSTEM MEMORY CACHE MAINTENANCE LOCATION REGISTER 1 (xSMCMLR1)

Bit	Name	Description	Access	Reset
15:0	MntAddr	This field contains the high-order address bits [53:38] of the byte address on which the maintenance operation is to be performed	Read/Write	0x0
31:16	MntRange	This field indicates the range for flush operations in number of cache lines. This field is used when doing flushes based on address or set/way range.	Read/Write	0x0

TABLE 4-26 : SYSTEM MEMORY CACHE MAINTENANCE DATA REGISTER (xSMCMDR)

Bit	Name	Description	Access	Reset
31:0	MntData	This field contains the data resulting from a maintenance read operation or the data to be used for a maintenance write operation.	Read/Write	0x0

1761

TABLE 4-27 : SYSTEM MEMORY CACHE SCRATCHPAD BASE ADDRESS REGISTER 0 (xSMCSPBR0)

Bit	Name	Description	Access	Reset
31:0	ScPadBaseAddr	Scratchpad base address lower bits. Should be cacheline aligned	Read/Write	0x0

1764

TABLE 4-28 : SYSTEM MEMORY CACHE SCRATCHPAD BASE ADDRESS REGISTER 1 (xSMCSPBR1)

Bit	Name	Description	Access	Reset
31:0	ScPadBaseAddrHi	Scratchpad base address upper bits including ns bit in MSB.	Read/Write	0x0

TABLE 4-29 : SYSTEM MEMORY CACHE SCRATCHPAD CONFIGURATION REGISTER 0 (xSMCSPCR0)

Bit	Name	Description	Access	Reset
0	ScPadEn	Scratchpad RAM enable.	Read/Write	0x0
6:1	NumScPadWays	Number of ways that are to be used as scratchpad. Number of allocated ways = NumScPadWays + 1. Max of NumScPadWays = NumWays - 1.	Read/Write	0x0
31:7	Rsvd	Reserved	Read Only	0x0

1767

TABLE 4-30 : SYSTEM MEMORY CACHE SCRATCHPAD CONFIGURATION REGISTER 1 (xSMCSPCR1)

Bit	Name	Description	Access	Reset
31:0	ScPadSize	Scratchpad size in number of cachelines minus 1.	Read/Write	0x0

1770

As SMC supports up to 16 ways, each way provides the following registers for way partitioning, the number of ways required for way portioning that is configured in Maestro.

TABLE 4-31: SYSTEM MEMORY CACHE WAY PARTITIONING CONTROL REGISTER 0 (xSMCWPCRO)

Bit	Name	Description	Access	Reset
9:0	WpAgentId	Identify way partitioning agent ID.	Read/Write	0x0
30:10	Rsvd	Reserved	Read/Write	0x0
31	Valid	Way partitioning is valid	Read/Write	0x0

1773

TABLE 4-32 : SYSTEM MEMORY CACHE WAY PARTITIONING CONTROL REGISTER 1 (xSMCWPCR1)

Bit	Name	Description	Access	Reset
15:0	WpWayVector	This vector specifies ways to which the source ID identified by the associated WpAgentId can allocate to.	Read/Write	0x0
31:16	Rsvd	Reserved	Read Only	0x0

1776

TABLE 4-33 : SYSTEM MEMORY CACHE INFORMATION REGISTER (xSMCIFR)

Bit	Name	Description	Access	Reset
19:0	NumSet	This field indicates the number of sets in the system memory cache minus one in this DMIU. To determine the total number of sets in the system memory cache, this value must be multiplied by the number of DMIUs that implement the system memory cache	Read Only	0x0
25:20	NumWay	This field indicates the number of ways(i.e. the associativity) minus one in the system memory cache	Read Only	0x0
26	SP	This field indicates if scratch pad feature is enabled when set	Read Only	
27	WP	Way Partitioning support exist	Read Only	
31:28	nWP	Number of way partitioning register pair minus one	Read Only	0x0

1779

4.7 Transaction flows

1782 This section goes over different transaction flows within the Ncore 3 system. The flow diagram consists of two AIUs, which can be any possible AIU type, one DCE and one DMI (which can be treated as DII in the case of non-coherent transactions). Responses are shown in orange, and data is shown in red.

1785 Dashed purple arrows show dependencies at the unit for initiation of the message. The arrival time show in just an example and is dependent on network delay which is not captured here. Note that time flows top to bottom.

1788 4.7.1 Non-Coherent transactions

Non-coherent transaction flow does not involve DCE. AIUs directly communicate with DMI / DII depending on the identified target. Non-Coherent read transaction flow is shown in Figure 4-1 and the write transaction flow is shown in Figure 4-2. Though the diagrams only show DMI the same flow applies to DII. StrRsp and DtrRsp are just used for message ID release and have no other significance in DMI / DII.

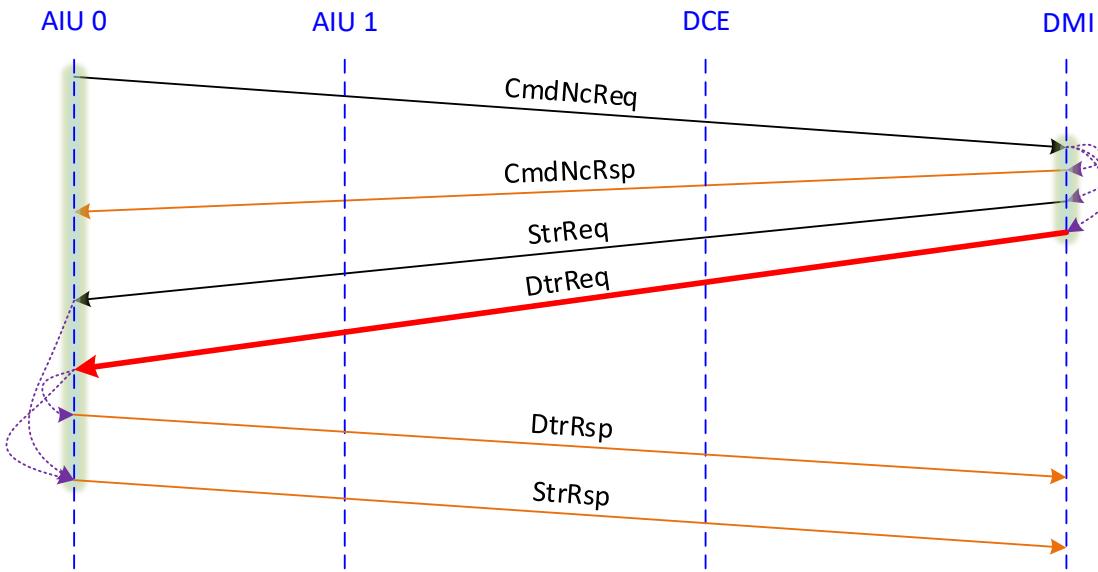


FIGURE 4-1: NC READ TRANSACTION FLOW

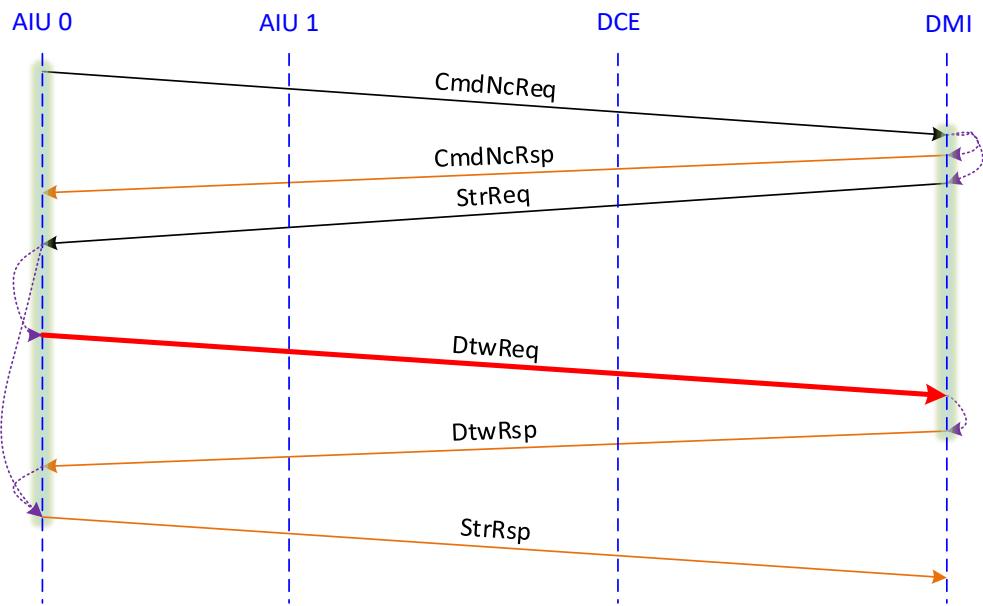


FIGURE 4-2 NC WRITE TRANSACTION FLOW

1800

Non-coherent atomic transaction flow is shown in Figure 4-3. The flow is valid for CmdWrAtm, CmdRdAtm, CmdSwapAtm & CmdCompAtm. Note that the Dtr flow shown will not be present in the case of Store atomics (CmdWrAtm).

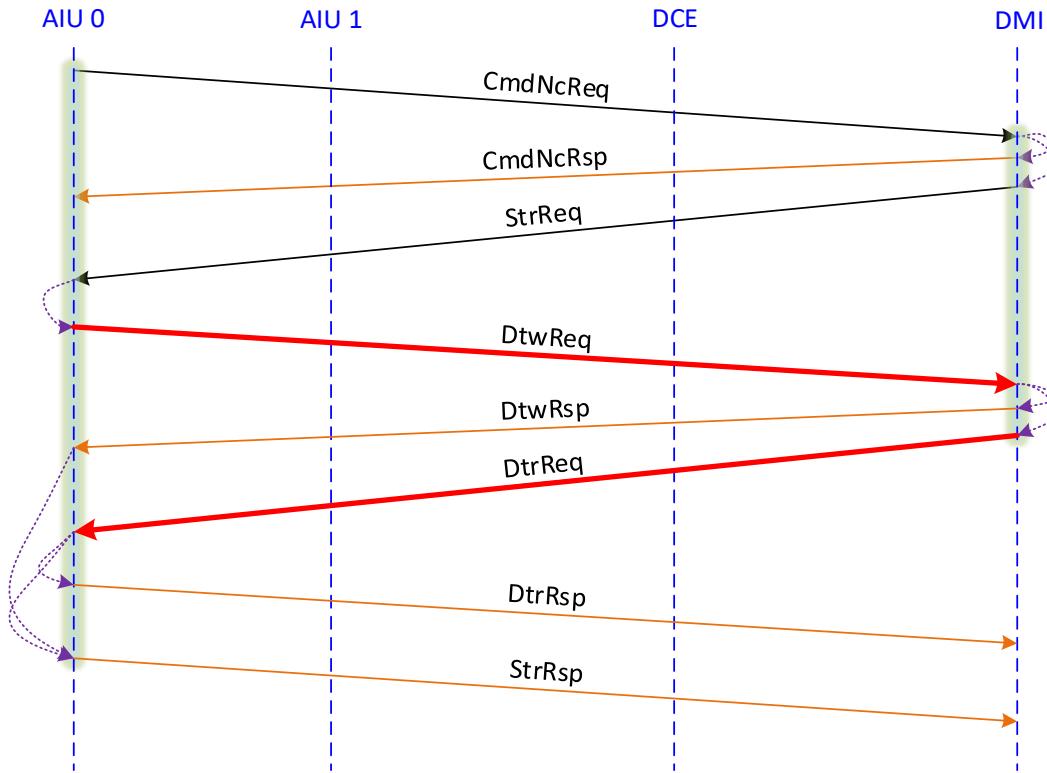


FIGURE 4-3 NON-COHERENT ATOMIC TRANSACTION FLOW

4.7.2 Coherent Read and CMO transactions

1806 In the following cases AIU0 is treated as the requesting AIU and AIU1 as the snooping AIU.

1809 Read transaction flow with snoop data is shown in Figure 4-4. The flow is valid for CmdRdVld, CmdRdUnq, CmdRDNitc and CmdRdNitcMI. Note that in the latter two cases the Dtr must be a clean Dtr while in the former two cases it can be either clean or dirty.

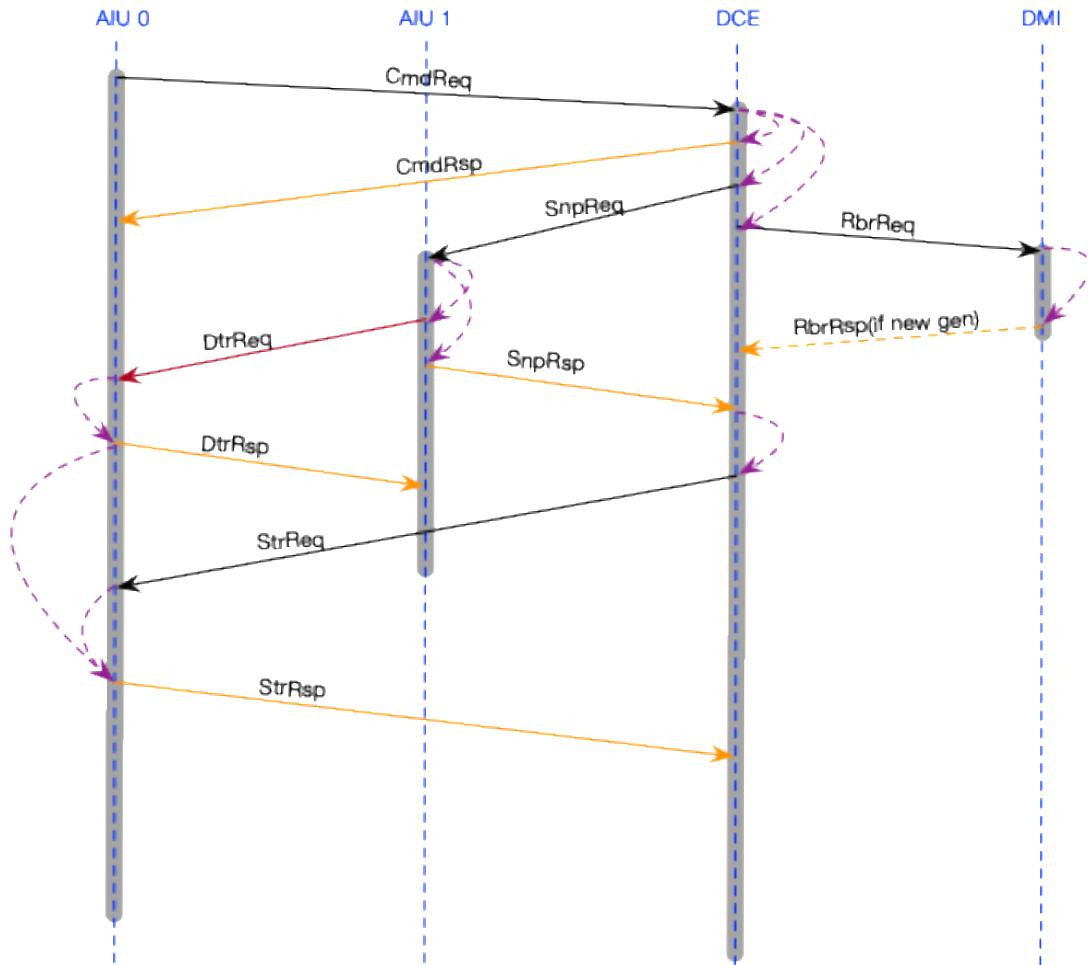
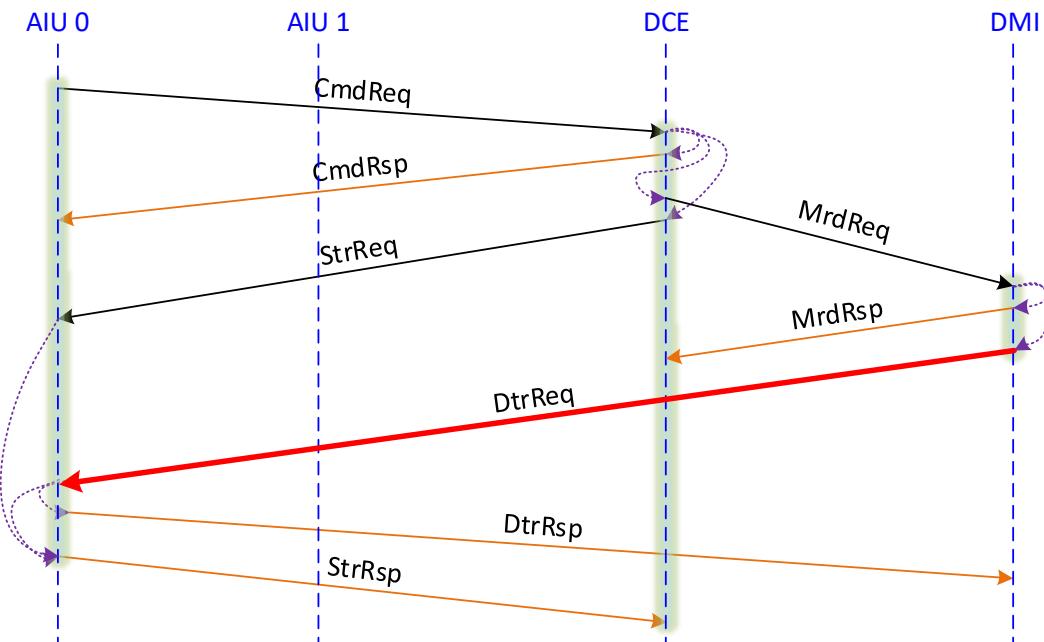


FIGURE 4-4 READ WITH SNOOP DATA

1812

Read transaction flow where snooping AIU does not provide the data, and the data is read from DMI is shown in Figure 4-5. The flow is valid for CmdRdVld, CmdRdUnq, CmdRdCln, CmdRdNitc, CmdRdNitcCl and CmdRdNitcMI. Note that in the first two cases the Dtr can either be clean or rest of the cases it must be clean.

1815



1818

FIGURE 4-5 READ WITH DMI DATA

1821

Read clean transactions with snoop data flow is shown in Figure 4-6. The flow is valid for CmdRdCln and CmdRdNitcCl. The Dtw shown is issued to write dirty data back to memory as the requesting AIU cannot accept dirty data. The Dtw is not required in cases where ownership is retained by the processor providing the data or the data is already clean.

1824

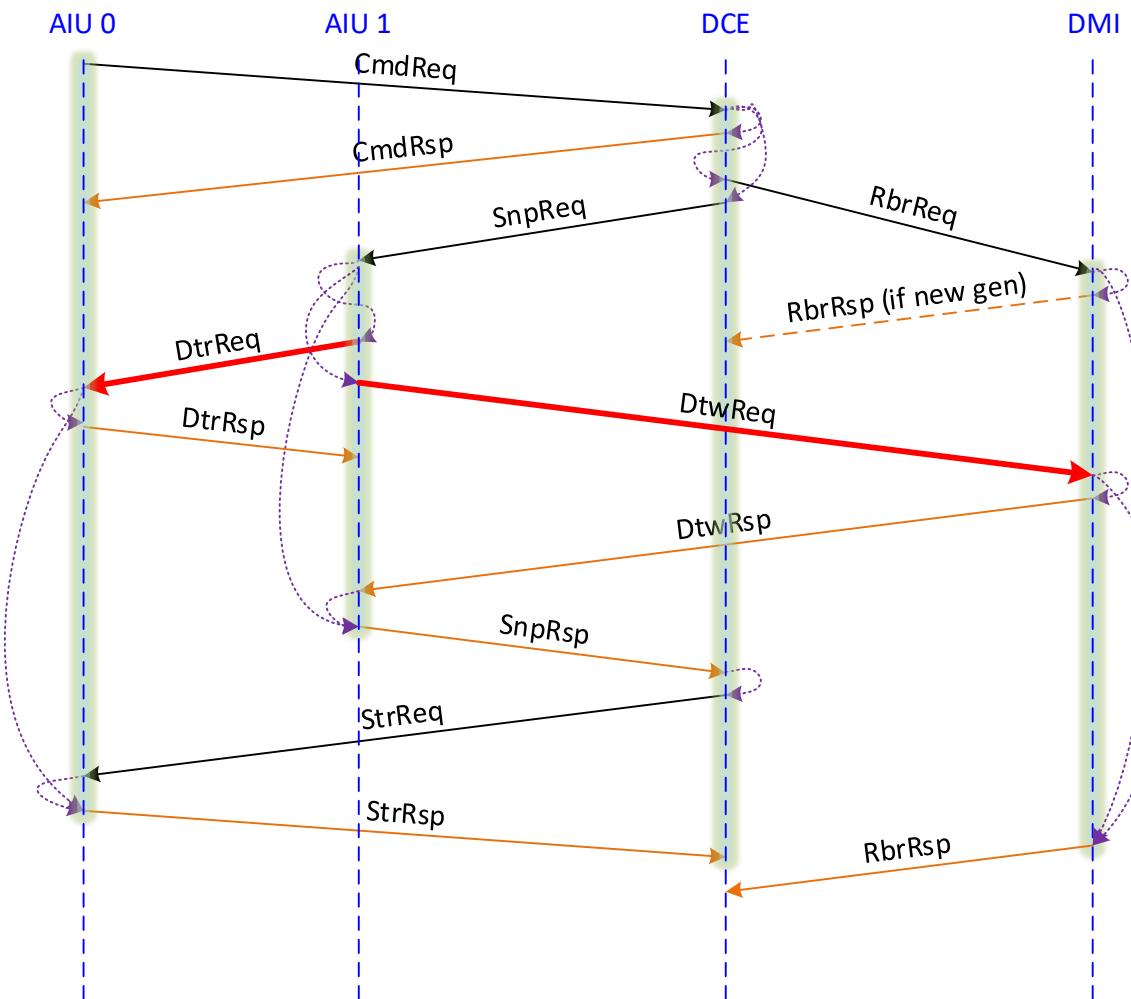
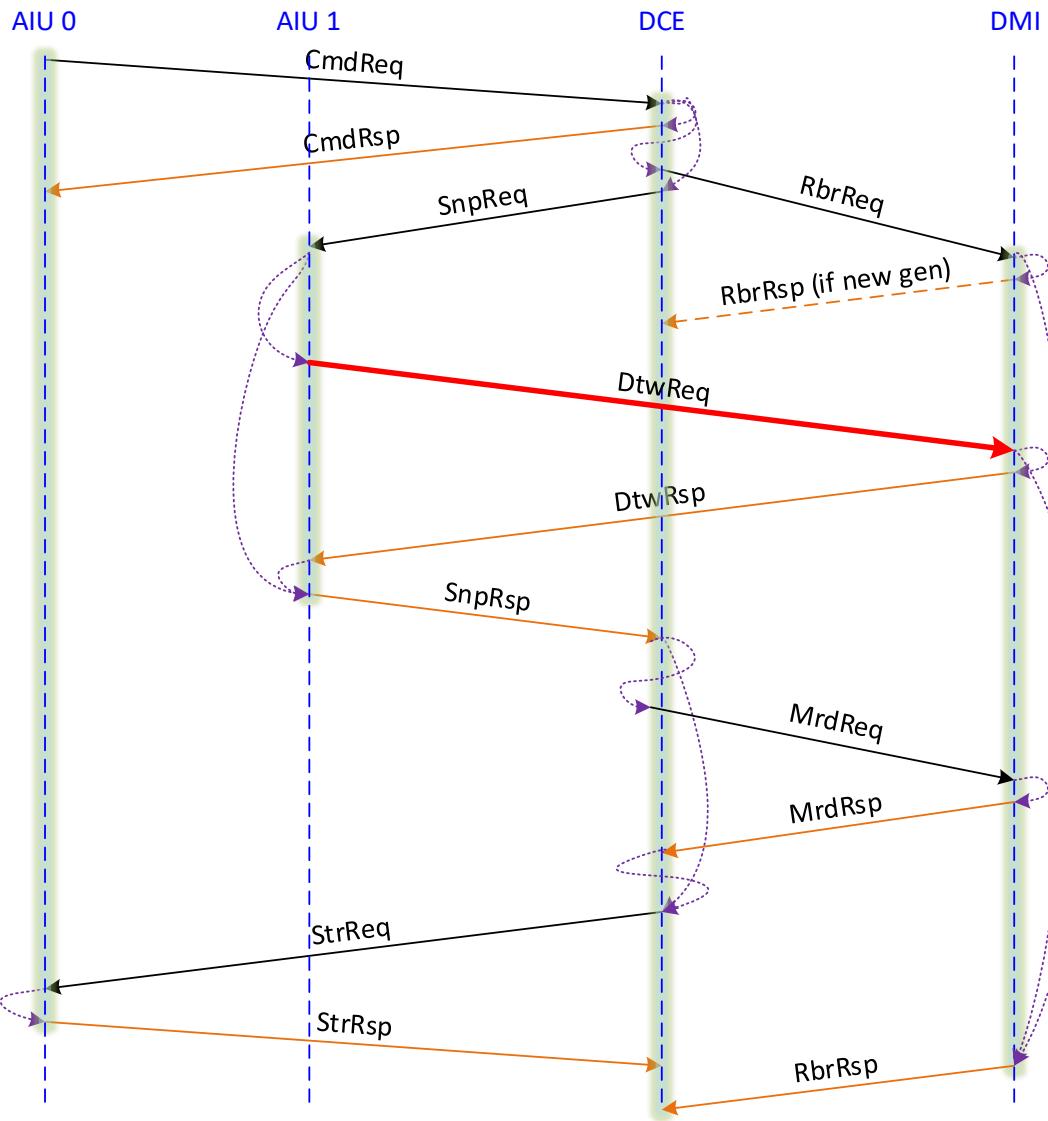


FIGURE 4-6 READ CLEAN WITH SNOOP DATA

1827

Clean operations (data less) with dirty snoop data transaction flow is shown in Figure 4-7. The flow is valid for CmdClnUnq, CmdWrAtm, CmdRdAtm, CmdSwapAtm, CmdCompAtm, CmdMkUnq, CmdClnInv, CmdMkInv, CmdClnVld & CmdClnShPsist. Note that Mrd is issued by DCE only in the last four cases to enforce CMO at the SMC after receiving snoop responses. Furthermore, in current Ncore Arch specification coherent atomic transactions are treated as clean transactions by DCE. Please refer to 4.7.4 for coherent atomic transaction processing.

1830



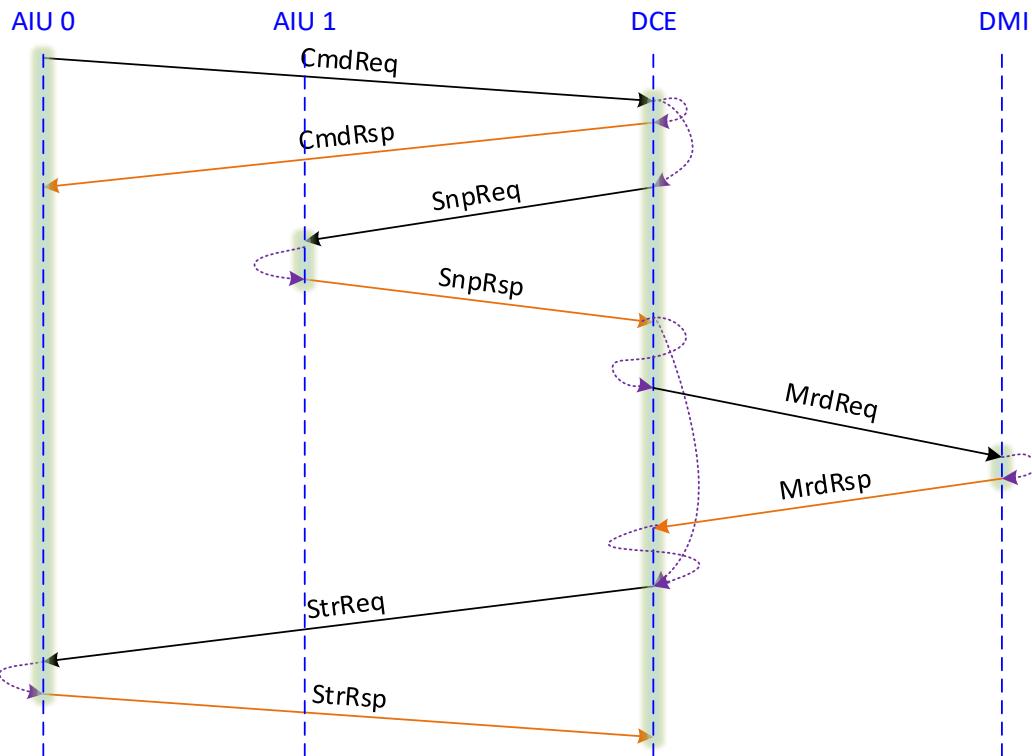
1833

C

FIGURE 4-7 CLEAN WITH DIRTY SNOOP DATA

1836

Invalidate transaction flow is shown in Figure 4-8. The flow is valid for CmdClnInv (agents with clean data) & and CmdMkInv.

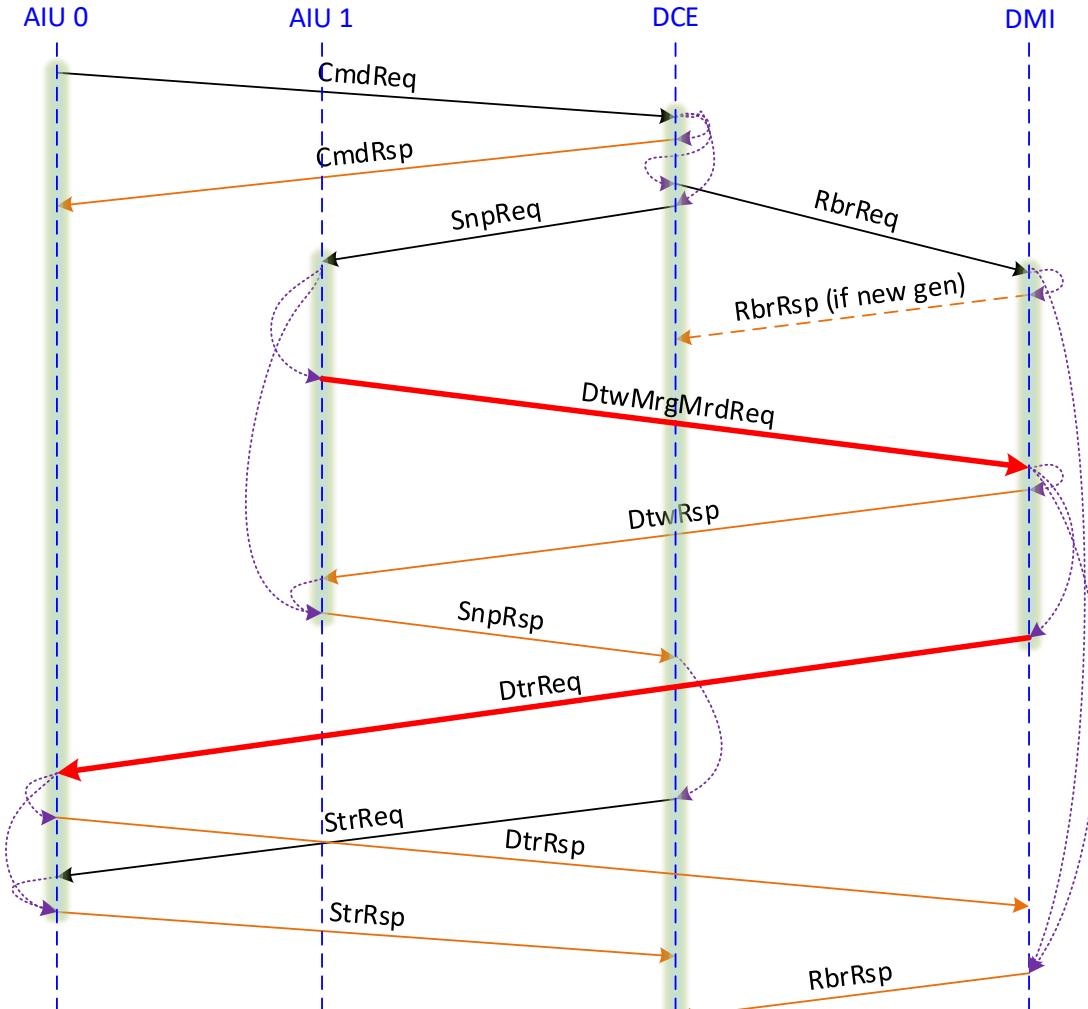


1839

FIGURE 4-8 INVALIDATE TRANSACTION FLOW

1842

Read when snooped processor is in partial state transaction flow is shown in Figure 4-9. This flow is valid for all read commands when the owner is in unique partial state. Note that DtwMrgMrdReq processing in DMI differs in the case of stash commands where the DtwRsp is delayed till after DtrRsp is received by DMI.



1845

FIGURE 4-9 READ WHEN THE CACHE OWNER IS IN THE UNIQUE PARTIAL STATE

1848 4.7.3 Coherent write transactions

Write line unique transaction flow is shown in Figure 4-10. This flow is valid for CmdWrUnqPtl and CmdWrUnqFull, note that DtwReq secondary is optional in the case of CmdWrUnqPtl and will not exist in the case of CmdWrUnqFull. Transaction flow for CHI AIU CmdWrBkPtl, CmdWrBkFull, CmdWrClnPtl, CmdWrClnFull, CmdWrEvict and CmdEvict is shown in Figure 4-11. Note that CmdEvict will not have an associated Dtw. In the case of ACE AIU WriteBack/WriteClean and AXI AIU with proxy cache evictions are treated as non-coherent writes to DMI. WriteClean will retain a clean copy of the line in the initiator's cache, no Update command will be sent to DCE. WriteBack will invalidate the line in the initiator's cache and must be followed by an Update command to DCE, this is shown in Figure 4-12.

1851

1854

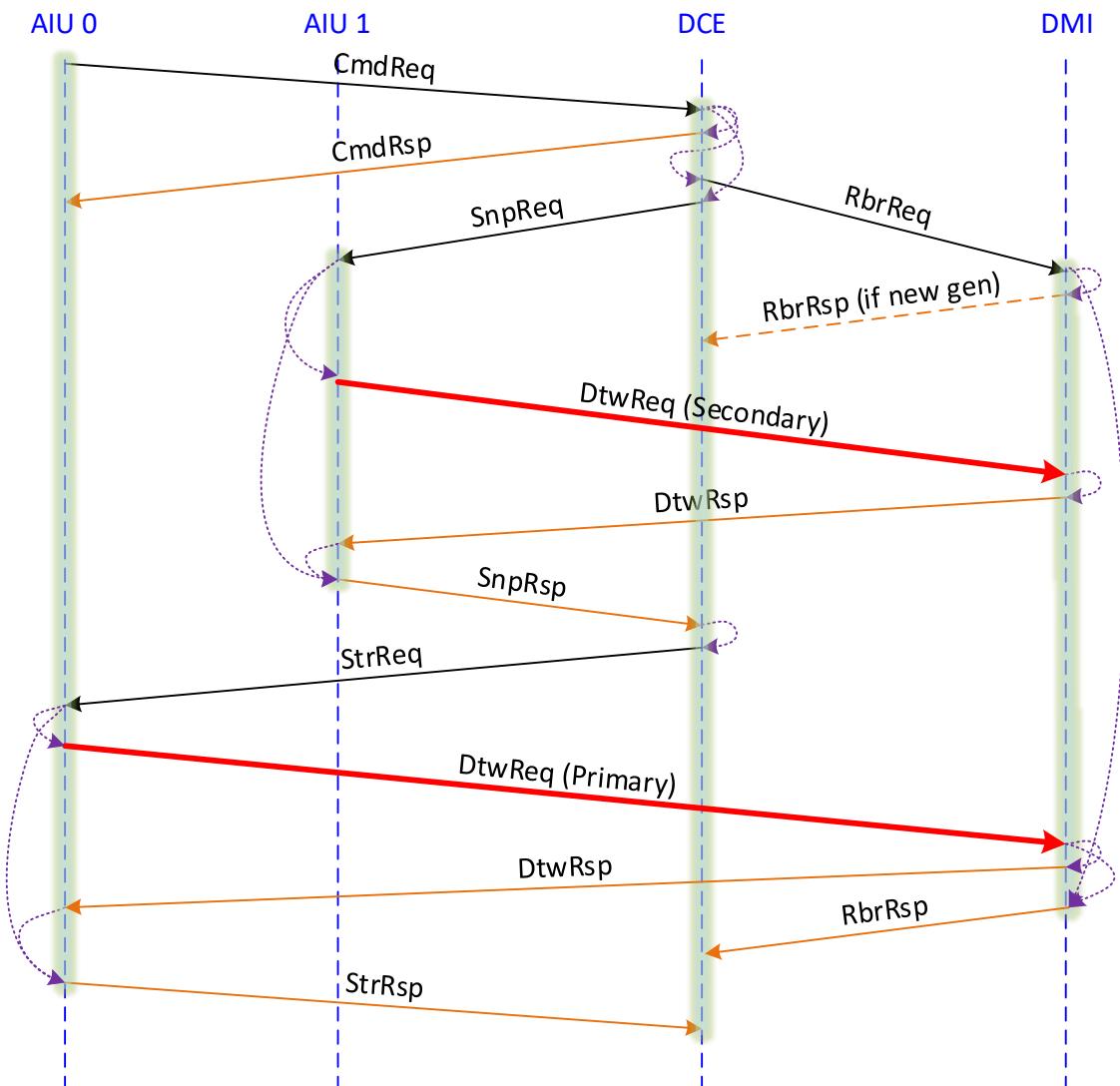


FIGURE 4-10 WRITE UNIQUE TRANSACTION FLOW

1857

1860

1863

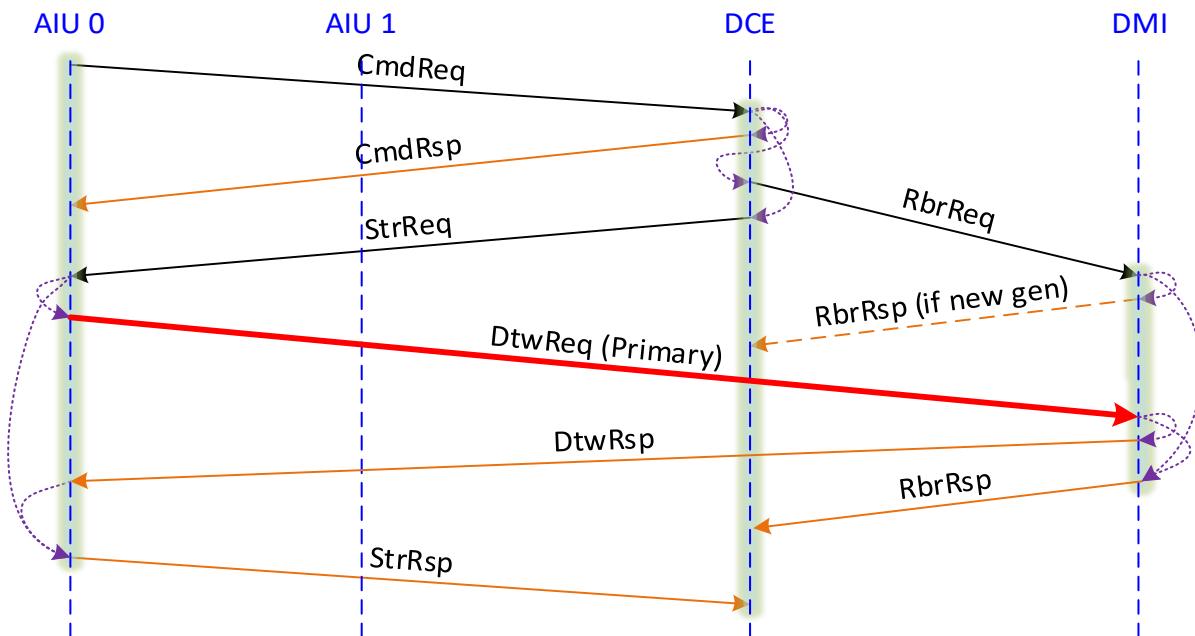


FIGURE 4-11 CHI COHERENT WRITE TRANSACTION FLOW

1866

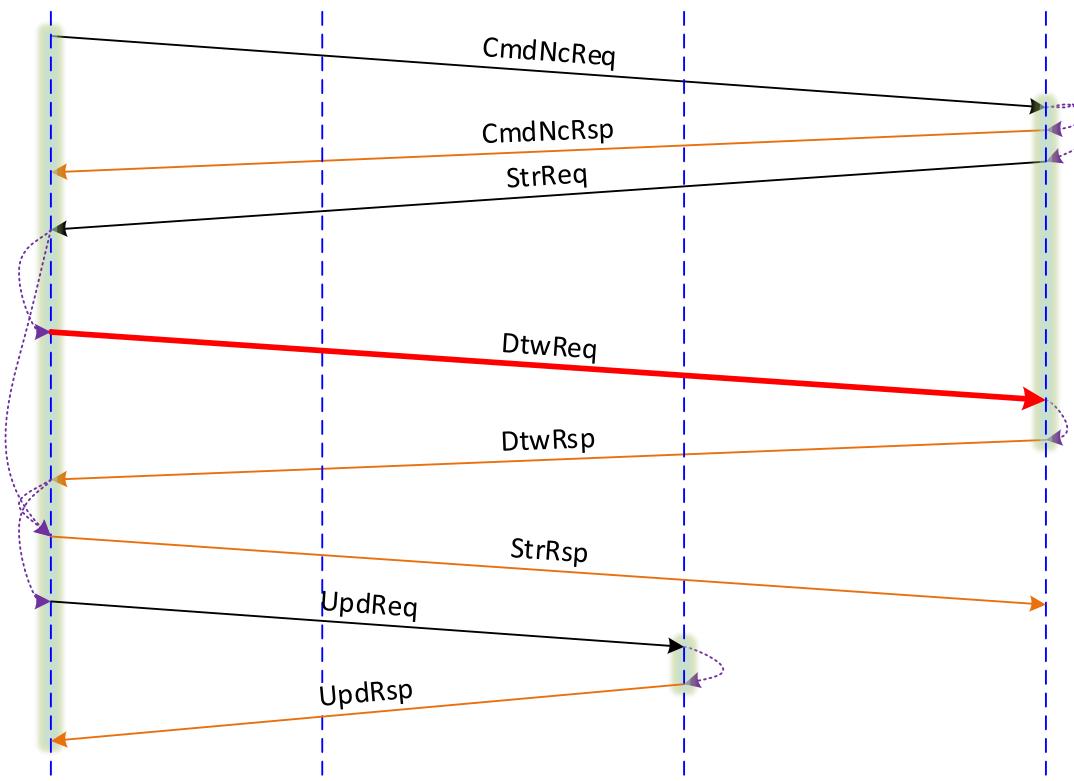


FIGURE 4-12 ACE WRITE BACK TRANSACTION FLOW

4.7.4 Coherent atomic transactions

1869

Coherent atomic transactions are broken into two parts, coherent clean part which is done by DCE and non-coherent atomic part which is done by DMI. The flow for this transaction and its dependencies are shown in Figure 4-13. The flow is valid for CmdWrAtm, CmdRdAtm, CmdSwapAtm & CmdCompAtm.

1872

Note that the Dtr flow shown will not be present in the case of Store atomics (CmdWrAtm).

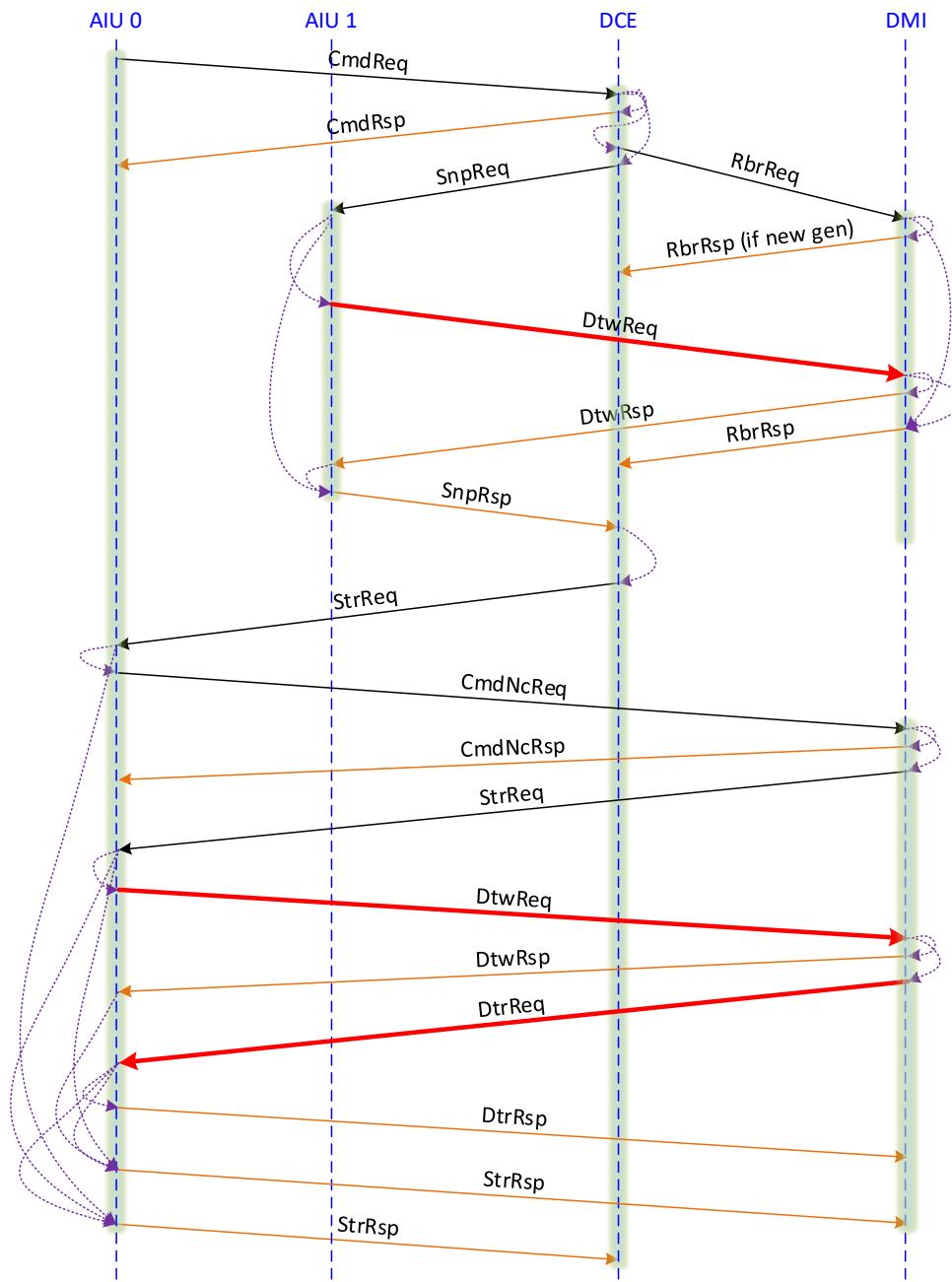
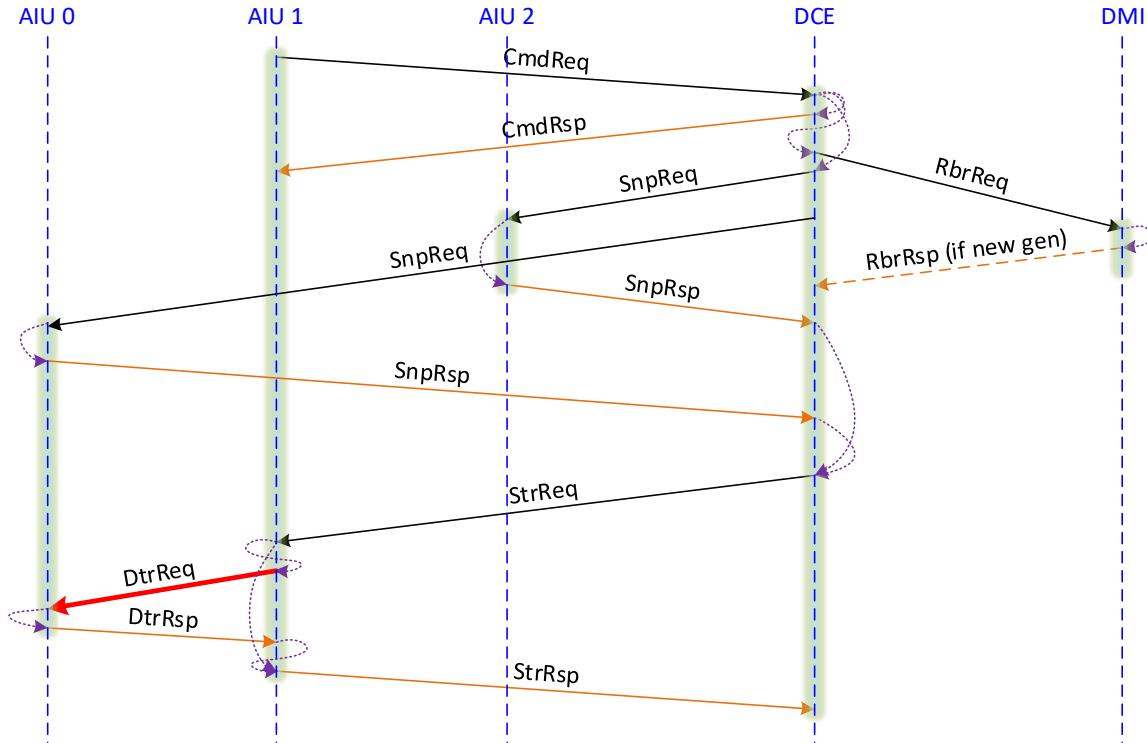


FIGURE 4-13 COHERENT ATOMIC TRANSACTION

1875 **4.7.5 Stash transactions**

In the following cases AIU1 is treated as the requesting AIU; AIU2 as the snooping AIU and AIU 0 as the target AIU.

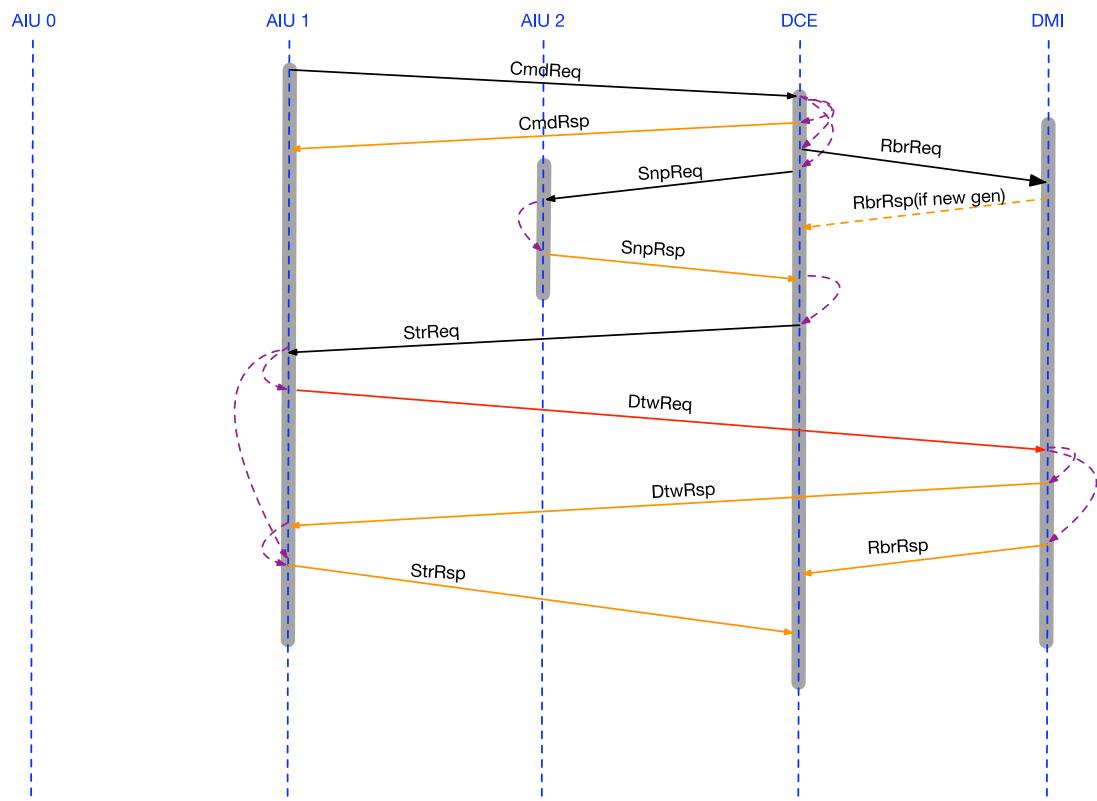
1878 Write stash full transaction flow when target is identified and accepts the stash is shown in Figure 4-14.



1881

FIGURE 4-14 WRITE STASH FULL ACCEPT TRANSACTION FLOW

Figure 4-15 shows the Write Stash flow when the Stash target is not identified.



1884

FIGURE 4-15 WRITE STASH WHEN THE STASH TARGET IS NOT IDENTIFIED

The flow when the target does not accept the write stash is shown in Figure 4-16.

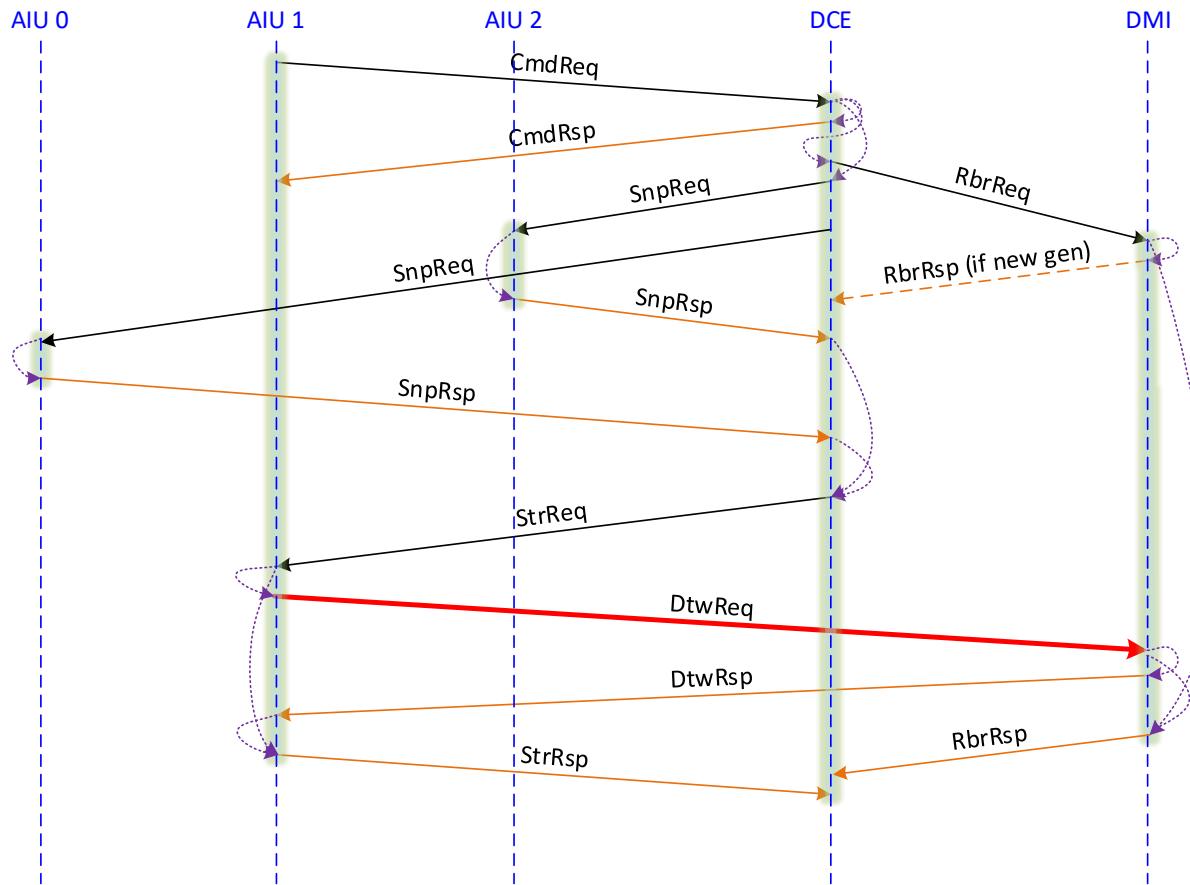
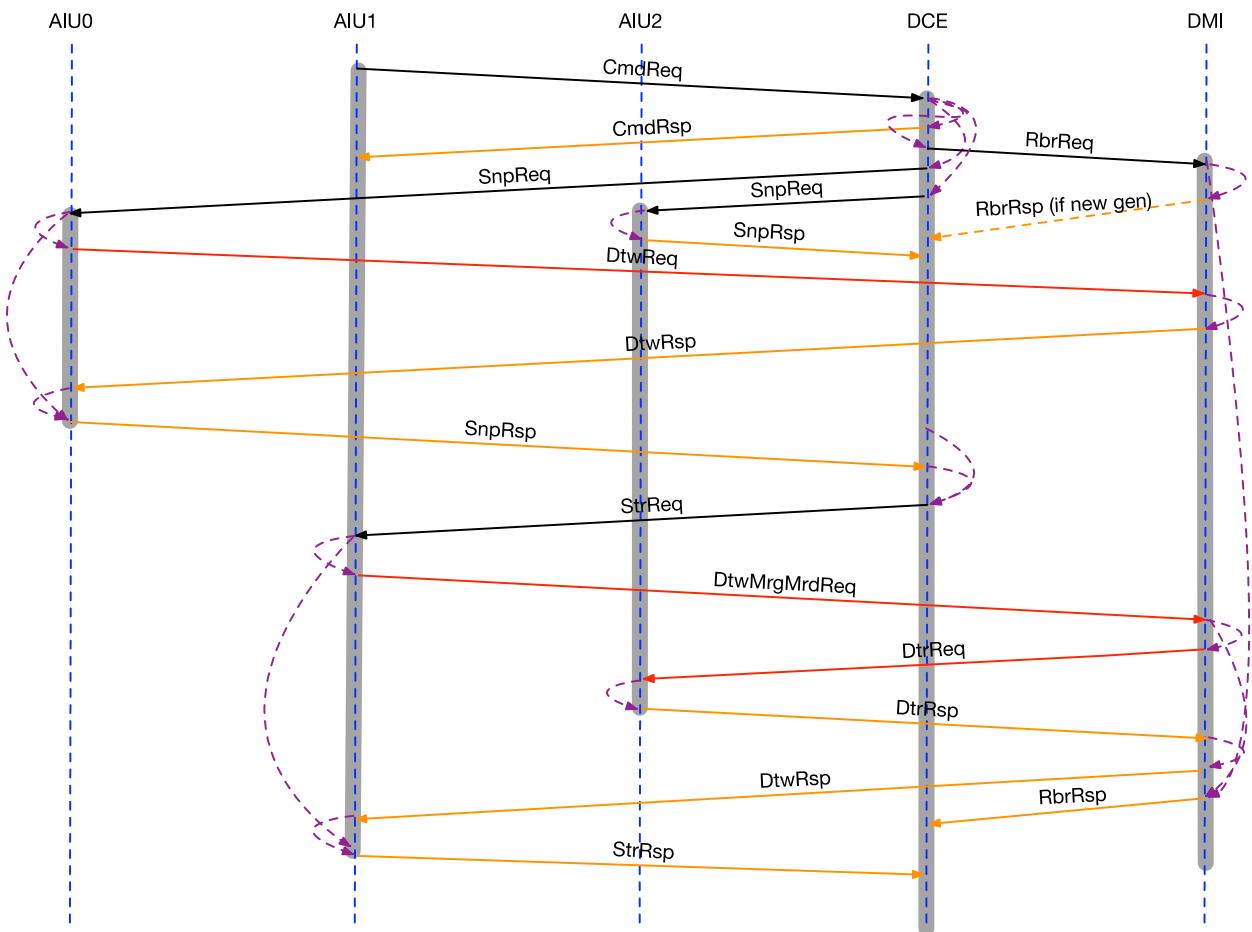


FIGURE 4-16 WRITE STASH DECLINE TRANSACTION FLOW

Write stash partial when target is identified and accepts the stash and it was in invalid state is shown in Figure 4-17.



1893

FIGURE 4-17 WRITE STASH PARTIAL ACCEPT FLOW WHEN THE TARGET CACHE WAS IN INVALID STATE

Write stash partial when target is identified and accepts the stash is shown in Figure 4-18.

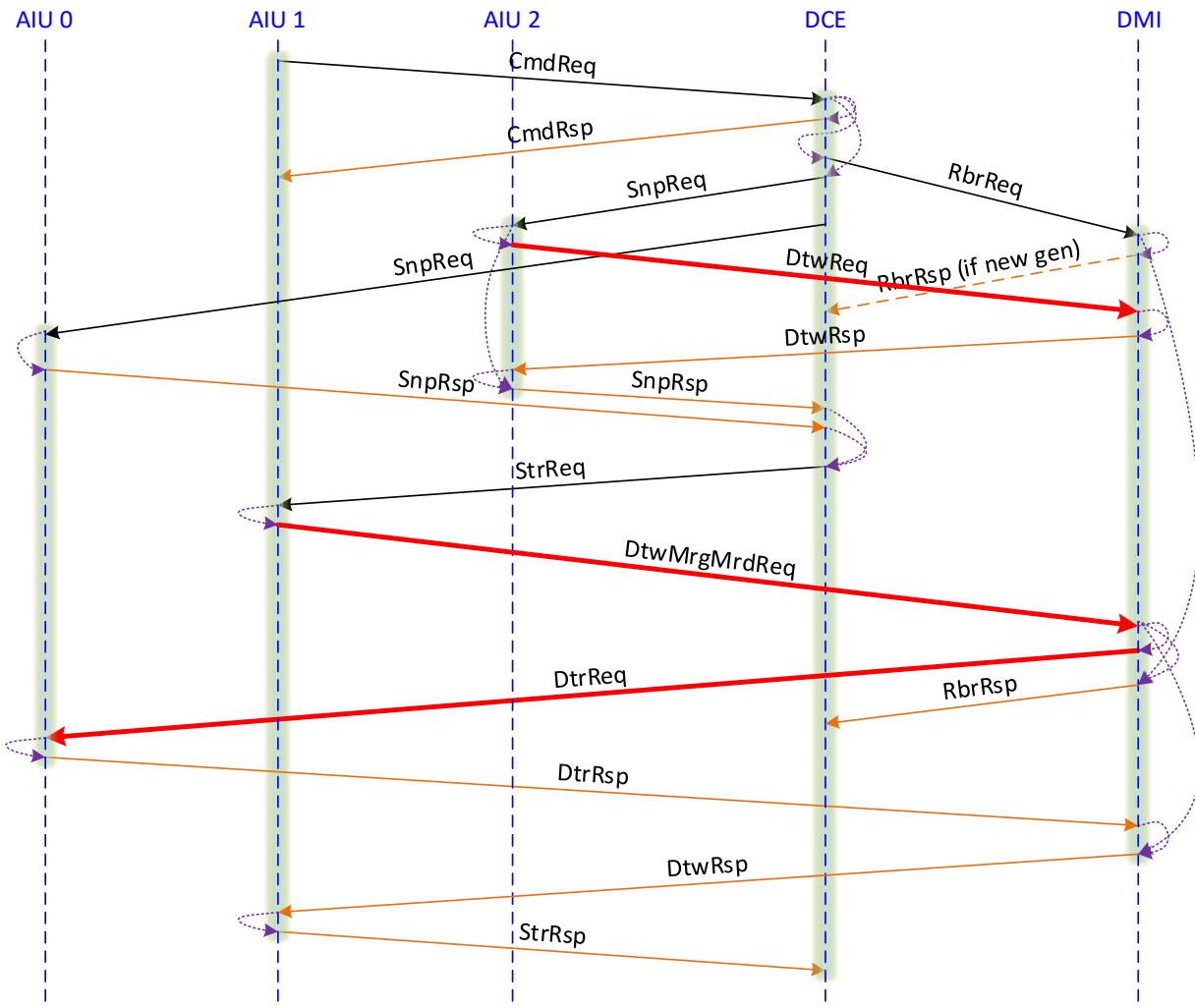


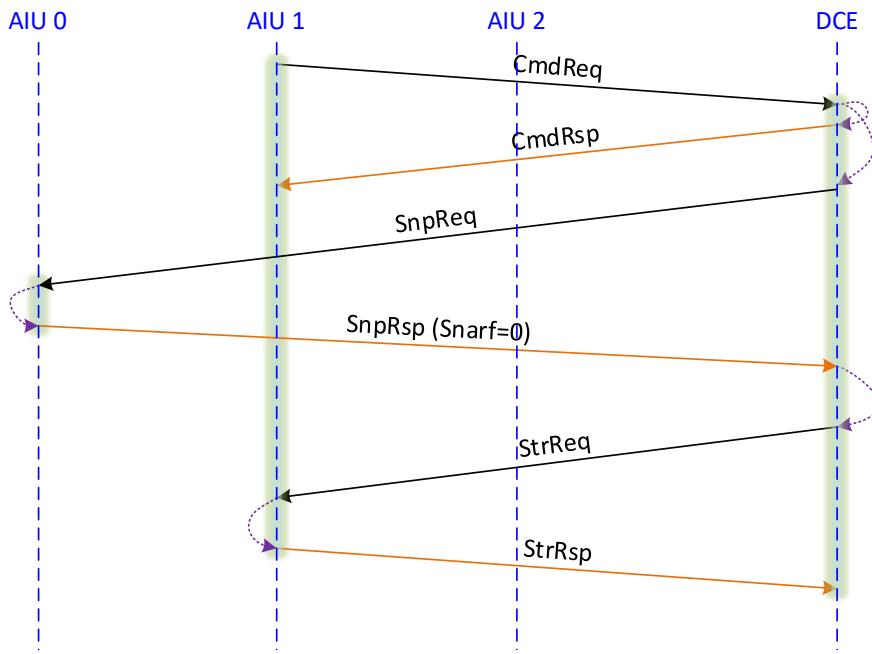
FIGURE 4-18 WRITE STASH PARTIAL ACCEPT FLOW

Please note that the “Read Stash” mentioned next is the same as the independent stash requests described in ARM CHI protocol. These stash requests are generated either by StashOnceShared or StashOnceUnique transactions which don’t carry any data compared with the write stash with hint transactions. The target stash agent or the shared system cache (if the stash target is not specified) is expected to fetch/read the data to its cache at the end of the transaction.

Read Stash decline flow is shown in Figure 4-19. Note this is different than target not identified case that no snoop is sent to target and no MRDPref is going to be sent out to DMI for the declined request. Read stash target not identified flow is shown in Figure 4-20. This is the case where no coherent agent is registered as either an owner or a sharer for the cache line. If there exists at least one owner or a sharer for the cache line, the DCE can properly finish the transaction without sending MrdPref as shown in Figure 4-21

1911 Read Stash accept flow is shown in Figure 4-22, when Read stash is accepted, if there's a peer with dirty copy of the data, the data is first written to DMI, and a MRDReq will be sent out by DCE after the write completes. (the read after write sequence is guaranteed by DTWReq -> DTWRsp -> SNPRsp -> MRDReq). If no peer is providing the data, data will be directly read from DMI.

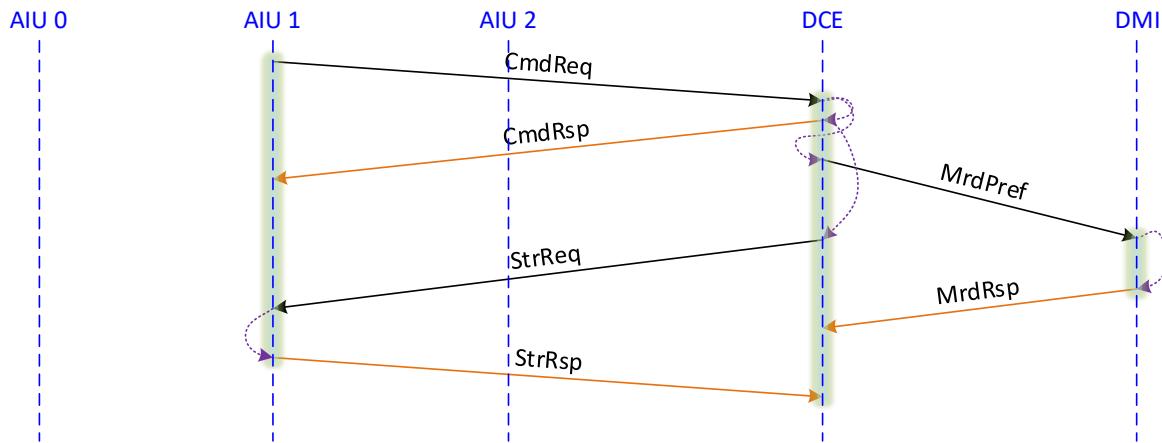
1914



1917

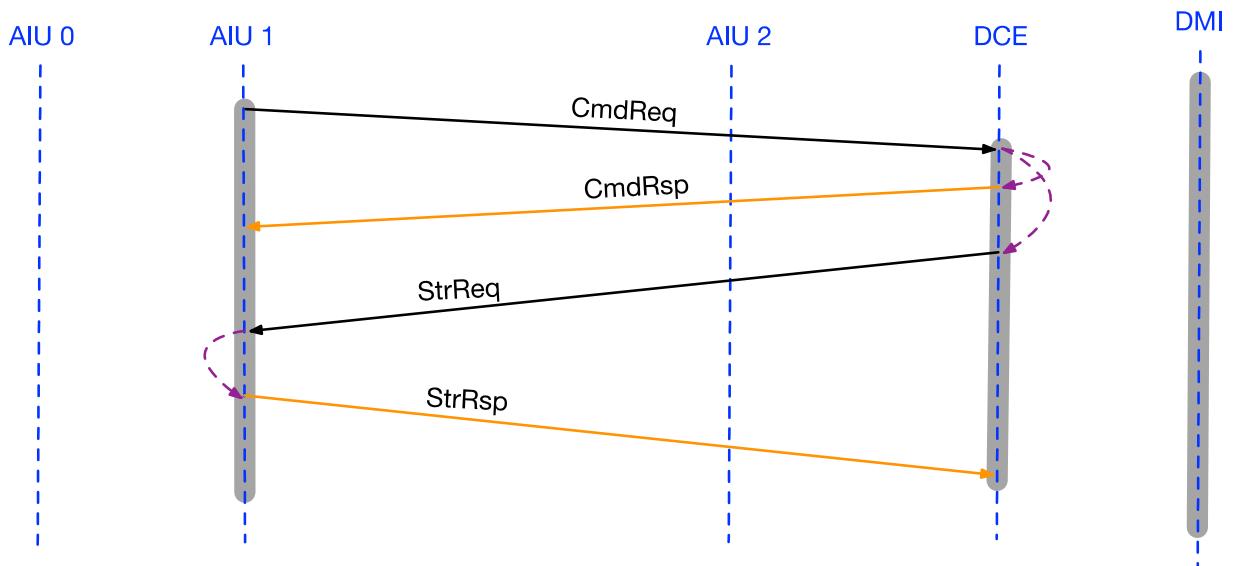
FIGURE 4-19 READ STASH DECLINE FLOW

1920 Read Stash accept flow with a peer agent has a clean copy of cache line is shown in Figure 4-23. When Read stash is accepted, if there's a peer with clean copy of the data, the data is directly returned from the peer cache.



1923

FIGURE 4-20 READ STASH WHEN THE TARGET IS NOT IDENTIFIED AND THE CACHE LINE IS NOT CACHED



1926

FIGURE 4-21 READ STASH WHEN THE TARGET IS NOT IDENTIFIED AND THE CACHE LINE IS CACHED

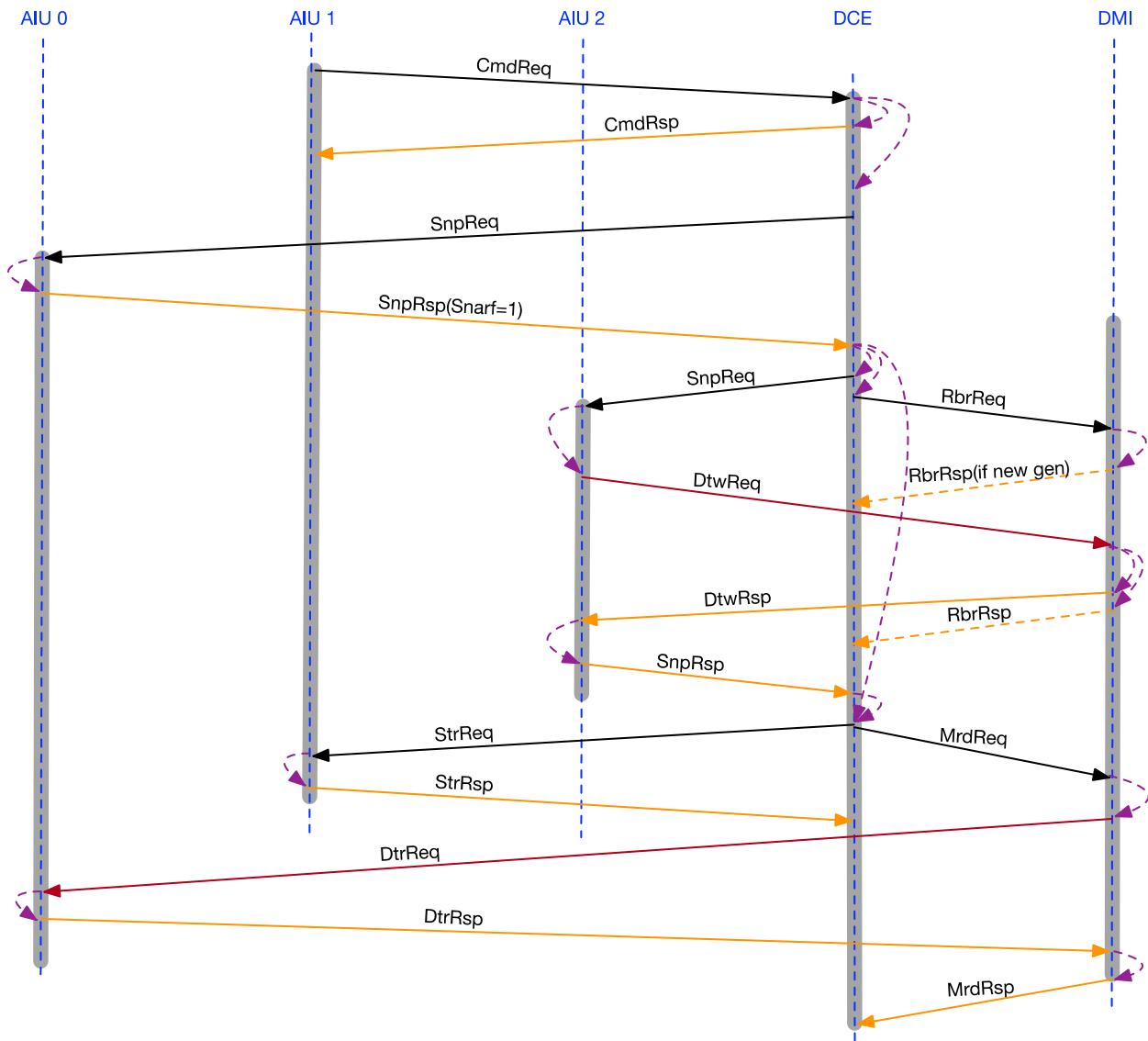


FIGURE 4-22 READ STASH ACCEPT FLOW WITH A PEER CACHE HAS PARTIAL DIRTY DATA

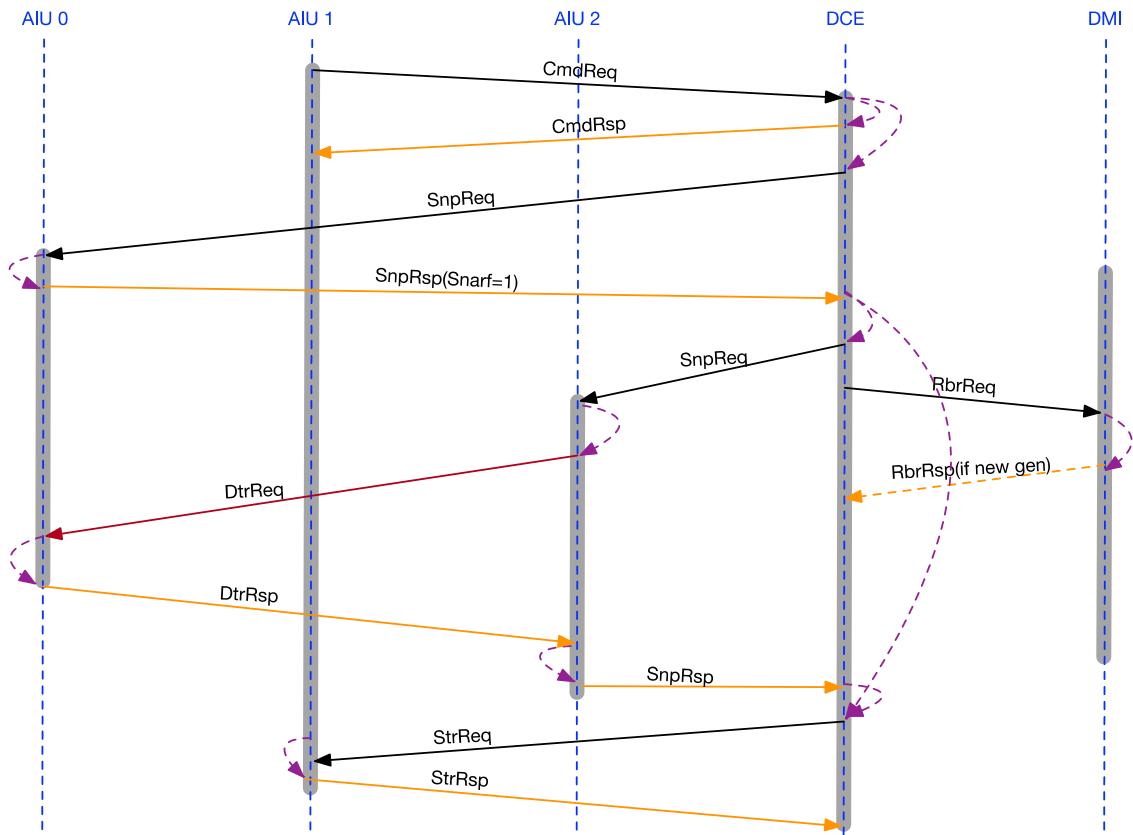


FIGURE 4-23 READ STASH ACCEPT FLOW WITH A PEER AGENT HAS A CLEAN COPY OF THE CACHE LINE

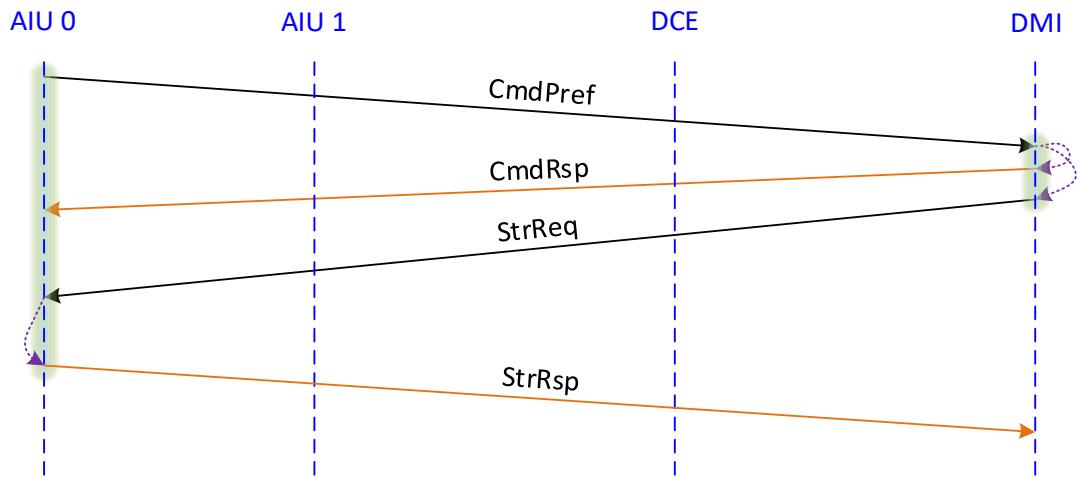
1932

4.7.6 Prefetch transactions

1935

Prefetch transaction flow does not involve DCE. AIUs directly communicate with DMI depending on the identified target. Prefetch transaction flow is shown in Figure 4-24. The Prefetch command fills the SMC if the line is not present alternatively if the line is already present in the SMC, resources are not available or if there is a collision then it just gets acknowledged. Note that prefetch command may collide with Mrd of the same address as it does not serialized by DCE.

1938

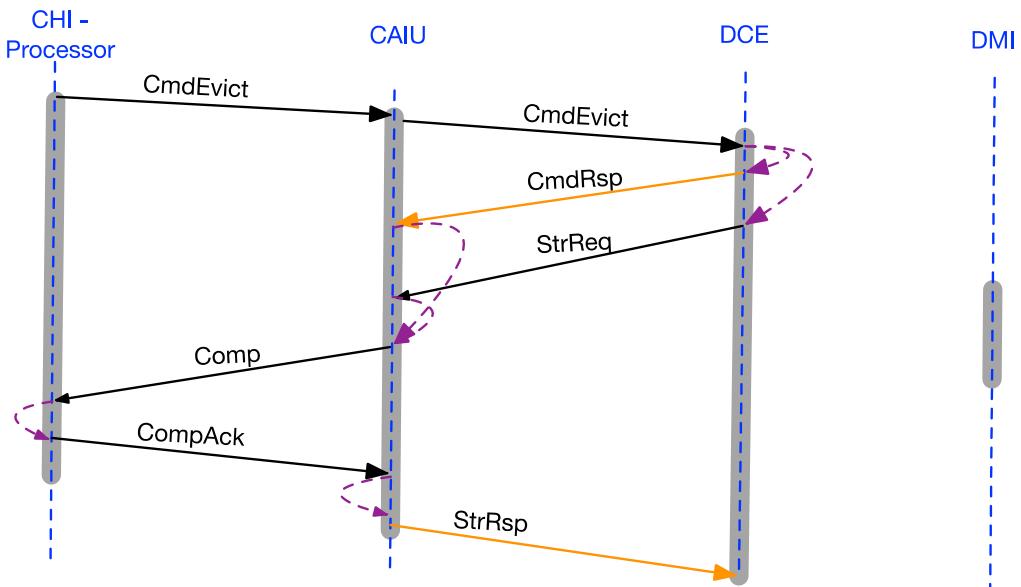


1941

FIGURE 4-24 PREFETCH TRANSACTION FLOW

1944 4.7.7 Evict transactions

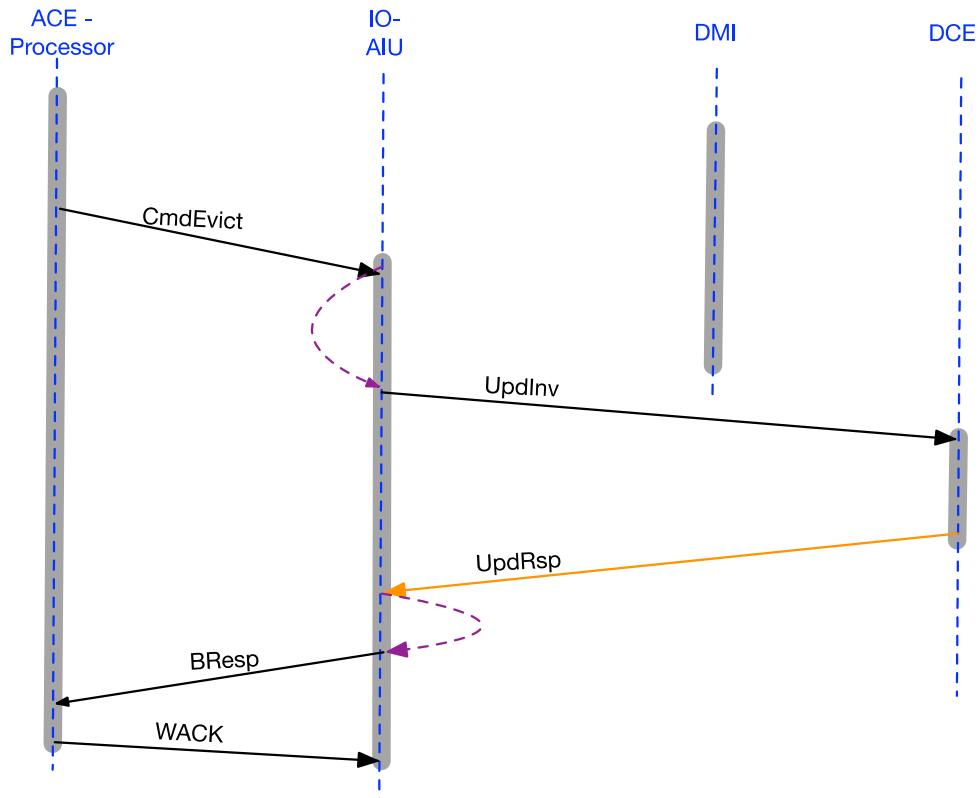
1947 Evict transaction is a dataless transaction. The handling and flow is different for a CHI-B/E based processor with a CAIU and for an ACE based IOAIU. As shown in Figure 4-25, Evict transaction is taken as is and processed by the DCE directly.



1950

FIGURE 4-25 EVICT FLOW OF A CHI-B/E BASED PROCESSOR

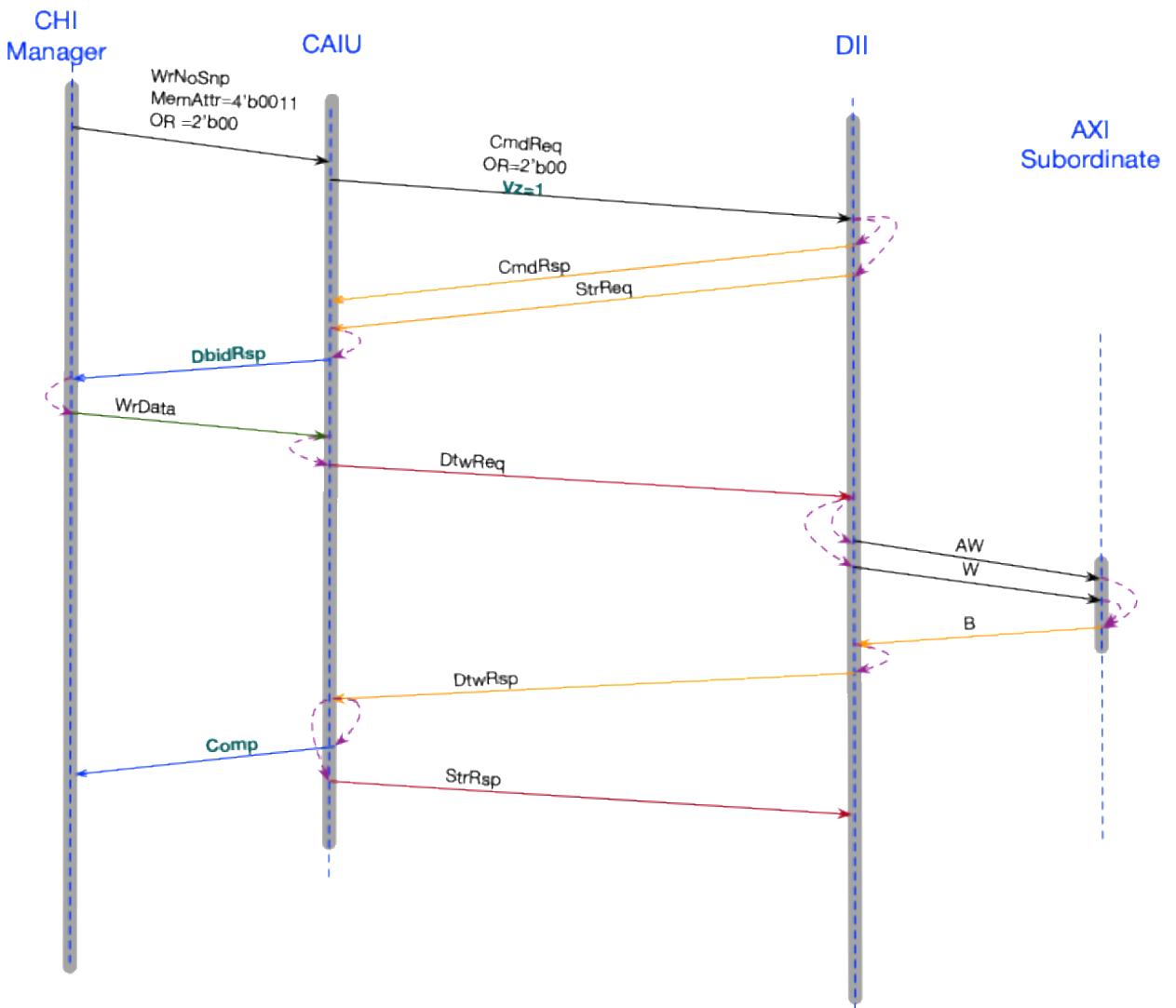
1953 However, the Evict transaction is converted as a UpdInv command by the IOAIU and sent to DCE to complete the transaction for an ACE based processor as shown in Figure 4-29.



1956

FIGURE 4-26 EVICT FLOW OF AN ACE-BASED PROCESSOR

1959 4.7.8 Late response for a non-coherent write targets a DII with an EWA attribute



1962

FIGURE 4-27 HANDLING OF A NON-COHERENT WRITE TARGETS A DII WITH NO ORDER AND EWA ATTRIBUTE

As stated in section 1.2.8, currently for non-coherent writes that target a DII with “No order” mode and with an EWA attribute, a CAIU always enforces LATE responses as shown in Figure 4-27. By doing so, it implies that a DII needs to pass the EWA attribute to the downstream subordinate or an interconnect.

1968

4.8 CHI-E support

This chapter goes over how CHI-E features are mapped on to concerto protocol.

1971

4.8.1 CHI-E Request bus

This section describes how the CHI-E request bus is integrated into Ncore 3.6, changes in this section are primarily limited to AIUs. Note that DVMs are covered in a different section 4.10.

4.8.1.1 CHI-E Command transactions

1974

The mapping of native CHI-E commands that have been added in addition to CHI-B ones is shown in Table 4-34. CHI AIU shall meet the CHI E interface requirements as per the CHI-E on the native command issued by the CHI agent, the mapping here is for internal Ncore 3 handling of the commands.

1977

TABLE 4-34:CHI-E REQUEST MAPPING

CHI E Native Command	Concerto Commands	Notes
ReadNoSnpSep	N/A	This command can only be issued by a Home Node. Not Issued by DSU
CleanSharedPersistSep	CmdClnShPsist	
MakeReadUnique (Not Excl)	CmdRdUnq	
MakeReadUnique (Excl)	CleanUnique + CmdRdNshDty	
WriteEvictOrEvict	Evict	Downgrade to always do Evict
WriteUniqueZero	CmdWrUnqFull	Emulate a DtwReq with 64 bytes of data as Zeros (DtwDataFullDty)
WriteNoSnpZero	CmdWrNCFull	Emulate a DtwReq with 64 bytes of data as Zeros (DtwDataFullDty)
StashOnceSepShared	N/A	Disable in DSU by setting appropriate bits in CLUSTERECTLR_EL1
StashOnceSepUnique	N/A	Disable in DSU by setting appropriate bits in CLUSTERECTLR_EL1
ReadPreferUnique	CmdRdNshDty	Treat it as Read not shared dirty
WriteNoSnpFullCleanSh	CmdWrNCFull + CmdClnVld	Combine cmd: Issue two commands, write followed by CMO
WriteNoSnpFullCelanInv	CmdWrNCFull + CmdClnInv	Combine cmd: Issue two commands, write followed by CMO
WriteNoSnpFullCleanShPerSep	CmdWrNCFull + CmdClnShPsist	Combine cmd: Issue two commands, write followed by CMO
WriteUniqueFullCleanSh	N/A	Not issued by DSU
WriteUniqueFullCleanShPerSep	N/A	Not issued by DSU
WriteBackFullCleanSh	CmdWrBkFull + CmdClnVld	Combine cmd: Issue two commands, write followed by CMO
WriteBackFullCelanInv	CmdWrBkFull + CmdClnInv	Combine cmd: Issue two commands, write followed by CMO
WriteBackFullCleanShPerSep	CmdWrBkFull + CmdClnShPsist	Combine cmd: Issue two commands, write followed by CMO
WriteCleanFullCleanSh	CmdWrClnFull + CmdClnVld	Combine cmd: Issue two commands, write followed by CMO
WriteCleanFullCleanShPreSep	CmdWrClnFull + CmdClnShPsist	Combine cmd: Issue two commands, write followed by CMO
WriteNoSnpPtlCleanSh	N/A	Not issued by DSU
WriteNoSnpPtlCleanInv	N/A	Not issued by DSU
WriteNoSnpPtlCleanShPerSep	N/A	Not issued by DSU
WriteUniquePtlCleanSh	N/A	Not issued by DSU
WriteUniquePtlCleanShPerSep	N/A	Not issued by DSU

1980

Combined commands which include a write command followed by a CMO must be executed one after another. The write must be completed at-least to a point where it has been ordered by DCE/DMI/DII i.e. StrReq has been received by the initiator AIU before processing the CMO. Implementation may decide to

execute the write completely before processing the CMO. If the write returns an error, then the CMO must not be executed, and an error response must be returned on the native interface. Implementation of combined commands using a single transaction table entry is desirable.

4.8.1.2 CHI-E Snoop transactions

Ncore will only issue currently supported CHI-B snoops. Support for new CHI E snoops is not required and they will not be generated by Ncore.

Because CHI-E specification has removed the DoNotDataPull bit in the snoop request. For a CHI-E AIU, when it hasn't any stashing entry available to accommodate the incoming stash, this CHI AIU, which is the stash target, would downgrade the stash to the non-stashing version for the write stash snoop and it would drop the stash for the read stash.

Since the DoNotDataPull bit is supported in CHI-B specification, for a CHI-B AIU, when it hasn't any stashing entry available to accommodate the incoming stash, the stash target CHI AIU, it asserts DoNotDataPull on its reply for both a read or write stash.

If there is room to accommodate a stashing request, the stash target CHI AIU would accept the stash request, which it can be either a read or write stash. This CHI AIU would further pass the stash to the upstream coherent PE for further processing.

4.8.1.3 New CHI E request fields

THE NEW COMMAND REQUEST FIELDS ARE SHOWN IN TABLE 4-35 AND IN

Table 4-36 for snoops. Note that the fields shown are the new fields which were added in addition to CHI-B ones. When a field width increased (like different IDs) it must be stored in the transaction table to be restored with the proper width in the response (padded with zeros if needed).

TABLE 4-35:COMMAND REQUEST FIELDS

CHI E Request Field	Notes
PGroupId	The field is not used in Ncore 3.6 and must be ignored. Must be stored in OTT to generate proper Persist and CompPersist responses
Deep	The field is not used in Ncore 3.6 and must be ignored
DoDWT	The field is not used in Ncore 3.6 and must be ignored. In general, Ncore already does direct write transfers as the data does not flow through DCE
SLCRepHint	The field is not used in Ncore 3.6 and must be ignored.
TagOp	The field is not used in Ncore 3.6 and must be ignored.
TagGroupID	The field is not used in Ncore 3.6 and must be ignored.
MPAM	The field is not used in Ncore 3.6 and must be ignored. The field must be configured to a width of zero.

2004

TABLE 4-36:SNOOP REQUEST FIELDS

CHI E Request Field	Notes
MPAM	The field is not used in Ncore 3.6 and must be ignored. The field must be configured to a width of zero.

4.8.2 CHI-E Data bus

2007

This section describes how the CHI-E data bus is integrated into Ncore 3.6, changes in this section are primarily limited to AIUs. Note that DVMs are covered in a separate section. Data fields are shown in Table 4-37. Note that the fields shown are the new fields that were added in addition to CHI-B ones.

2010

TABLE 4-37: DATA FIELDS

CHI E Data Field	Notes
CBusy	Not used
OpCode	DataSepResp is not issued by Ncore Ncore must handle NCBWrDataCompAck issued by RN
TagOp	The field is not used in Ncore 3.6 and must ignored or tied to zero
Tag	The field is not used in Ncore 3.6 and must ignored or tied to zero
TU	The field is not used in Ncore 3.6 and must ignored or tied to zero

4.9 Response bus

2013

This section describes how the CHI-E response bus is integrated into Ncore 3.6, changes in this section are primarily limited to AIUs. Note that DVMs are covered in a separate section. Response fields are shown in Table 4-38. Note that the fields shown are the new fields that were added in addition to CHI-B ones.

2016

TABLE 4-38: RESPONSES FIELDS

CHI E Response Field	Notes
CBusy	Not used
PGroupId	The field is not used in Ncore 3.6 and must be copied over form the original request
StashGroupId	The field is not used in Ncore 3.6 and must be copied over form the original request
Opcode	TagMatch is not used RespSepData is not used Persist is not used, always issue combined response CompPersist issued for Persist CMOs, always use combined response DBIDRespOrd is not used StashDone is not used as Sep stash are not supported CompStashDone is not used as Sep stash are not supported CompCMO Used for non-persist CMO, in the case of Persist CMO combined response is not used <double check>
TagOp	The field is not used in Ncore 3.6 and must ignored or tied to zero
TagGroupId	The field is not used in Ncore 3.6 and must ignored or tied to zero

2019

4.10 DVM support

DVM_v8.4 flow stays the same in CHI -E.c apart from few extra fields which require mapping changes within Ncore for both DVM commands and DVM snoops. In addition, Ncore supports ACE5-H.c. This requires changes in CHI AIU, DVE and IOAIU. DVM command mapping is shown in CCMP specification.

2022

2025

DVM version system level parameter is introduced, and it is calculated and user settable based on the following table. A read only register is also introduced in GRB block to let the software/firmware know the capability/suggested DVM version of the system.

Configuration	DVM version	DVM master	DVM snooper	Note
ACE	v8	Conditional yes	Conditional Yes	Enabled by DVM_v8 property. Supported if it is set, otherwise, it can only support DVM_v7
ACE	v8.1	no	no	ACE protocol defined in ARM AMBA AXI and ACE protocol specification version E
ACE	v8.4	no	no	ACE does not support v8.4
ACE-Lite	v8, v8.1, v8.4	no	no	
ACE5-Lite	v8, v8.1, v8.4	no	no	
ACE5-LiteDVM	v8	Conditional Yes	Conditional yes	Enabled by DVM_v8 Property
ACE5-LiteDVM	v8.1	Conditional Yes	Conditional Yes	Enabled by DVM_v8.1 property
ACE5-LiteDVM	v8.4	Conditional Yes	Conditional Yes	Enabled by DVM_v8.4 property
CHI.B	v8, v8.1	Yes	yes	
CHI.E	v8, v8.1, v8.4	Yes	yes	

TABLE 4-39 DVM VERSION CAPABILITY

2028

4.11 End to end credit

Ncore 3 units uses an end-to-end credited protocol scheme.

2031

Each credit represents a free entry at the receiver and a sender needs to have at least one credit available before sending a message.

2034

The receiver in each target will be configured by Maestro to implement sufficient buffering (skid buffer) to store messages arriving from all communicating initiators.

The communication requirements are determined based on:

2037

- Address map support required by the SoC use case
- Interleave factor - directories and memories can be interleaved to improve performance

A more detailed discussion including the definition and manipulation of the interconnect matrix can be found in section 3.4.4 Connectivity mapping.

2040

The number of buffers is calculated by Maestro, based on the number of initiators, and for each initiator the number of allowed flows is defined as a design configurable parameter. A single parameter for an initiator defines the number of supported flows between that initiator and **all** targets. Therefore:

2043

- All skid buffers associated with an initiator have the same depth

The max. bandwidth available to an agent depends on the

2046

- Number of transactions it can have in flight
- The roundtrip latency for sending the request and receiving a response back
- The amount of data moved per transaction request

2049

The Ncore 3 architecture only supports a single, design time defined parameter for each initiator. The user must determine the number of outstanding transactions based on the longest latency that initiator has to any agent it communicates with. As a result, this

2052

- Leads to oversizing the total buffer in target (DCE/DMI/DII)
- Allocation is fixed at design time – buffer space may be assigned even for agents that will not communicate in the real system (e.g. due to address map configuration)

2055

4.11.1 Previous Skid buffer architecture

2058

Each target implements a skid buffer. This structure consists of a n-entry deep queue to store arriving requests and an arbiter that picks the oldest request, given a certain priority/QoS level. The implementation of an age buffer for the arbitration grows with the square of the number of entries. The data for each request occupies about 145 bits in the queue storage.

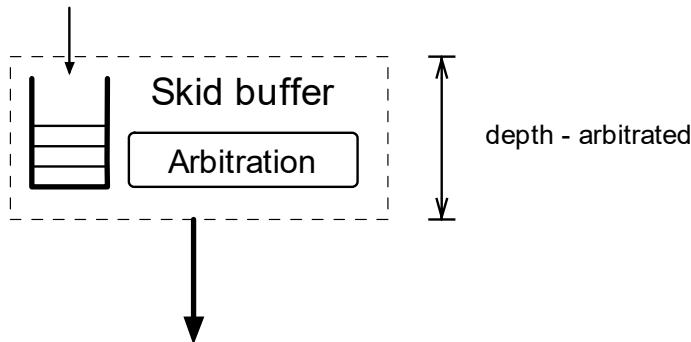
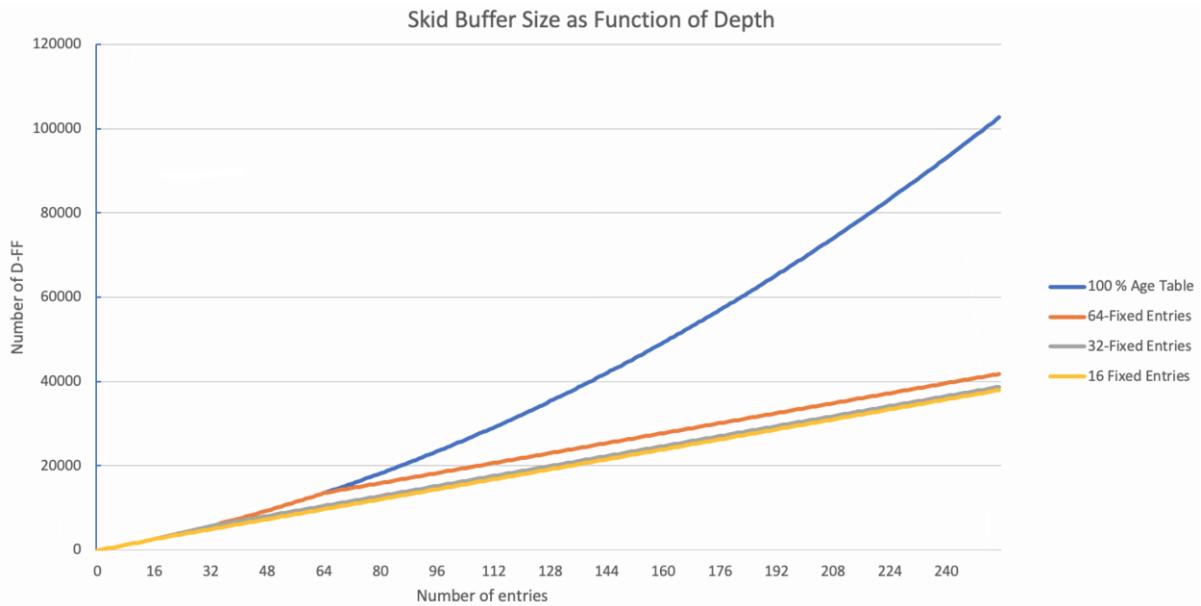


FIGURE 4-28: SKID BUFFER OVERVIEW

2061

The physical size of the skid buffer is highly dependent on the total number of entries and grows quadratically with the number of entries.



2064

FIGURE 4-29: SKID BUFFER AS FUNCTION OF DEPTH

The logic structure to implement the arbitration is growing proportionally to the age buffer size and the complexity leads to significant loss in performance (speed).

2067

As the total useful buffer is determined by an agent's bandwidth and latency – there is no use in frontloading a DMI with 100's of GB worth of traffic – an upper bound of skid buffer size for a target agent can be determined by looking at the total BW supported in steady state operation, the temporal distribution of requests and the number of interconnect buffers in the request path (queueing model interarrival time λ , Little's Law, service time μ).

2070

2073 4.11.2 Skid buffer optimization

The following chapters will describe several modifications to the previous implementation to address the problem of skid buffer explosion. Each proposal covers a different aspect of the issue and the combination of them will improve the power and area efficiency of Ncore and increase the flexibility of each design for the future.

4.11.2.1 Command Buffer Partitioning

2079 The following issues of the previous skid buffer are addressed by this change:

- The previous implementation of Ncore implements the command buffers as a single, monolithic queue where arriving command requests are stored as they arrive from initiators and retrieved based on their age and priority
- The logic structure (age buffer) attached to this queue grows with the square of the number of entries
- In steady state traffic, the skid buffer will use only some part of the entire structure

The new command buffer architecture have the following requirements.

The physical implementation of the new command buffer shall consist of two parts:

- A fixed size, limited skid buffer - This limits depth of (arbitration) visible entries – only these entries will require arbitration in age-buffer (growing with $O(N^2)$)
- An overflow buffer to maintain total depth, by adding a FiFo in front of skid buffer – most efficient implementation, only needs D-FF/SRAM for txn-data storage

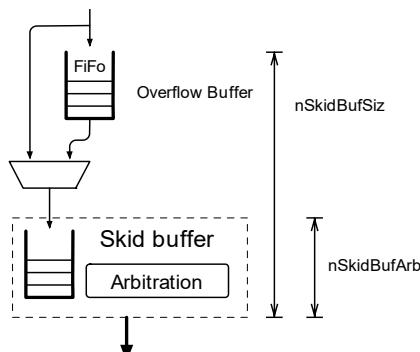


FIGURE 4-30: SKID BUFFER PARTITIONING

2094 Figure 4-30 shows how the skid buffer shall be partitioned into an arbitration visible window at the bottom and an overflow buffer at the top. Two parameters are introduced to describe the depth of the entire skid buffer ($nSkidBufSiz$) and the size of arbitration window ($nSkidBufArb$). Please refer to the parameter specification for more details.

2100 Static credit budgeting leads to overprovisioning of buffer space. Indeed, the number of credits actively used may be limited by SW scheduling – For some applications, the agents’ credit may be adjusted by SW (driver) before kicking off active burst. For dynamic credit management overflow buffer can be small – just to protect against backup. Finally, the command buffer shall have sufficient depth to store

2103 all credited transactions – for example during overlapped activity on multiple agents – without backing up traffic into interconnect (danger of deadlock). In steady state operation, the command buffer is only partially filled.

4.11.2.1.1 Area optimization for the overflow buffer with the usage of SRAM

2106 The size of the skid buffer grows significantly with the increasing number of Ncore units and the outstanding commands an Ncore unit can support for high performance configurations. When the 2109 depth of the overflow buffer/FIFO is over 256 entries, an implementation with the usage of SRAM start to provide more area advantage rather than with the usage of Flops. Therefore, the usage of SRAM shall be available as an option for all the skid buffers employed across an Ncore configuration.

4.11.2.2 Software initialization of credit counters

2112 What issues will be addressed by this change:

- The previous implementation of Ncore allocates a fixed amount of buffer space for each flow
- The allocation is fixed at design time and may not be changed
- The assignment of credits for an initiator treats all targets to the same amount of credits, independent of differences in round trip latency and BW requirements

The Ncore 3 new architecture have the following requirements:

1. The value of credits shall be programmable at each initiator
 - a. For each reachable target, a CSR shall provide a field to modify the allocation of credits for a flow
 - b. Maestro shall provide path vectors (calculated based on connectivity) to support generation of the required Credit Control Registers:
 - i. For each CAIU:

Name	Elements	Description
boolDcePath[i]	# of DCE in system	a boolean, indicating a command path exists from CAIU to DCE[i]
boolDmiPath	# of DMI in system	a boolean, indicating a command path exists from CAIU to DMI[i]
boolDiiPath	# of DII in system	a boolean, indicating a command path exists from CAIU to DII[i]

2124 ii. For each NCAIU:

Name	Elements	Description
boolDmiPath	# of DMI in system	a boolean, indicating a command path exists from CAIU to DMI[i]
boolDiiPath	# of DII in system	a boolean, indicating a command path exists from CAIU to DII[i]

iii. For each DCE:

Name	Elements	Description
boolDmiPath	# of DMI in system	a boolean, indicating a command path exists from CAIU to DMI[i]

- c. The CSR shall provide a means to determine if a communication path between this initiator and a specific target exists

- d. The max. number of credits available for a flow shall be programmable at runtime
 - 2. A mechanism to determine the configured skid buffer size for each target shall be provided by implementing a read-only CSR
 - 3. The initial allocation (at power-on-reset) shall be determined as follows:
 - a. If a Boot Region has been configured at an initiator, the non-coherent target defined by the MIG used for the initial boot region shall be initialized to 2 credits
 - b. If a Boot Region has been configured at an initiator, the target(s) associated with the system DII shall receive two credits - this needs to consider possible interleaving (unlikely to be used, but possible if DMI used to host the boot region?)
 - c. all other credit counts in CAIU/NCAIU/DCE shall receive 0 credits - the boot loader firmware shall determine the available budget for each agent by reading the Skid Buffer Size Register (SBSR) for each
 - 4. This description does not apply to credits allocated to snoop transactions or DV messages

The implementation is described hereafter.

2142 The format of the credit control field shall be 8-bits wide:

TABLE 4-40: CREDIT CONTROL FIELD FORMAT

Bit	Type	Counter State	Description
7:5	RO	000: Normal Operation	Counter is operating normally, some outstanding credits
		001: Empty (== 0)	All credits have been used - should be a transient state during which no additional transactions may be sent
		010: Negative (< 0)	All credits have been used - this state would normally be reached when SW reduces the credit limit to a smaller value by an amount that exceeds the currently available credits. This is a transient state, during which no transactions may be sent. As outstanding credits arrive, the counter will increment through zero to allow requests to resume
		011: Reserved	Should never be observed - Error
		100: Full (== Limit)	No outstanding transactions, all credits are back
		101: Reserved	Should never be observed - Error
		110: Reserved	Should never be observed - Error
		111: No Connection	Special signature to indicate a non-existing connection between this initiator and the target represented by this control field. Maestro implements a connectivity map where some routes may not be required, this code allows firmware to recover the implemented connectivity map between initiators and targets
		Credit Limit	
4:0	RW	0 .. 31	This 5-bit value may be programmed to set the credit limit available for this connection. It is the user firmware's responsibility to set this value correctly, so that the total number of credits assigned between all initiators does not exceed the available buffer space

The credit counters:

2145 The credit counter shall implement a two's complement counter using 6 bits. The counter shall be updated:

- when a credit is consumed - decrement counter
- when a credit is returned by receiving a response - increment counter
- when the CreditLimit is written - add the value calculated by newCreditLimit - oldCreditLimit. This value may be negative if the new value is smaller than the old value, effective decreasing the available credit

2148 All 3 events may occur in the same clock cycle! At reset the counter shall be cleared to zero or preset to a positive value. Any counter value ≤ 0 indicates that no credits are available and requests must not be sent.

2151 The Credit Control Registers (CCR) in CSR space:

- Ncore architecture may eventually support up to 32 DCE/DMI/DII and we shall plan our register map accordingly
- Each agent will be assigned an ordinal number within its group (0..31)
- For AIU/NCAIU, each 32-bit Funit.CSR[index] shall pack credit control fields for all agent types (DCE, DMI, DII) using the same index, starting at the least significant byte, for example:
 - AIU[x].CCR[0] = {0xE0, DII_CCF, DMI_CCF, DCE_CCF}
 - AIU[x].CCR[1] = {0xE0, DII_CCF, DMI_CCF, DCE_CCF}

2157 The most significant field in the register has been reserved for future expansion

- CCR registers shall be starting at offset 0xC00 within each unit's local address window
- The number of registers created shall be determined by the unit with the highest index
- Partially filled slots in registers shall be initialized with 0xE0, indicating to firmware that either no unit exists with this index or that the connection between this initiator and the target, mapped into this slot, is not implemented (no path exists)

2160 The Skid Buffer Size Info Register (SBSIR) in CSR space:

2169 Each unit implementing a skid buffer at its frontend shall announce the implemented size of the skid buffer in a CSR read-only register or a read-only field in an existing register. The register shall be using this format:

TABLE 4-41: SKID BUFFER SIZE INFO REGISTER FORMAT

Bit	Type	Meaning	Description
7:0	RO	SkidBufArb (0 .. 255)	Number of entries visible to arbitration in a split skid buffer configuration, value must be \leq SkidBufSize. This value is supplied by a new parameter: nSkidBufArb
15:8	RZ	Reserved (0)	Keep for future expansion

Bit	Type	Meaning	Description
25:16	RO	SkidBufSize (.. 1023)	Total Size of skid buffer implementation - this value may be identical to SkidBufArb if no split skid buffer has been implemented This value is supplied by a new parameter: nSkidBufSize
30:26	RZ	Reserved	Keep for future expansion
31	RO	Valid = 1	Valid bit, indicates presence of the register

The CSR address space for DCE/DMI/DII has an empty slot at 0xFF0 which shall be used to implement this register, DMI shall implement an additional register at 0xFE0 to implement a register for MRD buffer space information.

4.11.3 Software Support (Maestro)

New parameters are required to configure skid buffers at each target. For DCE and DII only one parameter set is required, DMI implements two skid buffers, one for coherent, the other for non-coherent traffic. Each FU shall have a private version of their parameters to support individual customization.

2175 4.12 Exclusive monitor

4.12.1 Coherent Exclusive support

CHI specifies Ex Load as ReadClean, ReadNotSharedDirt & ReadShared. These translate to CmdRdCln, CmdRdNshDty and CmdRdVld in Concerto. Ex Store is specified as CleanUnique which translates to CmdClnUnq in concerto.

On receiving Ex Load CHI-AIU always responds back with pass when data is transferred.

2181 The DCE implements a basic monitor and a configurable number of tagged monitors. (A DCE may be configured with zero tagged monitors.) The basic monitor consists of a valid bit for each AIU unit ID and LpID pair, i.e. one bit for each processor in the system, while each tagged monitor consists of a basic monitor and an associated cacheline address field. The valid bit for each type of monitor indicates whether a given processor is performing an exclusive access sequence, while the cacheline address field captures, or tags, the cacheline address for a given sequence. A tagged monitor is in-use if one or more processors are performing an exclusive access on the tagged address, i.e. any valid bit is set in the tagged monitor, and available if no processor is performing an exclusive access on the tagged address, i.e. no valid bits are set. At reset, the valid bits in the basic monitor and in any tagged monitors are set to the invalid state.

2184

2187

2190

When DCE receives an Ex Load an address cam is done on all active tagged monitors and either one of the following three scenarios will get executed:

- 2193
- If there is an address match corresponding processor's ID valid bit is set in that monitor and the valid bits of the processor are cleared in other tagged monitors and basic monitor.

- If there is no address match and an empty tagged monitor is available, then that monitor is loaded with the address and the corresponding processors ID valid bit is set. Furthermore, the valid bits of the processor are cleared in other tagged monitors and basic monitor.
- If there is no address match and no empty tagged monitors are available, the corresponding processors ID valid bit for basic monitor is set. Furthermore, the valid bits of the processor are cleared in other tagged monitors.

Note that above actions of clearing the processor ID bits in other monitors ensures that at any given time a processor can do only one exclusive per DCE (in other words address region specified by DCE interleaving).

When DCE receives an EX Store an address cam is done on all active tagged monitors and either one of the following scenarios will get executed:

- If the requestor holds the cacheline and the address matches and the valid bit for that processor in the tagged monitor is set, then the valid bit for the processor is set in the basic monitor. In addition, the valid bit for the processor is cleared in the matching tagged monitor. In this case, the exclusive store passes.
- If the requestor does not hold the cacheline and the address matches a tagged monitor, then the valid bit for the processor is set in the matching tagged monitor, and the valid bits for the processor are cleared in all other tagged monitors and the basic monitor. In this case, the exclusive store fails.
- If the address matches and the valid bit for that processor in the tagged monitor is not set, then the valid bit for the processor is set in the matching tagged monitor. In addition, the valid bits for the processor are cleared in all other tagged monitors and the basic monitor. In this case, the exclusive store fails.
- If the requestor holds the cacheline and the address does not match and the valid bit for that processor in the basic monitor is set, then the valid bit for the processor remains set in the basic monitor. In addition, the valid bits of other processors within the basic monitor are cleared. In this case, the exclusive store passes.
- If the requestor does not hold the cacheline and the address does not match and at least one tagged monitor is available, then that tagged monitor is selected, the valid bit for the processor is set in the tagged monitor, and the address is tagged in that monitor, and the valid bits for the processor are cleared in all other tagged monitors and the basic monitor. In this case, the exclusive store fails.
- If the requestor does not hold the cacheline and the address does not match and no tagged monitors are available, then the valid bit for the processor is set in the basic monitor, and the valid bits for the processor are cleared in all tagged monitors. In this case, the exclusive store fails.
- If the address does not match and the valid bit for that processor in the basic monitor is not set and at least one tagged monitor is available, then that tagged monitor is selected, the valid bit for the processor is set in the tagged monitor, and the address is tagged in that monitor. In addition, the valid bits for the processor are cleared in all other tagged monitors and the basic monitor. In this case, the exclusive store fails.

- 2235 • If the address does not match a tagged address and the valid bit for that processor in the basic monitor is not set and no tagged monitors are available, then the valid bit for the processor is set in the basic monitor. In addition, the valid bits for the processor are cleared in all tagged monitors. In this case, the exclusive store fails.

2238 In the case when an exclusive message passes DCE completes the exclusive store as expected by sending out required snoops and updating the snoop filter. DCE will also set the ExOkay bit in the StrReq.

2241 In the case where exclusive message fails DCE completes the transaction but does not send out any snoops (that may have been required) or change the snoop filter status. DCE will also not set the ExOkay bit in the StrReq.

2244 Note that this implementation restricts one exclusive operation per processor per address region. here the address region is defined by the interleaving done across DCEs.

4.12.2 CHI-E Exclusive transaction support

2247 CHI E supports a mechanism for exclusive transactions that does not require point of coherency PoC monitor. This mechanism relies on a precise snoop filter and snooping the requester. To limit the changes in Ncore 3.6 these exclusive transactions are emulated within the CHI AIU. The emulation mapping and process is shown in

CHI E Native Command	Concerto Commands	Notes
ReadPreferUnique	CmdRdNshDty	Treated as read not shared dirty
MakeReadUnique	CleanUnique + CmdRdNshDty	Issue CleanUnique exclusive if it passes issue Comp_UC response, if the CleanUnique exclusive fails then issue CmdRdNshDty to get the data. always send the data back to agent as SC i.e., CompData_SC even if the DtrReq received is unique. Downgrading here is okay from coherency perspective and is required by CHI E spec

TABLE 4-42: CHI E EXCLUSIVE REQUEST MAPPING

2253 Exclusive MakeReadUnique can end up being processed as two transactions, in this case it is desirable to use a single transaction table entry.

Note: CmdRdNshDty generated from ReadPreferUnique(Excl) or second part of MakeReadUnique(Excl) needs to set ES (Exclusive Access) bit in CmdReq. Same thing applies to CleanUnique(Excl).

2256

4.12.3 Non coherent exclusive support

2259 Ncore 3.6 implements an optional non-coherent exclusive monitor. The monitor shall be instantiated at the PoS (point of serialization) namely DMI or DII. Please note that if a cache is present in DMI the exclusive monitor is then required.

[2262](#) In the absence of exclusive monitor for non-coherent transactions, the target device connected to DMI or DII is required to implement the exclusive monitor.

[2265](#) In contrast with Ncore 3.4, all non-coherent exclusive transactions should be cacheable requests with visibility attribute set as system visible.

4.12.3.1 Non coherent exclusive support from a DII⁹

[2268](#) There will be an entry for each exclusive transaction flow. Each entry will consist of an “ID” that must match constructed from the combination of the mpf2 field and the initiator ID. In this case the mpf2 field will contain the AXID which will be the same ID used for the native layer transaction.

The DII will only see non-coherent exclusives.

[2271](#) To support exclusives the DII needs two changes:

- a) To resolve RAR and WAW hazards the AxID allocation is not based of address. This enforces that all transactions to the same address will be ordered within the read and write channel. This change is for all DII configurations.
- b) For DII configurations with an exclusive monitor the DII adds RAW and WAR hazard checking against transactions with no ordering causing a head of line block at the exit of the skid buffer. This is because if transactions are outstanding with no ordering the DII will not enforce any cross table address hazards.
- c) The DII will force all exclusive transactions to be at least RO ordering, and will keep EO if it is EO

[2280](#)

Type of request	Match ns + Addr	Match AxId, FunId	Tag Monitor status (full/Not full)	Tag Monitor update	Monitor response
Load Ex	Match	Match	X	- If on the same entry: Do nothing - If on different entries: Replace the Tag on the ID that matched	PASS
		No Match	Full	Replace an existing entry. Selection is round robin.	PASS
			Not Full	Set a new entry	PASS
	No Match	Match	X	Replace the Tag	PASS
		No Match	Full	Replace an existing entry. Selection is round robin.	PASS

⁹ This section is merged from Ncore 3.6 Exclusive Monitor Micro-architecture, version 0.53

Type of request	Match ns + Addr	Match AxId, FunitId	Tag Monitor status (full/Not full)	Tag Monitor update	Monitor response
			Not Full	Set a new entry	PASS
Load	x	x	x	Do nothing	x
Store	Match	x	x	Clear all the entries with matching address	x
	No Match	x	x	Do nothing	x
Store Ex	Match	Match	X	Clear all the entries with matching address	PASS
				Do Nothing	FAIL
	No Match	x	x	Do nothing	FAIL
			x	Do nothing	FAIL

TABLE 4-43: MONITOR UPDATE REQUIRED IN A DII

2283

For load exclusive, the ID match has priority over address match. Which means that if an entry matches for address but not for ID and another one matches for ID but not for address the expected behavior is to replace the tag in the entry which matched ID.

2286

If there is a fail for an exclusive store then that command will be dropped and the cmstatus will correspond to the following table. The DII will be responsible for dropping the command, data, and properly completing the protocol.

2289

When the exclusive is a fail the DtwRsp will always be an early response and will contain a cm_status indicating the success/failure of the exclusive operation. When it is a pass, the DtwRsp is a late response, meaning that the transaction must wait for the response from the native interface. The exclusive monitor status will be stored in the context table and will be used to generate the late response per the table below (See CCMP spec 4.5.3.1 CMStatus, and error architecture specification):

Status	Native response	CMStatus[7:6]	CMStatus[5:0]
Pass	OKAY	2'b00	6'b000001
Pass	SLVERR	2'b10	6'b000011
Pass	DECERR	2'b10	6'b000100
Fail	OKAY	2'b00	6'b000000

2295

TABLE 4-44: SM STATUS DEPENDING ON THE SUCCESS OR FAILURE OF THE EXCLUSIVE TRANSACTION

4.12.3.2 Non coherent exclusive support from a DMI⁹

2298

Each monitor entry is used for one and only one exclusive sequence. Consequently, it will store the address, the ns bit, the AxId contained in the mpf2 field and the funitID. Assuming we do not support 128 byte exclusive transaction, 64 byte aligned address is used such that we do not need to store the size of the transaction. This way narrower access will always match wider access.

Type of request	Match ns + Addr	Match AxId, FunitId	Tag Monitor status (full/Not full)	Tag Monitor update	Monitor response
Load Ex	Match	Match	X	- If on the same entry : Do nothing - If on different entries : Replace the Tag on the ID that matched	PASS
		No Match	Full	Replace an existing entry. Selection is round robin.	PASS
			Not Full	Set a new entry	PASS
	No Match	Match	X	Replace the Tag	PASS
		No Match	Full	Replace an existing entry. Selection is random.	PASS
			Not Full	Set a new entry	PASS
Load	x	x	x	Do nothing	x
Store	Match	x	x	Clear all the entries with matching address	x
	No Match	x	x	Do nothing	x
Store Ex	Match	Match	X	Clear all the entries with matching address	PASS
		No Match		Do Nothing	FAIL
	No Match	x	x	Do nothing	FAIL
			x	Do nothing	FAIL

2301

TABLE 4-45: MONITOR UPDATES REQUIRED IN A DMI

2304 For load exclusive, the ID match has priority over address match. Which means that if an entry matches for address but not for ID and another one matches for ID but not for address the expected behavior is to replace the tag in the entry which matched ID.

2307 In the tables above a match can only occur if the entry is valid. The response indicated assumes that the native interface response is OKAY and not an error response.

It is recommended having the size set to the number of agents which are expected to use exclusives at the same time to limit the number replacements. This should be well communicated to the customer.

2310 When the monitor is full, an entry will be selected for replacement. It will be selected round robin starting by entry 0. Every time an entry is replaced the entry number to be selected will increase by 1. When it reaches the last entry, it will reset and wrap back to entry 0.

2313

4.13 Constraint of Mixed Coherent and Non-coherent Transactions

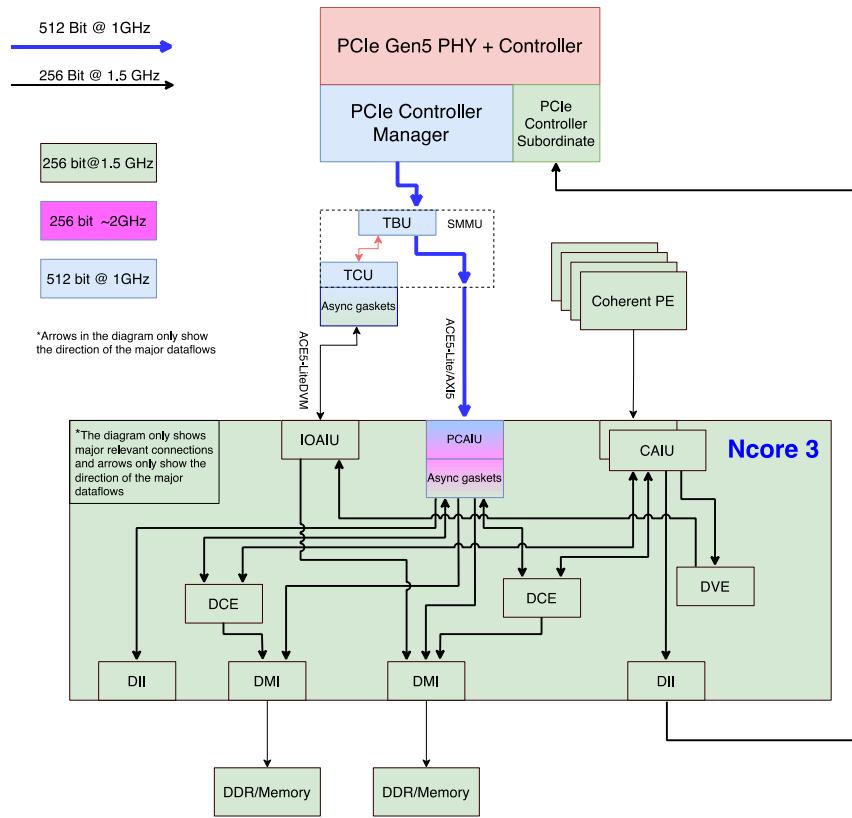
Ncore 3 rely on CPU to control the ordering behavior of the issued transactions. For cacheable transactions from same AIU, it is based on the assumption there wont be outstanding cacheable transactions to the same cacheline address. For non-coherent(ReadNoSnoop/WriteNoSnoop) and non-cacheable(ReadOnce and WriteUnique) transactions, Ncore 3 does not guarantee order of mixed non-coherent transactions with non-cacheable transactions.

4.14 PCI Express support and acceleration

A new configuration of IOAIU, which is called as PCAIU configuration¹⁰, is described in this section to accelerate PCIe traffic. Please note that a PCAIU and a PCAIU configuration carry the same meaning in this section.

4.14.1 The system view of PCIe acceleration

¹⁰ Please note this acceleration still observes the same code base and it is just a new configuration only



2328

FIGURE 4-31: THE SYSTEM VIEW OF PCIE ACCELERATION WITH ONE PCIE INTERFACE

2331

Figure 4-31 shows the system view on how a PCAIU configuration is used. It is used to directly connect to a 3rd party PCIe controller to provide sufficient throughput while observing the Ordered Write Observation ordering rule throughout an Ncore. Please note that blue line out of the AXI bridge of the 3rd party PCIe controller might have the combined traffic of the MSI-X interrupts and data, and necessary SoC level components such SMMU and GIC are required to filter out the data traffic to one or two IOAIU(s) with the PCAIU configuration. Since a PCAIU configuration does NOT provide DVM capability, all SMMU virtual address translation required DVM operations MUST be provided by an extra IOAIU with either an ACE/ACE5-LiteDVM interface configured.

2340

4.14.2 Assumptions and limitations

2343 A PCAIU configuration accelerates PCIe traffic with the following assumptions and limitations:

- PCIe observes the producer-consumer model of operation, which implies that processing elements across the system should be well behaved and do not attempt to read the data while a stream of writes is still updating it.
 - The overall performance degrades even though this situation has been fully comprehended in a PCAIU configuration
- 2346
• Directly interface with an external 3rd party¹¹ PCIe controller along with an AXI bridge, which manages and enforces PCIe ordering rules
 - It represents a combination of PCIe PHY with a same or newer generation PCIe controller and its associated AXI bridge as shown in Figure 4-31
- 2349
• The data interface can be configured as AXI4, AXI5, ACE-Lite or ACE5-Lite without the snoop interface
 - Supported AXI5 features are as shown in Table 4-46
 - If configured as an ACE-Lite/ACE5-Lite interface, the master interface always sets AxBAR and AxSNOOP to '0' so that requests are restricted to ReadNoSnoop, WriteNoSnoop, ReadOnce, and WriteUnique. Supported transaction types are shown in Table 4-48
 - WriteLineUnique shall be supported in a PCAIU configuration just to have better portability across different 3rd party vendor
- 2352
• 256-bit data interface must be configured to support the throughput of PCIe a Gen5 interface with 12 lanes and more, 128-bit interface can be configured if a PCIe Gen5 interface is deployed with only 8 or 4 lanes
- 2355
• Posted Requests from PCIe using AXI-ID = 0, when Posted ID management feature is disable in the AXI bridge¹², non-posted Requests also use AXI-ID =0. However, transactions with AxID not equal to zero are expected to be observed
 - A PCAIU configuration strictly maintains the order by an AxID and
 - It follows AMBA ordering rules with the same AxID as per described in section **Error! Reference source not found.**
- 2358
• The Observed Write Observation property is always enabled for a PCAIU configuration
- 2361
• Proxy cache is always not available for a PCAIU configuration
- 2364
• DVM functionality is always not supported for a PCAIU configuration
 - Any virtual address to the local physical address translation as shown in Figure 4-31 shall be branched off and connected to an IOAIU with either ACE/ACE5-LiteDVM configuration to handle the necessary DVM operations associated with PCIe.
- 2367
• It handles the accesses to both coherent and non-coherent regions

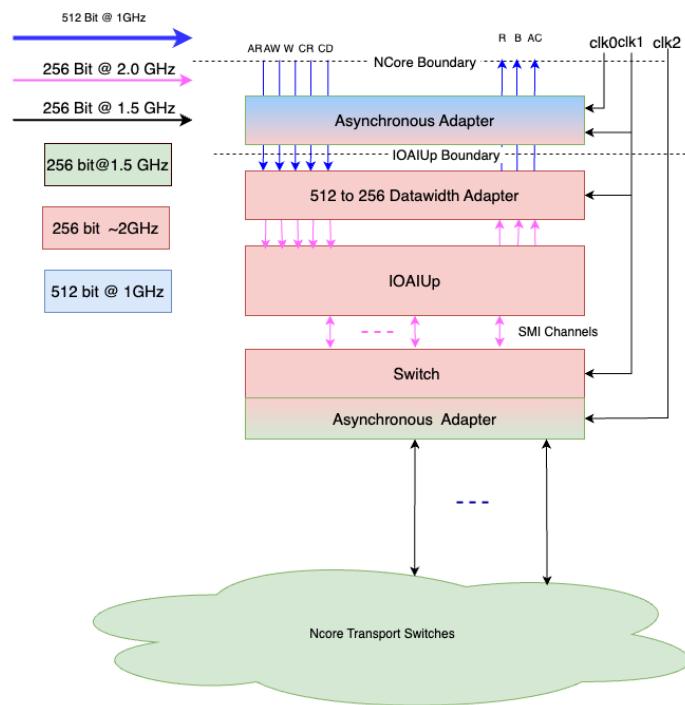
¹¹ Synopsys PCIe Gen5 or higher controller and its associated AXI bridge is assumed as the base for this proposal.

¹² In section 5.4.3 of Synopsys PCIe controller data book (version 6.20a, April 2024)

- 3rd party AXI Bridge can only support address bus width of either 32 or 64. An Ncore takes the smaller address bus width supported between CHI agents and AXI/ACE agents, this leads to:
 - 2379 • Maximum 52 bits of physical address space can be accessed if any CHI coherent agent is configured
 - 2382 ▪ This implies that only maximum 52 bits effective access space within an Ncore even if the 3rd party controller can support up to 64 bits address space
 - 2385 ▪ Even though ARM architecture has some typical address width with different versions of its architecture, PCAIU should support address width from 32 bits all the way to 52 bits just to provide full compatibility with RISC-V cores or other 3rd party CPU/DSP cores
 - 2388 • A PCAIU observes the same capabilities and constraints in terms of Atomic support such as Atomic operation has to be supported for DMI only if an SMC is configured
 - 2391 • PCIe only supports three Atomic operations which are: Atomic Compare and Swap, Atomic Fetch and Add and Atomic Fetch and XOR¹³. Its capabilities and handling are shown in Table 4-47
 - 2394 • Since the Atomic support has to be supported with an SMC is configured in (a) DMI(s), it implies the Atomic result is observable inside of the Ncore and no alternative external data path exists between an Ncore and the downstream storage that is connected to this specific DMI. Otherwise, the agents that are connected to the alternative data path might not observe the correct Atomic results since they are stored inside of the SMC inside of this specific DMI.
 - 2397 • To seamlessly interface with a PCIe Gen5 x 16 lanes configuration:
 - 2400 • A PCAIU configuration targets to run at 2 GHz with 256-bit data bus at a technology node equivalent to TSMC 5nm or better (smaller)
 - 2403 ▪ An AXI4/5, ACE-Lite or ACE5-Lite interface with 512-bit data runs at 1GHz can be used to seamlessly interface with 3rd party PCIe controller to provide more flexible integration options
 - 2403 ▪ Necessary asynchronous/synchronous bridge(s) between the native interface and the kernel of a PCAIU is(are) required to provide frequency and data width adaptions as shown in Figure 4-32
 - 2406 • Alternatively, a PCAIU configuration can run at 1 GHz with 512-bit data bus
 - 2406 ▪ Necessary asynchronous/synchronous bridge(s) between a PCAIU and the transport network is(are) required to provide frequency and data width adaptions
 - 2409 • It is recommended to have two separate gaskets to fulfil both frequency and data width adaption needs: one for frequency adaption and one for data width adaption

¹³ As defined in section 6.15 of PCIe Express Base Specification Revision 5.0, Version 1.0, published on 22 May 2019

- 2412 ▪ The instantiation of the above gaskets can be enabled once Maestro identifies the master interface from the 3rd party PCIe controller has a wider data width than the native data width of PCAIU
- 2415 ▪ Recommend placing the frequency adaption gasket in front of the data width adaption gasket, then connecting a PCAIU
- 2418 • Necessary pipelines to aid timing closure and physical design should be considered to achieve this goal
 - For example, Multi-cycle SRAM option should be an option for the Outstanding Data (OD) buffer
- 2421 • Proxy cache is NOT expected to be configured along with a PCAIU configuration. However, a PCAIU participates cache coherent operations, thus, necessary interfaces should be connected to a DCE(s) just as if a proxy cache is configured to fulfil the functionalities.
- 2424 • Cache_Stash_Transactions property is NOT expected to be enabled for a PCAIU configuration
- 2427 • No extra or special error handling for this configuration
 - No multi-ported option is expected for this configuration
 - PCIe doesn't support native WRAP transaction. However, the 3rd party PCIe controller does issue WRAP transaction when PCIe generates Atomic transactions as a manager. Also, the subordinate port of the 3rd party PCIe controller does support WRAP transaction once it is enabled in its PCIe configuration.



2430

FIGURE 4-32: HOW ASYNCHRONOUS AND DATAWIDTH ADAPTERS ARE CONNECTED

2433

TABLE 4-46: AXI5 FEATURES SUPPORTED BY SYNOPSYS CONTROLLER

AXI5 Feature	Support
Atomics	Yes
Unique ID Indicator	Yes
Read Data Chunking	Yes
Poison	Yes
Interface Check	Yes but with *user bits

2436

TABLE 4-47: SUPPORTED PCIE ATOMIC OPERATIONS FOR A PCAIU

PCIe Supported Atomic Operations	Operation Granularities	Corresponding AXI5 Atomics Transactions
FetchAdd	32 bits, 64 bits	AtomicLoad (ADD)
Swap	32 bits, 64 bits	AtomicSwap
CAS (Compare and Swap)	32, 64 and 128 bits	AtomicCompare

2439

TABLE 4-48: ACE LITE TRANSACTIONS – 3RD PARTY PCIE IP¹⁴

2442

Cache Coherency	Request Type	Peripheral Type	Memory Type ¹⁵ 0: Peripheral 1: Main Memory	NS ¹⁶	TH ¹⁷	AxSNOOP	AxBAR	AxDomain	Shareability Domain	Memory Type
Non-coherent	Message	Peripheral	X	X	X	4b0000	2b00	2b11	System	Device, Non-bufferable
Non-coherent	Read or Write	Peripheral	0	X	X	4b0000	2b00	2b11	System	Device, Non-bufferable
Non-coherent	Read or Write	Memory	1	1	X	4b0000	2b00	2b11	System	Normal, Non-cacheable Non-bufferable
Coherent	Read	Memory	1	0	0	4b0000	2b00	2b10	Outer Shareable	Writeback, No-allocate
Coherent	Write	Memory	1	0	0	4b0000	2b00	2b10	Outer Shareable	Writeback, No-allocate

¹⁴ This table has been copied from SNPS PCIe IP Databook (version 6.20a April 2024), Table 5-23 in section 5.5¹⁵ Set by the CFG_MEMTYPE_VALUE field of the COHERENCY_CONTROL_1_OFF register¹⁶ NS = non-snoop property of PCIe TLP, this is available as a sideband signal which we DON'T use¹⁷ TH=PCIe TLP Processing Hints

Cache Coherency	Request Type	Peripheral Type	Memory Type ¹⁵ 0: Peripheral 1: Main Memory	NS ¹⁶	TH ¹⁷	AxSNOOP	AxBAR	AxDomain	Shareability Domain	Memory Type
Coherent	Read	Memory	1	0	1	4b0000	2b00	2b10	Outer Shareable	Writeback, Read-allocate
Coherent	Write	Memory	1	0	1	4b0000	2b00	2b10	Outer Shareable	Writeback, Write-allocate

²⁴⁴⁵ 4.14.3 Function descriptions of the PCAIU configuration

A PCAIU configuration tries to accelerate PCIe traffic with the following goals:

1. Comply and take advantage of PCIe producer-consumer model
2. Optimize data transfer efficiency for both read and write traffic with a payload as big as 4096 bytes
3. Observe the ordering rules imposed by PCIe

For example, a burst write with the maximum payload size of a PCIe can be as big as 4096 bytes. This translates to a burst length of 128 for a PCAIU configuration with 256-bit data bus. As shown in Figure 4-33, the write command and address information is available right at the time when AW channel is received. In a couple of cycles¹⁸, a PCAIU configuration should be able to process all the necessary information such as how many cache lines the incoming burst has, does it fall in coherent region or not etc.. While at the same time, the corresponding write data still takes many cycles to fill up the Outstanding Data (OD) buffer. The longer the burst, the wider the window between AW and W can be. Thus, the design intent is to leverage this window to accelerate the write update for both coherent and non-coherent regions.

¹⁸ Implementation depended and it is not a timing critical path

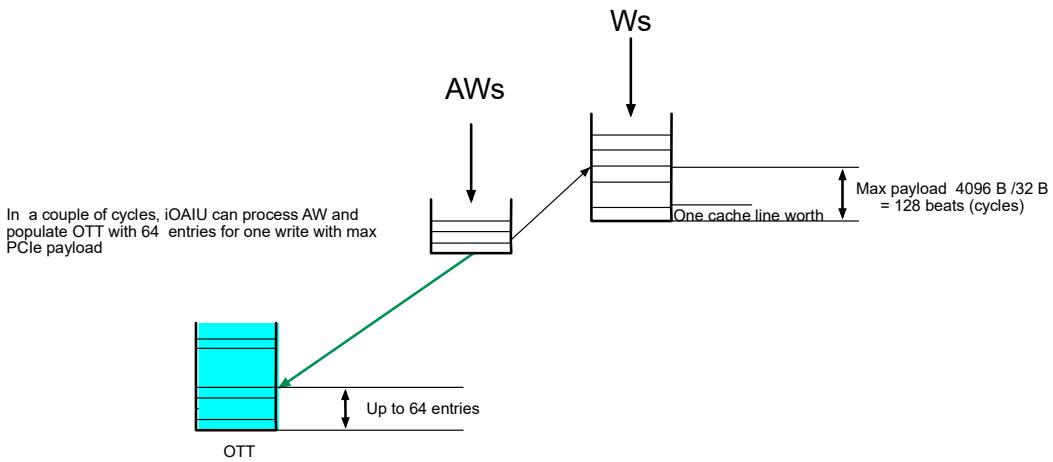


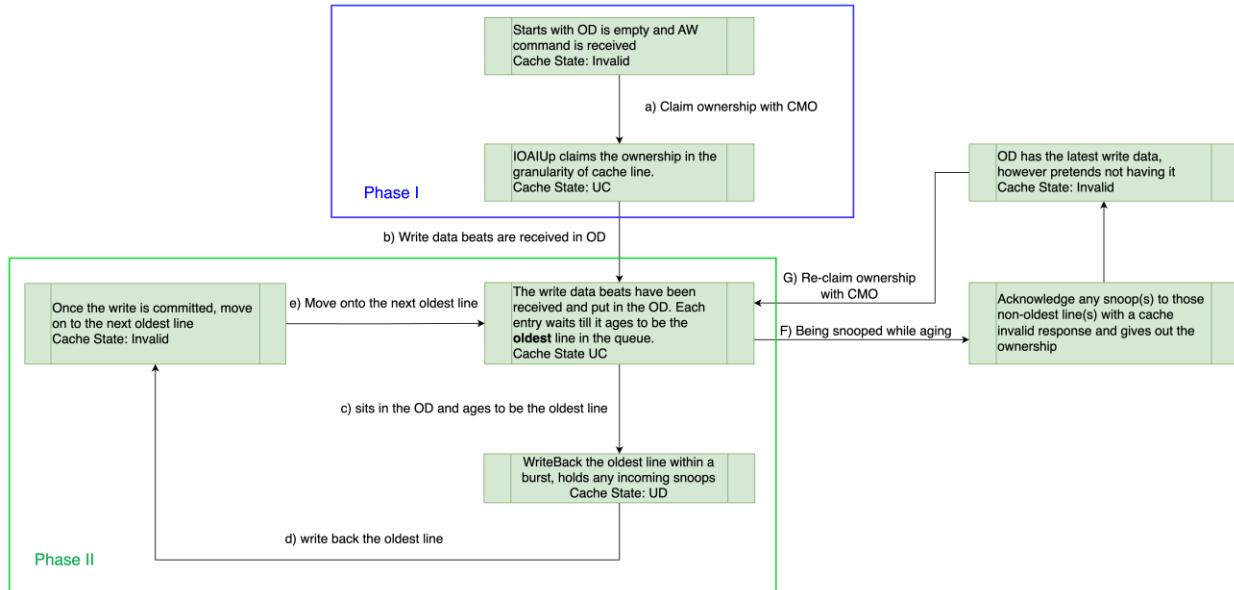
FIGURE 4-33: THE WRITE DATA STREAM OF A PCIE TRANSACTION

2463 4.14.3.1 Handling of the write traffic to the coherent regions

As shown in Figure 4-34, the two-phase flow can be summarized in the following steps:

- 2466 a) During the first phase, the window between AW and W is fully leveraged to claim the ownership while the write data is still arriving at the same time. Thus, a CmdClnUnq (CleanUnique) transaction(s) (CmdMkUnq (makeUnique) might also be considered to speed up the process) is(are) used to claim the ownership for all the cache lines included in a write at a granularity of a cache line. The incoming write will perform a CMO to get it in a UCE state.
- 2469 b) All the write data are put into a queue in a granularity of a cache line, each of them is aging to become the oldest line before it can be committed to the memory. The cache line state stays at UC before it becomes as the oldest line in the queue.
- 2472 c) Once it is the oldest on its AXID chain it will start blocking snoop requests, and essentially “commit” the data making it UD/UDP.
- 2475 d) Once it is in the UD/UDP state it can start the Writeback. Right at the time when it starts the WriteBack, all incoming snoops will be held till the end of step e)
- 2478 e) Once the Writeback completes, it transitions to the IX state. It responds all snoops received back in step d) and replies with an invalid response(s)
 - a. It is recommended to conducting a UPDReq to the DCE at this step to make the next coherent read more performant. But it is up to the designer to make an implementation depended decision at the micro-architecture level

The same flow is repeated till all the data, which are represented in multiple cache lines within a specific burst write, are committed to the memory.



2487

Figure 4-34: THE TWO-PHASE FLOW CHART

Notice that right after step b), a not-the-oldest line(s) in the OD, might be snooped by other coherent agents even though this behavior is not considered as a well-behaved producer-consumer PCIe usage model. Under such circumstance, the following procedures are taken:

- 2490
- F) A PCAIU configuration acknowledges any snoop(s) with an invalidate response and gives out the ownership for the cache that is being snooped
 - G) OD has the latest write data but pretends it doesn't and it needs to re-claim the ownership once it becomes the oldest line

2496

Please note that the Atomic transaction doesn't go through the first phase of the flow but only starts from step b when it becomes the oldest transaction in OD.

2499

Figure 4-35 shows the details of relevant CCMP sequences to complete a two-phase flow. Once the 2nd phase starts for a specific cache line, a PCAIU delays any snoop request from a DCE(s) until it makes the forward write update (starts from CmdNcReqx and finishes at the point of UpdRspx) to finish as shown as the colored sidelines (blue and cyan bars). This delay guarantees whatever reads to the updated lines are placed after the corresponding write updates are completed, which enables streaming the writes from a PCAIU to different DMIs even out of order among the writes included in the same burst even they target different DMIs. One side note is that DMI needs to be sized properly for its skid buffer to make sure the write buffers can always be available once the write update commands are received from a PCAIU. This implies that an StrReq can always be generated once a CmdNcReq is received from a PCAIU.

2505

Please note that all the necessary coherent connections from DCE to PCAIU are required even though proxy cache option is not configured for the PCIe acceleration. The behaviors described above require a PCAIU to participate snoops just as a proxy cache is configured. Also, the two requests that target to the same DCE in the first phase of the flow are assumed to have the similar behaviors as shown in Figure 4-35 just for the simplicity.



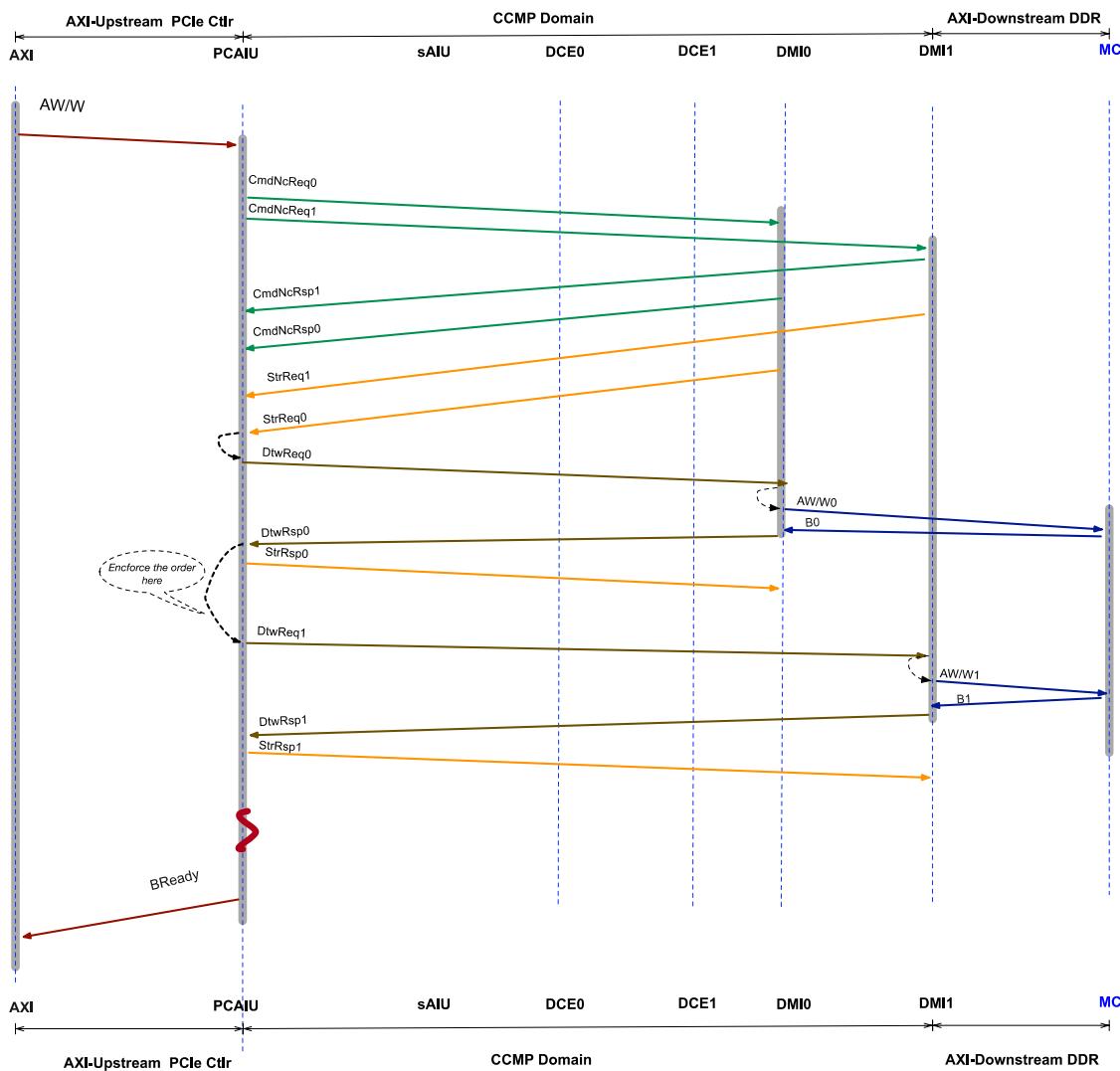
Figure 4-35: THE TWO-PHASE FLOW TO HANDLE THE WRITE TRAFFIC TO THE COHERENT REGIONS

4.14.3.2 Handling of the write traffic to the non-coherent regions

2514 The handling of the write traffic to the non-coherent regions is a subset of that as in the coherent regions, which is shown in Figure 4-36. An ordering point exists and applies to the messages replied from multiple DMIs if they are configured. Please note that DCE(s) is(are) and associated UpdReq/UpdRsp are not part of this flow because
2517 this flow is for the accesses to the non-coherent regions.

In this scenario, order needs to be enforced once a PCAIU switches writes between multiple DMIs. However, streaming can also be achieved if there is one DII that terminates the traffic from a PCAIU.

2520



2523

Figure 4-36: THE HANDLING FLOW OF NON-COHERENT WRITE TRAFFIC

[2526](#) Please note that PCAIU also needs to check DTRReq (not shown in Figure 4-36) on top of DTWrsp at the ordering point for all Atomic transactions defined in Table 4-47.

[2529](#) **4.14.3.3 Handling of the read traffic**

The handling of the read traffic stays the same handling schemes as the other IOAIU variations to fulfil the basic [2532](#) transport functions of PCIe traffic. Read data chunking feature is recommended as described in section 4.14.6

4.14.4 Relevant PCIe information

[2535](#) **4.14.4.1 The rules for PCIe transactions (see PCIe specification, Section 2.4 Transaction Ordering)**

Table 4-49 defines the ordering requirements for PCIe Transactions. the columns represent a first issued transaction [2538](#) and the rows represent a subsequently issued transaction. The table entry indicates the ordering relationship between the two transactions. The table entries are defined as follows:

Yes The second transaction (row) must be allowed to pass the first (column) to avoid deadlock. (When blocking occurs, the second transaction is required to pass the first transaction. Fairness must be comprehended to prevent starvation.)

Y/N There are no requirements. The second transaction may optionally pass the first transaction or be blocked by it.

No The second transaction must not be allowed to pass the first transaction. This is required to support the producer/consumer strong ordering model.

TABLE 4-49: PCIE ORDERING RULES SUMMARY

Row Pass Column?		Posted Request (Col 2)	Non-Posted Request		Completion (Col 5)
			Read Request (Col 3)	NPR with Data (Col 4)	
Posted Request (Row A)		a) No b) Y/N	Yes	Yes Yes	a) Y/N b) Yes
Non-Posted Request	Read Request (Row B)	a) No b) Y/N	Y/N	Y/N	Y/N
	NPR with Data (Row C)	a) No b) Y/N	Y/N	Y/N	Y/N
Completion (Row D)		a) No b) Y/N	Yes	Yes	a) Y/N b) No

[2541](#)

Posted Request is a Memory Write Request or a Message Request.

Non-Posted Request (with Data)	Configuration Write Request, an I/O Write Request, or an AtomicOp Request.
Non-Posted Request	Read Request or an NPR with Data
Row A, B, C	<p>Special cases:</p> <p>a) applies to all transactions unless condition b) applies</p> <p>b) Requests are allowed to pass when</p> <ul style="list-style-type: none"> ▪ RO (relaxed ordering attribute) is set ▪ IDO (ID ordering) applies, and the Requester IDs are different ▪ Both requests have been issued using different PASID
Row D	<p>2a) Completion must not pass a Posted Request</p> <p>2b) Exception:</p> <ul style="list-style-type: none"> ▪ An I/O or Configuration Write Completion is permitted to pass a Posted Request ▪ Completions with IDO are permitted to pass a Posted Request if they belong to independent flows (C.ID <> R.ID) <p>5a) Completions with different Transaction IDs are permitted to pass each other</p> <p>5b) Completions with the same Transaction ID are not allowed to pass each other</p>

4.14.4.2 Relevant PCIe transaction types and the corresponding semantics information

PCIe supports multiple types of transactions. The relevant transaction types are listed in Table 4-50.

2544 Depending on the address space selected and the semantics of the transaction, an Ncore 3 would then propagate these to one of 3 types of functional interfaces:

- 2547
- coherent memory --> DCE
 - non-coherent memory --> DMI
 - non-coherent memory and device transactions --> DII

2550 TABLE 4-50: EXPECTED PCIE TRANSACTION TO AXI MAPPING

Item	Transaction Type	Mode	Target	ACE-Lite Transaction - AxCACHE[3:0]
1	Memory Read	Non-Posted	DCE ¹⁹	normal, cacheable, bufferable
2			DMI	normal ²⁰
3			DII	normal, non-cacheable ²¹
4	Memory Write	Posted	DCE	normal, cacheable, bufferable
5			DMI	normal, non-cacheable, bufferable
6			DII	normal, non-cacheable, bufferable/non-bufferable ²²
7	Memory Read Lock ²³	Non-Posted	DCE/DMI	normal, non-bufferable
8			DII	normal, non-cacheable, non-bufferable
9	IO-Read	Non-Posted	DII	device, non-bufferable
10	IO-Write	Non-Posted	DII	device, non-bufferable

¹⁹ All cacheable memory accesses are bufferable

²⁰ Technically any normal memory access is supported

²¹ Cacheable transactions are not expected

²² Both transaction types are legal - SNPS IP uses non-bufferable transactions

²³ AXI4 does no longer support locked transactions

Item	Transaction Type	Mode	Target	ACE-Lite Transaction - AxCACHE[3:0]
11	Configuration Read (Type 0/1)	Non-Posted	DII	device, non-bufferable
12	Configuration Write (Type 0/1)	Non-Posted	DII	device, non-bufferable
13	Message	Posted	DII	device, non-cacheable, non-bufferable
14	AtomicFetchAdd ²⁴	Non-Posted	DCE/DMI	normal, cacheable, non-bufferable
15	AtomicSwap ²⁴	Non-Posted	DCE/DMI	normal, cacheable, non-bufferable
16	AtomicCAS ²⁴	Non-Posted	DCE/DMI	normal, cacheable, non-bufferable

The following lists some of the PCIe relate semantics, which are carried over the sideband interfaces²⁵ from the 3rd party PCIe controller, could be useful to improve the PCIe performance if implemented. Please note that a different 3rd party PCIe controller might choose different set PCIe information to pass onto the application, thus one of more signals described in the following list might not always available.

- TYPE: Type of PCIe transaction as shown in Table 4-50, normally this information is represented by a 5-bit wide field
- IDO: This bit is to indicates whether ID-based Ordering is to be used for the current AXI transaction it is associated with.
- EP: If EP=1, the data accompanying this data should be considered invalid although the transaction is being allowed to complete normally
- RO: Relaxed ordering is allowed when set it to 1. Otherwise, PCIe strict ordering must be observed as shown in Table 4-49
- TC: Traffic Classes and normally is used to indicate different level of QoS. A PCI Express controller might support up to 8 TCs and represent them with different virtual channels. The higher the value, the more important traffic it will be.
- NS: No Snoop: when set to 1, requester is indicating that no host cache coherency issues exist for this transaction. The overall system can save time by skipping the normal processor cache snoop for this request. When 0, normal processor cache snoop is required.

4.14.5 Ordering Considerations

4.14.5.1 IOAIU ordering

²⁴ Our ACE-Lite implementation supports atomics but atomics must be cacheable and will not terminate properly if the addressed region is not backed up by SMC or if the region is not addressing scratch pad memory

²⁵ As described in details in section 5.3.1 of Synopsys Controller IP PCI Express DM controller Databook (version 6.20a, April 2024)

IOAIU follows the ordering rules defined in CCMP and complies the supported combinations as described in section 5.4.7.1. The relevant fields such as Policy, ReadID and WriteID are defined in GPRAR as shown in Table 5-14.

2580 4.14.5.2 PCAIU ordering

For a PCAIU configuration, the following rules apply:

- 2583 • In this mode, the OR bits are always set as 2'b01, which implies the Write Order mode defined in CCMP
- The GPRAR policy bits, along with either WriteID or ReadID bit is not expected to be programmed in this mode
- 2586 • Writes arriving at the PCAIU from the 3rd party follow AXI or ACE-Lite protocol. Write transactions are tagged with the AWID, all transactions that are part of the same flow crossing multiple memory targets shall be considered sequentially ordered within that flow.
- 2589 • The VZ bit must be 1'b1 to both DMI and DII to indicate system visibility is expected
 - Except VZ bit is 1'b0 for the atomic transactions
- A PCAIU observes a sequential stream of writes within a flow exactly in the same order they were received by complying the Ordered Write Observation and required by sequential memory consistency. AXI or ACE-Lite transactions arriving at the PCAIU carry AxCACHE[3:0] attributes
 - A PCAIU shall treat any transaction with AxCACHE[3:1] == 3b000 and targets a DII as device transaction and enforces Endpoint order
- 2595 • The Cache Maintenance Operations can be sent in any order, and the PCAIU can gain ownership of the cache lines in any order for the first phase of the working flow as shown in Figure 4-35.
- 2598 • OR bits are ignored by a DCE/DMI, which is the same handling as that of an IOAIU
- For every write to DMI, system wide visibility needs to be always observed
 - A write response is received from the SMC inside a DMI is also considered as system wide visible as long as an SMC is configured in a specific DMI, and write-allocate is enabled
- 2601 • If the transaction is non-coherent, the CMDReq must be sent to the DIs/DMIs in AXI ID order and wait for the STRReq before the next command is sent if it accesses the same target. Otherwise, it has to wait for DTWRsp before the next command is sent as shown in Figure 4-36.
- 2604

4.14.5.3 Response expected to for a PCAIU configuration

- 2607 • All responses within an AXI read or a write flow (same ARID or AWID), must be generated in the order the transactions arrive at a PCAIU. This property must be guaranteed, independent of their completion order at downstream agents.
- 2610 • Responses may be generated when the event message arrives and no older transaction with the same AxID is outstanding (issued and waiting to complete, or completed and waiting to generate a response)

2613 4.14.6 PCIe support forward looking architectural recommendations

2615 PCIe acceleration and customization is deemed to be an important feature to support data center and server markets. Currently PCIe Gen5 is already in a massive deployment stage, Gen6 standards were already introduced in 2021 and Gen7 standards are on the horizon to be approved soon. With that, the following shall be considered:

- 2619 • To directly interface and sustain a PCIe Gen5 with 16 lane traffic, a PCAIU needs to hit 2 GHz with 256 bit data interface. This should be the baseline for the first implementation.
 - On the same token, to directly interface and sustain a PCIe Gen6 with 16 lane traffic, the next challenging goal for a PCAIU configuration is to hit 2 GHz with 512-bit data interface. Thus, necessary architectural and timing closure considerations must be taken while the baseline implementation is carried out
- 2622 • The read data chunking function²⁶ is recommended to further improve the read data return efficiency with the following considerations:
 - The latency of read data return across different DMIs could vary a lot, a read with multiple cache lines worth represents a nature of out of order data return. Quickly passes the read data once a PCAIU receives the data from a DMI rather than holds it in the re-order buffer improves the overall latency for the read transactions.
 - It reduces the costs of using re-order buffers, PCIe supports long reads and the re-order buffer comes with significant costs
- 2625 • A 12-bit wide PCIe semantics interface, which comprehends all the sideband signals as described in section 4.14.4.2 should be considered to further improve the overall performance by taking advantage of the extra ordering and transaction type of information
 - Unique ID Indicator feature should also be considered to work with the extra PCIe semantics to further improve overall PCIe related performance

2631

2634 4.15 Special handlings of cache stashing

²⁶ The 3rd party PCIe AXI bridge has an option to support the read data chunking function of AXI5 by setting the CX_AXI_RCHUNK_ENABLE parameter to '1'.

2640 4.15.1 Stash target not identified²⁷

4.15.1.1 For WriteUniquePtlStash or WriteUniqueFullStash requests

In this situation:

- 2643 • If the cache line is not owned by any coherent agent, a DCE must only send SnpInvDtr as required, and must not send SnpUnqStsh to any coherent agent
- 2646 • For WriteUniqueFullStash and WriteUniquePtlStash requests, perform the writes to the main memory
- It is recommended allocating the cache line in the system cache if it is supported while performing the writes

2649 4.15.1.2 For StashOnceUnique or StashOnceShared requests

In such a situation:

- 2652 • If the cache line is not cached, where no coherent agent is registered either as an owner or a sharer for the cache line in the DCE, the DCE prefetches the cache line to the system cache
- 2655 • If the cache line is cached, where at least one coherent agent is registered as an owner or a sharer for the cache line in the DCE, the DCE can properly finishes the request
- This is because the cache line is already in the proximity of the coherence domain for future use

2658 4.15.2 Illegal Stash target

If the specified stash targets are **non-Stash-capable** agents as defined in CCMP or even not an initiator unit, they are defined as illegal stash targets. Under such a situation, a DCE must not signal an error to the requester. And such a wrongly specified Stash target can be attributed to a software-based error as what ARM CHI specification²⁸ defines.

In general, a DCE must disregard the stash hint and completes the transaction without stashing. The handling can be summarized as the following:

4.15.2.1 For WriteUniquePtlStash or WriteUniqueFullStash requests

Perform the writes to the main memory

- 2667 • It is recommended allocating the cache line in the system cache if it is supported while performing the writes

²⁷ The following conclusions are based on what it is defined and recommended in section 7.4.2 of ARM CHI specification version E.c – ARM IHI 0050E.c ID092622

²⁸ The following conclusions are based on what it is defined and recommended in section 9.4.6 of ARM CHI specification version E.c – ARM IHI 0050E.c ID092622

4.15.2.2 For *StashOnceUnique* or *StashOnceShared* requests

2670 The handling is IMPLEMENTATION DEFINED per discussion with ARM support²⁹. And an Ncore chooses to do the following:

- 2673
- If the cache line is not cached, where no coherent agent is registered either as an owner or a sharer for the cache line in the DCE, the DCE prefetches the cache line to the system cache
 - If the cache line is cached, where at least one coherent agent is registered as an owner or a sharer for the cache line in the DCE, the DCE can properly finishes the request

2676

²⁹ As described and discussed in ARM support case No. 03484148 raised by Hao Luan on September 10, 2024

5 Addressing and Memory Regions

2679

Ncore 3 address map is categorized into three main spaces:

- Ncore 3 Register Space (NRS)
- General Purpose Address Space (GPAS)
- Boot Region (BR)
- Each space may contain one or more address regions.

2682

NRS is the address space reserved for peripheral storage space, hosting Ncore unit configuration and status registers (CSR). The Organization of NRS is shown in Figure 5-1

2685

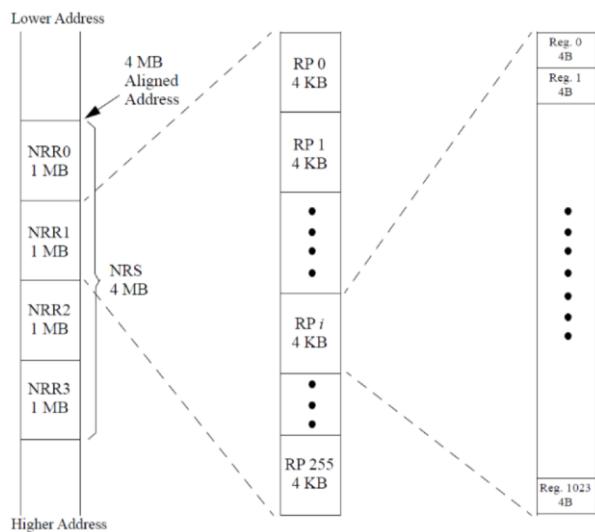


FIGURE 5-1: NRS STRUCTURE

2688

5.1 Ncore Register Space

NRS may contain one or more Ncore register regions (NRR). Each NRR is of 1MB and is further divided into 256 register pages (RP) of 4KB.

2691

Each Ncore 3 component is associated with an RP and may implement up to 1024, 4 Byte (32-bit) registers.

2694

Currently, Ncore 3 system supports only one NRR. The number of valid RPs within this NRR is equal to the total number of Ncore 3 components (Function Units, FU) configured in the system.

Table 5-1 shows the assignment of RPs to different Ncore 3 components. Note that within the table:

2697

- nCAIUs refers to the number of CAIUs in the system, and the number of other Ncore 3 components.
- nDII is always equal to total number of DIIIs configured, plus one. The additional DII is the Ncore 3 system DII that will be implicitly mapped into the NRS.
- There will always be only one DVE and one GRB.

2700

TABLE 5-1: RP ASSIGNMENT TO NCORE COMPONENTS

Item	Ncore Component	RPNs
1	CAIU (Coherent AIU)	RPN(0) to RPN(nCAIU - 1)
2	NCAIU (Non-Coherent AIU)	RPN(nCAIU) to RPN(nCAIU + nNCAIU - 1)
3	DCE (Distributed Coherence Engine)	RPN(nCAIU + nNCAIU) to RPN(nCAIU + nNCAIU + nDCE - 1)
4	DMI (Distributed Memory Interface)	RPN(nCAIU + nNCAIU + nDCE) to RPN(nCAIU + nNCAIU + nDCE + nDMI - 1)
5	DII (Distributed I/O Interface)	RPN(nCAIU + nNCAIU + nDCE + nDMI) to RPN(nCAIU + nNCAIU + nDCE + nDMI + nDII - 1)
6	DVE (Distributed Virtualization Engine)	RPN(nCAIU + nNCAIU + nDCE + nDMI + nDII)
7	GRB	0xFF (255)

2703

The base address of this region shall be specified at Ncore system build time and must be 4MB aligned. Figure 5-2 shows the address distribution.

2706

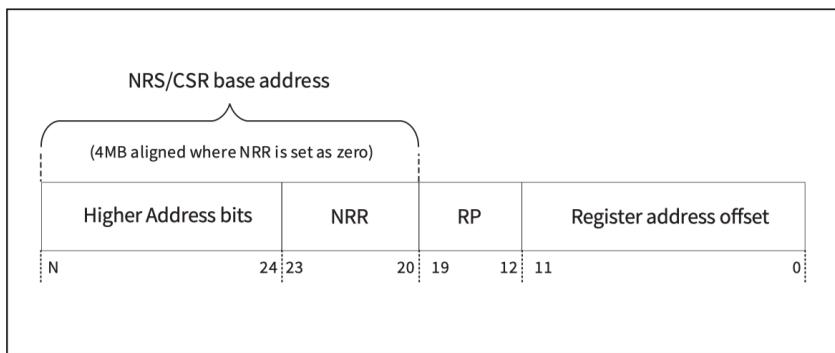


FIGURE 5-2: ADDRESS BIT MAPPING

2709

5.1.1 Global Register Block (GRB)

A block of Global Registers is implemented for each NRR within the NRS. In each NRR, this

2712

block is mapped to the Register Page with RPN of 0xFF. It includes the following CSR instances:

GRBUCSSFIDR0: GRBU Coherent Subsystem Snoop Filter Identification Register [Offset: 0xf00]

GRBUCSSFIDR1: GRBU Coherent Subsystem Snoop Filter Identification Register [Offset: 0xf04]

2715

GRBUCSSFIDR2: GRBU Coherent Subsystem Snoop Filter Identification Register [Offset: 0xf08]

GRBUCSSFIDR3: GRBU Coherent Subsystem Snoop Filter Identification Register [Offset: 0xf0c]

GRBUNRRIR: GRBU NRR Identification Register [Offset: 0xff0]

2718

GRBUENGIDR: GRBU Engineering ID Register [Offset: 0xff4]

GRBUNRRUCR: GRBU NRR Unit Census Register [Offset: 0xff8]

GRBUNSIDR: Ncore Subsystem Identification Register [Offset: 0ffc]

2721

5.1.1.1 Unit Self-Identification Register(SELFIDR)

Register Number

2724

Offset 0x000

Description

2727

There is no physical register implemented at this location. Instead, it is a reserved Read-only location with the following special behavior.

When an AIU receives a Read from its native interface to SELFIDR belonging to any NRR within the NRS, the AIU returns the contents of its own AIUIDR.

2730

A Read access to this location via any other pathway returns a zero value. Any Write to this register is ignored. SELFIDR can be read by an agent to identify the AIU it is connected to, to which RPN its own registers are mapped, and which NRR within the NRS its own Register Page lies.

2733

5.1.1.2 Coherent Subsystem Snoop Filter Identification Registers(CSSFIDR0-3)

Offset 0xF00-0xF0c

TABLE 5-2: COHERENT SUBSYSTEM SNOOP FILTER IDENTIFICATION REGISTER

Bits	Field Name	Access	Description
19:0	nSets	RO	Number of Snoop Filter Sets. This field indicates the number of sets in the snoop filter minus one in each DIRU. To determine the total number of sets in the snoop filter, this value must be multiplied by the number of DIRUs. For an unimplemented filter or a null filter, the value of this field is zero
25:20	nWays	RO	Number of Snoop Filter Ways. This field indicates the number of ways (i.e. the associativity) in the snoop filter minus one. For an unimplemented filter or a null filter, the value of this field is zero.
28:26	FilterType	RO	Snoop Filter Type. This field indicates the type of snoop filter. The type of the snoop filter is given as follows (all other values are RESERVED): 3'b000- Unimplemented filter, 3'b001-Null filter, 3'b010-Tag filter-presence vector, 3'b011-Tag filter-owner pointer/sharer vector,

Bits	Field Name	Access	Description
			3'b110-Tag filter with victim buffer presence vector, 3'b111-Tag filter with victim buffer owner pointer/sharer vector
31:29	Reserved	RO	

2736

5.1.1.3 NRR Identification Register (NRRIR)

Offset 0xFF0

2739

TABLE 5-3: NRR IDENTIFICATION REGISTER

Bits	Field Name	Access	Description
3:0	NRRI	RO	Ncore Register Region Identifier of this Global Registers block.
15:4	Reserved	RO	
19:16	NRRUsed	RO	Total number of NRRs used in this Ncore 3 instance is given by NRRUsed + 1. NRRs with indices 0 through NRRUsed are expected to be used in this instance.
31:20	Reserved	RO	

Description

2742

The NSUNRRIR reports the number of units in this Ncore subsystem. This register consists of the following bits and fields:

2745

- NRRI: Ncore Register Region Identifier to which this Global Register block belongs.
- NRRUsed: Number of NRRs being used in this Ncore 3 instance. NRRs are populated contiguously starting with 0, through NRRUsed. If NRRUsed = 0, it implies that a single NRR with NRRI = 0 is being employed in the Ncore 3 platform.

2748

5.1.1.4 Engineering ID Register (ENGIDR)

[Offset: 0xff4]

TABLE 5-4: ENGINEERING ID REGISTER

Bits	Field Name	Access	Description
31:0	RelV	RO	Engineering Version ID. Version Identifier for this Ncore 3 platform

2751

Description

2754

The Ncore Platform Version Identification Register identifies the version of the current Ncore 3 platform. Please see section 2.5 for more details.

2757

5.1.1.5 NRR Unit Census Register (NRRUCR)

[Offset 0xFF8]

2760

TABLE 5-5: NRR UNIT CENSUS REGISTER

Bits	Field Name	Access	Description
7:0	nAIUs	RO	Number of AIUs within this NRR.
13:8	nDCEs	RO	Number of DCEs within this NRR.
19:14	nDMIs	RO	Number of DMIs within this NRR.
25:20	nDIIs	RO	Number of DIIs within this NRR.
26:26	nDVEs	RO	Number of DVEs within this NRR.
31:27	Reserved	RO	Reserved (RAZ/WI)

Description

2763

The NRRUCR reports the number of units in this Ncore subsystem. This register consists of the following bits and fields:

2766

- Number of Coherent and Non-coherent Agent Interface Units – This field identifies the number of C-AIUs and NC-AIUs mapped within this NRR.
- Number of Directory Units – This field identifies the number of DCE units mapped within this NRR.
- Number of Distributed Memory Interface Units – This field identifies the number of DMI units mapped within this NRR.
- Number of Distributed I/O Interface Units – This field identifies the number of DII units mapped within this NRR.
- Number of Distributed Virtual Memory Engine Units – This field identifies the number of DVE units mapped within this NRR.

2772

2775

Software may use the fields of this register to determine which register page numbers are defined and which are reserved.

5.1.1.6 Ncore Subsystem Identification Register (NSIDR)

2778

[Offset 0xFFc]

The parameter implVerId is expanded from 12 bits to 16 bits to include a 4 digits large Ncore version number.

2781

Release version is provided as 16 bits in NSIDR register. The new description of NSIDR is hereunder:

TABLE 5-6: NRR SUBSYSTEM IDENTIFICATION REGISTER

Bits	Field Name	Access	Description
15:0	RelVer	RO	Release Version

Bits	Field Name	Access	Description
19:16	CachelineOffset	RO	Directory Cacheline Offset. This field indicates the width of the directory cache line offset. The number of bits in the directory cache line offset equals the value of this field + 5, e.g. for a 6-bit offset the value of this field equals 1. The size in bytes of the directory cache line is equal to two to the power of the offset.
27:20	nSnoopFilters	RO	Number of Snoop Filters. This field indicates the number of snoop filters in the coherent derived. The value of this field equals the number of snoop filters minus one.
31:28	Rsvd	RO	Reserved

2784

5.1.2 Ncore CSR access security

This section describes the new CSR access method, improved from a security perspective. This secure access method was required in NCore 3.4 because the existing security check based on NS (Non Secure) field was don't care for transactions targeting CSRs and boot region. Ncore 3.6 shall enforce security to configuration accesses. Each AIU shall be enabled or disabled to initiate CSR accesses by programming its NRS valid bit. Ncore 3.6 introduces NS bit check also for CSR access. A non-secure access to the CSR region will result in an error.

At least one AIU shall be enabled in the system. As a reminder, Ncore 3.6 includes a debug APB port which is also master of the configuration network. The NRS valid bit security check does not apply for accesses from the debug APB port.

As a safety requirement, Ncore 3.6 may limit to only one, the number of masters in the configuration network by disabling all AIUs, the APB debug port remains the unique master.

2799

5.1.2.1 Parameters

A new unit level parameter named fnCsrAccess that applies to all AIUs is introduced. It enables or disables CSR access via each AIU. At least one AIU is enabled in the system. Please refer to the parameters specification for more detail.

2802

5.1.2.2 Detailed Description

A new NRSAR register is added. This register has a valid field that is set based on fnCsrAccess parameter. If the parameter is true, then the valid field resets to 1. If the parameter is false, then the valid field resets to 0. Hardware should use this valid field to qualify a transaction hit to the CSR address space. When valid is not set this will likely result in a no BAR hit error.

2805

2808 NRSAR becomes a read-only register when the corresponding fnCsrAccess parameter is set. This is required to prevent the access from being removed. Nevertheless, an exception is made for write accesses coming from the debug APB interface.

2811 A write access coming from the debug APB port shall always be allowed to modify the NRS valid bit for all agents. This will allow the debug port granting permission to other agents to access CSR.

5.1.2.3 Ncore register space attribute register (xNRSAR)

Bits	Name	Access	Reset	Description
30:0	Reserved	RO	0x0	
31	NRS valid	R/W or RO*	fnCsrAccess	Set high to enable CSR access via this AIU (This field must be RO* (*except for writes from the debug APB port) for AIUs where the fnCsrAccess parameter is set and R/W where fnCsrAccess parameter is not set)

2814

5.2 General Purpose Address Space

2817

General purpose address space is for general purpose use. It can support multiple number of address regions. The number of regions needed within a system must be specified at build time, minimum one region is required. The regions can only be configured via CSR accesses and must be configured by software at boot up.

2823 They can be mapped to either normal memory (DMI) or a peripheral device (DII). The size of these regions must be a power of 2 within the range of 4 KB and 32 TB (achieved via interleaving). The base address configured must be aligned to the size of the region.

2826 Boot address space is to be used for system bootup. Current Ncore system supports only one boot address region. This region can be mapped to either normal memory (DMI) or a peripheral device address space (DII). The size of this region must be a power of 2 within the range of 4 KB and 8 TB. The base address of this region must be specified at Ncore system build time and must be aligned to the size of the region.

2832 Address decoding is priority based. NRS has the highest priority followed by general purpose address space and lastly boot address space. If an access matches higher priority address space, then overlapping lower priority address space matches are ignored, and the higher priority space is selected for access. Within an address space multiple address region matches are treated as errors; this specifically applies to general purpose address space. An access will result in an error if multiple address region matches are detected within a single address space or no matches are detected to any address space.

2835

5.3 Interleaving

2838

Ncore 3 supports interleaving across snoop filters and system caches. This capability enables higher access bandwidth and eases physical design of the chip. Snoop filters are implemented within DCE and can be interleaved/distributed across 1, 2, 4, 8 or 16 instances of DCE. System caches are implemented within DMI.

2841

DMIs can be interleaved/distributed as a Memory Interleave Group (MIG) of 1, 2, 4, 8 or 16 DMIs.

2844

Multiple memory interleave groups form a Memory Interleave Group Set (MIGS). For example, if a system has 7 DMIs, DMI0 to DMI6, they can be

categorized into 3 different memory interleave groups:

2847

- Group 0 of four DMIs (DMI0, DMI1, DMI2, DMI3);
- Group 1 of 2 DMIs (DMI4 and DMI5) and
- Group 2 of one DMI i.e. DMI6.

2850

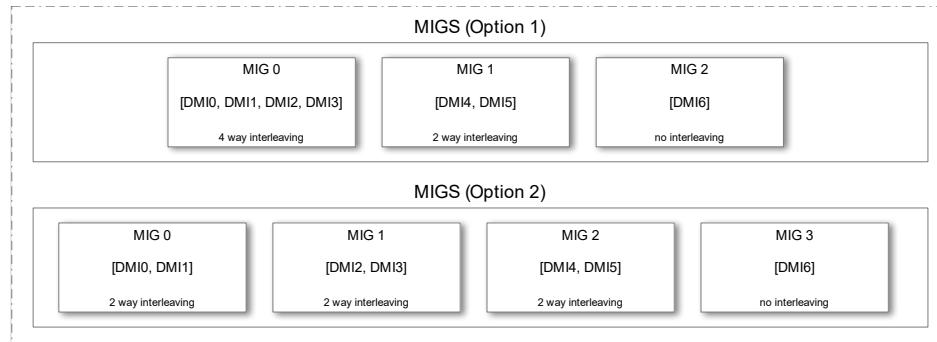
Three groups together are referred to as Memory Interleave Group Set. Alternatively, the MIGS may be configured as follows:

2853

- Group 0 of two DMIs (DMI0, DMI1);
- Group 1 of two DMIs (DMI2, DMI3);
- Group 2 of two DMIs (DMI4 and DMI5) and
- Group 3 of one DMI i.e. DMI6

2856

Examples for groups have been illustrated in Figure 5-3:



2859

FIGURE 5-3 MIGS OPTIONS (EXAMPLES)

5.3.1 Relevant CSR registers

2862

Nore currently supports 2 MIGS, the CSR registers for memory interleaving function and group selection are listed below:

TABLE 5-7 : ACTIVE MEMORY INTERLEAVE GROUP REGISTER (xAMIGR)

Bit	Name	Description	Access	Reset Value
0	Valid	Memory Interleave Group Set valid, when set the MIGS	Read/Write	0x0

Bit	Name	Description	Access	Reset Value
		specified in AMIGS field is being used for DMI interleaving else MIGS 0 is used by default		
4:1	AMIGS	Active Memory Interleave Group Set in use currently when Valid is set	Read/Write	0x0
31:5	Rsvd	Reserved	Read Only	0x0

2865

TABLE 5-8 : MEMORY INTERLEAVE FUNCTION SELECT REGISTER (xMIFSR)

Bit	Name	Description	Access	Reset Value
2:0	MIG2AIFId	Active function ID for 2-way interleaving. Selects the address bits to be used for interleaving of DMI within the selected MIGS	Read/Write	0x0
7:3	Rsvd	Reserved	Read only	0x0
10:8	MIG4AIFId	Active function ID for 4-way interleaving. Selects the address bits to be used for interleaving of DMI within the selected MIGS	Read/Write	0x0
15:11	Rsvd	Reserved	Read only	0x0
18:16	MIG8AIFId	Active function ID for 8-way interleaving. Selects the address bits to be used for interleaving of DMI within the selected MIGS	Read/Write	0x0
23:19	Rsvd	Reserved	Read only	0x0
26:24	MIG16AIFId	Active function ID for 16-way interleaving. Selects the address bits to be used for interleaving of DMI within the selected MIGS	Read/Write	0x0
31:27	Rsvd	Reserved	Read only	0x0

2868

5.4 Instance and Set Selection

2871

DCE & DMI component instances, system memory cache sets, proxy cache sets and snoop filter sets are selected as a function of address bits. The method for calculating the selection index is configurable, and the selection index is based on simple interleaving, in which the selection index is determined by the value of a set of N address bits, known as the primary selection bits. The value of selection index bit n equals the value of the address bit defined by primary selection bit n. For example, if primary selection bit 0 is specified as address bit 6, the value of selection index bit 0 equals the value of address bit 6.

2874

2877

Each address bit in the set of primary selection bits must be unique, i.e. an address bit must appear only once in the set of primary selection bits. The address bits must be chosen from a range whose upper bound is less than the size of the system address and whose lower bound is greater than or

2880 equal to the size of a cacheline. For example, if the size of the system address is 4 GB and the size of
 2881 the directory cacheline is 64 Bytes, the highest address bit that can be selected is 31 and the lowest
 2882 address bit is 6. Address bits less than the size of the directory cacheline comprise the directory
 2883 cacheline offset, which are bits 0 through 5 in this example.

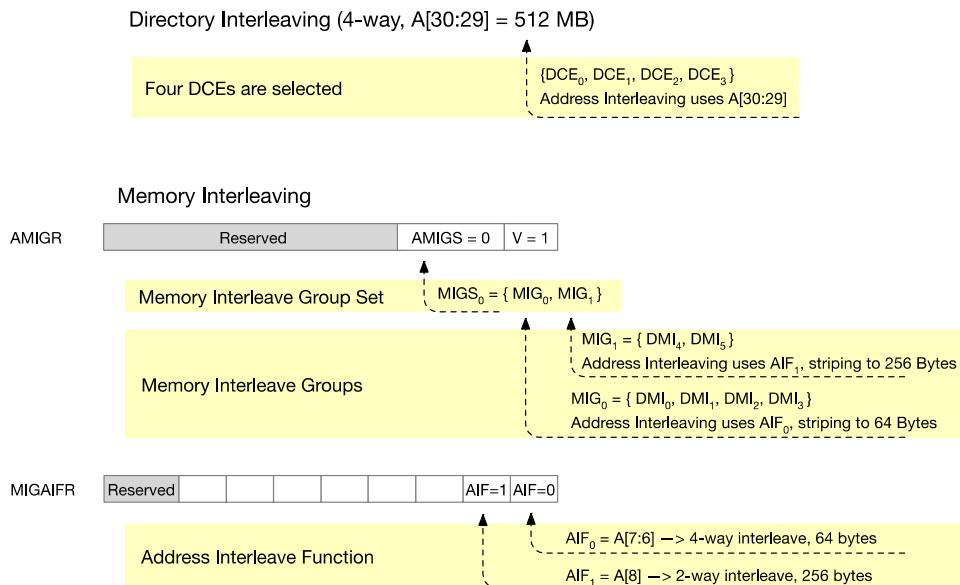


FIGURE 5-4: MEMORY AND DIRECTORY INTERLEAVING

2886 An identifier is computed by taking the value of the selection index modulo the number of items
 2887 being selected. To select an instance on a component, an instance identifier is calculated. To select a
 2888 set in a system memory cache, a proxy cache, or a snoop filter, a set identifier is calculated. In the
 2889 case of Snoop filter and system memory cache the final set index is computed by concatenating the
 2890 instance identifier with the set identifier, i.e. the instance identifier represents the most significant
 2891 bits of the set index, while the set identifier represents the least significant bits. The address bits in
 2892 the set of primary selection bits that determine the instance identifier must not appear in any of the
 2893 sets of primary selection bits that determine the set identifier.

2895 Additional constraints that apply to various components are described in more detail below.

5.4.1 Directory Interleaving

2898 The coherency protocol in Ncore is directory based, directories are located within the DCE. To improve
 2899 performance up to 16 directories may be interleaved.

- Interleaving is based on one (2-way interleaving), up to four address bits (16-way interleaving)

- 2901 • Directories are mapped into groups (DIG = Directory Interleave Group), where each group uses a fixed interleave factor of 2^N ($N = 0 \dots 4$), configured in **Maestro**
- 2904 • Multiple Groups may be combined to form a DIGS
- 2907 • DIGS (Directory Interleave Group Set), each set may only combine DIG in a way so that no DCE appears more than once in the merged list
- 2907 • Multiple DIGS may be defined in **Maestro**, one of these must be selected at system start by configuring the ADIGR in each AIU

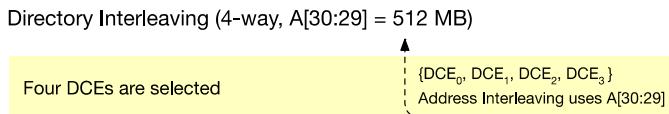


FIGURE 5-5: DIRECTORY INTERLEAVING

2910 5.4.2 Snoop Filter, System Memory Cache and Proxy Cache

The Set selection is additionally constrained as following:

- 2913 • The number of sets per port must be a power-of-two integer
- 2913 • The number of primary selection bits must equal the binary logarithm of the number of sets.

2916 5.4.3 Distributed Memory Interface Selection

Ncore may be configured to use up to 16 Distributed Memory Interfaces (DMI). For performance, to balance the load and to distribute traffic evenly, DMI may be interleaved. The interleaving options are configured in **Maestro** by defining up to 8 Address Interleaving Functions.

- 2922 • Interleaving is implemented by an Address Interleave Function (AIF)
- 2922 • An AIF is based on 0 (no interleaving) to 4 (16-way) address bits and must be defined in **Maestro** (hard-coded). Each predefined AIF is assigned a unique 3-bit AIF ID.
- 2925 • At least one AIF_m with a matching interleave factor N_m must exist for each defined MIG.
- 2925 • DMI are mapped into Memory Interleave Groups (MIG). Each MIG must enumerate N members, where N is the interleaving factor. MIG are defined in **Maestro**.
- 2928 • Ncore supports up to 8 MIG – an active AIF may be set for each MIG by setting the associated field in the MIGAIFR
- 2928 • Multiple MIG may be combined to form a Memory Interleave Group Set (MIGS), each set may only combine MIG in a way so that no DCE appears more than once in the merged list
- 2931 • Multiple MIGS may be defined in **Maestro**, one of them must be selected at system start by configuring the AMIGRs in each DCE and AIU

2934

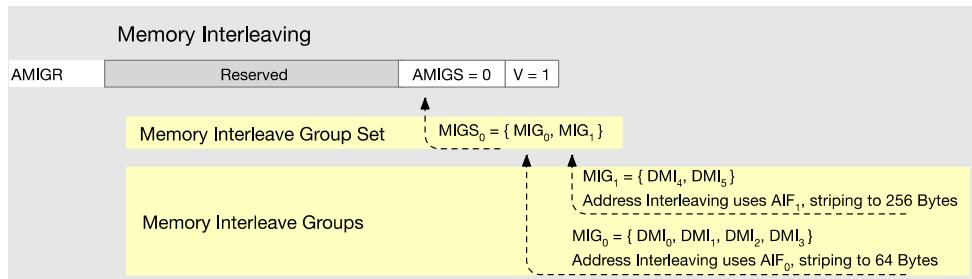


FIGURE 5-6: MEMORY INTERLEAVING GROUP REGISTER

2937

5.4.4 Distributed Coherency Engine Selection

DCE selection is additionally constrained as follows:

2940

2943

2946

2949

2952

2955

- The number of instances may be any integer in the range of 1, 2, 4, 8 and 16
- If the number of instances equals a power-of-two integer, the number of primary selection bits must equal the binary logarithm (\log_2) of the number of instances
- If the number of instances does not equal a power-of-two integer, the number of primary selection bits must equal an integer greater than the binary logarithm of the number of instances
- The primary selection bits must be chosen from the address bits common to all snoop filters and above the cacheline offset
- If the number of ports is not equal to a power-of-two integer, the distribution of snoop filter cacheline addresses is non-uniform. For example, if the DCE is configured with three instances, the minimum number of primary selection bits equals two. In this configuration, 50% of cacheline addresses maps to one instance, and 25% maps to each of the other two instances. The non-uniformity may be smoothed by increasing the number of primary selection bits. By specifying four primary selection bits, 37.5% of cacheline addresses map to one instance, and 31.25% of cacheline addresses map to each of the other two instances. By making the distribution of cacheline addresses more uniform, hot-spots are less likely to develop at an DCE instance.

2958

5.4.5 Address hashing SecSubRows

Ncore 3.6 supports extra configuration of address hashing to AIU (proxy cache)/DCE(Snoop Filter)/DMI(System cache) interleaving and set select function.

2961

In a set-way cache, multiple sequential streams that have the same mid-lower physical address bits will be indexed into the same sets, resulting in cache thrashing and the low utilization of capacity.

Example:

Assuming there is a 1MB, 8-way cache with 64B cacheline. 2048 sets altogether. A sequential stream

2964 (usually 4KB) is likely to exhaust all permutations of physical address [11:0], leaving only physical address [16 : 12] as variables. So, the chance that two streams collide is 1/32. They are likely mapped to the same 64 sets even though we have 2048 sets. When we have more streams, the chance of collision is even higher. And when more than 8 streams collide, our 8-way cache gets thrashed.

2967
2970 That is why, Ncore 3.6 offers the possibility to apply a hash function that involves the physical tag portion and cache index portion of the physical address. Now that the new index is more random, a sequential stream will scatter into different sets, resulting in less potential same index thrashing.

The parameter SecSubRows enables the feature:

Assumption of use:

- 2973 - These additional address bits are used to hash the ways selected by the primary bits.
- These may not include address bits that are chosen for the Primary bits themselves and offset bits
- The secondary bits are chosen on a per primary bit basis. The bits within the set for a primary bit are combined together and the primary bit with an Exclusive OR combination. A given address bit may belong to Secondary bit sets of multiple primary bits.
- 2976

This provides secondary masking capabilities which would result in a resultant interleaving/hash function as described below:

2979 Assume PriSubDiagAddrBits to be A[3:0] corresponding to some combination of Tag and/or Index bits.

Assume SecSubRows to be B[7:0] again corresponding to some combination of Tag and/or Index bits.

2982 The resultant Hash function output C[3:0] would be:

$$C[0] = A[0]^B[0]^B[1] \dots ^B[7]$$

$$C[1] = A[1]^B[0]^B[1] \dots ^B[7]$$

2985 $C[2] = A[2]^B[0]^B[1] \dots ^B[7]$

$$C[3] = A[3]^B[0]^B[1] \dots ^B[7]$$

2988 5.4.6 Address Space Compaction

Through N-way interleaving, each memory region will be spread to N DMI modules – each memory request will arrive at DMI_x with an address relative to the base of the region and needs to be relocated to remove gaps in the physical memory address space:

- 2991
- Each DMI provides a configurable memory remapping function to support address space compaction
 - The number of descriptors to describe compactable blocks is defined at configuration time in **Maestro**

- Each descriptor has 3 programmable registers
 - ATER - Address Translation Enable Register
 - RFAR - Relocation From Address Register
 - RTAR - Relocation Target Register

2997

3000

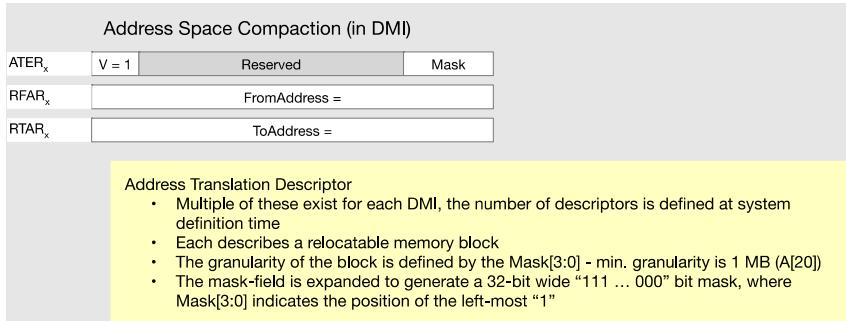


FIGURE 5-7: ADDRESS SPACE COMPACTION

3003

The incoming physical memory address will be masked off by a 32-bit mask and compared to the RFAR (relocation "from" address register) in all valid ATR (Address Translation Descriptor)

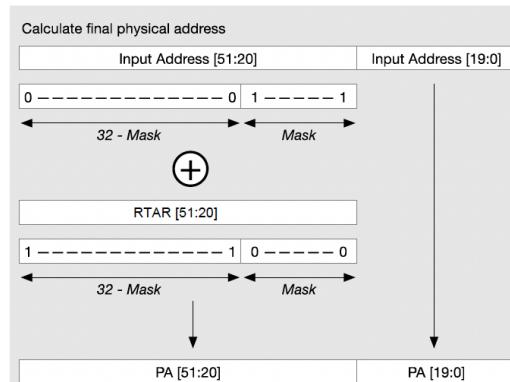
3006



FIGURE 5-8: MATCHING INPUT ADDRESS TO ATR DESCRIPTOR

3009

If a descriptor matches, the masked value of the RTAR (relocation target address register) will replace the previously masked MSBs in the original address



3012

FIGURE 5-9: RELOCATION TO NEW BASE ADDRESS

5.4.6.1 Relevant CSR registers

3015

The following CSR registers are employed for normal operations of address translation and relocation.

TABLE 5-9 : ADDRESS TRANSLATION ENABLE REGISTER (xATER)

Bit	Name	Description	Access	Reset Value
3:0	Mask	Treated as binary number from 0 to 15. Actual bit must covers (Mask + 20) bits of address, with a maximum of 35 bits. This enable a block of up to $2^{(Mask + 20)}$ bytes to be relocated.	Read/Write	0x0
30:4	Rsvd	Reserved	Read Only	0x0
31	Valid	0: Address translation triplet does not have a valid translation 1: Address translation triplet has a valid translation and translation is enabled	Read/Write	0x0

3018

TABLE 5-10 : REALLOCATE FROM ADDRESS REGISTER (xRFAR)

Bit	Name	Description	Access	Reset Value
31:0	FromAddr	Bits 51 down to 20 of incoming address.	Read/Write	0x0

3021

TABLE 5-11 : REALLOCATE TO ADDRESS REGISTER (xRTAR)

Bit	Name	Description	Access	Reset Value
31:0	ToAddr	Bits 51 down to 20 of outgoing address.	Read/Write	0x0

3024 5.4.7 Definition of a Memory Address Map

As previously described, General Purpose Address Space is partitioned into regions. Regions are defined by
 3027 region descriptors in GPRegister space.

GPRAR _x	V = 1	DMI	Size = 4 GB	MIG = 0	NS[1:0]	NC	Order[4:0]
GPRBLR _x	BaseAddress.L → A[43:12]						
GPRBHR _x	BaseAddress.H → A[51:44]						

3030

FIGURE 5-10: LAYOUT OF GP ADDRESS SPACE DESCRIPTOR

Agent interfaces for Ncore 3 implement address space decoding, transactions will be directed to a target for
 3033 completion based on the aperture within the global address space.

Each aperture is described by a set of 3 General Purpose Region Definition Registers, two registers are required
 3036 to define the base address of a region (GPRBLR = AddrLow, GPRBHRx = AddrHigh). The base address of any
 aperture is aligned to 4096 bytes.

TABLE 5-12: APERTURE BASE REGISTERS

Bit	Name	Description	Access	Reset
31:0	AddrLow	Low order bits 43:12 of a region's base address	R/W	0x00000000

3039

TABLE 5-13: APERTURE HIGH REGISTERS

Bit	Name	Description	Access	Reset
7:0	AddrHigh	High order bits 51:44 of a region's base address	R/W	0x00
31:8	Rsvd	Reserved	RO	0x000000

3042 The third register, GPRARx, defines the region attributes. The number of apertures is configurable by the user, a special (default) boot region exists and uses the same register format. A similar set of registers exists in DCE.

TABLE 5-14: APERTURE ATTRIBUTE REGISTER

Bit	Name	Description	Access	Reset
0	Rsvd	Reserved This bit had been defined as the Hazard flag in the PCIe document and was no longer required	RO	0x0

Bit	Name	Description	Access	Reset								
1	ReadID (ARID)	No ordering by AxID (free listing) for reads ³⁰ , please refer to section 5.4.7.1 on the supported combinations with the Policy below	RW	0x0								
2	WriteID (AWID)	No ordering by AxID (free listing) for writes ³¹ , please refer to section 5.4.7.1 on the supported combinations with the Policy below	RW	0x0								
4:3	Policy[1:0] ³¹	<p>Policy determines the setting of our internal OR[1:0] field which defines the behavior of the agent at the bottom of Ncore Response policy:</p> <table border="1" style="margin-left: 20px;"> <tr><td>11</td><td>Endpoint Order</td></tr> <tr><td>10</td><td>Relaxed Order</td></tr> <tr><td>00</td><td>Reserved</td></tr> <tr><td>01</td><td>Reserved</td></tr> </table> <p>11: Endpoint/Request Order: Refer to section 5.4.7.1 on the supported combination with ReadID/WriteID 10: Relaxed Order: Refer to section 5.4.7.1 on the supported combinations with ReadID/WriteID 00/01: Reserved and unpredictable behaviors</p>	11	Endpoint Order	10	Relaxed Order	00	Reserved	01	Reserved	RW	0x0
11	Endpoint Order											
10	Relaxed Order											
00	Reserved											
01	Reserved											
5	NC ³²	<p>Non-Coherent - this bit applies only for AXI transactions, ignore for CHI/ACE/ACE-Lite and use transaction property NC:</p> <ul style="list-style-type: none"> 0: Use coherent mode as indicated by incoming transaction 1: Enforce non-coherent transaction 	RW	0x0								
7:6	NSX[1:0]	This field describes the Security Level required to access this region. NSX[0] is mapped to NS(non-secure) NSX[1] is mapped to NSE (non-secure extension, reserved for later use)	RW	0x0								
8	Rsvd	Reserved	RO	0x0								
13:9	HUI	Home Unit Identifier used to access this memory regions - this field uses the index of the target HU within the enumerated set of DMI or DII	RW	0x0								
19:14	Rsvd	Reserved	RO	0x0								
24:20	Size	This field describes the size of the aperture in address space. The size of a region is calculated as: $\text{size_of(IG)} * 2^{(\text{Size} + 12)}$ with IG = Interleave group	RW									
28:25	Rsvd	Reserved	RO	0x0								
29	Rsvd	Reserved - this bit has been reserved to be used as an extension to HUT when hierarchical gateways or chip-to-chip interfaces will be implemented	RO	0x0								
30	HUT	This field describes the Home Unit Type <ul style="list-style-type: none"> 0: System Memory 1: I/O (Peripheral Memory/Devices) 	RW	0x0								
31	Valid	This bit indicates if an aperture descriptor is valid <ul style="list-style-type: none"> 0: Invalid Mapping - this descriptor is not describing a valid region 1: Valid region descriptor 	RW	0x0								

3045

³⁰ Setting ReadID and WriteID (freelisting) will force the internal OR[1:0] field to 2b00 (unordered) for memory targets

³¹ ReadID/WriteID/Policy: These fields are not applicable to CHI or ACE transactions and shall be reserved in CAIU

³² Each aperture shall be configurable to either use of coherent or non-coherent transactions Coherency does not apply to AIU target = DII and the value of the bit shall be ignored for this setting

ReadID/WriteID/Policy: These fields are not applicable to CHI or ACE transactions and shall be reserved in CAIU

NC - bit: Each aperture shall be configurable to either use of coherent or non-coherent transactions Coherency does not apply to AIU target = DII and the value of the bit shall be ignored for this setting

5.4.7.1 Supported combinations of among policy and Read/WriteID

3048 Starting from Ncore 3.7.1, the following supported combinations among policy, ReadID and WriteID are enforced to gradually align the same ordering definitions between CHI and AXI to streamline the definition, supports and implementations:

- 3051 • Policy = 2'b11, WriteID = 1'b0, ReadID = 1'b0 => Maps to OR = 2'b11
 - Enforce strict device ordering to a memory region
 - 3054 • Policy = 2'b10, WriteID = 1'b1, ReadID = 1'b1 => Maps to OR = 2'b00
 - Skip AxID checking, every transaction behaves as in a unique ID mode. Two writes to the same address with the same AwID may be re-ordered. Any write response is always forced to be a late response
 - 3057 • Policy = 2'b10, WriteID = 1'b0, ReadID = 1'b0 => Maps to OR = 2'b10
 - Strict ID ordering. Address hazard is checked in a DII when the corresponding StrReq is sent
 - Policy = 2'b00/01 => Unpredictable behavior(s) and NOT available for any customer usage
- 3060 OR = 2'b01, which is the Write Ordering mode defined in CCMP, is only available to be used internally to support PCIe ordering mode as described in section 4.14

3063

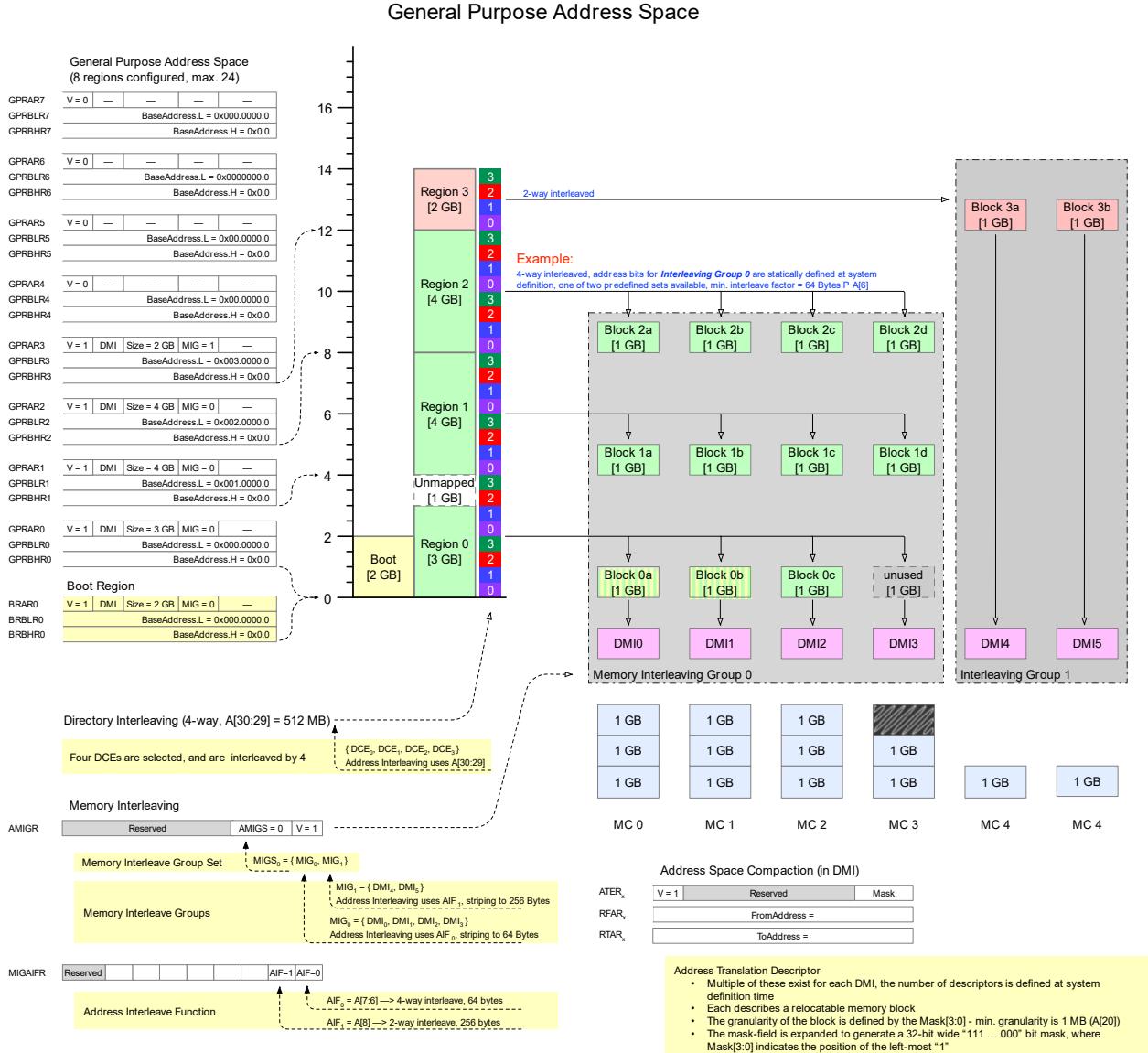


FIGURE 5-11: EXAMPLE ADDRESS MAP

3066

5.5 Boot Region Address Space

3069

Boot address space is to be used for system bootup. Current Ncore system supports only one boot address region. This region can be mapped to either normal memory (DMI) or a peripheral device address space (DII). The size of this region must be a power of 2 within the range of 4 KB and 8 TB. The base address of this region must be specified at Ncore system build time and must be aligned to the size of the region.

3072

Besides, each AIU has the following registers to remap BR address configuration:

TABLE 5-15 : BOOT REGION BASE ADDRESS LOW REGISTER (xBRBLR)

Bit	Name	Description	Access	Reset Value
31:0	AddrLo	Lower order bits 43:12 of the base address of the region	Read/Write	0x0

3075

TABLE 5-16 : BOOT REGION BASE HIGH ADDRESS REGISTER (xRBHBR)

Bit	Name	Description	Access	Reset Value
7:0	AddrHigh	Higher order bits 51:44 of the base address of the region	Read/Write	0x0
31:8	Rsvd	Reserved	Read Only	0x0

3078

TABLE 5-17 : BOOT REGION ATTRIBUTE REGISTER (xBRAR)

Bit	Name	Description	Access	Reset Value
8:0	Rsvd	Reserved	Read only	0x0
13:9	HUI	This bit indicates the Home unit identifier of the access	Read/Write	0x0
19:14	Rsvd	Reserved	Read only	0x0
25:20	Size	This field indicates a binary number from 0 to 31 from which the region's Size is calculated as (Size of IG) * 2 ^ (Size +12) bytes	Read/Write	0x2
29:26	Rsvd	Reserved	Read only	0x0
30	HUT	This bit indicates the Home Unit Type- 0: DMI, 1:DII	Read/Write	0x1
31	Valid	This bit indicates if the region is valid - 0: Invalid mapping, 1:Valid region mapping	Read/Write	0x1

3081

6 System messages

Ncore 3 uses the following request and response message pairs to implement data and coherency service:

3084

TABLE 6-1: OVERVIEW NCORE 3.0 MESSAGING

Message Class	Direction	Request	Response	Reference
CMD (coherent)	iAIU → DCE	CMDreq	CMDrsp	
CMD (non-coherent)	iAIU → DMI/DII	CMDreq	CMDrsp	
SNP	DCE → sAIU	SNPreq	SNPrsp	
MRD	DCE → DMI	MRDreq	MRDrsp	
Virtualization	iAIU → DVE DVE → sAIU	DVM Snoop	SNPrsp	
State Reply	DCE → iAIU	STRreq	STRrsp	
Directory Update	AIU → DCE	UPDreq	UPDrsp	
Request Buffer Request	DCE → DMI	RBRreq	RBRrsp	
Completion	DMI/DII → iAIU	--	CMPrsp	
Concerto Message Error	DMI/DII → iAIU	--	CMErsp	
Data Reply	DMI, DII, sAIU → iAIU	DTRreq	DTRrsp	
Data Write	iAIU → DMI/DII	DTWreq	DTWrsp	
System Message	iAIU → DVE iAIU → DCE/DVE DVE → sAIU/cAIU DCE → sAIU/cAIU	SysReq + OpCode	SysRsp + CMStatus	EventIn for broadcasting to other agents Coherence On/Off Request EventOut & Coherence Ack/Grant SysEvent, SysCo Broadcast & Coherence Ack/Grant

Note:

- *PCredits (option) – this response may carry back credits to an initiating agent to improve roundtrip latency for credits. If no credits are transported,*
- *Legend:*
iAIU – initiator AIU – AIU sending the first message in a transaction,
sAIU – snooper AIU – AIU being snooped by DCE or receiving a DVMOp from DVE

The purpose of system messages is to convey operating state information or state transitions for agents or asynchronous events within the endpoints of an Ncore domain. In the future they will be used to implement new functionality in the general class of system related activities.

3087

This service will be implemented by a new message class, **System**. System messages will be sent from a source agent to one or more destination agents.

3090

Every system message must receive a response to acknowledge receipt by the destination agent - depending on the protocol implemented by a specific message pair, receipt of response may initiate additional activity (for example a state transition at the source agent).

3093

6.1 SYReq and SYRsps Messages

3096

SysReq message is an implementation of the new system message class. The purpose of these messages is to propagate system related information between agents or functional units within the system.

3099 SysReq messages are asynchronous, do not use credit management as there shall be only one outstanding transaction per target, it shall be acknowledged by the receiver returning the SysRsp message. The SysRsp response implements status and error reporting in the CMStatus:

Command error :

- 3102** • Command was not properly formatted
- No support for this operation
- Wrong unit - this unit is not supporting the OpCode or unknown OpCode
- 3105** • Unit is busy and cannot perform the requested operation at this time
- Ok - no error occurred, command completed as expected

SysReq OpCode:

- 3108** • SysReq command uses CMType = 0x7B³³
- SysRsp response uses CMType = 0xFB³⁴

3111 TABLE 6-2: SYSREQ COMMAND LAYOUT

Name of Field	Width Param	Param Values	Description	Direction	Source
CMH:			CCMP Message Header		
TargetId	wTargetId	6 - 12	Target Identifier	In/Out	
InitiatorId	wInitiatorId	6 - 12	Initiator Identifier	In/Out	
CMType	wCMType	8	Type of Message - SysReq Opcode	In	
MessageId	wMessageId	6 - 12	MessageId	In/Out	
HProtection	wHProt	Derived	Protection for the Concerto Message Header fields	In/Out	
CMHE:			CCMP Message Header Extension		
TTier	wTTier	0 - 4	Traffic Tier of the message for use by the transport fabric	In/Out	
Steering	wSteering	0 - 4	Steering. This field is used to indicate steering of the message the transport fabric should apply to this message	In/Out	
Priority	wPriority	0 - 4	Priority of the message to be used by the transport fabric	In/Out	
QL	wQL	0 - 4	QoS Label. This field is used by the transport fabric for QoS functions such as bandwidth provisioning, isochronicity property, etc.	In/Out	

³³ This opcode is available - between 0x7A (STRreq) and 0x7C (RBRreq)

³⁴ One of the few free opcodes within the response block (0xF0 - 0xFF)

Name of Field	Width Param	Param Values	Description	Direction	Source
			to be applied for this message		
CMB:			CCMP Message Body		
RMessagelD	wRMessageID	6 - 12	MessageID for the command associated with this response	In/Out	
CMStatus	wCmStatus	8	Status - using standard command status layout	In/Out	
SysReqOp	wSysReqOp	4	As of now - only 16 different operations for this command class	In/Out	
NDProt	wSysReqProt	0 - 10	Protection bits for SysReq Message	In/Out	

3114

TABLE 6-3: SYSRSP RESPONSE LAYOUT

Name of Field	Width Param	Param Values	Description	Direction	Source
CMH:			CCMP Message Header		
TargetId	wTargetId	6 - 12	Target Identifier	In/Out	
InitiatorId	wInitiatorId	6 - 12	Initiator Identifier	In/Out	
CMTType	wCMTType	8	Type of Message - SysReq Opcode	In	
MessageId	wMessageId	6 - 12	MessageId	In/Out	
HProtection	wHProt	Derived	Protection for the Concerto Message Header fields	In/Out	
CMHE:			CCMP Message Header Extension	In/Out	
TTier	wTTier	0 - 4	Traffic Tier of the message for use by the transport fabric	In/Out	
Steering	wSteering	0 - 4	Steering. This field is used to indicate steering of the message the transport fabric should apply to this message	In/Out	
Priority	wPriority	0 - 4	Priority of the message to be used by the transport fabric	In/Out	
QL	wQL	0 - 4	QoS Label. This field is used by the transport fabric for QoS functions such as bandwidth provisioning, isochronicity property, etc. to be applied for this message	In/Out	
CMB:			CCMP Message Body		
RMessagelD	wRMessageID	6 - 12	MessageID for the command associated with this response	In/Out	
CMStatus	wCmStatus	8	Status - using standard command status layout	In	
NDProt	wSysRspProt	0 - 10	Protection bits for SysRsp Message	In/Out	

6.1.1 SysReq Commands

3117

Being not credited imposes restrictions on the use of SysReq messages. It requires that a functional unit must always be able to process a single SysReq command and generate a meaningful response using SysRsp. In the first implementation in these message operations will be supported:

3120

TABLE 6-4: SYSREQ COMMAND OPERATION PAYLOAD

Command	OpCode	Payload	Function
SysReq.NOP	0x00	TimeStamp	No function, beyond carrying the timestamp in both directions. This transaction may be used to measure the roundtrip latency between two agents. If an agent does not implement a timestamp counter, the value used in the response shall be -1 (all ones)
SysReq.Attach	0x01	TimeStamp SysCoReq	Attach the requester to the coherency domain. This command is used by a cache coherent initiator (CAIU) to attach itself to the coherency engine (DCE). The command needs to be sent to all interleaved DCE. The OK response signals successful attachment, only after that the agent will be allowed to send coherent requests and participate in snoop protocol
SysReqDetach	0x02	TimeStamp SysCoReq	Detach the requester from the coherency domain. This command removes the agent from the set of snooped coherent agents managed by DCE
SysReqEvent	0x03	TimeStamp EventReq	System Event - these events are generated within various agents ³⁵ in the system and convey asynchronous events between event producers and event-consumers. These agents are CPUs, monitors for exclusive transactions, SMMU, Accelerators or other agents. Agents may be producer, consumers or both.

6.1.2 Command CMStatus

3123

The CMStatus[7:0] field is shown only as input in the direction column, implying that the field is not transmitted along with the rest of the *SysReq* message at the initiator, but is an input-only field at the target of the message.

3126

The CMStatus field is used to report the result of a processing step of the operation, including detection of errors, to an Ncore unit. However, *SysReq* being the start of the operation, there are no results to report.

3129

If any type of error is detected in the native request transaction, the initiator AIU must not issue a corresponding *SysReq* message into the Ncore 3 system to commence the processing of the native operation. The operation must be locally terminated and error reported back to the native agent.

3132

A *SysReq* message may encounter a transport error along its path to the target. This error must be reported to the target via the CMStatus field constructed at the transport interface of the target Ncore 3 unit.

3135

TABLE 6-5: SYSCMD AND SYSRSP COMMAND STATUS FIELD ENCODING

Status Type	CMStatus [7:6]	CMStatus [5:0]
Success (No error)	2b00	SysRsp: System Response carries back the status of the command execution at the target agent

³⁵ In Ncore 3 only DCE/DM/DII (exclusive monitors) and AIU (EventInReq) will issue Event messages

Status Type	CMStatus [7:6]	CMStatus [5:0]		
		[5:3] = 3b000	[2:0]: xx0: No Operation performed - this may not be an error! 001: Completion - Execution state machine is still running 011: Final - Execution state machine went to IDLE after sending this response 101/111: reserved (TBD)	
		SysReq: {Reserved} - there should be no error on the incoming command, except transport problems		
Error	2b01	SysRsp: System Response carries back the status of the command execution at the target agent		
		[5:3] = 3b000	[2:0]: xx0: No Operation performed - unit signals error 001: Completion - with unknown error (conditions TBD) 011 - 110: Format Error - reserved 111: Unit is busy and cannot perform operation at this time	

Transport related error status uses the same representation as CmdRsp.

3138

6.2 SysCoReq Implementation

The SysCo protocol is a 4-state handshake protocol implemented by ARM processor DSU. The purpose of the protocol is to attach and detach the agent to the coherent domain.

3141

See ARM document *dsu_trm_100453_0401_03_en.pdf*, section A4.9 Cluster power down for a detailed description of the Initiator Agent handshake protocol.

3144

- On power up
 - Adds a request agent (DSU-CAIU) to the coherency domain
 - After de-asserting RESET:
 - SYSCOACK is inactive
 - Agent will respond to snoop and DVM requests but will not yet make cacheable requests
 - Agent will try to CONNECT by asserting SYSCOREQ signal
 - Interconnect is ready to receive cacheable requests
 - Interconnect shall assert SYSCOACK
- On power down
 - Remove a request agent (DSU-CAIU) from the coherency domain
 - At this time SYSCOREQ and SYSCOACK are asserted
 - Flushing caches and quiescing traffic:
 - Agent halting execution (WFI/WFE/HALT)
 - Agent de-asserts SYSCOREQ
 - Agent shall continue to respond to snoop and DVM requests but may no longer make cacheable requests
 - The interconnect has no longer active transactions for this agent and the system directory's snoop filters have not any cache lines recorded
 - De-assert SYSCOACK
 - Shut down the agent (assert RESET, power-down)

3147

3150

3153

3156

3159

3162

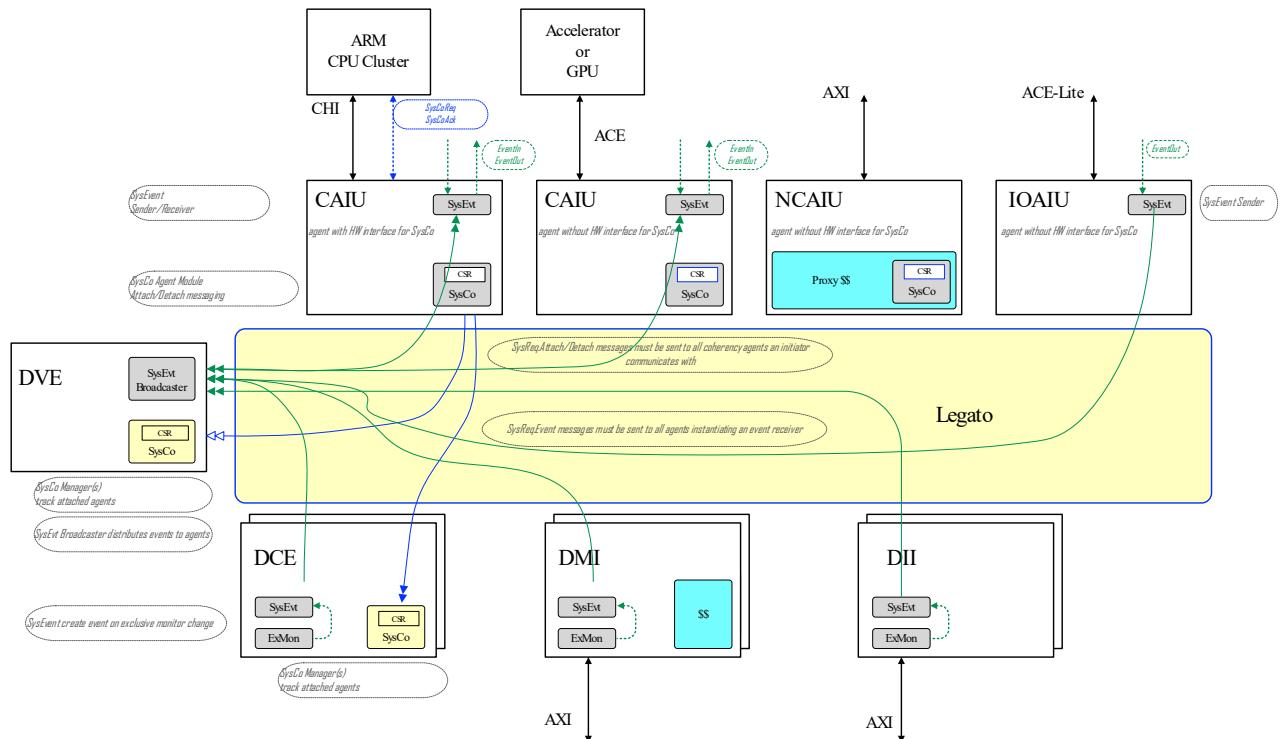
3165

6.2.1 System Architecture

In support of SysCo (Attach/Detach) each coherent agent (CAIU/ProxyCache³⁶) shall implement a SysCo-engine.

3168

In support of SysEvent each agent with event sources or receivers shall implement a SysEvent-engine.



3171

FIGURE 6-1: SysCo TOP LEVEL ARCHITECTURE³⁷

3174

After reset, an agent will not be part of a coherency domain, it may only send non-coherent transactions and will not respond to snoop requests.

Ncore will use SysReq messaging to notify all coherency managers (DCE) when an agent requires to be attached or detached from the coherency protocol.

³⁶ Any agent participating in the coherency protocol that does not support SysCoReq/Ack needs to implement a SysCo-engine using CSR protocol to attach/detach to the coherency domain

³⁷ This high level architecture shows optional exclusive monitors and SysEvent-engines in DMI/DII, these are part of Ncore3.6

3177 6.2.2 Attach/Detach Protocol

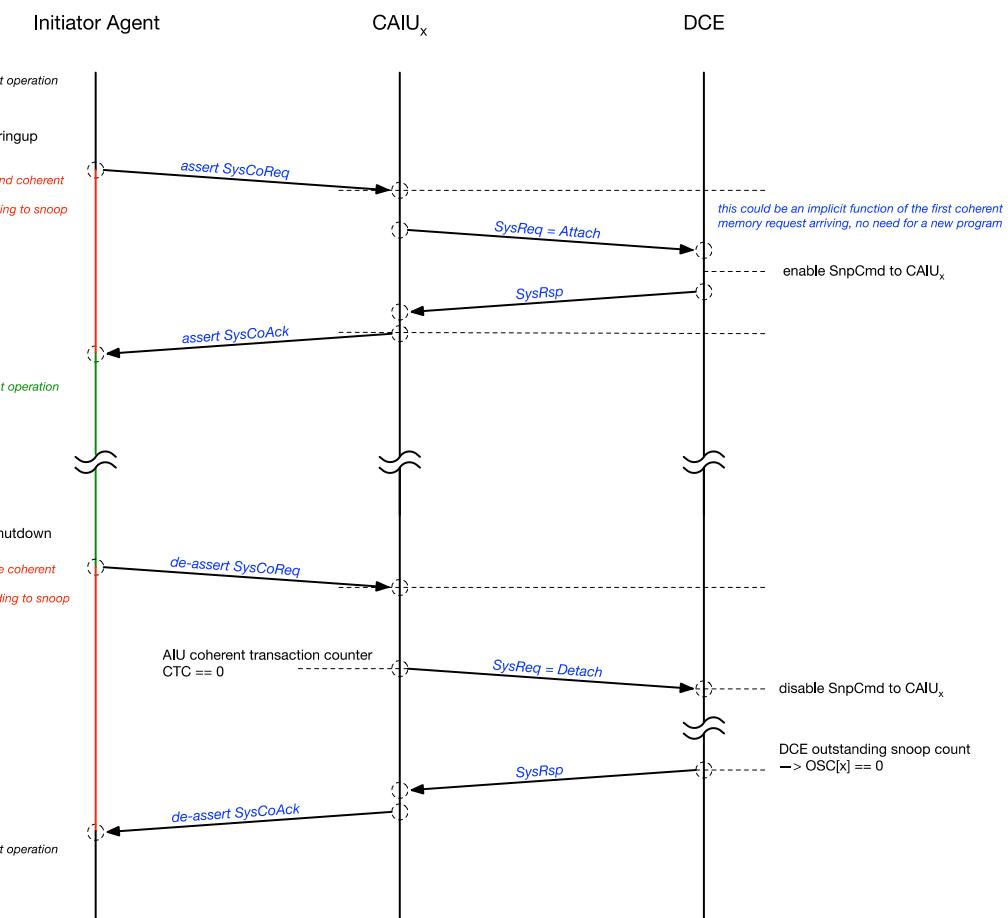
The initial state of any CAIU is detached - any CAIU that connects to a coherency agent with SYSREQ/SYSCOACK (SysCo) support must implement the SysCoReq interface and the SysCo message protocol engine.

3180

Any other coherent initiator agent (CAIU connecting agents that do not support SysCo, NCAIU with ProxyCache) must implement the SysCo message protocol engine. The engine must provide a CSR interface to initiate the coherency attach/detach process by SW (write to register).

3183

A coherency agent must not send any coherency transactions (Snoop/DVMSnoop) to a functional unit, unless that unit has been attached to this coherency agent by using the SysCo protocol.



3186

FIGURE 6-2: SysCo FLOW

Figure 6-2 shows the details of the SysCo protocol and the associated exchange of messages. For clarity, only messaging with a single DCE is shown in the flow chart - in a real system a CAIU needs to attach to all DCE and DVE covering the coherency domain by sending messages to each one. The CAIU may start using coherent transactions only after all SysRsp have been received.

3189

³¹⁹² While in *detached* state, CAIU must not send coherent transactions, it is permitted (but not required) to respond to snoop requests.

³¹⁹⁵ CAIU must keep track of outstanding requests and keep a running count of outstanding coherent transactions. When a transition from attached to *detached* state has been requested, either by HW SysCo protocol or by a CSR write request, it must stop making coherent transaction into the system (ARM DSU will no longer make coherent request after SysCoReq has been deasserted) and wait until all outstanding coherent transactions have been retired, before making a SysReq.Detach to DCEs.³⁸

³¹⁹⁸ A coherency agent (DCE/DVE) shall no longer snoop an agent after receiving SysReq.Detach from it³⁹

³²⁰¹ A coherency agent must keep track of outstanding requests and keep a running count of outstanding coherent transactions to an agent, SysReq.Detach shall only be acknowledged by a coherency agent after all outstanding coherent transactions for a snooped agent have been completed.⁴⁰

³²⁰⁴ 6.2.3 SysCo Engine at Initiator Agent

The SysCo engine manages the attach/detach process for each coherent initiator agent.

³²⁰⁷ For agent interfaces with HW protocol support 2 signals (SysCoReq = please attach me, SysCoAck = you are part of the coherency domain) will be provided. These signals may be asynchronous to the internal clock domain and shall be properly synchronized using proper CDC implementation.

³²¹⁰ For agent interfaces without HW protocol support, the CSR interface may be used to request attachment or detachment from the coherency system.

Internally, each SysCo Engine shall implement (also see Figure 6-3):

- CSR with 4 bits
 - C: Connecting, read-only
 - On read returns '1' when the agent is waiting to connect (FSM.state == **Connect**)
 - Req: Activate, read-write
 - Write to '1' to trigger FSM.state transition from **Idle** to **Connect**
 - Write to '0' to trigger FSM.state transition from **Connect** to **Detach**
 - Cleared by reset
 - A: Attached, read-only
 - On read returns the current state of the interface (0 - detached, 1 - attached)
 - Err: Error, read, WZ (write-to-zero)

³⁸ This requirement guarantees termination of concurrent traffic at the source and, assuming that software initiated a proper shutdown of local caches, also maintains consistent memory state

³⁹ This guarantees termination of snoop traffic initiated by other agents

⁴⁰ Only after all coherent traffic has completed, the agent may be transitioning to detached state and acknowledge the transaction to the DSU

3225

- read as '1' when a protocol error or time-out has been signaled
- read as '0' after reset - or after no protocol error has been detected in a transaction
- write to zero - clears the bit

3228

- SysCoFSM with 6 states:
 - **Idle** – after reset and when disconnected - *SysCoAck* shall be de-asserted in this state
 - On *SysCoReq* assertion or *CSR.Req* set, transition to **Connect**

3231

- **Connect** – request to connect by sending a *SysReq.Attach* message to all coherency agents this agent communicates with and wait for acknowledgement by protocol, a time-out counter shall be implemented to report error on no response.

3234

- **Attach-Error** - transient state, sets *CSR.Err* and transitions to **Detach**, reach a safe state

3237

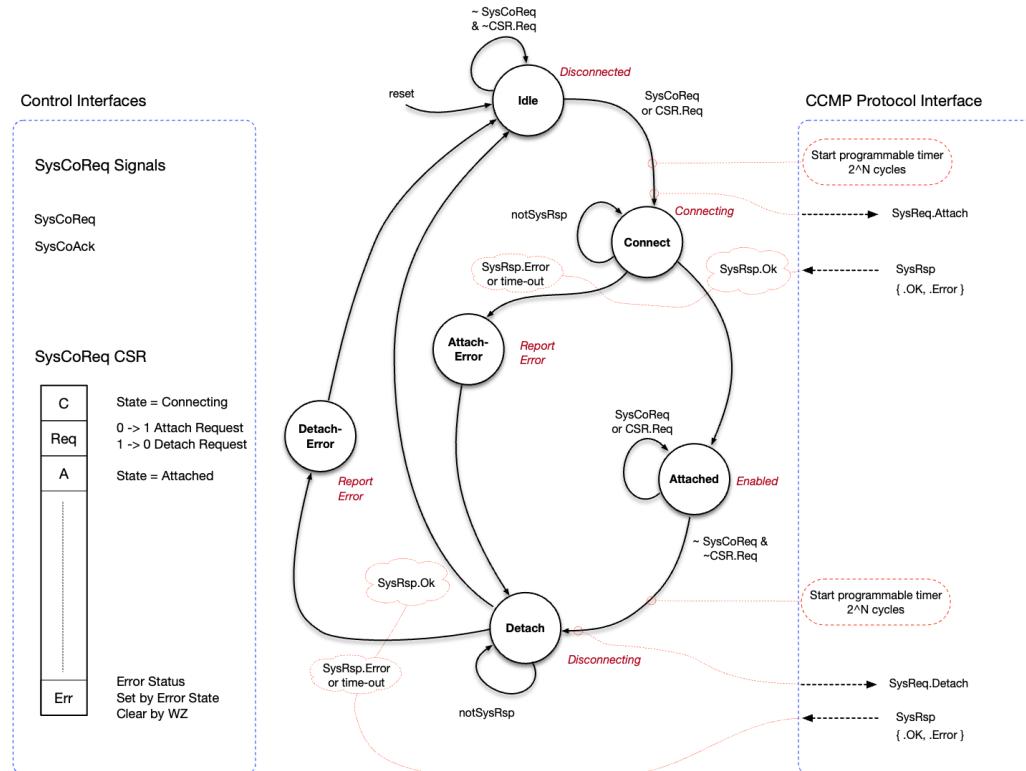
- **Attached**– connected, normal operating state - *SysCoAck* shall be asserted in this state
 - On *SysCoReq* de-assertion or *CSR.Req* cleared, transition to **Detach**

3240

- **Detach** – requesting to disconnect by sending a *SysReq.Detach* message to all coherency agents this agent communicates with and wait for acknowledgement by protocol, a time-out counter shall be implemented to report error on no response.

3243

- **Detach-Error** - transient state, sets *CSR.Err* and transitions to **Idle**, reach a safe state



3246

FIGURE 6-3: SYSCO STATE MACHINE

6.2.4 SysCo Engine at Coherency Agent

The SysCo engine manages the attach/detach process for each coherency agent. Coherency agents are functional units which issue Data Snoop or DVM Snoop requests. These agents need to know if message target is active and will respond to a request. Snooping an inactive agent would break the protocol and, even though it could be detected by using the currently implemented time-out mechanism, the performance impact of an unreliable transaction is not acceptable to customers.

The coherency agent's SysCo engine manages the participation of initiator agents in the snoop protocol by preventing snoops being sent to detached agents.

Agents that want to participate in the coherency protocol must register by sending a SysReq.Attach command to any coherency agent (DCE/DVM) they expect to be communicating with.

Agents that transition to sleep or any other inactive state and can no longer participate in the coherency protocol by responding to snoops, must detach from the coherency domain by sending a SysReq.Detach command to all coherency agents within said domain.

The coherency agent will track all outstanding transactions to agents and will respond by acknowledging the detach request as soon as no more active transactions exist for that agent (all outstanding snoop responses have been received).

Internally, each coherency agent's SysCo engine shall implement:

- At least one CSR with (at least) one bit $T[i]$ to tracked each agent's state, where i is the unique ordinal index of the initiator agent in the ordered set of initiators as assigned by Maestro
 - $T[i] == 0$ indicates agent_i is not actively participating in the coherency protocol and no transaction with that agent is allowed.
 - $T[i] == 1$ indicates the agent_i is active and participating in the coherency protocol, snoop or DVM transactions may be issued.
 - For DCE:
 - The coherency protocol allows cache lines to be silently evicted from any agent's cache. As a consequence, the tracking snoop filters implemented in DCE may not correctly reflect the agent's cache state and falsely indicate presence of a line.
 - It is required that agents that are no longer meant to participate in the coherency protocol go through a well defined sequence of steps:
 - i. Clean and invalidate the contents of the device's cache
 - ii. Initiate transition out of the coherency domain, by following the HW handshake provided for Arm DSU or by SW procol initiating the transition using the provided CSR interface
 - iii. Entering sleep or power down state
 - After steps (i) and (ii), it can be safely assumed that the agent does no longer hold valid data and any presence in the snoop filter is a result of silent evictions.
 - If a presence is indicated by a snoop filter and the agent is in detached state ($T[i] == 0$), no snoop to that agent shall be sent, the snoop filter entry for that

- 3288 agent shall be updated to remove the cache line and a spurious snoop filter event shall be generated to the performance counters

3291 o The set of CSR holding the T[i] bits shall provide read-only access to retrieve the current state (attached or detached)

3291 o An engineering register within CSR space shall be provided - writes to this register shall modify the vector T[i]

3294 o For DVE:
 - No DVMSnoop shall be sent to a detached agent

3297 • SysCoMgr to receive SysReq messages from initiator agents:

3297 o On receipt of SysReq.Attach:
 - Map the SourceID of the arriving SysReq to the associated T[i] and set the bit
 - Issue a SysRsp.Ok if the CMStatus of SysReq is OK
 - Issue a SysRSP.Error if
 - i. CMStatus or SysReq indicates an error
 - ii. target does not exist within the T-vector
 - iii. target is already set - we should not see duplicate attempts to set/clear a bit, this would be considered a protocol violation!

3300 o On receipt of SysReq.Detach:
 - Map the SourceID of the arriving SysReq to the associated T[i] and clear the bit
 - Issue a SysRsp.Ok if the CMStatus of SysReq is OK
 - Issue a SysRSP.Error if
 - i. CMStatus or SysReq indicates an error
 - ii. Target does not exist within the T-vector
 - iii. Target is already clear - we should not see duplicate attempts to set/clear a bit, this would be considered a protocol violation!

3309

3312

3315 SysReq messages are not credited - special care must be taken to avoid loss of messages and guarantee proper accounting through SysRsp. Initiating agents shall generate no more than one outstanding message per each coherency agent at a time. This limits the total number of transactions arriving at a coherency agent.

3318 It is an implementation choice to use a queue on the receiver side and execute SysReq only when it has the resources to respond with SysRsp.

6.3 Event Propagation

Events are asynchronous messages and will be used by agents to notify other agents in a system that an action shall be taken. Other than interrupts, events do not change the flow of program execution. Agents may be waiting on events, entering a lower-power state while doing so.

In the ARM ecosystem events may be used to quickly synchronize execution between agents by explicitly waiting for (WFE instruction) and sending events (SEV instruction). Other sources of events may be defined, for example, exclusive monitors changing state or SMMU service requests completed.

Events generated at a source within an agent will enter Ncore through the *EventOutputInterface* and will be forwarded to DVE for distribution. DVE will broadcast event messages to all agents that are event enabled⁴¹ with an Event Receiver. The Event Receiver's *EventInputInterface* will deliver events to the connected target (e.g. a processor cluster (DSU) or accelerator).

Event interfaces use a 4-phase handshake protocol implemented with 2 signals: EventReq, EventAck.

By nature, Events are not cumulative, multiple events arriving at an agent interface would only generate a single event handshake on the interface. Event messages arriving while a handshake is actively taking place would be aggregated and would not initiate another handshake after the previous has completed.

It is worth noting that since DVE centralizes events propagation, it is then the only source of events for receivers and the only target for senders. In Ncore 3.6, DVE serializes the handling of Events received from different sources. It will start a new broadcast after the completion of the previous one. Simultaneous Events from different sources will then generate successive Events at the receivers generated by DVE. The processing of an event at the target may be longer than the delay between two successive events at the Receiver, in that case the

⁴¹ An agent, which can be either CAIU or IOAIU, is considered as enabled if it has been configured by Maestro to have *EventInputInterface* or *EventOutputInterface* or both. Please note that an agent to be an event sender or receiver or both is NOT registered with the usage of SysCO req/ack process as that of the attachment flow as described in section 6.2

3342 two events shall be aggregated.

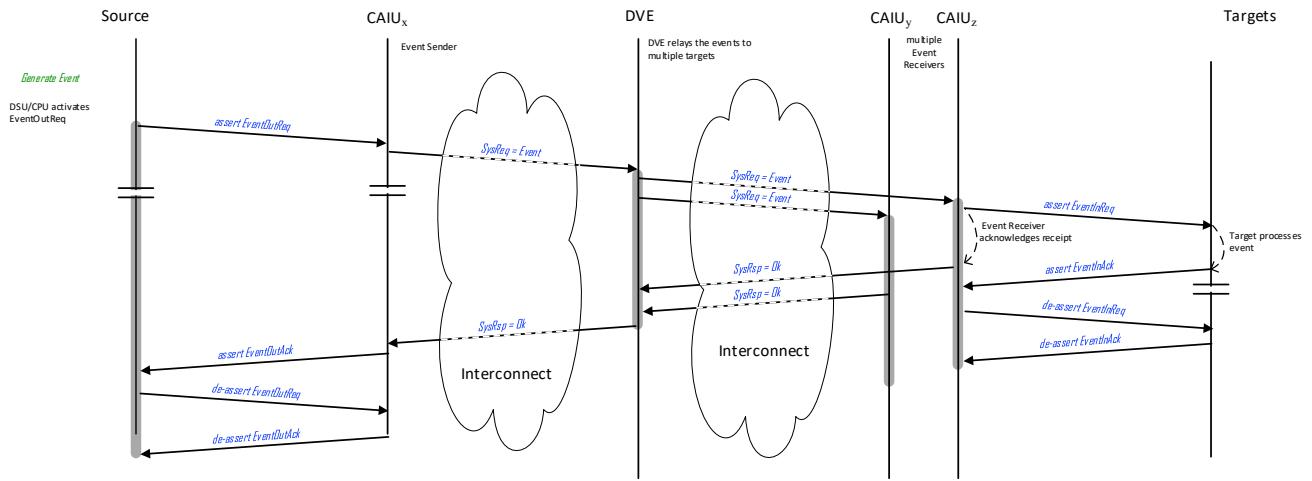


FIGURE 6-4: EVENT MESSAGING

3345 Requirements:

- Each AIU shall support an optional bi-directional event interface
- The event interface may receive events from the attached agent following the REQ/ACK-protocol
- The event interface shall forward events, generated internally or received from another agent, to the attached agent
- A received/generated event will be sent to DVE
- Events will be transported within Ncore using SysMsg transactions
- Event messages will be broadcast to the list of active AIU with receiver by DVE
- Events may originate within Ncore (when an exclusive monitor is cleared) - these events will be sent by the agent hosting the exclusive monitor

3357 6.3.1 Event Messaging Architecture

Please refer to Figure 6-1 for the system overview.

The event architecture knows different agents:

3360 **Source** = any system function that generates events, either as a consequence of state changes or by program execution (e.g. instructions SEV (send event))

- Processors executing SEV
- Page table activity, misses/errors/service requests in SMMU
- Accelerators, finishing tasks or computations
- Global exclusive monitors (DCE/DMI/DII) changing state

3366

3369

TABLE 6-6: EVENT MESSAGING INTERFACES - SOURCES AND DESTINATIONS

Component	Type	Signal	Present	Function
C-AIU CHI	Source Sender Receiver	EventInReq, EventInAck EventOutReq, EventOutAck	Yes/opt Yes/opt	CPU cluster sending events to system CPU cluster receiving events from NoC
C-AIU ACE	Source Sender Receiver	EventInReq, EventInAck EventOutReq, EventOutAck	Yes/opt Yes/opt	CPU/accelerator cluster sending events to system CPU cluster receiving events from NoC
NCAIU ACE5_Lite + DVM	Source Sender	EventInReq, EventInAck	yes/opt	peripheral I/F - with sMMU sMMU sending out event of page table activities
NCAIU AXI + ProxyCache	Receiver	--	no	AXI with Proxy Cache receives Event message from Exclusive Monitor event and does nothing about it. AXI with Proxy Cache issues SysReq.Attach/Detach to DCE for System Coherency.
NCAIU ACE_Lite	--	--	no	
NCAIU AXI	--	--	no	
DCE	Sender	--	yes	Exclusive monitor
DMI	Sender	--	yes	Exclusive monitor
DII	Sender	--	yes	Exclusive monitor
Note:				
1. Optional - allow configurability within Maestro to populate individual peripheral interfaces. NCAIU with ACE5-Lite + DVM, connecting to an SMMU shall implement the interface because SMMU is capable of emitting events				

3372

Sender - Block within an agent interface that implements event inputs (EventInReq, EventInAck). A sender will convert the arriving event (assertion of EventInReq) into SysReq.Event messages, passing the message to DVE and acknowledge the event using the above defined 4-phase handshake after receiving the acknowledgement from DVE. The sender will receive the SysRsp.OK from DVE and shall report an error on timeout (not receiving OK responses to the sent messages) or if response indicates an error.

3375

Receiver - Block within an agent interface that implements event outputs (EventOutReq, EventOutAck). A receiver will convert arriving SysReq.Event messages into event signals, asserting EventOutReq. The receiver shall respond back to the initiator by returning SysRsp.OK. The Receiver shall report an error on timeout at the target interface (target not responding to handshake).

3378

Broadcaster – Block within DVE that will broadcast SysReq.Event messages. A broadcaster will send each arriving SysReq.Event message from any Sender, to all Receivers (except the initiator). The broadcaster shall respond back to the initiator Sender by returning a single SysRsp.OK after receiving all the expected SysRsp.OK messages from the Receivers. The Broadcaster shall report an error on timeout (not receiving OK responses to the sent messages) or if any response indicates an error.

3381

The Broadcaster shall provision one entry for each Sender. It shall not aggregate events. The Broadcaster may handle only one broadcast at a time.

3384

Each agent participating in the Event protocol shall implement a CSR to provide:

3390

- Timeout value (implementation dependent)
 - Status Bit(s) to indicate Error or detailed Error Status (implementation dependent)
 - Enable Bit to enable send protocol - Even when disabled, the sender shall acknowledge event requests on the 2-wire interface
 - Enable Bit to enable receiving - Even when disabled, the Receiver shall properly terminate all received SysReq.Event messages by responding with a cmstatus==0 (no operation performed)
- 3393
3396

A first (protocol) timeout value shall be provided by the xSEPTOCR register shown in Table 6-7, the timeout shall be programmable to provide at least 4096 clock cycles of timeout - it may be sufficient to only allow powers of two - this timeout will be used to detect fatal protocol or initialization errors.

3399

TABLE 6-7 : SYSTEM EVENT PROTOCOL TIMEOUT CONTROL REGISTER (XSEPTOCR)

Bit	Name	Description	Access	Reset Value
30:0	TimeOutThreshold	Time out threshold value. Counts in increments of 4K cycles.	Read/Write	0x4000
31	Rsvd	Reserved	Read Only	0x0

3402

A second (handshake) timeout value shall be provided by the xEHTOCR register shown in Table 6-8, the timeout shall be programmable to provide a smaller range (64 to 256 clock cycles) - this timeout will be used to detect a non-responding target of events.

3405

TABLE 6-8 : EVENT HANDSHAKE TIMEOUT CONTROL REGISTER (XEHTOCR)

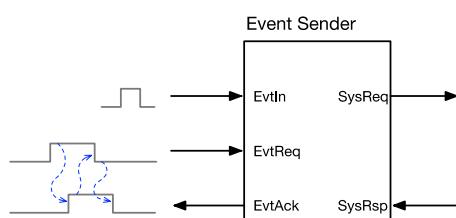
Bit	Name	Description	Access	Reset Value
7:0	TimeOutThreshold	Time out threshold value, up to 256 cycles.	Read/Write	0x0
31:8	Rsvd	Reserved	Read Only	0x0

3408

6.3.2 Event Sender

The sender state-machine will be idle after reset. When the EventInReq is asserted by the source, the state machine will enter the Send state and start sending SysReq.Event messages to the event broadcaster in the system. Maestro shall provide the broadcaster ID.

3411



3414

FIGURE 6-5: EVENT SENDER - INTERFACES

Event messages, like all SysReq transactions, are not credited and a sender must not send more than one transaction to the Broadcaster.

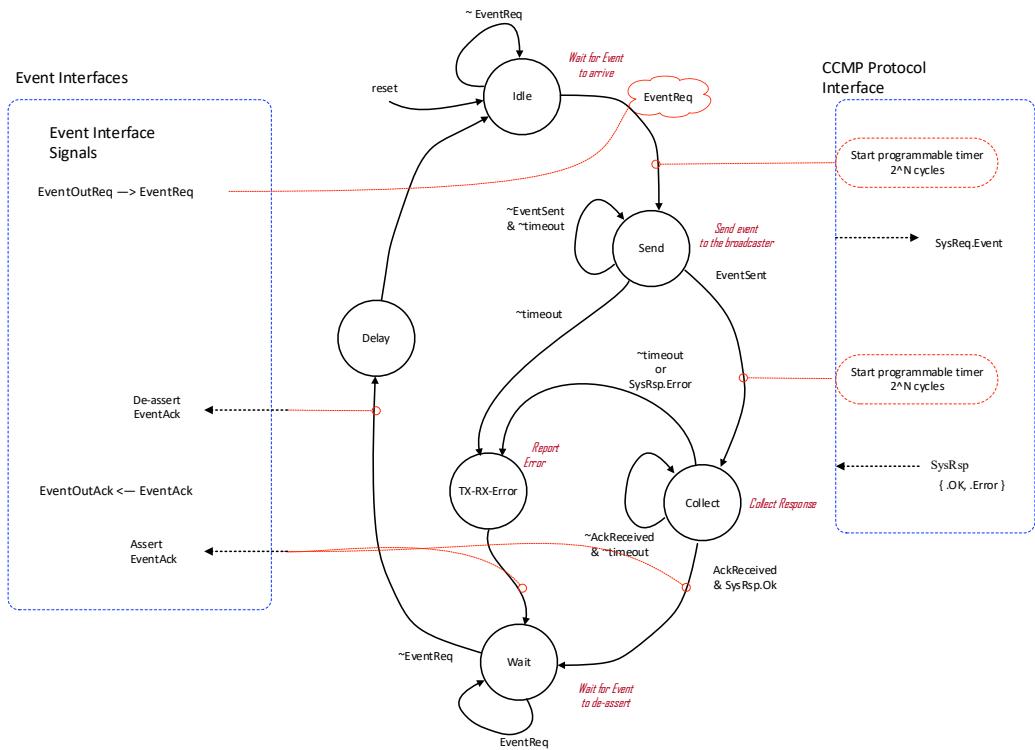


FIGURE 6-6: EVENT SENDER FSM

After sending out the message, the sender shall verify that the message receives its response -

Note: In Ncore 3.6, the sender targets only the broadcaster agent, only one response is expected.

An error is considered:

- The transaction does not receive a response within the timeout period
 - SysRsp return an error status

6.3.3 Event Receiver

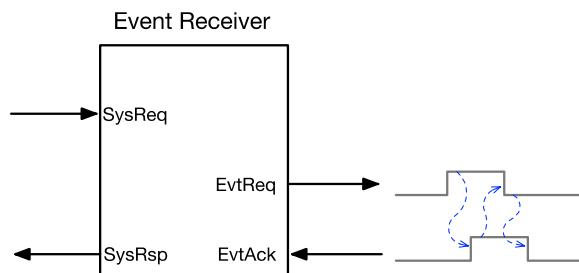


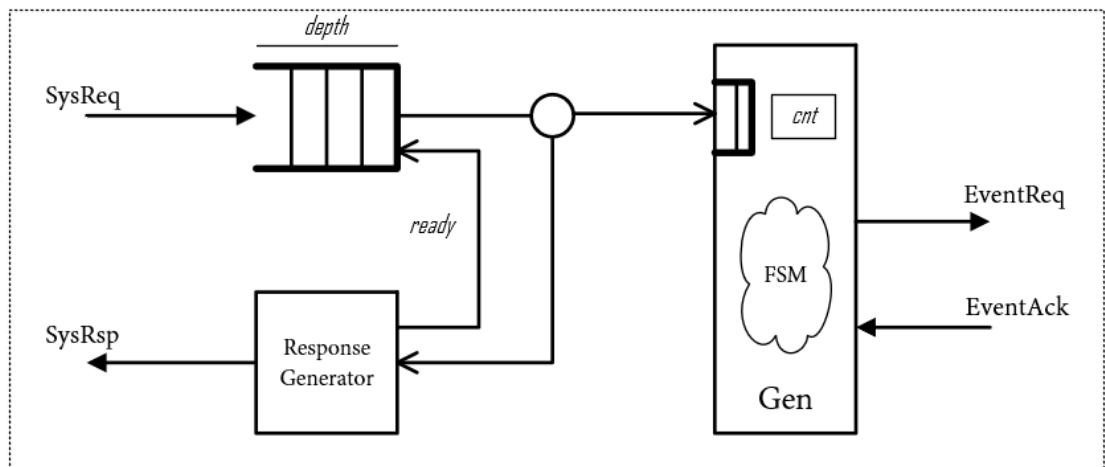
FIGURE 6-7: EVENT RECEIVER INTERFACE

Whenever a SysReq.Event message arrives, it will be recorded within the input queue. The queue shall provide one dedicated storage location for each source of events. The queue shall provide one dedicated storage location for each source of events. The Event Receiver shall provide a response for every SysReq.Event message.

Currently, for Event Receivers, DVE is the unique source of events hence one slot is required.

Note: In NCore 3.6, DVE waits for the end of a broadcast sequence to start a new one. The Event Receiver will receive the Event message only after the completion of the previous one. Nevertheless, the Event receiver responds to DVE to acknowledge the reception of the SysReq.Event message while the handshake is not finished at the target interface. The Event Receiver shall aggregate Events received during an active handshake sequence.

The architecture of the Event Receiver is shown in Figure 6-8. It consists of a FIFO queue, a Response Generator, and an Event Generator.



depth - one entry per messaging agent

cnt increments when a response sent and a FiFo entry has been consumed

FIGURE 6-8: EVENT RECEIVER ARCHITECTURE

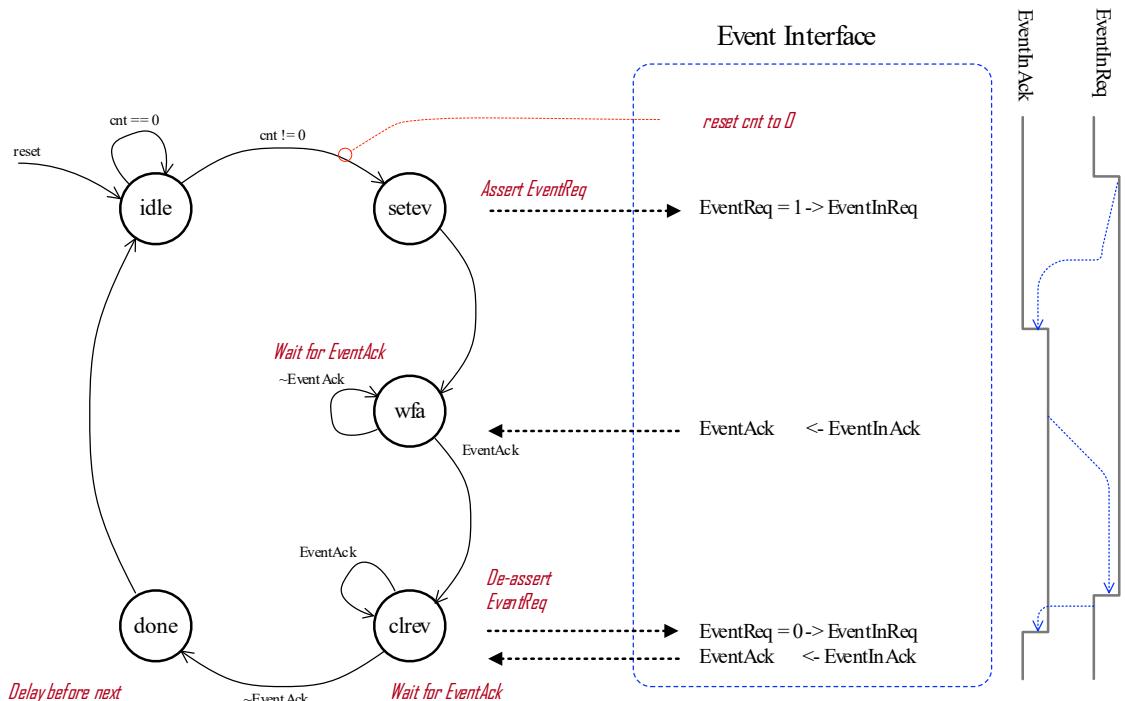
The output of the queue feeds into the event generator and the response generator - every arriving event must be responded to. Once Response Generator is ready, SysReq is popped from FIFO and cnt in FSM is incremented by 1, and SysRsp is returned on SMI interface. The SysRsp response is sent independently of the handshake status at the target interface.

If the arriving message does not indicate an error status, the response (order of severity) shall be:

- Ok - if the agent is enabled to receive events (least severe error)
- Busy - if the agent is disabled

- 3450
- Error - The event generator did not receive EventAck within the timeout period (note, the timeout period for the event handshake may be hard-coded to a significantly smaller value than the protocol timeout)

The Event Receiver State Machine, shown in Figure 6-9, receives arriving event messages and converts them into the 4-phase handshake protocol.



3453

FIGURE 6-9: EVENT RECEIVER STATE MACHINE

3456

3459

3462 6.3.4 Event Broadcaster

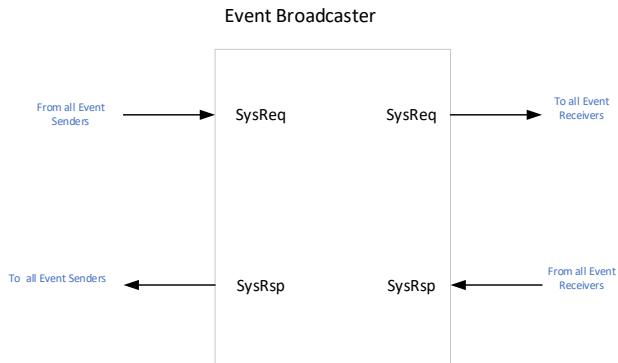


FIGURE 6-10: EVENT BROADCASTER INTERFACE

3465

The Event Broadcaster is a combination of an Event Receiver plus an Event Sender. Nevertheless, the Receiver part of the Broadcaster shall not aggregate Events and the Sender part shall send a message and collect responses to more than one agent.

3468

Whenever a SysReq.Event message arrives, it will be recorded within the input queue. The queue shall provide one dedicated storage location for each source of events. The queue shall provide one dedicated storage location for each Event Sender. The Event Broadcaster shall provide a response for every incoming SysReq.Event message. A broadcaster will send each arriving SysReq.Event message from any Sender, to all Receivers (except the initiator). The broadcaster shall respond back to the initiator Sender by returning a single SysRsp.OK after receiving all the expected SysRsp.OK messages from the Receivers.

3471

The Event Broadcaster DVE waits for the end of a broadcast sequence to start a new one. The Event Broadcaster shall not aggregate Events received.

3474

The Event Broadcaster must not send more than one transaction at a time to each Event Receiver.

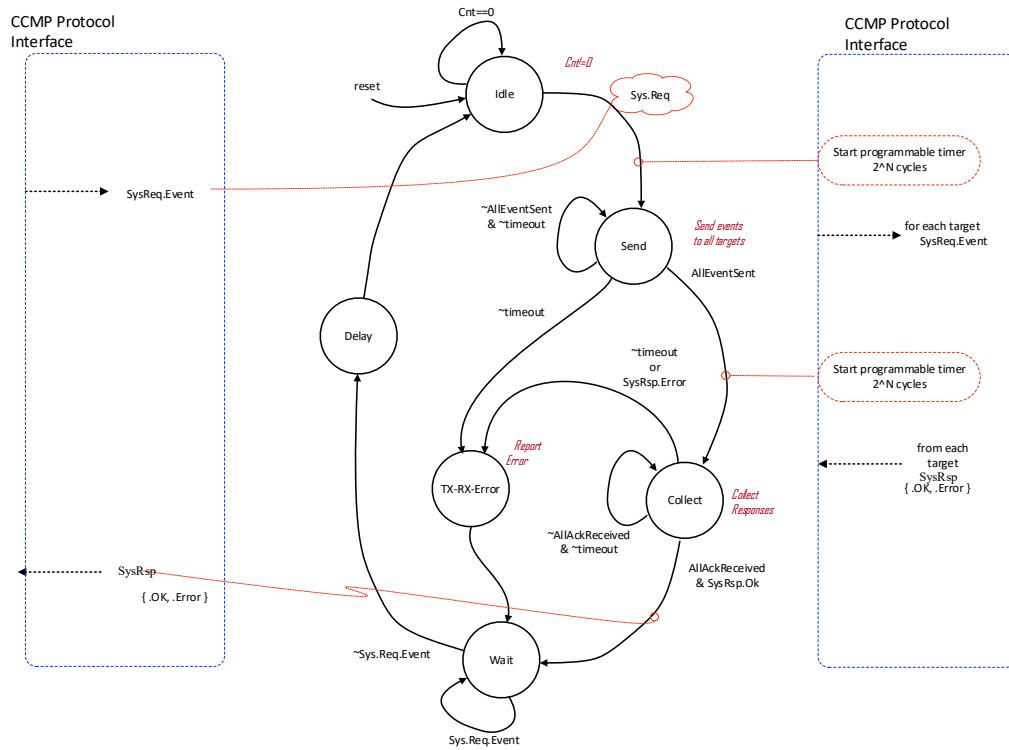
If the arriving message does not indicate an error status, the response (order of severity) shall be:

3480

- Ok - if the agent is enabled to receive events and has received all responses without error
- Busy - if the agent is disabled
- Error - the agent did not receive all responses within the timeout period or one of the responses includes an Error status

3483

3486



3489

FIGURE 6-11:BROADCASTER FSM

3492

3495

3498

3501

³⁵⁰⁴ 7 Quality of service (QoS)

³⁵⁰⁷ The purpose of QoS is to provide certain service guarantees, determined by bandwidth or latency requirements. This chapter describes Ncore 3 QoS-related features. The current implementation is based on message priority. The QoS value on native interface command is mapped to QoS bucket (priority) mapping function. The mapping is provided through predetermined design time parameters.

³⁵¹⁰ The mapping from QoS to Priority must be identical in each Ncore 3 unit.

³⁵¹³ The transport layer (CDTI/CSTI) doesn't have any QoS related features. NCore 3 offers priority arbitration in Concerto units. This bucket value is used for arbitration at all points in the system where requests accumulate in a buffer or transaction table. Indeed, the QoS arbitration happens in AIUs, DCEs and DMIs.

The general behavior to elect a transaction in each unit respects the following criterion:

- ³⁵¹⁶ - The transaction has no unsatisfied ordering dependencies.
- There is no other candidate transaction that is under starvation prevention.
- An appropriate credit is available.
- ³⁵¹⁹ - The transaction has the highest QoS value among the candidate transactions.
- The transaction is the oldest among candidate transactions with the same QoS value.

³⁵²² Ncore 3 also implements a QoS Starvation prevention mechanism that guarantees forward progress for low QoS transactions that may be stuck behind higher QoS transactions. This mechanism is implemented at all QoS priority arbitration points in the system.

³⁵²⁵ 7.1 Fields related with QoS

CCMP uses several distinct labels for expressing the types of QoS services requested for the message. These are presented in the message header using the following fields:

³⁵²⁸ **Priority:** This label refers to the relative preference level of the message at an arbitration station.

The 4-bit QoS value for an incoming native transaction is mapped to one of 8 QoS buckets (3-bit value priority field) by Maestro mapping. QoS value mapping is performed at native interface: AIUs/DMIs/DIIs.

³⁵³¹ TABLE 7-1: SYSTEM PARAMETERS FOR QoS CONFIGURATION

Parameter Name	Description	Type	Default	Min	Max	Enum	Notes
qosEnabled	Enable QoS support	Boolean	FALSE				

Parameter Name	Description	Type	Default	Min	Max	Enum	Notes
qosMap	QoS value to priority map	String					From Native QoS value (4-bit) to Priority (3-bit)
qosEventThreshold	QoS event threshold	integer	64	32	1024		

The system parameters for QoS are described in the parameters specification. Table 7-1 is here for illustration. In addition, **QoS** field is used to send QoS value received at native initiator to native target. The QoS field received with native transaction is copied into the QoS field of all messages issued in Ncore to process the transaction as well as all the related transactions generated on native interfaces. This is done by:

- Copying the QoS field within the transaction into the QoS field of the CMD request message generated by the AIU.
- Copying the QoS field of the message into QoS fields of all native transactions begotten by the message at its target unit.

Implementation note: the QOS field is not present in dtr_req messages, it is not used and it is removed from the current Ncore 3.4 implementation.

Qos Label (QL): This label may indicate a combination of other QoS attributes. It is currently unused and tied to 0.

Caution: smi_pri (Priority inside of the network) has opposite order (decreasing order) with AxQoS (increasing order). That is, in the network smaller priority values are higher QoS. So, by default QoS 15 will map to pri 0.

7.2 Starvation Avoidance

Starvation mechanism can be configured in the design with parameters and the behavior can be controlled through CSR. It is implemented as two common state machines with three bits per transaction table entry. It has two phases:

7.3 Starvation Detection:

A global counter is used to count commands sent. Once the counter reaches a programmable threshold, an overflow bit is set in all valid entries which have not sent out the initial command and have their protocol dependencies (Address, AXI ID etc.) resolved. This indicates the start of the period where the entry must make forward progress. The Overflow bit will be cleared if the entry sends a command. If the global counter reaches the threshold again while the overflow bit is still set, then that entry is starving because it hasn't made progress for at least one complete period. If there is one or more starved entry, then the design enters starvation mode.

3561 7.3.1 Starvation Handling:

In this mode only requests that are marked as starved can arbitrate and send commands out. Arbitration scheme used here is implementation defined, it can be age order, find first, round robin or priority based. Note that the starved transactions must be sent out with the same original QoS and priority. The global counter will be paused in this mode. If a starved request can't make forward progress due to non-availability of credits, then the design should simply wait for the credit to become available. Once all the starved requests have been serviced the normal processing resumes and the global counter resumes counting.

Software via CSR will have the option to disable the starvation logic and change the starvation threshold.

TABLE 7-2 : QoS CONTROL REGISTER (xQOSCR)

Bit	Name	Description	Access	Reset Value
15:0	EventThreshold	Event threshold value counts every event (command issues). If value is 0, event count is disabled (event starvation disabled).	Read/Write	0x10
16	useEvictionQoS	Use Eviction QoS value. If disabled, the eviction takes the QoS of the transaction causing the eviction.	Read/Write	0x0
20:17	EvictionQoS	Eviction QoS value	Read/Write	0xf

3573

7.4 NCore 3 Unit Functionalities

Ncore units AIUs, DCEs & DMIs participate in QoS and implement following:

3576 7.4.1 IOAIU

Transactions (initial commands) are sent out based on QoS values in age order after all other (AXID / address / read and write) dependencies are resolved.

3579 All outgoing associated messages will have the mapped priority value on it plus the initial QoS value.

Proxy cache evictions take the value of the transaction that caused the eviction.

7.4.2 CHI_AIU

3582 Transactions (initial commands) are sent out based on QoS values in age order after all other (LPID / address / read and write) dependencies are resolved.

All outgoing associated messages will have the mapped priority value on it plus the native QoS value.

3585 7.4.3 DCE

Incoming commands are stored in a skid buffer and QoS in age order is used to pick commands from the buffer.

3588 All outgoing associated messages will have the calculated priority value on it plus the native QoS value.

Recall transaction uses fixed QoS value that can be specified at design time or via CSR.

7.4.4 DVE

3591 Incoming commands are stored in a skid buffer and age order is used to pick commands from the buffer. Unlike in other Concerto units, priority based QoS is not used in DVE skid buffer.

3594 DVE propagates QoS and priority values from the initial command. DVE propagates the priority and QoS value of the command that caused the generated snoops. DVE propagates the priority value for other generated requests and responses.

7.4.5 DMI

3597 Incoming commands are stored in one of the skid buffers and QoS in age order is used to pick commands from the buffer. The buffers in this case are:

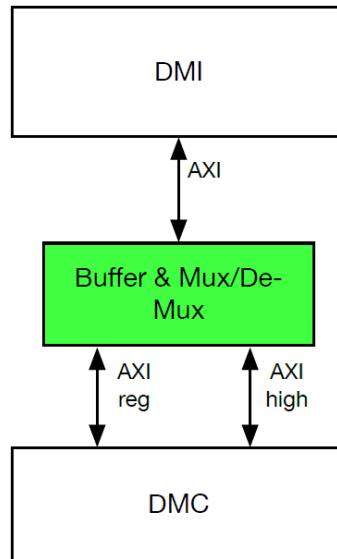
- MRD skid buffer
- RBID skid buffer
- NC read write command skid buffer (does same address checks)

All outgoing associated messages will have the calculated priority value on it plus the native QoS value.
3603 QoS value is then forwarded on native interface.

Cache evictions take the value of the transaction that caused the eviction.

7.4.5.1.1 DMI Threshold support

3606 The purpose of these changes is to work around AXI head of line blocking issue. Expected top-level view of DMI and DMC connectivity is shown in Figure 7-1. The user of NCore is expected to develop the below buffer and mux/demux.



3609

FIGURE 7-1 DMI AND DMC CONNECTIVITY

The DMC used has 2 AXI ports – one for regular traffic “AXI reg” and another for high priority or real time traffic “AXI high”. The buffer & mux/de-mux block contains buffer that is larger than the DMC’s AXI reg port buffer. And the module is responsible for routing the high-priority or real time traffic to DMC’s AXI, and other traffics will be routed to DMC’s AXI reg port. The buffer being larger than the buffer DMC’s AXI reg port buffer guarantees that high priority traffic does not see head of line blocking.

7.4.5.1.2 Parameters

Three new DMI level parameters are introduced:

3618

TABLE 7-3: DMI PARAMETERS FOR QoS CONFIGURATION

Parameter Name	Description	Type	Default	Min	Max
DmiQoSThVal	DMI QoS threshold value. Traffic with QoS equal to or above this value are considered as high priority hard real time traffic	Int	8	1	15
nDmiWttQoSResv	WTT entries in DMI reserved for high priority real time traffic	Int	8	1	32
nDmiRttQoSResv	RTT entries in DMI reserved for high priority real time traffic	Int	8	1	32

NOTE nDmiRtt/WttQoSResv Architecture max value for architecture is 64

Table 7-3 is here for illustration. Please refer to the parameters specification for the description of DMI parameters for QoS.

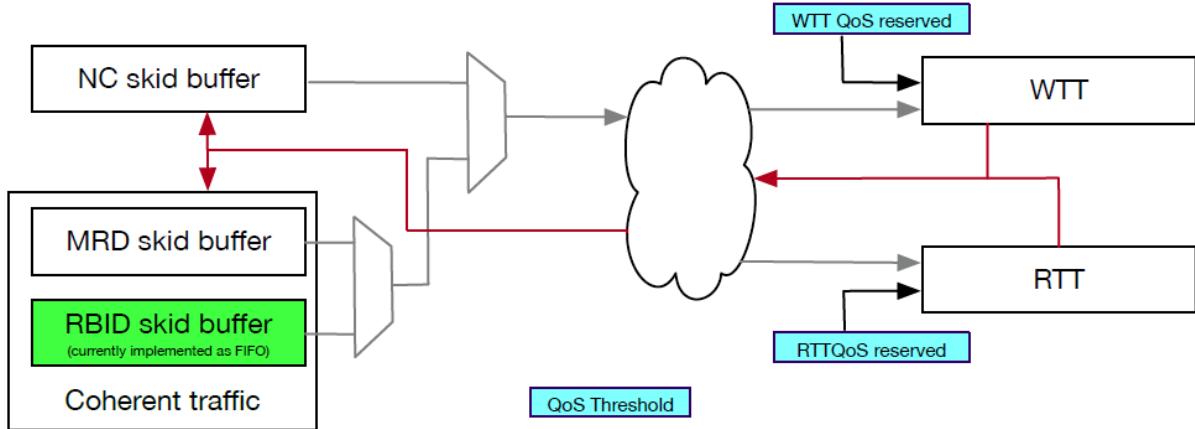
3621

7.4.5.1.3 Changes in DMI

Needed changes in DMI are shown in Figure 7-2. This change involves implementing a feedback loop from DMI egress AXI port i.e., both RTT/WTT to the SMI ingress skid buffers. RTT and WTT must reserve certain number of entries for high priority real time traffic. The number of reserved entries in RTT and WTT are defined by nDmiRttQoSResv and nDmiWttQoSResv parameters respectively. QoS threshold value

3624

3627 for high priority real time traffic is defined by parameter DmiQoSThVal. These three values can be changed at a boot time via a CSR.



3630

FIGURE 7-2 DMI FEEDBACK LOOP

3633 During runtime when WTT/RTT have only reserved entries left they individually give feedback to the skid buffers to send only high-priority real time traffic. As this traffic is provided individually the skid buffer is responsible to resend individually for either read or write traffic i.e., at any given time only one or both RTT/WTT can push back regular traffic, and the skid buffer should handle them separately.

3636

Once regular entries free up in RTT/WTT then the feedback is removed, and regular traffic can start making forward progress. The feedback path is shown with red arrows. Note that the current implementation of coherent writes in DMI is in FIFO order this will need to be changed to priority-based skid buffer.

3639

3642 The user or customer is expected to size the WTT/RTT and reserved entries with some margins to account for pipeline delays. The micro-arch is expected to provide DMI pipeline delay between Skid buffer and the WTT/RTT.

The skid buffer reservation logic should ignore the reserved entries feedback and push starved entries through.

3645

8 Error handling

3648

This section goes over Error handling in Ncore 3.6. This chapter is derived from the current implementation of Ncore 3.0 which was partially derived from Ncore 2.x. The document first describes different registers and encodings and then goes into details of how these errors are handled.

8.1 Error registers

3651

Refer to CSR CPRs in the hw-ncr repository under cpr/csr for register addresses.

8.1.1 Correctable Error Registers

8.1.1.1 Correctable Error Control Register (xCECR)

3654

Register Description: This register controls the detection and interrupt signaling of Correctable Errors in the unit.

TABLE 8-1: THE DEFINITION OF THE CORRECTABLE ERROR CONTROL REGISTER

3657

Bits	Name	Access	Reset	Description
0	ErrDetEn	RW	0b0	Correctable Error Detection Enable. When set to 1, this bit enables detection and logging of correctable errors.
1	ErrIntEn	RW	0b0	Correctable Error Interrupt Enable. When set to 1, this bit enables the assertion of Correctable Error Interrupt signal when a new Correctable Error is detected and ErrCount value equals to ErrThreshold.
3:2	Reserved	-	-	-
11:4	ErrThreshold	RW	0x00	Correctable Error Threshold. Number of corrected errors for which logging, and interrupt (if ErrIntEn is set to 1) is suppressed.
31:12	Reserved	-	-	-

8.1.1.2 Correctable Error Status Register (xCESR)

3660

Register Description: This register logs information of Correctable Errors in the unit. If a new Correctable Error attempts to log this register the same cycle xCESAR is configured, this register will contain information from xCESAR.

3663

TABLE 8-2: THE DEFINITION OF THE CORRECTABLE ERROR STATUS REGISTER

Bits	Name	Access	Reset	Description
0	ErrVld	W1C	0b0	Correctable Error Valid. This bit is set when a Correctable Error is detected and ErrCount equals to ErrThreshold. xCESR, xCEL0 and xCEL1 contain logged information about this Correctable Error. Write 1 to the field resets it to 0b0.
1	ErrCountOverflow	RO	0b0	Correctable Error Count Overflow. This bit is set to 1 when ErrVld is asserted, and a new Correctable Error is detected. Once the field is set, it will keep asserted until being reset. The field is reset to 0b0 when ErrVld is reset.
9:2	ErrCount	RO	0x00	Correctable Error Count. This field increments when a Correctable Error is detected. Once the field reaches ErrThreshold, the value will be frozen from that time until being reset. The field is reset to 0x00 when ErrVld is reset. If write 1 to ErrVld and a new Correctable Error is detected at the same cycle, the field will not increment for the error.
11:10	Reserved	-	-	-

Bits	Name	Access	Reset	Description
15:12	ErrType	RO	0x00	Correctable Error Type. When ErrVld is set to 1, the field indicates the type of error that has been detected and logged.
31:16	ErrInfo	RO	0x0000	Correctable Error Information. When ErrVld is set to 1, the field contains additional unit-specific and error-type-specific information about the error. For example, information that could help identify the site of the error.

8.1.1.3 Correctable Error Location Register (xCELRO)

3666

Register Description: This register logs location information of Correctable Errors in the unit. The information is unit-specific. The fields are made RW accessible to utilize this register as the alias register for error information injection purpose.

3669

TABLE 8-3: THE DEFINITION OF THE CORRECTABLE ERROR LOCATION REGISTER 0

Bits	Name	Access	Reset	Description
31:0	ErrAddress	RW	0x0	Error Address information. When ErrVld is set to 1, the field contains location information of the error. Depending on the type of the error, the register is interpreted in different way. If error is reported from a memory, buffer array or skid buffer implemented with SRAM: Error Entry = bit [19:0], and [31:20] are reserved If error is reported from a Set/Way associative cache: Error Set = bit[19:0] Error Way = bit[25:20] Error Word = bit[31:26] If error is reported as the physical address of the transaction or message: Error Address = bit[31:0] (lower 32 bits, upper bits are reported in xCELRI1)

8.1.1.4 Correctable Error Location Register (xCELRI1)

3672

Register Description: This register logs extra address information that cannot fit in xCELRO. The fields are made RW accessible to utilize this register as the alias register for error information injection purpose.

3675

TABLE 8-4: THE DEFINITION OF THE CORRECTABLE ERROR LOCATION REGISTER 1

Bits	Name	Access	Reset	Description
19:0	ErrAddr	RW	0x000	Error Address Higher Bits. Contains higher bits of error address if xELRO cannot fit the whole error address.
31:20	Reserved	-	-	-

3678 **8.1.1.5 Correctable Error Status Alias Register (xCESAR)**

Register Description: This register is used to inject error status into xCESR. If a new Correctable Error attempts to log the same cycle this register is configured, the information in this register will be logged in the xCESR.

3681

TABLE 8-5: THE DEFINITION OF THE CORRECTABLE ERROR STATUS ALIAS REGISTER

Bits	Name	Access	Reset	Description
0	ErrVld	RW	0b0	Alias bit for setting ErrVld in xCESR.
1	ErrCountOverflow	RW	0b0	Alias bit for setting ErrCountOverflow in xCESR.
9:2	ErrCount	RW	0x00	Alias field for setting ErrCount in xCESR.
11:10	Reserved	-	-	-
15:12	ErrType	RW	0x00	Alias field for setting ErrType in xCESR.
31:16	ErrInfo	RW	0x0000	Alias field for setting ErrInfo in xCESR.

3684

8.1.1.6 Correctable Resiliency Threshold Register (xCCTR)

Register Description: This register contains the resiliency correctable error threshold as an indication to the functional safety controller (FSC). Exists only if the unit enables resiliency.

3687

TABLE 8-6: THE DEFINITION OF THE CORRECTABLE RESILIENCY THRESHOLD REGISTER

Bits	Name	Access	Reset	Description
7:0	ResThreshold	RW	0x01	Resiliency Correctable Error Threshold. See FSC documents for more information.
31:8	Reserved	-	-	-

3690

8.1.2 Uncorrectable Error Registers

8.1.2.1 Uncorrectable Error Detect Register (xUEDR)

3693 Register Description: This register enables the detection of Uncorrectable Errors. Please note that each detection enable bit listed in Table 8-7 only to make the corresponding uncorrectable error detectable. In order to make the corresponding uncorrectable interrupt observable, both the detection enable bit and the corresponding interrupt enable bit defined in Table 8-8 need to be set to 1'b1.

3696

TABLE 8-7: THE DEFINITION OF THE UNCORRECTABLE ERROR DETECT REGISTER

Bits	Name	Access	Reset	Description
0	ProtErrDetEn	RW	0b0	Protocol Error Detection Enable. When set to 1, this bit enables the detection and logging of Protocol type Uncorrectable Error.

Bits	Name	Access	Reset	Description
1	TransErrDetEn	RW	0b0	Transport Error Detection Enable. When set to 1, this bit enables the detection and logging of Transport type Uncorrectable Error.
2	MemErrDetEn	RW	0b0	Memory Error Detection Enable. When set to 1, this bit enables the detection and logging of Memory type Uncorrectable Error. This field exists only when there are protected memory arrays in the unit.
3	DecErrDetEn	RW	0b0	Decode Error Detection Enable. When set to 1, this bit enables the detection and logging of Access type Uncorrectable Error.
4	TimeOutErrDetEn	RW	0b0	Time Out Error Detection Enable. When set to 1, this bit enables the detection and logging of Time Out Error.
5	SoftwareProgConfigErrDetEn	RW	0b0	Software Programming or Configuration Error Enable. When set to 1, this bit enables the detection and logging of Software Programming or Configuration Error.
6	IntfCheckErrDetEn	RW	0b0	Interface Checker Error Detection Enable. When set to 1, this bit enables the detection and logging of Interface Checker Error.
31:7	Reserved	-	-	-

3699

8.1.2.2 Uncorrectable Error Interrupt Register (xUEIR)

3702

Register Description: This register enables the interrupt signaling of Uncorrectable Errors.

TABLE 8-8: THE DEFINITION OF THE UNCORRECTABLE ERROR INTERRUPT REGISTER

Bits	Name	Access	Reset	Description
0	ProtErrIntEn	RW	0b0	Protocol Error Interrupt Enable. When set to 1, this bit enables the assertion of Protocol type Uncorrectable Error Interrupt signal.
1	TransErrIntEn	RW	0b0	Transport Error Interrupt Enable. When set to 1, this bit enables the assertion of Transport type Uncorrectable Error Interrupt signal.
2	MemErrIntEn	RW	0b0	Memory Error Interrupt Enable. When set to 1, this bit enables the assertion of Memory type Uncorrectable Error Interrupt signal. This field exists only when there are protected memory arrays in the unit.
3	DecErrIntEn	RW	0b0	Decode Error Interrupt Enable. When set to 1, this bit enables the assertion of Access type Uncorrectable Error Interrupt signal.
4	TimeOutErrIntEn	RW	0b0	Time Out Error Interrupt Enable. When set to 1, this bit enables the assertion of Time Out Error Interrupt signal.
5	SoftwareProgConfigErrIntEn	RW	0b0	Software Programming or Configuration Error Interrupt Enable. When set to 1, this bit enables the assertion of Software Programming or Configuration Error Interrupt signal.
6	IntfCheckErrIntEn	RW	0b0	Interface Checker Error Interrupt Enable. When set to 1, this bit enables the assertion of Interface Checker Error Interrupt signal.
31:7	Reserved	-	-	-

3705

8.1.2.3 Uncorrectable Error Status Register (xUESR)

3708 Register Description: This register logs information about Uncorrectable errors in the unit. If a new Uncorrectable Error attempts to log this register the same cycle xUESAR is configured, this register will contain information from xUESAR.

3711 TABLE 8-9: THE DEFINITION OF THE UNCORRECTABLE ERROR STATUS REGISTER

Bits	Name	Access	Reset	Description
0	ErrVld	W1C	0b0	Uncorrectable Error Valid. This bit is set when an Uncorrectable Error is detected. xUESR, xUELRO and xUELRL1 contain logged information about this Uncorrectable Error. Write 1 to the field resets it to 0b0. If write 1 to the field and a new Uncorrectable Error is detected at the same cycle, the field is cleared.
3:1	Reserved	-	--	-
7:4	ErrType	RO	0x00	Uncorrectable Error Type. When ErrVld is set to 1, the field indicates the type of error that has been detected and logged.
11:8	Reserved	-	-	-
31:12	ErrInfo	RO	0x0000	Uncorrectable Error Information. When ErrVld is set to 1, the field contains additional unit-specific and error-type-specific information about the error. For example, information that could help identify the site of the error.

8.1.2.4 Uncorrectable Error Location Register (xUELRO)

3714 Register Description: This register logs location information of Uncorrectable Errors in the unit. The information is unit-specific. The fields are made RW accessible to utilize this register as the alias register for error information injection purpose.

3717 Register Fields: see Correctable Error Location Register (xCELRO)

8.1.2.5 Uncorrectable Error Location Register (xUELRL1)

3720 Register Description: This register logs extra address information that cannot fit in xUELRO. The fields are made RW accessible to utilize this register as the alias register for error information injection purpose.

Register Fields: see Correctable Error Location Register (xCELRL1)

8.1.2.6 Uncorrectable Error Status Alias Register (xUESAR)

3723 Register Description: This register is used to inject error status into xUESR. If a new Uncorrectable Error attempts to log the same cycle this register is configured, the information in this register will be logged in the xUESR.

TABLE 8-10: THE DEFINITION OF THE UNCORRECTABLE ERROR STATUS ALIAS REGISTER

Bits	Name	Access	Reset	Description
0	ErrVld	RW	0b0	Alias bit for setting ErrVld in xUESR.
3:1	Reserved	-	-	-
7:4	ErrType	RW	0x00	Alias field for setting ErrType in xUESR.
11:8	Reserved	-	-	-
31:12	ErrInfo	RW	0x0000	Alias field for setting ErrInfo in xUESR.

3729

8.1.3 Error Type and Information Summary

8.1.3.1 Correctable ErrorType and Info Table

3732

TABLE 8-11: THE DEFINITION OF THE CORRECTABLE ERROR TYPE AND INFORMATION REGISTER

ErrType Code	Error Type and ErrInfo Code (16 bits)	Error Location
0x0	Data Correctable Error <ul style="list-style-type: none"> [2:0] – Storage Type <ul style="list-style-type: none"> 3'b000 – OTT-Data 3'b001 – Read Buffer 3'b010 – Write Buffer 3'b011 – Snoop Filter 3'b100 – Trace Buffer 3'b101 – Command Skid Buffer (if implemented with SRAM) 3'b110 – MRD Skid Buffer (if implemented with SRAM) [7:3] – Reserved [15:8] – Snoop Filter ID (Set field to zero for non-snoop filter) 	OTT/Read Buffer/Write Buffer/Trace Buffer : Entry Snoop Filter: Set/Way
0x1	Cache Correctable Error <ul style="list-style-type: none"> [0] – Array Type <ul style="list-style-type: none"> 1'b0 - Tag Array 1'b1 - Data Array [15:1] – Reserved (set to zero) 	Word/Way/Set
0x2 – 0x7	Reserved	N/A
0x8	Transport Error <ul style="list-style-type: none"> [5:0] – Reserved (set to zero) [15:6] – Source ID (FUnit_Id) 	N/A No address associated with packet
0x9 – 0xF	Reserved	N/A

*MBZ: Must Be Zero

3735

8.1.3.2 Uncorrectable ErrorType and Info Table

TABLE 8-12: THE DEFINITION OF THE UNCORRECTABLE ERROR TYPE AND INFORMATION REGISTER

ErrType Code	Error Type and ErrInfo Code (20 bits)	Error Location
0x0	<p>Data Uncorrectable Error (applies to data and memory address errors)</p> <ul style="list-style-type: none"> • [2:0] – Storage Type <ul style="list-style-type: none"> ◦ 3'b000 – OTT-Data ◦ 3'b001 – Read Buffer ◦ 3'b010 – Write Buffer ◦ 3'b011 – Snoop Filter ◦ 3'b100 – Trace Buffer ◦ 3'b101 – Command Skid Buffer (if implemented with SRAM) ◦ 3'b110 – MRD Skid Buffer (if implemented with SRAM) • [7:3] – Reserved (set to zero) • [19:8] – Snoop Filter ID (Set field to zero for non-snoop filter) 	OTT/Read Buffer/Write Buffer/Trace Buffer : Entry Snoop Filter: Set/Way
0x1	<p>Cache Uncorrectable Error (applies to tag/data SRAM and memory address errors)</p> <ul style="list-style-type: none"> • [0] – Array Type <ul style="list-style-type: none"> ◦ 1'b0 - Tag Array ◦ 1'b1 - Data Array 	Word/Way/Set
0x2	<p>Native Interface Write Response/Write Data Error</p> <ul style="list-style-type: none"> • [1:0] - Response • [2] - Security Attribute • [3]- Eviction • [7:4] - Reserved (set to zero) • [19:8] – AxID/CHI TxID¹ 	Transaction Address
0x3	<p>Native Interface Read Response Error</p> <ul style="list-style-type: none"> • [1:0] - Response • [2] - Security Attribute • [3]- Fill • [7:4] - Reserved • [19:8] – AxID 	Transaction Address
0x4	<p>Native Interface Snoop Response Error</p> <ul style="list-style-type: none"> • [1:0] – Response • [2] - Security Attribute • [7:3] - Reserved (set to zero) • [19:8] – CHI TxID¹ (Transaction ID has 12 bits) 	Transaction Address
0x5-0x6	Reserved	N/A
0x7	<p>Decode Error</p> <ul style="list-style-type: none"> • [3:0] – Type 	Transaction Address

ErrType Code	Error Type and ErrInfo Code (20 bits)	Error Location
	<ul style="list-style-type: none"> ○ 4'b0000: No address hit ○ 4'b0001: Multiple address hit ○ 4'b0010: Illegal CSR access format ○ 4'b0011: Illegal DII access type ○ 4'b0100: Illegal security access ○ 4'b0101 to 4'b1111: Reserved ● [5:4] – Command Type <ul style="list-style-type: none"> ○ 2'b00: Read ○ 2'b01: Write ○ 2'b1x: Not used, reserved ● [7:6] - Reserved (set to zero) ● [19:8] – Transaction ID/AxID¹ 	
0x8	<p>Transport Error</p> <ul style="list-style-type: none"> ● [0] – Type <ul style="list-style-type: none"> ○ 1'b0: Wrong Target Id ○ 1'b1: SMI Protection ● [7:1] – Reserved (set to zero) ● [19:8] – Source ID (FUnit_Id) 	<p>N/A No address associated with packet</p>
0x9	<p>Timeout Error</p> <ul style="list-style-type: none"> ● [1:0] – command type <ul style="list-style-type: none"> ○ 2'b00: Reads ○ 2'b01: Writes ○ 2'b10: CMO/Dataless ○ 2'b11: DVM ● [2] – Security Attribute ● [7:3] – Reserved (set to zero) ● [19:8] – Transaction ID/AxID¹ 	<p>Transaction Address</p>
0xA	<p>Sys Event Error</p> <ul style="list-style-type: none"> ● [0] – Type <ul style="list-style-type: none"> ○ 1'b0: Time out error on message (protocol timeout) ○ 1'b1: Time out error on interface ● [19:1] – Reserved (set to zero) 	<p>NA</p>
0xB	<p>SysCo Error</p> <ul style="list-style-type: none"> ● [0] – Type <ul style="list-style-type: none"> ○ 1'b0: Time out error on message (protocol timeout) ○ 1'b1: External error reported by system response(Protocol error and enabled it with ProtErrDetEn) ● [19:1] – Reserved (set to zero) 	<p>NA</p>
0xC	<p>Software Programming or Configuration Error</p> <ul style="list-style-type: none"> ● [3:0] – Type <ul style="list-style-type: none"> ○ 4'b0000: Atomic Transaction w/o CCP Only reported by DMI when atomics enabled without cache present ○ 4'b0001: No credits configured for access ○ 4'b0010: unconnected DMI unit access ○ 4'b0011: unconnected DII unit access ○ 4'b0101: unconnected DCE unit access ○ 4'b0110-4'b1111: Reserved ● [19:4] – Reserved (set to zero) 	<p>Transaction Address</p>

ErrType Code	Error Type and ErrInfo Code (20 bits)	Error Location
0xD	Interface Checker Error <ul style="list-style-type: none"> • [4:0] – Interface Channels <ul style="list-style-type: none"> ◦ 5'b0xxxx: Reserved for AXI5/ACE/ACE5/ACE-Lite/ACE5-Lite/ACE5-LiteDVM Error Encodings <ul style="list-style-type: none"> ◦ 5'b00000 – AR Channel ◦ 5'b00001 – AW Channel ◦ 5'b00010 – W Channel ◦ 5'b00011 – R Channel ◦ 5'b00100 – B Channel ◦ 5'b00101 – CR Channel ◦ 5'b00110 – CD Channel ◦ 5'b00111 – AC Channel ◦ 5'b01000 – RACK ◦ 5'b01001 – WACK ◦ 5'b01010 – 5'b01111 Reserved ◦ 5'b1xxxx: Reserved for CHI-B/E <ul style="list-style-type: none"> ◦ 10000: CHI REQ Channel ◦ 5'b10001: CHI RSP Channel ◦ 5'b10010: CHI WDAT Channel ◦ 5'b10011: CHI RDAT Channel ◦ 5'b10100: CHI SNP Channel ◦ 5'b10101: CHI SRSP Channel ◦ 5'b10110: CHI SYSCO Channel ◦ 5'b10111: CHI Common Channel ◦ 5'b11000 – 5'b11111 Reserved • [19:5] – Reserved (set to zero) 	NA
0xE	Unsupported Message Error <ul style="list-style-type: none"> • [6:0] – opcode of the transaction <ul style="list-style-type: none"> ◦ CHI: opcode[6:0] ◦ AXI/ACE/ACE-Lite: {AxLOCK[0],AxBAR[0],AxSNOOP[3:0]} • [7] – Reserved (set to zero) • [19:8] – AxID/CHI TxID¹ 	Transaction Address (if applicable)
0xF	Reserved	N/A

Note:

1. CHI Transaction ID or AxID where applicable, otherwise set field to zero. And it only captures the lower 12 bits of AxID if 20 bits AxID is supported for AXI, ACE-LITE or ACE interface.
2. All reserved fields shall be set to zero

3738

8.2 Native Interface Error Response Logging and Interrupt

Uncorrectable Error is logged when an error response is detected at the native interfaces if ProtErrDetEn = 1.

3741

- DMI/DII logs all AXI Bresp/Rresp errors
 - Bresp error => ErrorType Code 0x2 with errorinfo and location
 - Rresp error => ErrorType Code 0x3 with errorinfo and location
- CHIAIU logs all CHI data/non-data response errors

3744

- 3747
 - WriteData/WriteDataCancel/NCBWriteDataCompAck with Data Error => ErrorType Code 0x2 with errorinfo and location
 - SnpRespData with Data Error => ErrorType Code 0x4 with errorinfo and location
- 3750
 - SnpResp with Non-Data Error => ErrorType Code 0x4 with errorinfo and location
- 3753
 - IOAIU logs all ACE CRresp errors (CRresp[1] is logged into ErrInfo Response field)
 - CRresp error => ErrorType Code 0x4 with errorinfo and location

An Uncorrectable interrupt is raised if ProtErrIntEn = 1.

- 3756 CCMP must be completed with error CmStatus for DtwReq/DtwMrgMrdReq and DtrReq, if the first beat of data contains error else the CmStatus does not indicate an error. If following beats of data contain error, it is indicated by setting the appropriate DBad of the data beat. Native interface to CmStatus mapping is shown in Table 8-13.
- 3759

3762

TABLE 8-13: NATIVE INTERFACE TO CMSTATUS MAPPING

Native interface	Native interface error	CmStatus	Description
AXI (DMI/DII)	SLVERR	0b10000011	Data error in CmStatus. As per ARM spec this error is reported when the slave cannot provide data due to various reasons
	DECERR	0b10000100	Address error in CmStatus. As per ARM Spec this error is reported when the slave cannot be found by the network
CHI (CAIU)	Data Error	0b10000011	Data error in CmStatus. As per ARM spec this error is reported when data is corrupted. The error may be reported on datflit or rsplif.
	Non-Data Error	0b10000100	Address error in CmStatus. As per ARM Spec this error is reported when the response cannot be completed due to various reasons. The error may be reported on datflit or rsplif.
ACE (CAIU)	CRRESP[1:0] = 10 error without data transfer	0b10000100	Address error in CmStatus. As per ARM spec, the agent cannot complete the snoop request. (Today RTL issues Target Signaled error for DVM snoops, this needs to be updated in later versions to address error) Concerto expects following: If the originating snoop was an invalidating type, then the agent is expected to go to invalid state else stay in the same state. Snoop filer is updated accordingly.
	CRRESP[1:0] = 11 error with data transfer	0b10000011	AIU should forward data error in Dtr/Dtw/DtwMrgMrd And return normal in SnpRsp

3765

3768

In the cases where the data is provided at the native interface the error is propagated only on DtwReq or DtrReq. When data is not provided then the error is propagated only on SnpRsp or DtwRsp.

3771

- DMI/DII propagate AXI response with error

- Bresp error => DtwRsp with error status from Table 8-13
- Rresp error => DtrReq with error status from Table 8-13
- CHIAIU propagate CHI Snoop response/WriteData with error
 - WriteData/WriteDataCancel/NCBWriteDataCompAck with Data Error => DtwReq with Data Error
- SnpRespData with Data Error => Dtw/DtwMrgMrd/DtrReq with Data Error
- SnpResp with Non-Data Error => SnpRsp with Address Error
- IOAIU propagate ACE snoop response with error
 - CRresp[1:0] == 10(error without data transfer) => SnpRsp with Address Error
 - CRresp[1:0] == 11(error with data transfer) => Dtw/DtwMrgMrd/DtrReq with Data Error

3783 In Ncore System, data can be rotated per DW (Double Word), the beat data error information from native interface is carried in each DW, and after rotation, certain error type can overwrite the others. For example, in AXI, if the first beat sent on SMI contains double word for both SLVERR and DECERR, Address Error is injected into CMStatus.

3789 CmStatus to native interface mapping is shown in Table 8-14. In the case of DtrReq the first beat CmStatus may not indicate error, but consecutive beats may indicate DBad in this case the consecutive beats are treated as Data Error.

- CHIAIU propagate DtrReq/DtwRsp/StrReq/CmpRsp with error if response to native interface is required
 - DtrReq => CompData with error status from Table 8-14
 - DtwRsp => Comp with error status from Table 8-14
 - StrReq => Comp/CompData with error status from Table 8-14
 - CmpRsp => Comp with error status from Table 8-14
- IOAIU propagate DtrReq/DtwRsp/StrReq/CmpRsp with error if response to native interface is required
 - DtrReq => Rresp with error status from Table 8-14
 - DtwRsp => Bresp with error status from Table 8-14
 - StrReq => B/Rresp with error status from Table 8-14
 - CmpRsp => Rresp with SLVERR (DVMs)

3804 AIUs receive error from DtrReq/DtwRsp/StrReq/CmpRsp, when the native protocol is ACE in addition to the error field in RResp[1:0], RResp[3:2] includes the cache line status field. The cache line status field shall not be affected by CmStatus information. The other fields of the response are mapped to the native interface as defined when the CmStatus is not reporting error.

3807 TABLE 8-14 CMSTATUS TO NATIVE INTERFACE MAPPING

Native interface	CmStatus	Native interface error	Description
AXI/ACE-Lite/ACE5-Lite /ACE (NCAIU/CAIU)	0b10000011	SLVERR	Data error is best represented by SLVERR
	0b10000100	DECERR	Address error where the slave cannot be found is best represented by DECERR. In the case of DVMs (CmpRsp) this must be decoded to SLVERR
CHI (CAIU)	0b10000011	Data Error	Data error, this includes SLVERR (reported by DMI/DII) is best mapped to Data Error on CHI as Ncore does not have enough information to decode the SLVERR and it may be reported due to bad data

Native interface	CmStatus	Native interface error	Description
	0b10000100	Non-Data Error	Address error, this includes DECERR (reported by DMI/DII) is best mapped to Non-Data Error on CHI as this error is reported when the final target cannot be found.

8.3 Transport Error Logging and Interrupt

3810 Ncore 3 units support Wrong Target ID and SMI Protection Error.

if TransErrDetEn = 1:

- Wrong Target ID Error is logged when seeing message targetID (exclude Port_ID) mismatches unit's FUnit_ID.
- SMI Protection Error includes: Concerto Header Error, Concerto Message Error and Concerto Data Error.

Upon any of the error above happened, the message is dropped. ErrorType Code 0x8 with errorinfo and location is logged.

An Uncorrectable interrupt is raised if TransErrIntEn = 1.

3819

Ncore units also record and report correctable transport error if ECC single bit error is detected.

8.4 Resiliency Related Error Logging and Interrupt

3822 Please see the resiliency section for FSC(functional safety checker/controller) spec for more information.

A selected list of uncorrectable errors from a Ncore unit are reported to the fault checker in resiliency mode and will trigger mission faults.

3825

The detailed full list of errors are listed in each uArchitecture spec of each Ncore unit.

The following two tables help to summarize the current behavior regarding each unit's error types and its ability to generate a mission fault while in resiliency mode. Logged/Detected indicates the ability of the unit to detect and log error information for that type of error. Generates Interrupt indicates the ability of the unit to generate an interrupt for that error if enabled. The last column indicates that a mission fault will be generated by the fault checker which feeds the FSC module.

3831

TABLE 8-15 UNCORRECTABLE ERRORS

Uncorrectable Error Type	Logged/Detected	Generates Interrupt	Generates Mission Fault with Resiliency
IOAIU			
Data OTT Error	Yes	Yes	Yes
Cache Tag/Data Error	Yes	Yes	Yes
Native Intf Write Resp Write Data Error	No	No	No
Native Intf Read Resp Error	No	No	No
Native Intf Snoop Resp Error	Yes	Yes	No
Decode Error	Yes	Yes	No

Uncorrectable Error Type	Logged/Detected	Generates Interrupt	Generates Mission Fault with Resiliency
Transport TargID Error	Yes	Yes	Yes
Transport SMI Prot Error	Yes	Yes	Yes
Timeout Error	Yes	Yes	Yes
SysEvent Error	Yes	Yes	Yes
SysCo Error	Yes	Yes	Yes
Software Prog Error	Yes	Yes	No
Unsupported Msg Error	No	No	No
Placeholder Error	No	No	Yes
Interface Checker Error	Yes	Yes	Yes
CHI-AIU			
Native Intf Write Resp Write Data Error	Yes	Yes	No
Native Intf Read Resp Error	No	No	No
Native Intf Snoop Resp Error	Yes	Yes	No
Decode Error	Yes	Yes	No
Transport TargID Error	Yes	Yes	Yes
Transport SMI Prot Error	Yes	Yes	Yes
Timeout Error	Yes	Yes	Yes
SysEvent Error	Yes	Yes	Yes
SysCo Error	Yes	Yes	Yes
Software Prog/No credits Error	Yes	Yes	No
Software Prog/Unconnected DMI Error	Yes	Yes	No
Software Prog/Unconnected DII Error	Yes	Yes	No
Software Prog/Unconnected DCE Error	Yes	Yes	No
Interface Checker Error	Yes	Yes	Yes

Uncorrectable Error Type	Logged/Detected	Generates Interrupt	Generates Mission Fault with Resiliency
Unsupported Msg Error	Yes	Yes	No
Placeholder Error	No	No	Yes
DCE			
Data Snoop Filter Error	Yes	Yes	Yes
Transport TargID Error	Yes	Yes	Yes
Transport SMI Prot Error	Yes	Yes	Yes
Timeout Error	Yes	Yes	Yes
Software Prog/No credits Error	Yes	Yes	No
Software Prog/Unconnected DMI Error	Yes	Yes	No
Decode/Multi-hit Error	Yes	Yes	No
Decode/No-hit Error	Yes	Yes	No
SysEvent Error	Yes	Yes	No
DVE			
Data Trace Buf Error	Yes	Yes	Yes
Transport TargID Error	Yes	Yes	Yes
Transport SMI Prot Error	Yes	Yes	Yes
Timeout Error	Yes	Yes	No
DII			
Native Intf Write Resp Write Data Error	Yes	Yes	No
Native Intf Read Resp Error	Yes	Yes	No
Transport TargID Error	Yes	Yes	Yes
Transport SMI Prot Error	Yes	Yes	Yes
Placeholder Error	No	No	Yes
DMI			

Uncorrectable Error Type	Logged/Detected	Generates Interrupt	Generates Mission Fault with Resiliency
Data Read/Write Buf Error	Yes	Yes	Yes
Cache Tag/Data Error	Yes	Yes	Yes
Native Intf Write Resp Write Data Error	Yes	Yes	No
Native Intf Read Resp Error	Yes	Yes	No
Transport TargID Error	Yes	Yes	Yes
Transport SMI Prot Error	Yes	Yes	Yes
Software Prog/Atomic w/o CCP Error	Yes	Yes	No
Placeholder Error	No	No	Yes
Timeout Error	Yes	Yes	Yes
SysEvent Error	Yes	Yes	No

3834

TABLE 8-16 CORRECTABLE ERRORS

Correctable Error Type	Logged Detected	Generates Interrupt	Generates Mission Fault with Resiliency
IOAIU			
Data OTT Error	Yes	Yes	No. cerr_over_thres asserted after threshold met.
Cache Tag/Data Error	Yes	Yes	No. cerr_over_thres asserted after threshold met.
Placeholder Error	No	No	No. cerr_over_thres asserted after threshold met.
Transport SMI Prot Error	Yes	Yes	No. cerr_over_thres asserted after threshold met.
CHI-AIU			

Correctable Error Type	Logged Detected	Generates Interrupt	Generates Mission Fault with Resiliency
Transport SMI Prot Error	Yes	Yes	No. cerr_over_thres asserted after threshold met.
Placeholder Error	No	No	No. cerr_over_thres asserted after threshold met.
DCE			
Data Snoop Filter Error	Yes	Yes	No. cerr_over_thres asserted after threshold met.
Transport SMI Prot Error	Yes	Yes	No. cerr_over_thres asserted after threshold met.
DVE			
Data Trace Buf Error	Yes	Yes	No. cerr_over_thres asserted after threshold met.
Transport SMI Prot Error	Yes	Yes	No. cerr_over_thres asserted after threshold met.
DII			
Placeholder Error	No	No	No. cerr_over_thres asserted after threshold met.
Transport SMI Prot Error	Yes	Yes	No. cerr_over_thres asserted after threshold met.
DMI			
Data Read/Write Buf Error	Yes	Yes	No. cerr_over_thres asserted after threshold met.
Cache Tag/Data Error	Yes	Yes	No. cerr_over_thres asserted after threshold met.
Transport SMI Prot Error	Yes	Yes	No. cerr_over_thres asserted after threshold met.
Placeholder Error	No	No	No. cerr_over_thres asserted after threshold met.

8.5 Address Decode, Software Programming and Configuration Error Logging and Interrupt

3840 AIU and DCE detects and logs the following Uncorrectable Errors upon address decoding. If multiple of these errors are reported for the same transaction, then reporting order of priority is from top to bottom as below:

- 3843
 - No Address Hit
 - If the target cannot be found in the address map
 - Or if AIUs want to issue CSR access when it is not allowed
- 3846
 - Multiple Address Hit
 - If multiple targets are found in the address map
 - Illegal Security Access
 - If Non-Secure transaction access secure region as configured in the address map
 - Illegal CSR Access Format
 - If the target is decoded as 32-bit CSR DII, and the following requirements are not met
 - 4 Byte
 - Size-aligned
 - EndPoint order
 - Device Transaction
- 3852
 - Illegal DII Access Type
 - Coherent access on DII
- 3855
 - Unconnected DMI Unit Access
 - If the target DMI as decoded by the address map is not connected to the AIU
 - Unconnected DII Unit Access
 - If the target DII as decoded by the address map is not connected to the AIU
 - Unconnected DCE Unit Access
 - If the target DCE as decoded by the address map is not connected to the AIU
- 3861
 - No Credits Configured for Access
 - If the target as decoded by the address map does not have any credits configured

3867 If DecErrDetEn = 1:

No Address Hit/Multiple Address Hit/ Illegal Security Access/Illegal CSR Access Format/Illegal DII Access Type is logged as ErrorType Code 0x7 with errorinfo and location.

3870 An Uncorrectable interrupt is raised if DecErrIntEn = 1.

If SoftwareProgConfigErrEn = 1:

3873 Unconnected DMI Unit Access/ Unconnected DII Unit Access/ Unconnected DCE Unit Access/No Credits Configured for Access is logged as ErrorType Code 0xC with errorinfo and location.

3876 An Uncorrectable interrupt is raised if SoftwareProgConfigErrIntEn = 1.

In addition, an AIU needs to complete the protocol and return error in the response.

- 3879
 - ACE/ACE-LITE/AXI: DECERR
 - CHI: non-data error

3882 A DCE needs to drop the recall transaction, i.e., pretend it finished successfully. In the case of ‘no credits configured for access’ error (Mrd Credits), DCE must issue an address error with in the CmStatus field of the StrReq.

3885 8.6 CCMP Completion

AIU does not expect DtrReq if StrReq contains error CmStatus for a read request, and it needs to manufacture response to the processor.

3888 For Writes associated transactions, if StrReq contains error CmStatus, AIU does not issue DtwReq to DMI/DII, and it needs to complete the protocol flow to the Native Interface Agent with proper error response.

3891 When IOAIU detects an OTT data buffer uncorrectable error: ErrorType Code 0x0 with errorinfo and location

- DtwReq is returned with CmStatus = 8'b10000011 (Data Error) and poison bit set. If error is not detected on first beat, then only poison bit is set (writes)
- Data that is to be stored in cache the poison bit is set
- If the data is to be sent on to the native interface i.e., R Channel, Rresp is returned with SLVERR (Reads)
- If the data is NOT in use by the original transaction, the error is ignored. i.e., original transactions of CleanUnique/MakeUnique, CMOs, DVMs, CacheStashing, etc.

When IOAIU is configurated with cache: ErrorType Code 0x1 with errorinfo and location

- 3900 • For a tag Uncorrectable Error during cache lookup due to native interface request, IOAIU treats the request as a cache miss and furthermore does not allocate to the cache. In this case uncorrectable error is logged in CSRs and reported via interrupt.
- 3903 • For a tag Uncorrectable Error during SnpReq lookup, IOAIU issues SnpRsp with CmStatus = 8'b10000100 (Address Error).
- 3906 • For a data Uncorrectable Error upon access cache data RAM, if first beat data is poisoned and DtrReq/DtwReq is returned with CmStatus = 8'b10000011 (Data Error) and poison bit set, if a data beat after the first beat is poisoned then only poison bit is set and CmStatus may not indicate error. In the case where data is to be provided on the native interface i.e. R Channel, Rresp is returned with SLVERR on the appropriate data beat.

When IOAIU processes a multi-line transaction:

- 3912 • For read transaction each individual Cache line is for error reporting purposes is treated separately as if it was a single cache line transaction. Requirements are defined in the section above
- 3915 • For write transaction the final response on the native interface must be the accumulation of all individual cache line write responses. Here Address error (DECERR) has higher precedence than (SLVERR).

When DCE gets a snoop filter look up error: ErrorType Code 0x0 with errorinfo and location

- 3918 • DCE issues StrReq with CmStatus = 8'b10000100 (Address Error).

When DCE is configured with zero DMI credits: ErrorType Code 0xC with errorinfo and location

- 3921 • DCE issues StrReq with CmStatus = 8'b10000100 (Address Error).

3924

3927

3930

3933 When DCE gets any SnpRsp error: Refer to CHI E.c chapter 9 Error Handling:

- For invalidating snoop: `SnpInvDtw`, `SnpInvDtr`, `SnpInv`, `SnpInvStsh`, `SnpUnqStsh`, `SnpNITCIDtr`, `SnpNITCMIDtr`
 - If the snooped AIU returns `SnpRsp` error, in general the DCE DOES NOT change the status of requester and snoopee in SF, DCE issues `StrReq` with propagated error `CmStatus` from `SnpRsp`.
 - However, if the snoopee is a CHI agent and a `Non_data` Error is received from the AIU that is connected to this agent, which implies the snoopee has invalidated the local cached copy of the cache line in such a condition⁴². Thus, the corresponding entry of this specific snoopee can be removed from the SF in DCE.
 - If the `SnpRsp` without error DCE still clears the snoopee status in SF since it is an invalidating snoop
 - If none of snooped AIUs provides the data, then DCE issues `StrReq` with propagated error `CmStatus` from the last received `SnpRsp` error. And the requester's status in SF remains unchanged.
 - If one of the snooped AIU provides the data, the protocol is completed by the `DtrReq/DtwMrgMrdReq` and the error is not propagated by DCE via `StrReq`. And the requester's status is updated as if there is no error.
- For non-invalidating snoop: `SnpNITCDtr`, `SnpClnDtr`, `SnpVldDtr`, `SnpNoSDIntDtr`, `SnpVldDtw`, `SnpStshUnq`, `SnpStshShd`
 - If the snooped AIU returns `SnpRsp` error, in general the DCE DOES NOT change the status of requester and snoopee in SF, DCE issues `StrReq` with propagated error `CmStatus` from `SnpRsp`.
 - However, if the snoopee is a CHI agent and a `Non_data` Error is received from the AIU that is connected to this agent, which implies the snoopee has invalidated the local cached copy of the cache line in such a condition⁴³. Thus, the corresponding entry of this specific snoopee can be removed from the SF in DCE.
 - If the snooped AIU provides the data, the protocol is completed by the `DtrReq/DtwMrgMrdReq` and the error is not propagated by DCE via `StrReq`. And the requester's status is updated as if there is no error.
- In the case of Read Stash⁴⁴, the corresponding Stash Snoops are, which are generated accordingly by the native Stash requests such as `StashOnceUnique` and `StashOnceShared`
 - If the cache line state of the target is not the expected final state of the Stash request, before the `SnpStash*` is sent to the target, and even after the `SnpStash*` response is received from the target, the DCE shall NOT change the cache line state for the target, the corresponding final state for the cache line can ONLY be updated in the DCE once it sees the corresponding read request is processed
 - If non-target snooped AIU returns `SnpRsp` error DCE does not propagate it (and issues `MrdReq` to complete the request if target snooped AIU accepts the stash)
 - If target snooped AIU returns `SnpRsp` error, DCE propagates the error on `StrReq` and aborts the transaction
- In the case of Write stash
 - If non-target snooped AIU returns `SnpRsp` error, DCE clears the corresponding snoopee entry in SF, and the error is not propagated

⁴² As described in section 9.3 in ARM CHI version E.c – ARM IHI 0050E.c ID092622

⁴³ As described in section 9.3 in ARM CHI version E.c – ARM IHI 0050E.c ID092622

⁴⁴ As described as Independent Stash Request in ARM CHI version E.c – ARM IHI 0050E.c ID092622

- If target snooped AIU returns SnpRsp error, DCE clears the corresponding snoopee entry in SF, the error is not propagated and proceed as stash decline
- In the case of Write Unique SnpRsp errors are not propagated onto to StrReq, DCE clears all snoopee entry in SF, and the write part proceed

3981 When DMI is configurated with cache: ErrorType Code 0x1 with errorinfo and location

- For a tag Uncorrectable Error during SMC lookup due to CmdReq/MrdReq/DtwMrgMrdReq messages, DMI issues a control propagation DtrReq message that indicates an address corruption error. In addition, the DMI manufactures appropriately sized and poisoned data payload for the DtrReq with CmStatus = 8'b10000100 (Address Error). Since the entire data payload is poisoned, the actual content of the payload is not important.
- For a tag error during SMC lookup due to a prefetch message, DMI drops the message. Since DMI return early StrRsp/MrdRsp for prefetch transaction, no error is propagated.
- For a data Uncorrectable Error upon access SMC data RAM, data is poisoned and DtrReq is returned with CmStatus = 8'b10000011 (Data Error)

3984 When DVE gets a SnpRsp error:

- DVE issues CmpRsp with CmStatus = 8'b10000100 (Address Error).

3995 CmStatus error is propagated only on following responses:

- SnpRsp coming into DCE, only if no other related SnpRsp issued a DtrReq/DtwMrgMrdReq then this is propagated on to StrReq else it is not propagated on to StrReq
- DtwRsp coming into AIUs, this is propagated on to the native interface
- MrdRsp coming into DCE, this is propagated on to StrReq(for CMOs to SMC)
- CmpRsp coming into AIUs, this is propagated on to the native interface

4002 CmStatus error is propagated only on following requests:

- StrReq going out of DCE
- DtrReq going out of AIUs, DMI, and DII
- DtwReq going out of AIUs

4005 In the case of coherent Atomic transactions, where there are two parts the coherent part (clean operation with DCE) and the non-coherent part (atomic transaction with DMI) following applies:

- If an error is reported back to the initiating AIU during the first coherent part, then the error is propagated on the Native interface and the second part is not carried out. Note that the AIU is expected to issue proper response and deallocate its transaction entry.
- If an error is reported back to the initiating AIU during the second non-coherent part, then the error is propagated on the Native interface. Note that the AIU is expected to issue proper response and deallocate its transaction entry.
- For Atomic Load/Swap/Compare where the Bresp and Rdata/Rresp is required, two responses can report different types of error from DtwRsp and DtrReq. An AIU needs to wait for both responses and return a consolidated error response on RRESP back to the Native interface. If there isn't any error on the read segment but there is an error on the write segment. The error on the write segment needs to be presented on the RRESP back to the native interface.
- The priority of error types is: Address Error (DECERR) > Data Error (SLVERR) > OK
- In case of DMI receives Atomic Transaction but without CCP configured or enabled, Software Programming or Configuration Error is reported

4023 In the case of ACE and IOAIU with proxy cache configurations where WriteBacks, WriteClean, WriteEvict, Evict and cache eviction can have two parts i.e. non-coherent write to DMI and coherent update to DCE.

4029 If an error is reported back during the non-coherent transaction part, then the coherent update part needs to be completed. In the case of ACE the error needs to be propagated on the native interface.

In the case of CHI AIU where WriteBacks, WriteClean, WriteEvict, Evict, the protocol semantics must be fulfilled.

4032 AIU DOES NOT propagate error on UpdReq, therefore DCE updates SF as if there is no error.

DtwReq is not allowed to be sent if AIU receives StrReq with error, it need to complete the protocol by manufacturing response to the native interface if necessary.

4035

8.7 Data Poisoning

In DMI, if DBad is asserted on DtwReq, it will not log error and just return normal CmStatus in DtwRsp.

4038 In this case, AIUs will not respond error to native interface.

If the DtwReq is written into SMC, DMI will set the poison bit of the DtwReq beat.

If the DtwReq is written to downstream AXI, DMI will deassert the write strobes of the DtwReq beat.

4041 In DMI, if any Address Error is detected, the poison bits of whole cache line will be set and propagate on DtrReq.

Otherwise, poison bits are propagated in per DtrReq beat based.

4044 Note that there can be cases where the CmStatus of the DtrReq and DtwReq may not report the error but DBad may be set. This happens in cases where the error was detected after processing the first beat of data.

4047 In case of CHIAIU or IOAIU without proxy cache, please refer to chapter 1.3.

In case of IOAIU with proxy cache:

4050 For non-coherent or non-cachable or cache miss without allocation transactions, follow the rule as IOAIU without proxy cache, chapter 1.3.

For full CCP Data Width write hit, the poison bit of the CCP will be overwritten by write data

4053 For partial CCP Data Width write hit, it will result in a RMW, and if either write data from AXI or data in CCP is corrupted, the poison bit will be set

For full cache line write miss, CCP DO NOT generate linefill request and when allocation is done, it will proceed as **2. full CCP data width writes hit**, and the poison bit will be overwritten by write data

4056 For partial cache line write miss, CCP will generate linefill request, so the fill data now comes from 2 part AXI write data and DtrReq, if BEs from AXI write data of entire CCP beat are set, the poison bit of that beat will be overwritten with poison bit from AXI write data.

4059 In summary, Ncore guarantee the granularity of poison bit to be AXI/ACE/CHI Data width = CCP Data width = Dtw/DtrReq data packet width, if requesters perform full writes of the granularity of the memory location, Ncore will overwrite the poison bit, otherwise the poison bit is preserved.

4062

4065

4068

8.8 Timeout Error

Timeout mechanism is implemented in AIUs, DCEs, DVEs, DMIs and DIIs; All Tracking Tables inside a Ncore Unit implement a Timeout Detection logic and Handling logic.

Timeout Detection:

One global counter is designed to count cycles. Once the counter reaches a programmable threshold, the timeout overflow bit in all valid entries is set. The timeout overflow bit will be cleared if the entry deallocates. If the global counter reaches the threshold again while the timeout overflow bit is still set, then that entry has timed out. The event is logged in an error register to allow an interrupt to be raised if enabled as described in Table 8-17.

TABLE 8-17 : TIMEOUT CONTROL REGISTER (xTOCR)

Bit	Name	Description	Access	Reset
30:0	TimeOutThreshold	Time out threshold value. Counts in increments of 4K cycles.	Read-Write	0x4000
31	Rsvd		Read Only	0x0

4080

Timeout Handling:

The status is logged in the CSR, software have the option to either disable timeout and continue or treat this as a fatal error. The timeout counter will stop running, until software restarts it via CSR.

4083

ErrorType Code 0x9 with errorinfo and location

8.9 Sys event and SysCo Errors

Each type of timeout error below has its own timeout counter and CSR setting.

4086

1. Sys Event Protocol Timeout: Sys event sender can report a timeout error if it does not get a SysRsp message for the SysReq it sent out. ErrorType Code 0xA
2. Sys Event Handshake Timeout: Sys event receiver can report a timeout error if it does not get an ack back on the event pins. ErrorType Code 0xA
3. Sys Co Protocol Timeout: Sys Co handler can report a timeout error if it does not get a SysRsp message for the SysReq it sent out. ErrorType Code 0xB

4092

CSR registers for system event protocol and handshake timeout control registers are described in Table 6-7 ad Table 6-8. Table 8-18 describes Sys Co protocol timeout control register.

4095

TABLE 8-18 : SYSTEM COHERENCY PROTOCOL TIMEOUT CONTROL REGISTER (xSCPTOCR)

Bit	Name	Description	Access	Reset
30:0	TimeOutThreshold	Time out threshold value.	Read/Write	0x4000

Bit	Name	Description	Access	Reset
		Counts in increments of 4K cycles.		
31	Rsvd	Reserved	Read Only	0x0

8.10 Unsupported Message Type

- 4098 If Ncore units receive an unsupported CCMP Message (for example DMI gets a snoop command), the message will not be processed and eventually trigger a timeout error. No error is reported in these cases.
- 4101 In case of Ncore AIUs receive an unsupported transaction, the transaction will be resolved inside AIUs and will not generate further CCMP messages to Ncore system. The AIU should return Non-Data Error/DECERR to the Native Interface. The AIU also needs to finish transaction semantics by generating required messages such as DBIDresp, etc.
- 4104 Uncorrectable Error is logged when AIUs does not support the transaction, or the transaction is decoded into unknown if ProtErrDetEn = 1. An Uncorrectable interrupt is raised if ProtErrIntEn = 1.
- 4107 ErrorType Code 0xE with errorinfo and location

8.11 Error Reporting in CMStatus

- 4110 If multiple errors are detected in a message, NCORE Unit will report control errors (eg. Address Error) over data error in CmStatus.

8.12 Interface Checker Error

- 4113 Ncore AIUs support a placeholder at Native Interface side for customers to insert their customized Native Interface protection algorithm, eg SECDEC ECC, Parity, etc. Upon an error happens, the Checker logs the errors, raises appropriate interrupt(s) to the SoC level and propagates the messages.
- 4116 If IntfCheckErrDetEn = 1, the Interface Checker will detect and log any message that contains an error. ErrorType Code 0xD with errorinfo (the channel of where the error is detected).
- An Uncorrectable interrupt is raised if IntfCheckErrIntEn = 1.

8.13 CHI-E transaction error handling

This section will focus on error handling of added transactions to support CHI-E.

1. For transactions that are supported thanks to a 1-to-1 mapping: CleanSharedPersistSep, MakeReadUnique(non-exclusive), WriteUniqueZero, WriteNoSnpZero, and ReadPreferUnique. The error handling remains the same than for any supported transactions.
2. For transactions that are not supported in Ncore 3.6: CHI-AIU resolves the transaction inside the unit and returns Non-Data error response, no further messages(CCMP) would be generated to the Ncore

units. CHI-AIU also needs to finish the transaction semantics if the transaction flow requires certain messages such as DBIDresp, etc.

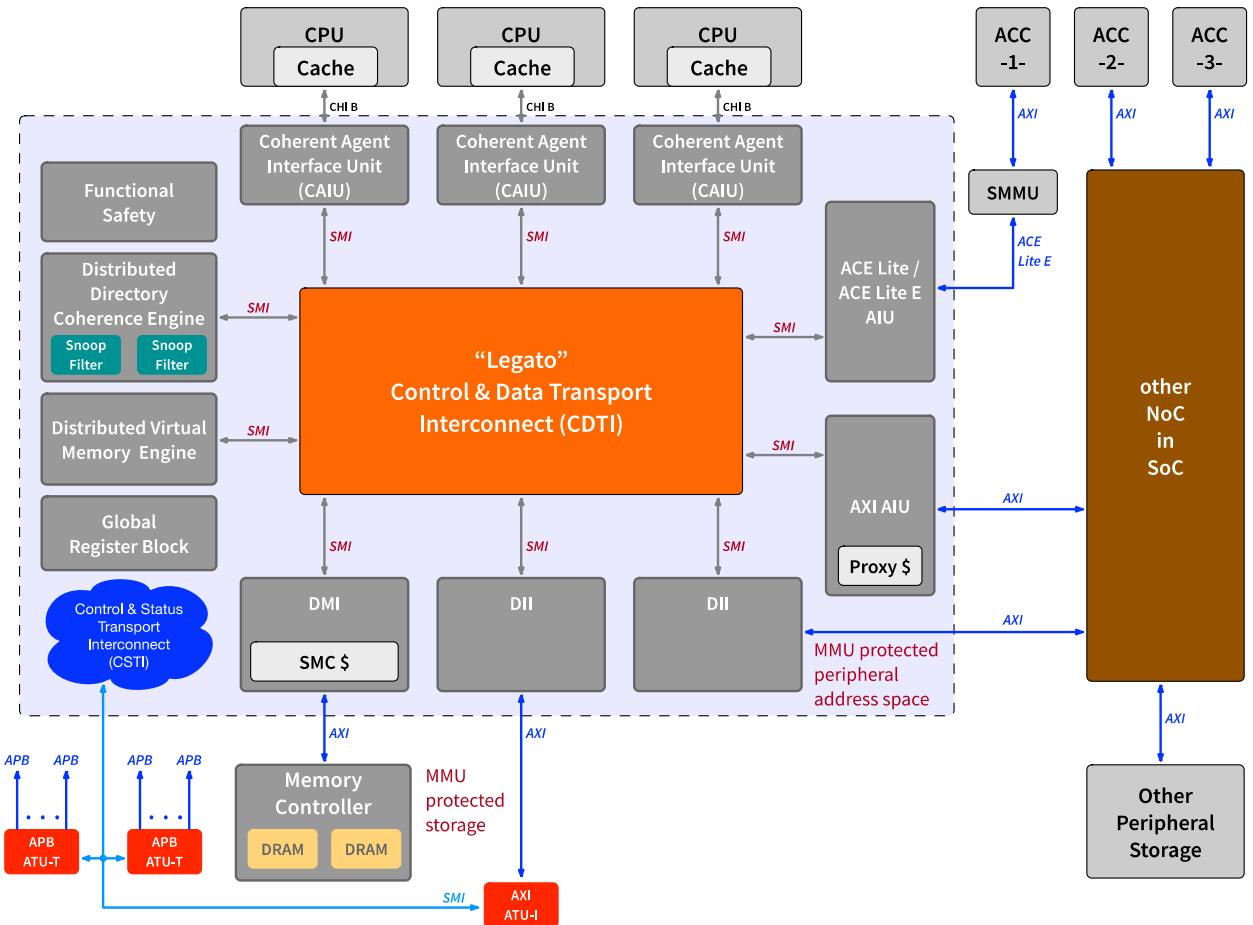
- 4128 3. For Combined Write with CMO transactions: WriteNoSnpFull_CleanSh/CleanInv/CleanShPerSep, WriteBackFull_CleanSh/CleanInv/CleanShPerSep, and WriteCleanFull_CleanSh/CleanShPerSep. These transactions will be mapped into 2 steps:
- 4131 a) If an error occurs during the 1st part (write transaction), the 2nd part (CMO transaction) shall not be executed and the two responses shall signal the same error code. The final response of Completion (write response) and CompCMO/CompPersist(CMO response) must be synced and returned with same type of error response.
- 4134 b) If 1st part (write transaction) is successfully conducted but an error occurs during the 2nd part (CMO transaction), it is permitted to return Comp(write response) with success and CompCMO/CompPersist(CMO response) with error response.
- 4137 4. For exclusive MakeReadUnique transaction: it will be mapped into CleanUnique + optional ReadNotShareDirty
- 4140 a) If an error occurs during the 1st part (CleanUnique transaction), the 2nd part ReadNotShareDirty transaction will not be executed, and Comp with error response shall be returned.
- 4143 b) If the 1st part (CleanUnique transaction) is successful conducted with exclusive fail, but an error occurs during the 2nd part ReadNotShareDirty transaction, either Comp or CompData response is allowed to be returned. Based on the implementation decision, if an error occurs at command/address decoding/control part there won't be any data movement, the final response will be Comp with error. If the error is data corruption or any data related error, the final response will be CompData with error.

4149

9 Functional Safety

4152

This section specifies the Functional Safety features. A complete Ncore 3 system level view with various components including the Functional Safety controller is shown in Figure 9-1. Note that, for the sake of simplicity, not all features are shown in this figure.



4155

FIGURE 9-1: NCORE 3 PROTECTION SYSTEM LEVEL VIEW

4158

4161

9.1 Functional Safety Features

4164

The Ncore 3 Functional Safety Architecture supports ASIL B and ASIL D by implementing:

TABLE 9-1: FUNCTIONAL SAFETY SUPPORT

Protection Level	Ncore 3.4	Ncore 3.6	Ncore 3.7
none	<ul style="list-style-type: none"> • No protection wrappers instantiated • No Fault Checkers • No Functional Safety Controller 		
ASIL B	<ul style="list-style-type: none"> • Full unit duplication 	<ul style="list-style-type: none"> • Full unit duplication 	<ul style="list-style-type: none"> • Partial unit duplication • Full unit duplication
ASIL-D		<ul style="list-style-type: none"> • Full unit duplication 	<ul style="list-style-type: none"> • Full unit duplication

4167

Protection is provided through:

- Unit duplication with 1 to 4 cycle delay (3.4, 3.6, 3.7)
- Native interface protection via place holder (3.4, 3.6, 3.7)

4170

- Transport protection on SMI interface, this can be either **parity** or **ECC** (SECDEC) (3.4, 3.6, 3.7)

4173

- SRAM structures will use **parity** or **ECC** (SECDEC) for address and data (3.4, 3.6, 3.7)
- Internal protection within functional units for all data paths, pipelines and state machines (3.7)

4176

- Memory like structures (large register files & Flop arrays), for example the **OTT/ATT** or skid buffers shall use parity (3.6, 3.7)
 - Pipelines, Queues and address Fifos shall use parity

4179

- State-machines shall detect illegal (non-reachable) states and preferably encode state information in a way to have all state encodings separated by a Hamming distance ≥ 2 . One-hot encodings shall verify that only one bit is set
- All CSR registers shall use parity protection

4182

Any system configuration with **ASIL** level functional safety must instantiate a wrapper for each functional module. This wrapper shall include at least one active functional unit and a fault checker unit (with BIST support).

4185

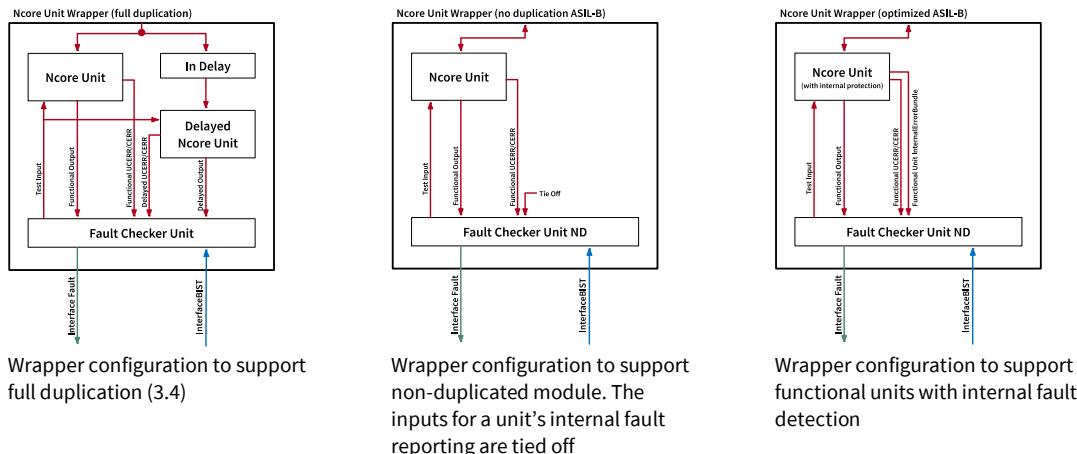
Up to Ncore 3.4, **ASIL** protection always required a duplicated functional unit, the fault checker performs a cycle-by-cycle comparison of the active and the checker unit. Full duplication may not always be required to achieve lower levels of protection (**ASIL B/C**), with Ncore 3.6 area optimization is possible by performing FMEDA analysis on the full configuration and optionally remove duplicate units from the system configuration. In an optimized, partially duplicated configuration, non-duplicated units will also be encapsulated by a wrapper and use a modified fault checker – this fault checker does not require the cycle-by-cycle comparator unit. Eventually,

4188

4191

4194

functional units in Ncore 3.7 will be equipped with an optional internal fault checking mechanism. Every unit must be designed to independently meet ASIL B safety requirements – fault reporting will use an additional port on the fault checker module – starting with Ncore 3.6, the alternate fault checker module used to observe non-duplicated FUs shall provide a bundle of fault reporting inputs.

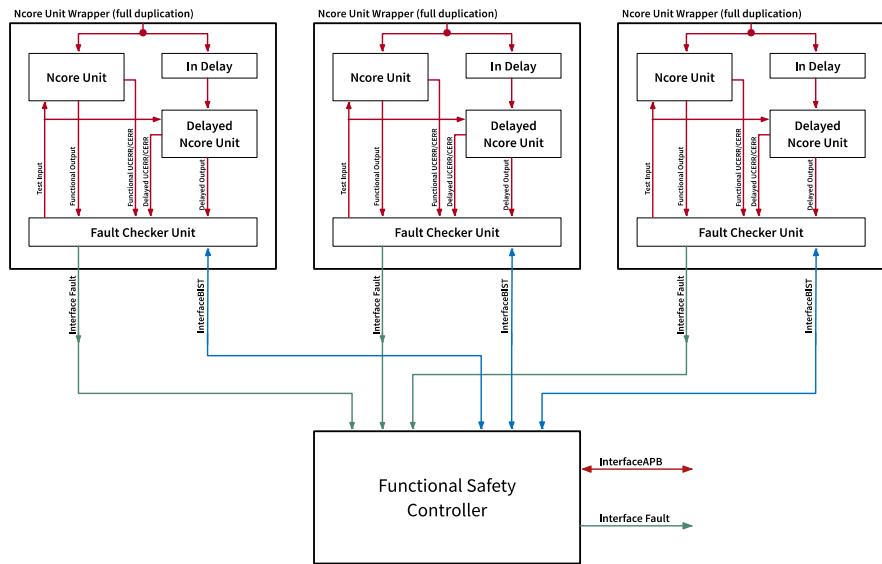


4197

FIGURE 9-2A TO 9-2C: NEW WRAPPER CONFIGURATIONS SUPPORTED

4200

Figure 9-3 to Figure 9-4 show example configurations of Ncore systems, taking advantage of the new optimization.

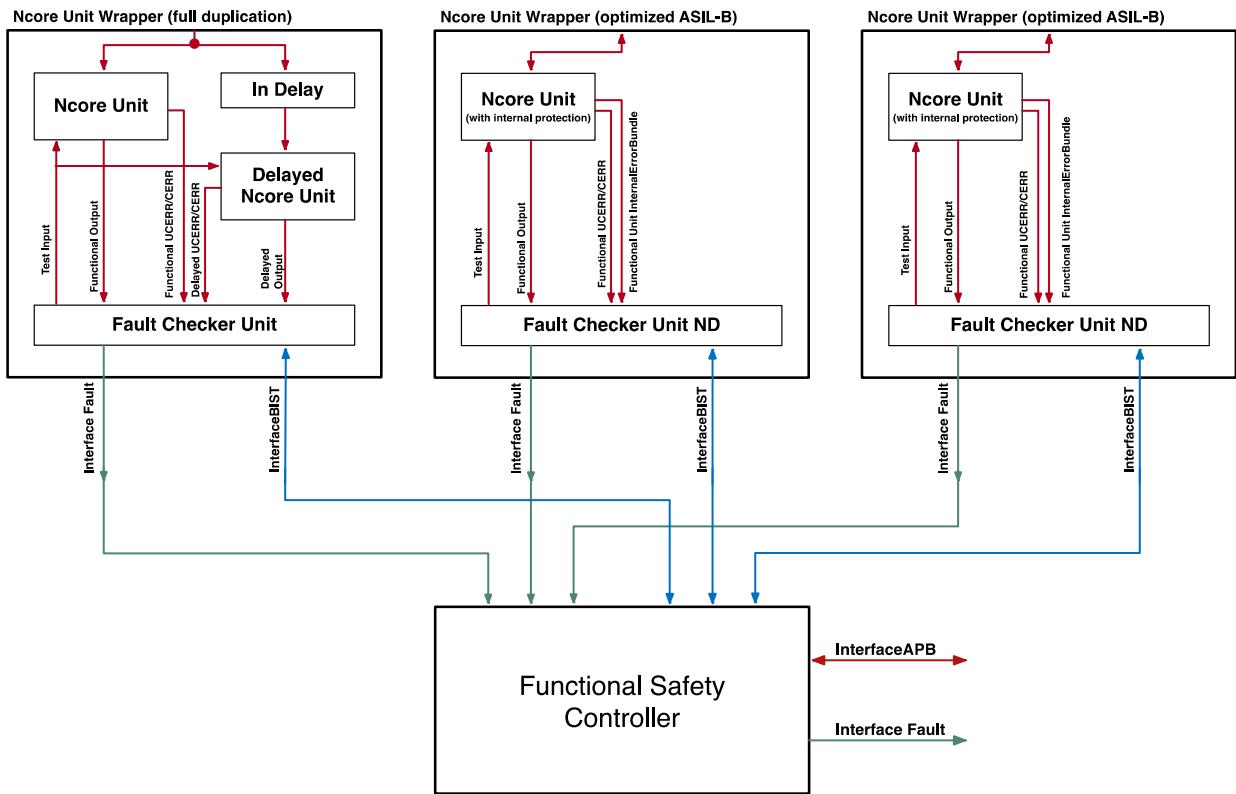


4203

FIGURE 9-3: FULL DUPLICATION APPLIED

shows the current approach (Ncore 3.4), any system with ASIL protection at any level requires full duplication in all modules.

- 4206 A new parameter *protMode* shall be defined for each unit to control the choice between: no-protection, unit-protection, full-duplication. If any ASIL level has been configured, any non duplicated unit shall protect internal registers by parity or ECC and implement BIST access ports to support testing the reporting infrastructure, also refer to Section Detectable internal fault conditions in this document.
- 4209



- 4212 Figure 9-4 shows an example where each functional unit conforms to **ASIL B** and therefore the higher system level only needs to provide the proper infrastructure to report detected faults and a **BIST** infrastructure to verify the integrity of said infrastructure. Each Ncore unit is accompanied by a fault checker to detect, aggregate, and record the fault signals arriving from the local unit. A **BIST** controller will sequentially activate all implemented fault signals to verify the reporting infrastructure – local **BIST** controllers within the fault checkers will be triggered one-by-one from the centralized **BIST** manager within **FSC**. Every time a local **BIST** sequence has been completed, a handshake in the *interfaceBIST* tells the central manager to proceed with the next module.
- 4215
- 4218

- 4221 A detailed view of a complex Ncore unit with all Functional Safety features (for a duplicated module) is shown in Figure 9-5. Note that the SRAMs are not duplicated and must be protected with either **ECC** or **parity**. This protection can be configured in Maestro, before RTL generation.

4224 Functional units with a native interface port (e.g. **CAIU**, **NCAIU**) provide a place holder on the native interface where a customer may add his own protection logic to detect faults on the native protocol . This custom logic shall implement appropriate error detection for incoming transactions or add correction checksum (**ECC**, **parity**) for the protected signals output by the Ncore unit. In addition, it shall also implement mechanisms to verify and report faults based on the correctness of the applied checksum on the protected signals that are input to the Ncore unit. The implemented logic must track the native interface protocol in signaling and timing.

4227

4230

The network protection logic adds either **ECC** or **parity** protection on communication with the **CDTI**. The type of protection can be chosen during configuration before RTL generation. It adds the protection on outgoing **SMI** packets and checks incoming **SMI** packets for errors and report appropriate faults.

4233

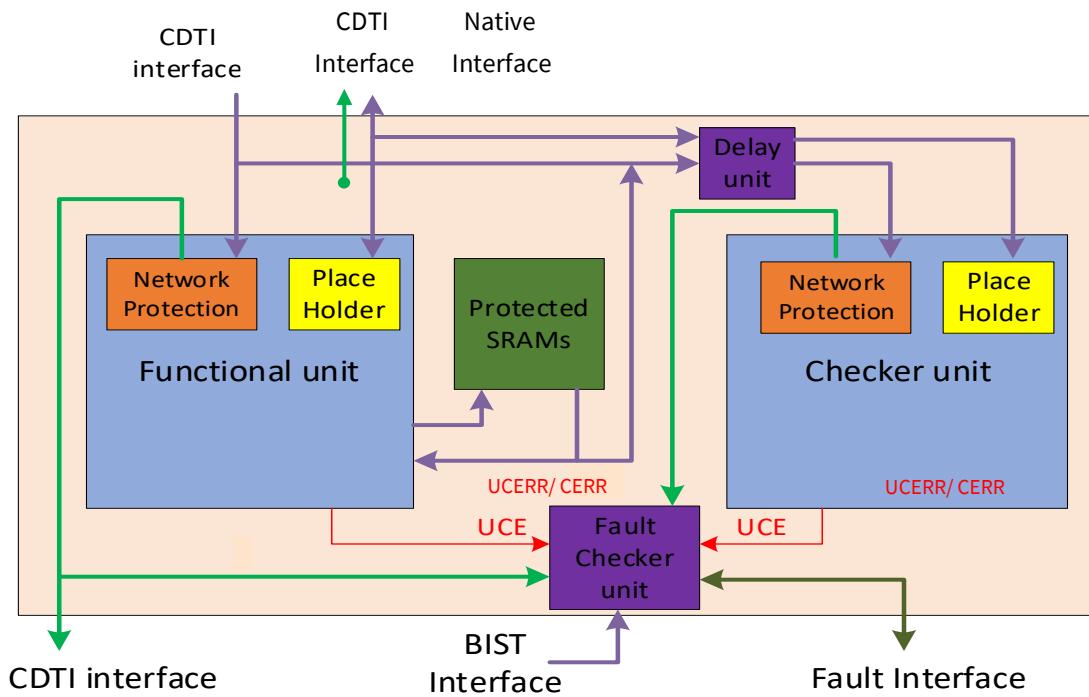


FIGURE 9-5: NCORE UNIT VIEW

4236

9.2 Fault Checker

4239

9.2.1 Architecture of fault checker used for duplicated units

4242

Figure 9-6 shows the detailed structure of the current (3.2, 3.4) Fault Checker Unit used in systems with unit duplication. The main components include the (duplicated) comparator trees and the BIST FSM. The BIST FSM has been augmented with a timeout trigger output.

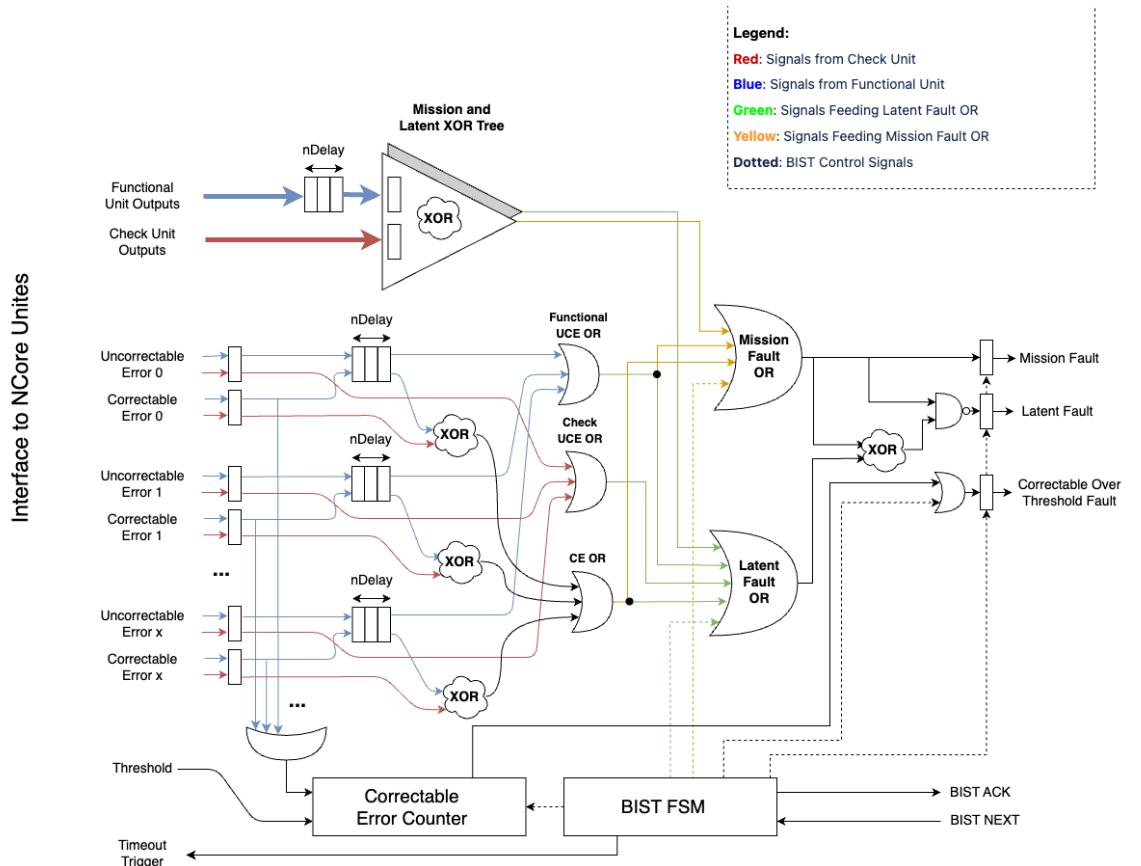


FIGURE 9-6: FAULT CHECKER UNIT

4245

The fault checker unit has 3 main functions.

4248

1. Compare a “late” unit's delayed output to the functional block's output. If a discrepancy is detected, a fault will be signaled and then propagate through the fault path upstream. This feature is active when unit duplication is enabled.

4251

- Timeout event outputs from duplicate units will be part of the comparator input bundle and therefore the Fault Checker will detect it as a mismatch between functional and checker unit when only one-unit times out.
- The BIST controller shall implement a timeout trigger as a step within the self-testing sequence. This output signal shall be an input to both, the functional and the checker unit and, when activated, trigger a timeout signal within the timeout detection unit.

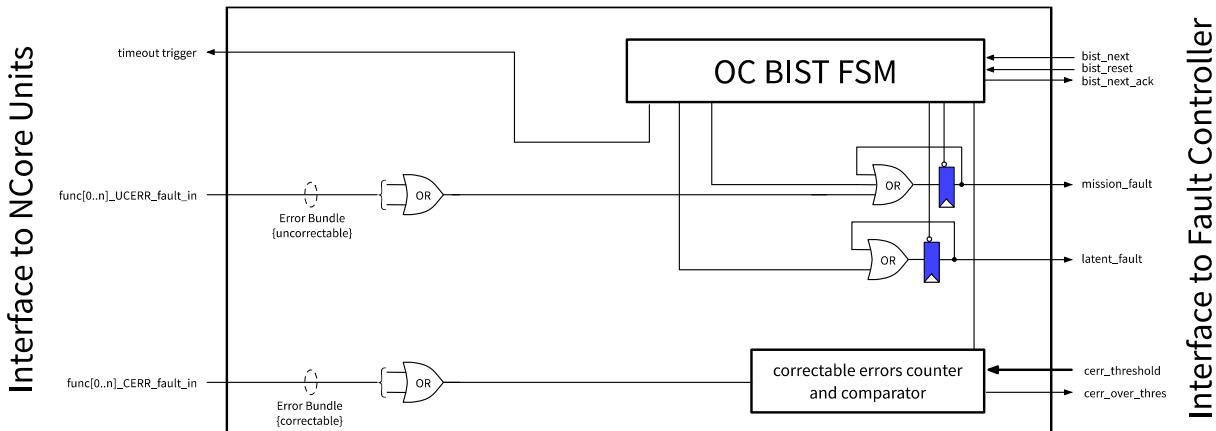
4254

The preferred implementation would preset the timeout counter to a value of (threshold - 1), followed by running the counter for a small number of clock cycles to exercise the counter, the comparator logic and the communication path to the Fault Checker.

- 4257 2. This block also accumulates faults reported outside the check in function 1. Using
4260 *numFaultInputs* the checker creates ports to take in outside uncorrectable (*ucerr*) and correctable error (*cerr*) faults. The checker accumulates these faults in a sticky register bit and reports them upstream. The checker also implements a counter to count the number of *cerr* faults, the counter is compared to a programmable threshold (*cerr_threshold==1*) and a fault will be reported upstream (to the fault controller) as soon as the threshold is reached.
- 4263 3. The checker also has BIST functionality. A BIST finite state machine is implemented within the fault checker unit, its functionality is:
4266
 - 4269 • Reset the sticky bits set by detected faults or as part of the self-test sequence
 - Reset the error counter keeping track of correctable errors
 - Perform self-test sequences
 - The communication between the safety controller and the BIST FSM is asynchronous, it uses 2 wires, *bist_next* and *bist_next_ack*. These 2 wires implement a full handshake. The BIST FSM has six states, these are sequentially executed, under control of the safety controller (after each handshake):
 - o Reset fault D-FF and correctable error counter. The fault controller expects to see *cerr_over_thres*, *mission_fault* and *latent_fault* return to 0.
 - o Force the output of the functional comparator tree to 1. The fault controller expects to see *mission_fault* = 1 or *latent_fault* = 1.
 - o Reset the sticky fault D-FF, and force the output of the duplicated comparator tree to 1. The fault controller expects to see *mission_fault* = 0 *latent_fault* = 1.
 - o Reset faults D-FF, and force both outputs of the functional and duplicated comparator trees to 1. The fault controller expects to see *mission_fault* = 1 *latent_fault* = 0.
 - o Reset faults D-FF, and back to mission mode. The fault controller expects to see *mission_fault* = 0 *latent_fault* = 0.

This Fault Checker Unit architecture will continue to be used in Ncore 3.6 and 3.7 for any system that requires full duplication, independent if a single, a subset or all blocks will be duplicated.

Figure 9-7 shows a proposed structure for a new (3.6 →) Fault Checker Unit used in systems without unit duplication.



4290

FIGURE 9-7: FAULT CHECKER ND UNIT

This checker is significantly simpler as it does no longer need to implement the comparator structures to check duplicated units against each other. The BIST FSM is protected by the *bist_next* and *bist_next_ack* sequence. The rest of logic is implemented with a few gates, thus removes the requirement for duplication. The BIST unit is the same as in the current Fault Checker units.

4293

9.3 Detectable internal fault conditions

Starting with Ncore 3.7 each functional unit shall include internal fault detection to make the unit fault resilient. The goal shall be that each unit reaches the SPFM level required by ASIL B, i. e. $\geq 90\%$ of faults shall be detected.

4299

The following type of faults shall be detected and signaled as part of the error bundle:

TABLE 9-2: UNIT ERRORS

Location	Error Type	Classification	Comment
Address path	Parity	Uncorrectable	Address paths, including internal queues, pipelines and FiFo structures shall use parity protection
Data path	Parity/ECC	Uncorrectable	Data paths, including internal queues, pipelines, FiFo structures and storage arrays (register files or SRAMs) shall use protection
OTT/ATT	Address Field	(Un-)correctable	Protected by parity
	Control Field		Protected by parity
	Linked List		Protected by parity
	Tracking State		Use resilient state encoding
	Timeout		Detect transactions that have seen starvation for a very long time; use a starvation counter with a very slow clock, add two extra bits to the entry, make this a maskable fault, optionally (CSR control) report as correctable, non-correctable, interrupt generation, ignore
Skid buffer	Overrun	Correctable	Skid buffer reached a threshold - optionally report as correctable, non-correctable, interrupt generation, ignore Threshold configurable to arbitrated range, FiFo half or fully occupied

	Backup	Uncorrectable	Skid buffer overrun with FiFo structure full and this state exists for ≥ 127 clocks
Protocol	Illegal command	Uncorrectable	Unrecognizable or unexpected command arrived
	Timeout	Uncorrectable	Protocol timeout – e.g. a response does not come back within a certain time
	Credit error	Uncorrectable	Native transition arrives at a unit that is not configured properly, e.g. has no credits allocated to a decoded target unit
Control	Illegal/Unreachable state in logic	Uncorrectable	Depends on the individual agent and logic block
Coherence	SysCoReq	Uncorrectable – maybe recoverable	coherent transaction arrives while unit is not participating in coherence protocol – check against SysCoReq FSM
CSR error	Parity	Uncorrectable	CSR parity check is thrown
Concerto Mux	TBD	uncorrectable	Parity error on internal queue or FiFo, any logic error

4302

This list may not be exhaustive – depending on the individual units and their internal parchitecture, detection of additional error may be possible and desirable. FMEDA and future updates to this document will be required during the parchitecture and implementation phase. All of the above errors shall be setting a sticky bit in a status register – this status register shall be readable in a units CSR space.

4308

9.3.1 SRAM protection

SRAMs shall be protected with parity or SECDEC in Ncore 3 units. In addition to the data bits, the address bits shall also be protected thanks to the following sequence of operations.

4311

For Write:

4314

- The address is not written into the SRAM.
- The ECC is calculated over a concatenation of address bits and data bits, with address bits being placed as the upper bits.
- The ECC and the data are written into the SRAM.

For Read:

4317

- A concatenation of the expected address bits and the data bits from SRAM, together with the ECC bits from SRAM, is fed into the ECC logic for error detection and correction.
- If the ECC-corrected address bits do not match the expected address bits, then an uncorrectable error is detected.

4320

9.3.2 Transport protection

The Legato transport layer features parity and ECC checks both on headers and data payload. CDTI

4323

network enables data and header protection end to end for SMI messages between Ncore 3 units.

CDTI may comprise several individual networks, each shall allow to enable parity or ECC

protection. CSTI shall also enable parity or ECC protection. In addition, the transport layer is

4326

protected by a timeout for each transaction sequence. The loss of a message is expected to trigger

4329 a timeout detection at the protocol layer. Other checks are implemented to verify the validity of the message at reception: the Target ID of the message shall correspond to the ID of the unit receiving it. It augments the coverage of errors captured for each transmission.

9.3.3 CSR register protection

Configuration and status registers shall be protected by parity or duplication.

4332 9.3.4 Correctable Error Threshold

Each block will have a register controlling its correctable error threshold specifically for reporting to the FSC. (Each block may also have a register for a correctable error interrupt threshold). This value is driven to the Fault Checker. In addition, this value must be part of the interfaces that are checked by the fault checker. The fault checker uses this value to count correctable errors before it asserts a cerr_over_thresh signal to the FSC.

4338 9.3.5 Memories

An Ncore 3 unit might have external memories. If this is the case it will instantiate it inside the top wrapper and not within the unit itself. The signaling to the memories will be included in the fault checker inputs like all other signals. The signaling from the memories will be delayed and driven to the delayed unit like all other inputs.

9.4 Mission and Latent Fault Causes

4344 Table 9-3 shows the Fault Checker Unit *Mission_Fault* and *Latent_Fault* outputs values based on the values of the Functional unit and Checker unit (delayed Ncore Unit) uncorrectable error signals values.

4347 Any mismatch in output signals of the functional unit and checker unit during the normal operation causes a mission fault. If either the functional unit or the checker has an uncorrectable error during the normal operation, it causes a mission fault.

4353 Any mismatch in the latent signal compare XOR trees inside of the fault checker causes a latent fault as shown in Figure 9-6. There is ever a situation that both mission and latent fault appear, only a mission fault is asserted.

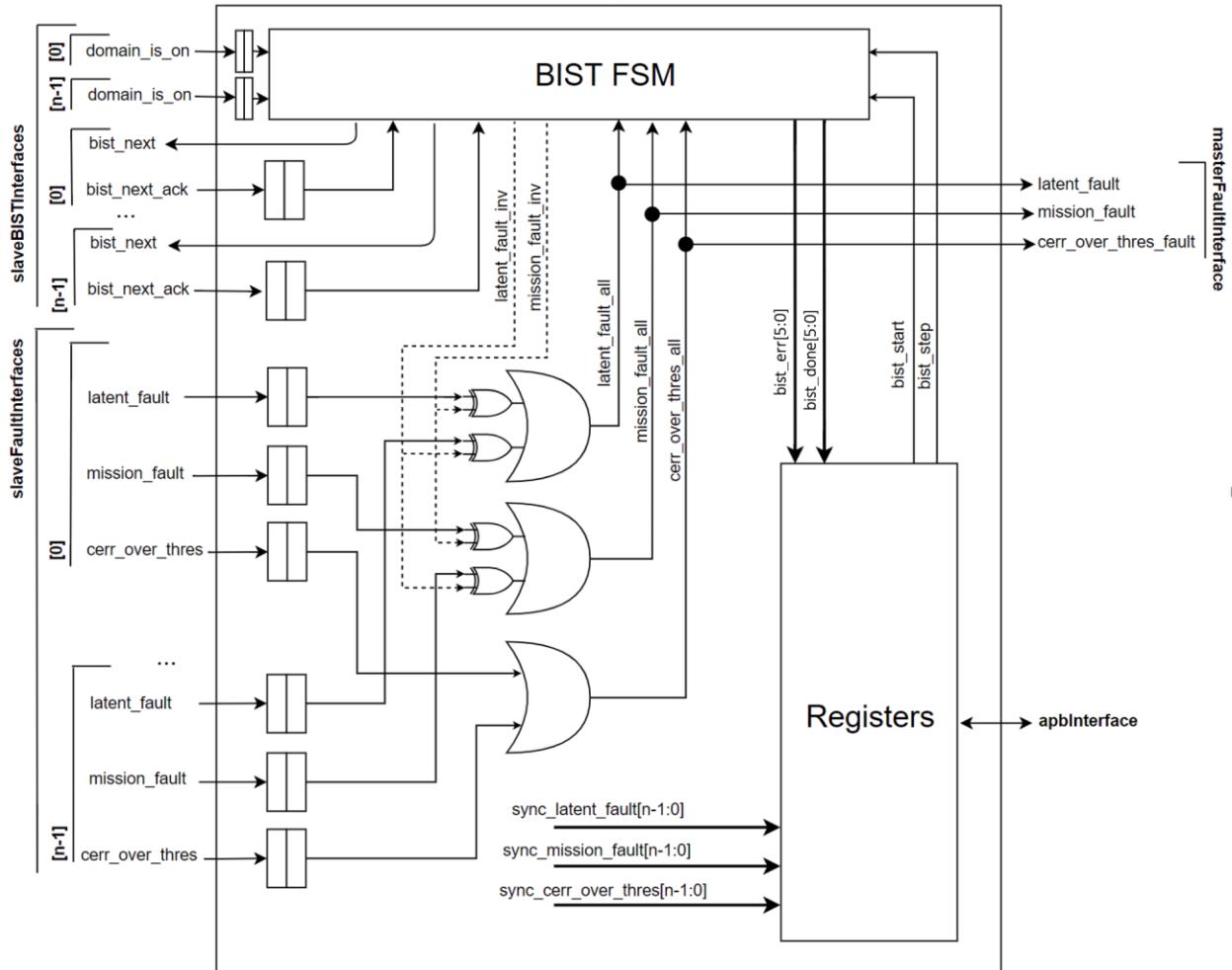
Table 9-3: Mission _Fault and Latent _Fault Signals Outputs Values

UCERR Functional	UCERR Checker	Mission_Fault	Latent_Fault
0	0	0	0
0	1	1	0
1	0	1	0
1	1	1	0

4356 9.5 Functional Safety Controller

4359 The FSC accumulates fault interfaces of multiple blocks which can be in multiple clock and power domains. It then reports any faults seen on these interfaces up stream and through registers. The FSC in addition can perform BIST on the Resiliency reporting logic of each of the blocks.

Figure 9-8 shows the detailed block diagram of FSC.



4362

Figure 9-8: FSC top level block diagram

4365 9.5.1 Feature List

FSC supports the following features:

- 4368 • Accumulates faults and reports them upstream and in registers.
- Performs BIST of Resiliency reporting logic of connected blocks.
- Configurable through an APB Interface.
- 4371 • Can connect to blocks in multiple power and clock domains.
- All internal registers shall be protected by parity

4374 9.5.2 BIST FSM

A BIST FSM can control BIST operations in each output checker connected to the safety controller, 4377 under software control, through access to the safety controller registers.

Communication with the BIST FSM in each output checker is done through a full handshake 4380 mechanism: the safety controller asserts `bist_next` to indicate that the checkers FSM need to execute the next step of the BIST sequence. The checkers FSM assert in turn `bist_next_ack`. When all `bist_next_ack` from all checkers are asserted, the safety controller de-asserts `bist_next`. This deassertion is the event that will make the checkers FSM execute the step of the sequence. After 4383 the checkers are done executing that step, they de-assert `bist_next_ack`. When the safety controller sees all `bist_next_ack` de-asserted, it checks for the BIST step result.

Two modes of operation are supported: automatic and step-by-step. In automatic mode, the 4386 software writes a bit in a register to start the BIST sequence, and all six steps listed below are sequenced automatically in every output checkers in parallel. At the end of the sequence of six steps, a register reports when the sequence is complete, and another register reports a success/failure bit per step. The sequence will always complete whether any specific step has an error or not.

In step-by-step mode, the software writes into a register for each BIST step, one by one. This mode 4392 allows for accessing more detailed information in case a step is reporting an error in automatic mode. Every time the software request execution of the next step, the BIST FSM send a request to execute the next BIST step to all output checkers. A register reports when the sequence is 4395 complete, and through access to the details of the `mission_fault` and `latent_fault` inputs it is possible to identify the source of a failure.

During BIST, the BIST FSM can invert all the faults inputs, to detect that all inputs are 0, or all inputs 4398 are 1, using the same OR tree, and per the step in the BIST sequence.

The BIST State Machine states and associated detailed information are described in

4401

Table 9-4

State	Description	State Outputs	Conditions for Next State
0 (Idle)	Idle State.	<code>Bist_done[5:0] = {1,1,1,1,1,1}</code>	<code>(bist_start bist_step) == 1</code>
1 (Check_1)	The fault controller expects to see all <code>cerr_over_thres</code> , <code>mission_fault</code> and <code>latent_fault</code> go to 0.	<code>bist_done[5:0] = {0,0,0,0,0,0}</code> <code>latent_fault_inv = 0</code> <code>mission_fault_inv = 0</code> <code>cerr_fault_in = 0</code>	<code>~bist_next &</code> <code>bist_all_de_ack &</code> <code>(bist_start bist_step) == 1</code>
2 (Check_2)	The fault controller expects to see all <code>mission_fault = 0</code> and all <code>latent_fault = 0</code> , and <code>cerr_over_thresh_fault = 1</code>	<code>bist_done[5:0] = {0,0,0,0,0,1}</code> <code>latent_fault_inv = 0</code> <code>mission_fault_inv = 0</code> <code>cerr_fault_in = 1</code>	<code>~bist_next &</code> <code>bist_all_de_ack &</code> <code>(bist_start bist_step) == 1</code>
3 (Check_3)	The fault controller expects to see all <code>mission_fault = 0</code> and all <code>latent_fault = 1</code> , and <code>cerr_over_thresh_fault = 0</code>	<code>bist_done[5:0] = {0,0,0,0,1,1}</code> <code>latent_fault_inv = 1</code> <code>mission_fault_inv = 0</code> <code>cerr_fault_in = 0</code>	<code>~bist_next &</code> <code>bist_all_de_ack &</code> <code>(bist_start bist_step) == 1</code>
4 (Check_4)	The fault controller expects to see all <code>mission_fault = 1</code> and all <code>latent_fault = 0</code> , and <code>cerr_over_thresh_fault = 0</code>	<code>bist_done[5:0] = {0,0,0,1,1,1}</code> <code>latent_fault_inv = 0</code> <code>mission_fault_inv = 1</code> <code>cerr_fault_in = 0</code>	<code>~bist_next &</code> <code>bist_all_de_ack &</code> <code>(bist_start bist_step) == 1</code>
5 (Check_5)	The fault controller expects to see all <code>mission_fault = 1</code> and all <code>latent_fault = 0</code> , and <code>cerr_over_thresh_fault = 0</code> . However, in this state the mission fault should come from the Timeout logic in each block.	<code>bist_done[5:0] = {0,0,1,1,1,1}</code> <code>latent_fault_inv = 0</code> <code>mission_fault_inv = 1</code> <code>cerr_fault_in = 0</code>	<code>~bist_next &</code> <code>bist_all_de_ack &</code> <code>(bist_start bist_step) == 1</code>
6 (Check_6)	The fault controller expects to see all <code>mission_fault = 0</code> and all <code>latent_fault = 0</code> , and <code>cerr_over_thresh_fault = 0</code>	<code>bist_done[5:0] = {0,1,1,1,1,1}</code> <code>latent_fault_inv = 0</code> <code>mission_fault_inv = 0</code> <code>cerr_fault_in = 0</code>	<code>~bist_next &</code> <code>bist_all_de_ack &</code> <code>(bist_start bist_step) == 1</code>

Table 9-4: BIST FSM

4404

Note: During BIST in automatic mode the behavior of interrupt signals is undefined.

However, in manual mode the interrupt signals are valid after the respective steps
`bist_done` bit is set.

4407

9.5.3 Registers

Register Name	Register Offset	Description
FSCBISTCR	0x000	Safety Controller BIST control register
FSCBISTAR	0x004	Safety Controller BIST activity register
FSCERR	0x008	Safety Controller Error register
FSCLF0	0x010	Latent Fault inputs values 31:0
FSCLF1	0x014	Latent Fault input values 63:32
FSCLF2	0x018	Latent Fault input values 95:64
FSCLF3	0x01C	Latent Fault input values 127:96
FSCLF4	0x020	Latent Fault input values 159:128
FSCMF0	0x024	Mission Fault inputs values 31:0
FSCMF1	0x028	Mission Fault input values 63:32
FSCMF2	0x02C	Mission Fault input values 95:64
FSCMF3	0x030	Mission Fault input values 127:96
FSCMF4	0x034	Mission Fault input values 159:128
FSCCETHF0	0x038	Correctable errors counter above threshold (CECAT) inputs values 31:0
FSCCETHF1	0x03C	Correctable errors counter above threshold input values 63:32
FSCCETHF2	0x040	Correctable errors counter above threshold input values 95:64
FSCCETHF3	0x044	Correctable errors counter above threshold input values 127:96
FSCCETHF4	0x048	Correctable errors counter above threshold input values 159:128

4410

Table 9-5: Register's Address Map

The FSC supports up to 160 error inputs for each fault category. These signals are generated by the **Fault Checker Units** within each wrapper, see Figure 9-6 and Figure 9-7. Ncore configurations may vary widely in the number of supported FUnits; to simplify fault analysis, Table 9-6 defines an **architected** mapping between **bit location** in any of the 4 fault status registers and the FUnit it is associated with.

4413

4416

Functional Unit Type	Error Input Index	Description	Register
DVE	159	There will be only one DVE in the system	FSCCETHF4, FSCMF4, FSCLF4[31]
Reserved	144..158	No unit connected – tied off to be zeros	
DCE	143..128	{Latent, Mission, CECAT}-input [143:128]	FSCCETHF4, FSCMF4, FSCLF4[(num_DCE-1):0]
DII	127..96	{Latent, Mission, CECAT}-input [127:96]	FSCCETHF3, FSCMF3, FSCLF3[(num_DII-1):0] ⁴⁵
DMI	95:64	{Latent, Mission, CECAT}-input [95:64]	FSCCETHF2, FSCMF2, FSCLF2[(num_DMI-1):0] ⁴⁶

⁴⁵ Supporting up to 32 DIIs⁴⁶ Up to 32 DMIs

Functional Unit Type	Error Input Index	Description	Register
IOAIU/NCAIU	63..32	{Latent, Mission, CECAT}-input [63:32]	FSCCETHF1, FSCMF1, FSCLF1[(num_IOAIU-1):0] ⁴⁷
CAIU	0..31	{Latent, Mission, CECAT}-input [31:0]	FSCCETHF0, FSCMF0, FSCLF0[(num_CAIU-1):0]

4419

Table 9-6: Register Overview

4422

Configuration software (Maestro) shall use the enumerated ID for each FU (within its class) to connect the fault outputs. For example, DCE0's fault signals shall be connected to the fault signal #96 within the 128-bit wide bundle representing the Latent-, Mission- and Error-Threshold-Fault. Every 32-bit register will be associated with a single unit type, except register #4 in each group which will collect DCE and DVE fault status. Any unused bits in these registers shall read back as 0.

4425

9.5.3.1 FSCLFX Register Bit Assignment

Bit	Name	Description	Access	Reset
N-1:0	latent_fault	Each bit indicates a latent fault on the corresponding fault interface in slave Interfaces	RO	0x0

Table 9-7:FSCLFX Register Bit Assignment

4428

9.5.3.2 FSCMFX Register Bit Assignment

Bit	Name	Description	Access	Reset
N-1:0	mission_fault	Each bit indicates a mission fault on the corresponding fault interface in slave Interfaces	RO	0x0

Table 9-8: FSCMFX Register Bit Assignment

9.5.3.3 FSCCETHFX Register Bit Assignment

Bit	Name	Description	Access	Reset
N-1:0	cerr_over_thresh	Each bit indicates the amount of correctible errors went over the threshold on the corresponding fault interface in slave Interfaces	RO	0x0

Table 9-9: FSCCETHFX Register Bit Assignment

4431

9.5.3.4 FSCBISTCR Register Bit Assignment

FSCBISTCR is a read/ write register, a read access will always return the last value written.

Bit	Name	Description	Access	Reset
31:2	Reserved	Reserved	RO	0x0
1	bist_mode	1: Sequential mode (BIST FSM runs all 6 BIST steps in sequence) 0: Single step mode	R/W	0x0
0	bist_start	Writing a 1 will start the engine, depending on bist_mode the engine will perform a single step or run to completion. If there is an error, BIST will restart the sequence when bist_start is written to again.	R/W	0x0

⁴⁷ Even though Ncore 3.6 and 3.7 will not support more than 64 AIUs, we reserve two registers – Coherent AIUs' status will be reflected in registers {FSCCETHF, FSCMF, FSCLF} [0], non-coherent AIUs' will be mapped to {FSCCETHF, FSCMF, FSCLF} [1]

Table 9-10: FSCBISTCR Bit Assignment

- 4434** One write operation is required to run the BIST; all 4 combinations having a defined behavior and 6 writes are needed to complete the BIST in step mode. While the BIST is running, any write shall be disregarded.
- 4437** BIST can be 1st run in step mode for 1 or more steps and then BIST run can be completed in automatic mode or be reset by writing “0” in “bist_start”. “bist_done” in the FSC BIST Activity Register shall be reset at the same time.
- 4440** A parity bit shall be added to the BIST Control and Activity registers for the application to be able to discriminate between hardware and software errors.

9.5.3.5 FSCBISTAR Register Bit Assignment

Bit	Name	Description	Access	Reset														
31:12	Reserved	Reserved	RO	0x0														
11:6	bist_err	<p>Each bit in this register represents one step of the BIST sequence. When the sequence starts, it's reset. As each BIST step completes, its bit is set to 1 if the sequence has completed in error</p> <table> <thead> <tr> <th>Bit</th> <th>Field</th> </tr> </thead> <tbody> <tr> <td>6</td> <td>BIST full reset error (Step1)</td> </tr> <tr> <td>7</td> <td>BIST functional comparator tree force error (Step2)</td> </tr> <tr> <td>8</td> <td>BIST duplicate comparator tree force error (Step3)</td> </tr> <tr> <td>9</td> <td>BIST both comparator tree force error (Step4)</td> </tr> <tr> <td>10</td> <td>BIST timeout test error (Step5)</td> </tr> <tr> <td>11</td> <td>BIST final full reset error (Step6)</td> </tr> </tbody> </table>	Bit	Field	6	BIST full reset error (Step1)	7	BIST functional comparator tree force error (Step2)	8	BIST duplicate comparator tree force error (Step3)	9	BIST both comparator tree force error (Step4)	10	BIST timeout test error (Step5)	11	BIST final full reset error (Step6)	RO	0x0
Bit	Field																	
6	BIST full reset error (Step1)																	
7	BIST functional comparator tree force error (Step2)																	
8	BIST duplicate comparator tree force error (Step3)																	
9	BIST both comparator tree force error (Step4)																	
10	BIST timeout test error (Step5)																	
11	BIST final full reset error (Step6)																	
5:0	bist_done	<p>Each bit in this register represent on step of the BIST sequence. When the sequence starts, it's reset. As each BIST step completes, its bit is set to 1</p> <table> <thead> <tr> <th>Bit</th> <th>Field</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>BIST full reset done (Step1)</td> </tr> <tr> <td>1</td> <td>BIST functional comparator tree force done (Step2)</td> </tr> <tr> <td>2</td> <td>BIST duplicate comparator tree force done (Step3)</td> </tr> <tr> <td>3</td> <td>BIST both comparator tree force done (Step4)</td> </tr> <tr> <td>4</td> <td>BIST timeout test done (Step5)</td> </tr> <tr> <td>5</td> <td>BIST final full reset done (Step6)</td> </tr> </tbody> </table>	Bit	Field	0	BIST full reset done (Step1)	1	BIST functional comparator tree force done (Step2)	2	BIST duplicate comparator tree force done (Step3)	3	BIST both comparator tree force done (Step4)	4	BIST timeout test done (Step5)	5	BIST final full reset done (Step6)	RO	0x0
Bit	Field																	
0	BIST full reset done (Step1)																	
1	BIST functional comparator tree force done (Step2)																	
2	BIST duplicate comparator tree force done (Step3)																	
3	BIST both comparator tree force done (Step4)																	
4	BIST timeout test done (Step5)																	
5	BIST final full reset done (Step6)																	

4443

Table 9-11: FSCBISTAR Bit Assignment

- The expected value of the “bist_done” in FSC BIST Activity Register shall always be defined. This ensures software can take appropriate action: “0” after reset and after any write operation, report the value corresponding to the step completed.

4446

9.5.3.6 FSCERR Register Bit Assignment

- All registers described in section 9.5.3 are protected by parity checking. The parity is continuously checked for every register value against its parity bit. An error will be generated once a mismatch is identified. This error bit is a read only and it can be reset once BIST test starts.

4449

Bit	Name	Description	Access	Reset
31:1	Reserved	Reserved	RO	0x0
0	err	It will be asserted once there is a parity error inside of Function Safety Controller . The error will be cleared once the bist_start bit of the FSCBISTCR register is set to 1'b1	RO	0x0

Table 9-12: FSCERR Bit Assignment

4452

9.6 Protections to the native interfaces

4455 9.6.1 Odd parity check protection to NCAIU supported interfaces

Ncore odd parity check protection scheme follows the Check_Type protection defined by ARM AMBA AXI and ACE protocol⁴⁸. The protocol defines the following two options:

- Odd_Parity_Byte_Data
 - Odd parity checking included for data signals with names that end in DATA⁴⁹ defined. Each bit of the parity covers exactly 8 bits
- Odd_Parity_Byte_ALL
 - Odd parity checking included for all signals. Each bit of the parity signal generally covers up to 8 bits.

Ncore only takes Odd_Parity_Byte_ALL option once Check_Type is enabled, and this is applicable to all the following interfaces an IOAIU supports:

- AXI5
- ACE5
- ACE5-Lite
- ACE5-LiteDVM

Please note that different *chk signals⁵⁰ need to be added accordingly depends on what a specific native interface is enabled for odd parity protection.

⁴⁸ The details of the Check_Type definition can be in section E2 of AMBA AXI and ACE Protocol Specification (ARM IHI 0022H.c ID 12621)

⁴⁹ The details of the signal lists are defined in section A2 of AMBA AXI and ACE Protocol Specification (ARM IHI 0022H.c ID 12621)

⁵⁰ Please refer to section E2.6 of AMBA AXI and ACE Protocol Specification (ARM IHI 0022H.c ID 12621)

4473 Also, it is recommended having an option to exclude Q Channel signals since some of the ARM IPs such as SMMU support such an option

9.6.2 Odd parity check protection to CHI-B interface

4476 On the same token, Ncore odd parity check protection follows the Check_Type protection defined by AMBA 5 CHI protocol. The protocol defines the following two options, and the protection is only available for CHI version E⁵¹ and beyond. Ncore enables this feature for CHI version B to better support other processors such as RISC-V cores etc.

- Odd_Parity_Byte_Data
 - The DataCheck field is present in the DAT packet
- Odd_Parity_Byte_ALL
 - Parity check signals are added to every channel

4482 Ncore only takes Odd_Parity_Byte_ALL option once Check_Type is enabled. Necessary sub fields are required to fulfill this protection as stated in AMBA CHI-E⁵² specification.

4485 Also, it is recommended having an option to exclude SYSCO signals since some of the ARM IPs such as DSU support such an option.

⁵¹ The details are available in section 16.1.7 of AMBA 5 CHI Architecture Specification (ARM IHI 0050E.c ID 092622)

⁵² The details are available in section 9.7.3 of AMBA 5 CHI Architecture Specification (ARM IHI 0050E.c ID 092622)

10 Power and Clock

4491

Ncore 3 clock and power are defined in terms of regions, domains, and sub domains.

Regions are defined as follows:

4494

- A power region represents a group of elements that run off a power supply that is driven by one source.
- A clock region represents a group of elements that are clocked by a single source. Clock regions are considered Asynchronous to each other.

4497

Domains are defined as follows:

4500

- A power domain represents a group of elements whose power can be turned on and off.
- A clock domain represents a group of elements whose clock can be turned on and off. A Clock domain may be defined at build time as synchronous or asynchronous with other clock domains within the clock region.

Sub Domains are defined as follows:

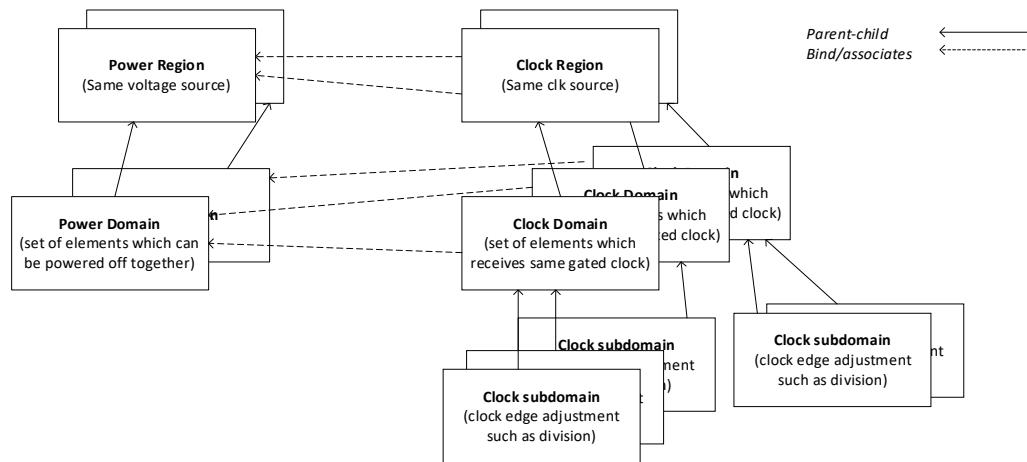
4503

4506

- There are no power sub domains.
- A clock sub domain is a group of elements in a clock domain whose clocks can be turned on and off dynamically as a part of logic function such as clock divider. These are not supported in the current version of Ncore 3 i.e., it supports only one clock subdomain per clock domain, and it cannot be divided down.

4509

The parent child relationship of regions, domains and sub domains is shown in Figure 10-1. A Clock region is associated to a power region. A clock domain is associated to a power domain within the same parent child relationship.



4512

FIGURE 10-1 POWER AND CLOCK, PARENT CHILD RELATIONSHIP

10.1 Synchronization

Synchronizing logic is inserted at every asynchronous crossing between two clock regions. As clock domains can be defined as synchronous or asynchronous, synchronizing logic is only inserted if two clock domains are defined as asynchronous.

Synchronizing logic may include any one or combination of the following:

- Multiple flopping of a single bit signal
 - Request Acknowledgment handshake protocol
 - Synchronizing FIFOs using gray counters

10.2 Power Gating

Ncore 3 does not support power gating. It supports only a single Power domain. It does not provide a unified power format (UPF) file that describes level shifters and clamping cells. A user may support multiple power domains by defining UPF file by themselves.

10.3 Clock Gating

Ncore 3 supports two levels of clock gating.

4527 First level of clock gating is done at the flop level. These clock gates are expected to be inserted by the synthesis tool. It is recommended to gate all collection of flops which can be grouped into three or more. RTL is expected to provide enable pins on these flops to achieve this. First level of clock gating is configurable as the user may decide not to enable the option during synthesis

4530

Second level of clock gating is at per Ncore unit basis. This is a single clock gate instantiated within each Ncore unit, It gates the whole Ncore unit except external interfaces and synchronizers. It is enabled when the Ncore unit is idle and does not have any transactions pending within itself. Second level clock gating is configurable via build time parameters as specified in the parameter specification.

Starting from Ncore 3.7, the SRAM clock gater is no longer as an option. With that, “useMemoryGating”

4536

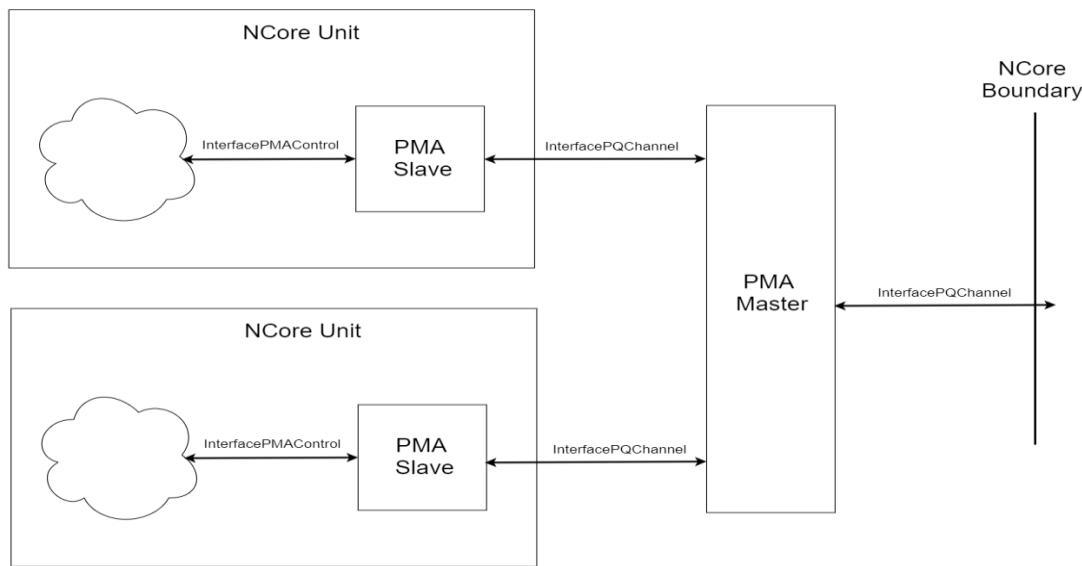
TACHL parameter will be defaulted to “0” for all Ncore units.

10.4 Q channel

The top-level system view with Q channel support is shown in Figure 10-2. Note that the view is only for a single clock domain implementation. In the case of multi clock domain implementation there will be one PMA master / Q channel interface per domain.

Q channel in Ncore can be used to provide additional clock gating capability where the clock gate exists in users’ logic and is not implemented by Ncore, which is enabled as “external” gating option in Maestro GUI. When this capability is used, two synchronous domains must be created, one that is always on and another that can be dynamically clock gated with the help of a Q channel. This is required to make sure that the CSR network connected to Ncore is always on and does not cause CSR transactions to be lost. Q channel clock gating requires Software mechanism as described in Q channel clock gating sequence section.

Q channel in Ncore does not support auto-wakeup, i.e., in powered down state QACTIVE will not be asserted to initiate a wakeup request by power management unit (PMU). Note that Ncore does not implement a PMU, this is expected to be user logic. Ncore only implements PMA master and PMA slave.



4551

FIGURE 10-2 Q CHANNEL PMA TOP-LEVEL VIEW

4554

11 Security

11.1 Non-secure bit of transactions

4557 NCore 3 supports ARM trustzone model. In this model, the security attribute represents the NS bit, or non-secure bit. When the NS bit equals zero, the agent is performing a secure memory access, and

4560 when the NS bit equals one, the agent is performing a non-secure access. On ACE and ACE-lite agents, the NS bit is signaled on bit[1] of the AxPROT signal, the value of the NS bit is copied into the Security bit.

4563 To support the Trustzone model in general, the security attribute must be stored in address buffers and tag filter entries, and any address comparisons must include comparison of the security attribute as well. To avoid security model violations, any address comparison where the security attribute

4566 mismatches is mismatch.

There is an exception, NS bit is not checked for transactions targeting CSR and boot regions.

4569 Nevertheless, an additional access security check (see section 5.1) is ensuring that only trusted agents are allowed to access CSR. CSR access must be disabled for untrusted agents while at least one agent must be enabled in the system.

4572 The NS bit in a CHI transaction or AxPROT[1] in an ACE, ACE-Lite, and AXI transaction when set to 0 indicate that the transaction is secure. The Ncore 3 platform takes specific actions to ensure the security semantics are satisfied within the platform.

4575 What various units in Ncore 3 need to do for handling the NS bit is listed below when Trust- Zone is enabled. When TrustZone is disabled, the NS bit is ignored by Ncore 3.

When TrustZone is enabled in the Ncore 3 system, secure and non-secure accesses can never access the same data via hardware. Any aliasing is expected to be resolved by software.

4578 TABLE 11-1: TRUSTZONE IMPLEMENTATION IN EACH UNIT

Component	
AIU	<p>CMDs and UPDs:</p> <ul style="list-style-type: none"> The CHI AIUs pass on the NS bit on the CHI interface to NS bit in ConcertoCMDreq messages. The ACE, ACE-Lite, ACE5-Lite, and AXI AIUs pass on the AxPROT[1] bit to the NS bit in the Concerto CMDreq messages. <p>SNPs:</p> <ul style="list-style-type: none"> The CHI AIUs pass on the NS bit in the SNPreq message to the NS bit on the CHI snoop interface. The ACE AIU passes the NS bit in the SNPreq to AxPROT[1] bit on the ACE snoop interface.
DCE	<ul style="list-style-type: none"> NS bit is treated as the most significant address bit. It is also stored as the most significant tag bit in the directory. DCEs treat the NS bit as the most significant address bit for directory look-up. A tag match requires the NS bit match the most significant tag bit. DCE copies the NS bit from the CMDreq to the corresponding SNPreqs, if any
DMI	<p>Coherent accesses:</p> <ul style="list-style-type: none"> NS bit arrives via MRDs and RBR requests. (This came to DCE with CMDreq.)

	<ul style="list-style-type: none"> • NS bit is treated as the most significant addressbit. • NS bit is stored in the tag arrays of the SMC as the most significant address bit. • Successful tag match in SMC requires that the NS bit matches the most significant bit of the address tag. • NS bit value is sent on AxPROT[1] bit on AXI when a CMDreq is directly forwarded to the AXI. • Cast out from SMC: Most significant address bit in the address tag of the cache line is sent on AxPROT[1] bit on AXI. The address itself on AXI is the tag address with the most significant tag bit set to 0 (or stripped off, as needed). <p>Non-coherent accesses:</p> <ul style="list-style-type: none"> • NS bit arrives via CMDreqs. • Non-coherent data can be stored in SMC. • The NS bit is stored in tag arrays of the SMC as the most significant address bit. • Successful tag match in the SMC requires: <ul style="list-style-type: none"> – NS == 0, and most significant bit of the tag can be 0 or 1, or <ul style="list-style-type: none"> ▪ Note: Coherency aliasing – meaning accessing the same data coherently and non-coherently can be a software error. However, under aliasing, 2 tags can match when NS == 0, one with most significant bit 0 and 1, which were perhaps stored under coherent accesses. Under this condition, SMC chooses the cacheline with most significant address bit matching the NS bit (i.e. == 0) – NS == 1, and most significant bit of the tag matches the NS bit value (i.e. == 1).
DII	<ul style="list-style-type: none"> • NS bit arrives via CMDreqs. • NS bit is forwarded as AxPROT[1] on AXI.
Proxy Cache	<ul style="list-style-type: none"> • Coherent accesses: AxPROT[1] bit must match the most significant bit of the tag (NS bit is stored as the most significant addressbit). • Snoops: NS bit in SNPreq must match the most significant bit of the tag (NS bit is stored as the most significant addressbit). • Cast out from SMC: Most significant address bit in the address tag of the cache line is sent on AxPROT[1] bit on AXI. The address itself on AXI is the tag address with the most significant tag bit set to 0 (or stripped off, as needed). • Non-coherent accesses: Same behavior as SMC.

11.2 Non secure attribute of memory regions

4581

As discussed in section 5.4.6 Definition of a Memory Address Map, Agent interfaces for Ncore 3 implement address space decoding, transactions will be directed to a target for completion based on the aperture within the global address space.

4584

Each aperture is described by a set of 3 General Purpose Region Definition Registers, two registers are required to define the base address of a region. The third register, GPRARx, defines the region attributes.

4587

Each aperture may have a security property encoded in the NSX[1:0] field. NSX[0] is the non-secure attribute of the memory region while NSX[1] has been reserved for later use in Arm v9.0 to support REALM and ROOT security state.

4590

When the region is secure (NSX[0] is 0):

Only secure transactions (with the NS bit on the agent interface set to zero) shall be accepted. All non-secure transactions shall be terminated with an error response, the illegal access shall be reported by the error handling system within Ncore.

4593

When the region is unsecure NSX[0] is 1: All transactions will be accepted by the AIU.

The NSX[0] bit shall be initialized to "high" (= 1'b1) for the GPRS defining the address window mapping the SysDII and the BootRegion. This allows any transaction to be forwarded to these agents. An alternate implementation may chose to ignore the NS bit for these address spaces.

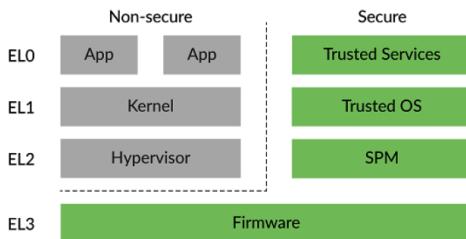
11.3 Background: New Security states

4599

TrustZone was introduced in Armv6 and provides the following two Security states:

- Secure state
- Non-secure state

The following diagram shows the two Security states in AArch64 with the software components that are typically found in each Security state:



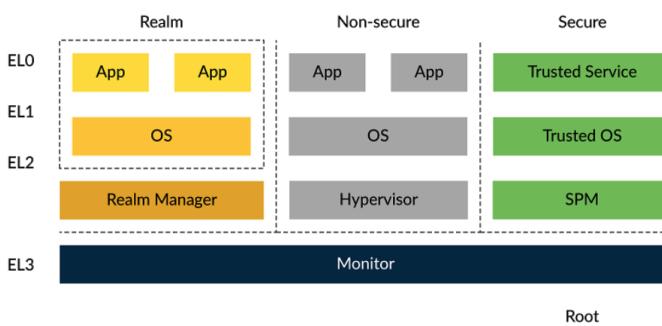
The architecture isolates software running in Secure state from software running in Non-secure state. This isolation enables a software architecture in which trusted code runs in Secure state and is protected from code in Non-secure state.

4605

Realm Mode Extensions is part of Armv9, RME builds on the Arm TrustZone technology, it extends the above model, and provides the following four Security states:

- Secure state
- Non-secure state
- Realm state
- Root state

We have reserved one bit in the NSX[1:0] field to support this feature in the future without having to move other register bits around. The following diagram shows the Security states in an RME-enabled PE, and how these Security states map to Exception levels:



12 Trace and Debug

4617

This section describes the trace and debug architecture for Ncore 3. Tracing can help localizing problems and errors in a NoC which may result from functional and performance anomalies. It requires taking a snapshot of traffic in a live system with temporal order to understand what is going on. A system in general will need to implement following functionality:

4620

- Label: Identify and select transactions based on a set criterion like address, target etc.
- Order: Identify temporal ordering of transactions, this requires a time stamp.
- Capture: Take a snapshot of the labeled transaction at a feasible location.
- Aggregate and access: Accumulate all captured transactions at a central location and provide SW access.
- Analysis: Software is required to access the captured information and analyze it.

4623

This specification is specified with restrictions to minimize Maestro software changes and not to add any new wires to the network, this is more of an add on to current Ncore system which does have some limitations.

4626

12.1 Register offset

4632

Debug and trace registers described in this document are located at 0x900 offset within each Ncore unit.

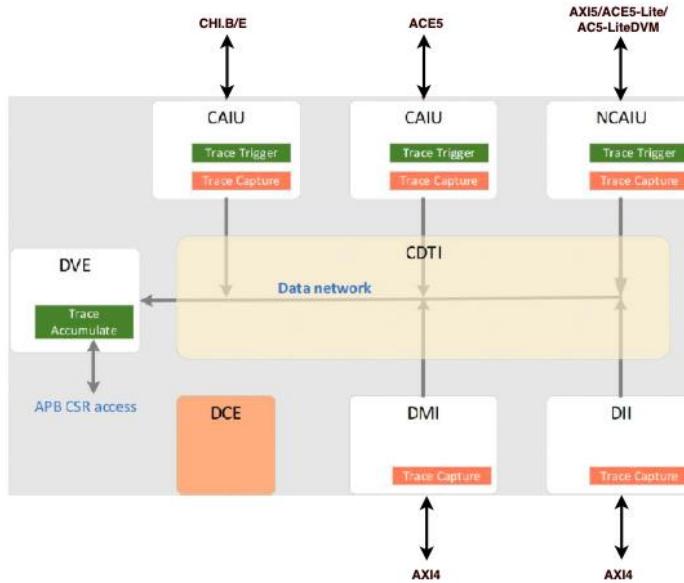
4635

A top-level overview of the system with trace and debug capability is shown in Figure 12-1. Existing data network is used to transport trace information. The Trace trigger block is present in all the AIUs. The capture block is present in all AIUs, DMIs and DIs. DCE and DVE do not participate in Trace capture.

4638

Note that DCE does not connect to the data network. Trace information from other units can be used to post process and build DCE and DVE trace. The trace trigger and capture blocks together fill in the functionality of label, order, and capture. Trace accumulate block is centrally located in DVE; it can be accessed via CSRs. It fills in the functionality of aggregate and access, note that it also participates in ordering transactions. The Analysis functionality falls within the software domain and is not specified in this document for now.

4641



4644

FIGURE 12-1 TRACE AND DEBUG OVERVIEW

12.2.1 Trace Trigger

4647

The trace trigger block is responsible for identifying transactions to be captured and marking them. Ncore protocol has a “Trace Me” field in its messages. Ncore 3 units shall propagate this trace signaling appropriately in all derived messages originating from a transaction that is marked to be traced (note that SysReq and SysRsp are not traced and will have their trace me field tied to zero). Furthermore, the trace signal shall be propagated on interfaces that support trace signaling based on the specific requirements of the interface (It can be CHI-B/E, AXI5, ACE5/ACE5-Lite/ACE5-LiteDVM).

4650

There are two classifications of marking a transaction to be traced.

4653

1. Master initiated trace, this applies to CHI.B/E, AXI5, ACE5/ACE5-Lite/ACE5-LiteDVM interfaces, which have trace signal capability on the interface.
2. Ncore 3 initiated trace, this applies to all AIUs in an Ncore, here an Ncore 3 provides CSRs which can be configured to mark desired transactions as trace transactions.

12.2.1.1 Master Initiated Trace

4659

CHI.B/E, AXI5, ACE5/ACE5-Lite/ACE5-LiteDVM interfaces have trace signaling capability, the master can identify transactions that are to be traced by appropriate interface signaling. Ncore 3 shall honor this signaling and meet the interface requirements. In this case, the more conservative approach must be

4662 taken where all trace related signals are added by default. It is expected that the end customers tie off the corresponding input signals if they decided to turn this feature off during the SoC level integration.

12.2.1.2 Ncore Initiated Trace

4665 All AIUs in the Ncore system including those that support trace signaling shall have the capability to initiate transaction tracing using internal CSRs. An incoming transaction on the native interface is compared with the trace CSR settings, if there is a match the transaction is marked to be traced.

4668 Multiple number of CSR sets can be present as specified at build time by the parameter nTraceRegisters. Different trace options are described below, in a single set of register all the options below can be enabled together, they are checked with an AND option i.e. that is all enabled options should match the incoming transaction. Between register sets it is an OR operation.

- **Trace Signal:** Trace transactions that are marked by the native interface, if trace signaling capability is available on the Native interface.
- **Address Range:** Trace transactions that match the specified address range. One address range can be specified per register set.
- **Op Code:** Trace transactions that match the specified Op codes. Up to 4 op codes can be specified at a time per register set.
- **Memory Attribute:** Trace transactions that match the specified memory attributes on the native interface. This is MemAttr for CHI and AxCache for AXI/ACE/ACE-Lite/ACE5-Lite. One memory attribute can be specified per register set.
- **User Bits:** Trace transactions that match the specified user bits on the native interface. One user bit value can be specified per register set.
- **Target Type:** Trace transactions that match the specified target type. The target type is specified using HUT and HUI. In the case of DII, HUI indicates DII NunitID and in the case of DMI, HUI indicates MIG number. One target type can be specified per register set.

4686

12.2.1.3 Trace Control Register (xTCTRLR)

Bits	Name	Access	Reset	Description
0	Trace Signal	R/W	0x1	Trace using the native interface trace signaling (only present if the Native interface supports trace else it is reserved)
1	Address Range	R/W	0x0	Trace if there is a match on the address range specified
2	Op code	R/W	0x0	Trace if there is a match on the op codes specified. (Does not apply to AXI NCAIU, must be reserved in the case)
3	Memory attribute	R/W	0x0	Trace if there is a match on the memory attribute specified
4	User bits	R/W	0x0	Trace if there is a match on the user bits specified (Reserved if user bits do not exist in the configuration)
5	Target type	R/W	0x0	Trace if there is a match on the target type
6	HUT	R/W	0x0	Specifies target type DMI or DII
11:7	HUI	R/W	0x0	Specifies the HUI (NunitID for DII and MIG number of DMI)
17:12	Reserved	RO	0x0	

Bits	Name	Access	Reset	Description
23:18	Size	R/W	0x0	Address range size, this field has a constraint where the region's Size, which is calculated as (Size of IG) * 2^(Size +12), should be equal or less than 2^52.
31:24	Memory Attribute	R/W	0x0	Specifies the memory attribute: CHI: bits 31:28 are MemAttr field. bits 27: 24 are reserved. AXI/ACE/ACE-Lite/ACE5-Lite: Bits 31:28 are AxCache field. Bits 27:26 are for AR and AW respectively, if both are set match is done on both AR and AW. Bits 25:24 are reserved

4689

12.2.1.4 Trace Base Address Low Register (xTBALR)

Bits	Name	Access	Reset	Description
31:0	Base address LO	R/W	0x0	Lower order bits 43:12 of the base address of the region

4692

12.2.1.5 Trace Base Address High Register (xTBAHR)

Bits	Name	Access	Reset	Description
7:0	Base address Hi	R/W	0x0	Higher order bits 51:44 of the base address of the region
31:8	Reserved			

4695

12.2.1.6 Trace Op Code Register (xTOPCR0)

Bits	Name	Access	Reset	Description
14:0	Op code 1	R/W	0x0	Op code number 1 (mapping defined based on Native interface, MSB unused bits are RO reserved) CHI: CHI opcode field ACE:{ATOP, DOMAIN, SNOOP} AXI: Not applicable
15	Valid 1	R/W	0x0	Valid bit for op code 1
30:16	Op code 2	R/W	0x0	Op code number 2 (mapping defined based on Native interface, MSB unused bits are RO reserved) CHI: CHI opcode field ACE:{ATOP, DOMAIN, SNOOP} AXI: Not applicable
31	Valid 2	R/W	0x0	Valid bit for op code 2

4698

12.2.1.7 Trace Op Code Register (xTOPCR1)

Bits	Name	Access	Reset	Description
14:0	Op code 3	R/W	0x0	Op code number 3 (mapping defined based on Native interface, MSB unused bits are RO reserved)

Bits	Name	Access	Reset	Description
				CHI: CHI opcode field ACE:{ATOP, DOMAIN, SNOOP} AXI: Not applicable
15	Valid 3	R/W	0x0	Valid bit for op code 3
30:16	Op code 4	R/W	0x0	Op code number 4 (mapping defined based on Native interface, MSB unused bits are RO reserved) CHI: CHI opcode field ACE:{ATOP, DOMAIN, SNOOP} AXI: Not applicable
31	Valid 4	R/W	0x0	Valid bit for op code 4

4701

12.2.1.8 Trace User Bits Register (xTUBR)

Bits	Name	Access	Reset	Description
31:0	User bits	R/W	0x0	Configured number of user bits rest of the field is reserved

4704

12.2.1.9 Trace User Bits Mask Register (xTUBMR)

Bits	Name	Access	Reset	Description
31:0	User bits mask	R/W	0x0	User bits mask register, set 1 for bits that need to be used for comparison.

4707

12.2.2 Trace Capture

All AIUs, DMIs and DIs shall support trace capturing capability. The block snoops SMI interface and captures messages that have the TraceMe field set. It captures non-data request, response and data messages (this includes all NDP header fields that are of non-zero width and NDP payload); actual data within the data message is not captured. Which SMI ports are to be snooped and captured is configurable via CSR settings. Multiple SMI ports can be snooped and captured simultaneously. The capture block has a capture buffer that is sized based on the parameter nUnitTraceBufSize, this parameter specifies the number of 64-byte entries in the buffer. The captured data packed into DTWs, once enough data is captured to build a single DTW, it is sent out on the SMI data network to the DVE in the system. If enough data is not accumulated to build a single DTW then a DTW with at-least a single concerto message and padding must be sent out once a timeout is reached (the timeout value is implementation defined per example 12bit counter). If the capture buffer is full then no more messages are captured until the buffer drains to accommodate at least one more DTW.

The DTW data format example is shown in Figure 12-2. The example is for a 128-bit bus width. The packet always starts with a 32-bit free running counter time stamp, followed by the captured concerto message. As shown multiple full concerto messages can be packed in a single a DTW. The DTW may end with padding of 0s if a full message cannot be packed into the DTW.

4722

4725 The capture block will give out two events. These events indicate SMI messages that were dropped and captured in a clock cycle respectively. As there can be up to 8 SMI messages that are dropped or captured, these event maybe 3 bits wide each.

4728 Ncore 3.6 supports an additional Non-Data network Ndn3. This network was added to improve performance for mixed read/write traffic scenario. To support trace capture on this new network, two additional control bits have been added for the CaptureControl Register.

4731

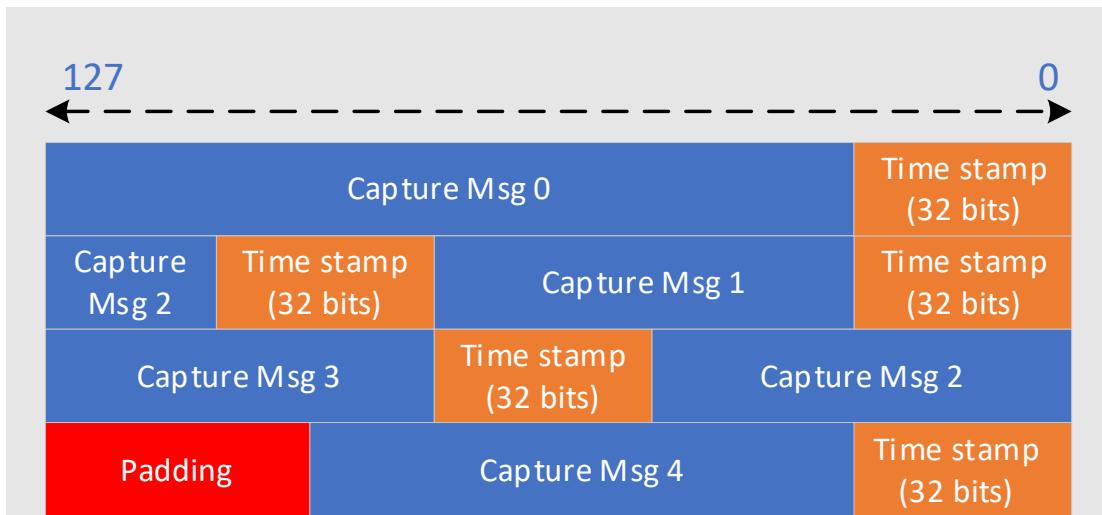


FIGURE 12-2 TRACE DTW DATA BUILD FORMAT

4734 The DtwRsp cm_status field is used to synchronize the Ncore unit local time stamp counter with the DVE time stamp counter. This filed is as described inTable 12-1.

TABLE 12-1: DTWRSP CM_STATUS DESCRIPTION

Field	Bits	Name	Description
cm_status	7	Signe	Positive (0) or negative (1)
	6:0	Value	Value by which the counter needs to be adjusted, this maps to counter bits [10:4] of the local counter, bits [3:0] are zero.

4737

4740 The general concept is to have a feedback loop with a small correction and programmable increment, as shown in Figure 12-3 master timeout stamp counter (MTSP) is compared with the unit timeout stamp counter (UTSC). The resultant error is multiplied with a gain and the UTSC increment value is updated accordingly.

4743

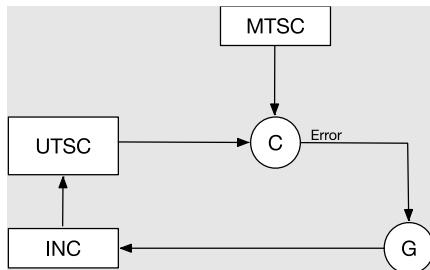


FIGURE 12-3 COUNTER SYNC FEEDBACK LOOP

C in the comparator of MTSC (counter in DVE) and UTSC (the local counter); comparison happens in DVE and error is sent back in DtwDbgRsp. G is the gain factor which is multiplied with the error and is used to correct INC (increment value of UTSC)

In this implementation INC is a register of 12 bits (4 bits of integer and 8 bits of fraction). This value initially represents the clock frequency difference between DVE and the Ncore unit, it gets updated based on the feedback error. Example values are shown in Table 12-2. The error is represented by 8 bits in signed magnitude format where bit 8 is the sign and lower 7 bits is magnitude within DtwDbgRsp. The 7 magnitude bits are multiplied with the 4-bit gain from CSRs to give an 11-bit number. MSB 8-bits of this 11-bit number are treated as fractional value that is either added or subtracted to the INC value based on the sign of the correction.

4755

TABLE 12-2: INCREMENT VALUE EXAMPLES

Clock ratio with DVE	Value in INC register
2	{4'b0010, 8'b0000_0000}
1	{4'b0001, 8'b0000_0000}
0.5	{4'b0000, 8'b1000_0000}
0.25	{4'b0000, 8'b0100_0000}
0.33	{4'b0000, 8'b1100_0000}

12.2.2.1 Capture Control Register (xCCTRLR)

4758

Bits	Name	Access	Scope	Reset	Description
0	Ndn0 SMI TX	R/W	All	0x0	Ndn0 SMI TX snoop and capture enable
1	Ndn0 SMI RX	R/W	All	0x0	Ndn0 SMI RX snoop and capture enable
2	Ndn1 SMI TX	R/W	All	0x0	Ndn1 SMI TX snoop and capture enable
3	Ndn1 SMI RX	R/W	All	0x0	Ndn1 SMI RX snoop and capture enable
4	Ndn2 SMI TX	R/W	All	0x0	Ndn2 SMI Tx snoop and capture enable
5	Ndn2 SMI RX	R/W	All	0x0	Ndn2 SMI Rx snoop and capture enable
6	Dn0 SMI TX	R/W	All	0x0	Dn0 SMI Tx snoop and capture enable
7	Dn0 SMI RX	R/W	All	0x0	Dn0 SMI Rx snoop and capture enable
8	Ndn3 SMI TX	R/W	All	0x0	Ndn3 SMI TX snoop and capture enable
9	Ndn3 SMI RX	R/W	All	0x0	Ndn3 SMI RX snoop and capture enable
15:10	Reserved	RO	All	0x0	
19:16	gain value	R/W	All	0x2	4-bit gain value
31:20	Inc value	R/W	All	0x100	Time stamp counter increment value: • top 4 bits are integer



12.2.3 Trace Accumulate

4761

This block is present only in DVE and the main functionality is to accumulate incoming trace DTWs from different Ncore capture units. The capture buffer is sized based on the parameter nMainTraceBufSize. Each entry in the buffer is organized as shown in Figure 12-4. It is a 72-byte entry with 64-byte payload (DtwReq data received from the capture block).

4764

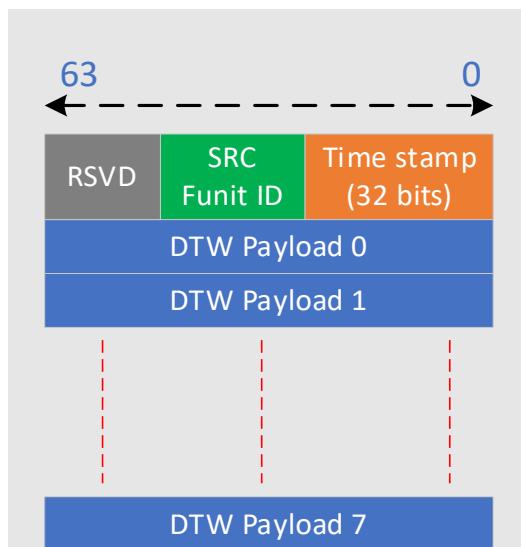


FIGURE 12-4 TRACE FORMAT

4767

The time stamp here is the local free running counter at DVE. This counter is used to synchronize other Ncore unit counters. This is done by taking the first-time stamp from the received DtwReq and comparing it with bits [31:4] of the local counter, if the received time stamp value is bigger, then the cm status bit 7 of the DtwRsp is set to 1 else set to 0. Bits [10:4] of the local counter are placed into the cm status bits [6:0]. If the counter values match, then the cm status bits [6:0] are set to zeros.

4770

The trace buffer shall be accessible via CSRs.

4773

The accumulate block will give out an event that indicates DTW messages that are dropped per clock cycle.

12.2.3.1 Trace Accumulate Status & Control Register (xTASCR)

4776

Bits	Name	Access	Reset	Description
0	Buffer empty	RO	0x1	Set when all the entries within the buffer are read and the buffer is empty
1	Buffer full	RO	0x0	Set when the buffer is full.
2	Circular buffer	R/W	0x0	When set, local buffer acts as a circular buffer, older messages are dropped once the buffer is full. When not set new messages are dropped when the buffer is full

3	Buffer clear	WSC	0x0	Write 1 to clear the complete buffer
4	Buffer read	WSC	0x0	Write one to trigger a read
31:5	Reserved	RO	0x0	

12.2.3.2 Trace Accumulate data header Register (xTADHR)

4779

Bits	Name	Access	Reset	Description
7:0	Funit ID	RO	0x0	Funit ID of the trace capture Ncore unit
30:8	Reserved	RO	0x0	
31	Valid	RSC	0x0	This is set once read data is valid, self clears on read

12.2.3.3 Trace Accumulate data Time stamp Register (xTADTSR)

Bits	Name	Access	Reset	Description
31:0	Time stamp	RO	0x0	Time stamp value from DVE free running counter

4782

12.2.3.4 Trace Accumulate data (0-15) Register (xTAD0R)

4785

These are 16 registers, where register 0 maps to data [31:0] and so on so forth.

Bits	Name	Access	Reset	Description
31:0	Capture data	RO	0x0	Capture data

12.3 Debug and BIST disable pin

4788

Resiliency requirements require that Ncore IP provide a pin that can disable enablement of BIST and debug & trace feature via CSRs. The user of the Ncore IP may decide to use this pin as an Effuse, pin on the chip or route it to a secure register.

4791

This pin “<prefix>_en_debug_bist” must be present only when resiliency is enabled via the resiliency enable parameter.

4794

Internal to Ncore the pin must be routed to all CAIUs, NACIUs, DMIs, DIs and FSC. Note that this pin is not propagated to DCE.

12.4 Debug APB port

4797

To enable debug of a hung Ncore 3 system a slave APB port must be added to the CSR network that can access all the Ncore CSRs. At top level this port signals must be “<prefix>_debug_apb_<rest of the signal name>”.

4800

Following APB port restrictions apply

4803

- Fixed data bus width 32 bits
- Fixed address bus width of 20 bits
- Fixed access size of 4 bytes
- All access are 4 byte aligned.

4806 This port is expected to be used for debug only, if same register is accessed concurrently via this debug APB port and the internal Ncore CSR accesses then the effect on the CSR is undefined. Ncore 3 does not guarantee any ordering between the two accesses.

12.4.1 APB4 PPORT Usage Clarifications

4809

Currently APB4 includes the protection encoding field PPROT[2:0].

bit [0] :

4812 1 = privileged access

0 = normal access

bit [1] :

4815 1 = non-secure access

0 = secure access

bit [2] :

4818 1 = instruction access

0 = data access

In order to access Ncore secured registers, PPROT[1] must be driven low at the SoC level.
4821 PPROT[0] is used at the SoC level to distinguish privileged access. In an SoC based on ARM architecture, applications are considered as EL0 level and their accesses are treated as unprivileged, thus the APB accesses associated with EL0 level applications should have a zero for PPROT[0]. In general, there are four exception level
4824 as the following:

EL0: Applications

EL1: OS kernel and associated functions

4827 EL2: Hypervisor

EL3: Secure monitor

4830 Any access associated with an application at EL1 and above is considered as a privileged access. And it should be distinguishable with the value of PPROT[0], which implies it should be 1'b1 for those accesses.

13 Performance Monitoring

4833

This chapter describes the performance counter architecture for Ncore.

4836 A performance counter unit must be implemented in each Ncore unit i.e. AIUs, DCEs, DMIs, DIs and DVE. This document goes over the architecture details and parameters of this unit and different events that are reported. The performance counter unit is not an optional unit and must always be present.

13.1 Parameters

4839

4842 Two unit level parameters are introduced: nPerfCounters and nLatencyCounters. They indicate for each type of counter the number to implement per Ncore 3 unit. See the parameter specification for more details on these parameters.

13.2 Detailed Description

4845

4848 The performance counter unit can track and report up to 31 events. The Ncore unit instantiating the performance unit specifies the events. These events may be single bit or multi bit events and are specified in 13.4 section. The performance counter unit can be configured to implement either 4 or 8 counters.

4851 Each counter is implemented as a 64 bit counter that is capable of counting up to 2 events at a time with following counter modes.

1. **Normal count:** In this mode the counter counts both the events together, if both the events are asserted then it is counted as two, if one event is asserted then it is counted as one
2. **AND count:** In this mode the counter counts one if both the events are asserted.
3. **XOR count:** In this mode the counter counts one only if one event is asserted and the other is de asserted.
4. **Instantaneous count:** In this mode the counter provides the instantaneous value of the multi bit event as is.
5. **32-bit count:** In this mode the 64 bit counter acts as two 32 bit counters for two separate events

The counter reports count via 2 registers one is a 32-bit count register that reports lower 32 bits and another configurable register which supports

4863 1. Capturing the upper 32 bits of the count

2. Used as an accumulation register for IIR filter

3. Use as max/saturation value for accumulation events

4866 4. Use as 32 bit counter for second event

Both count registers freeze when an overflow is detected at either of the two registers, with the

4869 exception when they are configured to work in tandem as a 64 bit counter.

13.3 Register Definition

Different registers supported by the performance counter unit are described below. A set of registers

4872 exist per counter configuration i.e. each Ncore unit can either have 4 or 8 set of registers. Note that xMCNTCR and xLCNTCR is only one per Ncore unit.

13.3.1 Counter Value Register (xCNTVR)

4875

Bits	Name	Access	Reset	Description
31:0	Count value	RO	0x0	Count value lower bits 31:0, freeze at overflow.

13.3.2 Counter Saturation Register (xCNTSR)

4878

Bits	Name	Access	Reset	Description
31:0	Count saturation value	RO	0x0	Can be configured as follows (freeze at overflow): <ol style="list-style-type: none"> Capture upper count value of 63:31 Use as IIR filter bits Use as max/saturation value for accumulation events Use as 32-bit counter, for count event second

13.3.3 Counter Control Register (xCNTCR)

4881

Bits	Name	Access	Reset	Description
0	Count Enable	R/W	0x0	Write one to enable counting, this may be set by the “Master Count Enable” signal from DVE or can be set or reset by “Local Count Enable”
1	Count Clear	WSC	0x0	Write one to clear the counter (both CNTVR and CNTSR)
2	Interrupt Enable	R/W	0x0	Write one to enable rollover or overflow interrupt (gets ORed with correctable error interrupt)
3	Rollover/Overflow status	RO	0x0	One indicates overflow, sticky bit clears by clearing the counter. (When either xCNTVR or xCNTSR overflow, with exceptions as specified above)
6:4	Counter control	R/W	0x0	000 – Normal count 001 – AND count

Bits	Name	Access	Reset	Description
				010 – XOR count 011 – Instantaneous count (used for multi bit events like Active OTT entries) 100 – use as 32-bit counter (count event first) 100 to 111 – reserved
9:7	SSR count	R/W	0x0	000 – Clear CNTSR (value of CNTSR is always zero) 001 – Capture upper 63:31 count in CNTSR 010 – use CNTSR as IIR filter (currently used only for active TT count) 011 – use CNTSR as max/saturation value (currently used only for CHI AIU interleave count) 100 – use as 32-bit counter (count event second) 101 to 111 reserved
12:10	Filter select	R/W	0x0	Low pass filter coefficients (IIR filter) 000 – 0 001 – ½ 010 – ¼ 011 – 1/8 100 – 1/16 101 – 1/32 110 – 1/64 111 – 1/128
15:13	Minimum stall period	R/W	0x0	Value is 2^{\wedge} (minimum stall period) clock cycles valid range is 0 to 7
16:21	Count event second	R/W	0x0	Select the second count event (must be different from Count event first), value of zero is not valid, if zero no second event is selected.
22:23	Reserved			
24:29	Count event first	R/W	0x0	Select the first count event, value of zero is not valid, if zero no event is selected.
31:30	Reserved			

13.3.4 BW Counter Filter Register (xBCNTFR)

4884

Bits	Name	Access	Reset	Description
19:0	Filter value	R/W	0x0	Value of user bits or Funit ID (as selected by filter select) to be filtered on. Must be LSB aligned
29:20	Reserved			
30	Filter select	R/W	0x0	Set to filter BW counting on Funit ID, else filter on user bits. This is valid only if Filter enable is set
31	Filter enable	R/W	0x0	Set to enable BW counting filtering else disabled

13.4 Performance events

4887

13.4.1 CAIU Performance events

Event #	Width	Name	Description
1	1	SMI 0 Tx Stall event	Counts every cycle when valid is set and ready is low
2	1	SMI 1 Tx Stall event	Counts every cycle when valid is set and ready is low
3	1	SMI 2 Tx Stall event	Counts every cycle when valid is set and ready is low
4		Reserved	

Event #	Width	Name	Description
5	1	SMI 0 Rx Stall event	Counts every cycle when valid is set and ready is low
6	1	SMI 1 Rx Stall event	Counts every cycle when valid is set and ready is low
7	1	SMI 2 Rx Stall event	Counts every cycle when valid is set and ready is low
8		Reserved	
9	1	ACE AW stall event	Counts every cycle when valid is set and ready is low (Does not apply to CHI AIU)
10	1	ACE W stall event	Counts every cycle when valid is set and ready is low (Does not apply to CHI AIU)
11	1	ACE B stall event	Counts every cycle when valid is set and ready is low (Does not apply to CHI AIU)
12	1	ACE AR stall event	Counts every cycle when valid is set and ready is low (Does not apply to CHI AIU)
13	1	ACE R stall event	Counts every cycle when valid is set and ready is low (Does not apply to CHI AIU)
14	1	ACE AC stall event	Counts every cycle when valid is set and ready is low (Does not apply to CHI AIU)
15	1	ACE CD stall event	Counts every cycle when valid is set and ready is low (Does not apply to CHI AIU)
16	1	ACE CR stall event	Counts every cycle when valid is set and ready is low (Does not apply to CHI AIU)
17	1	CmdReq WR event	Count all write commands that are associated with data, refer CCMP for all related commands.
18	1	CmdReq RD event	Count all read commands that are associated with data, refer CCMP for all related commands.
19	1	SnpRsp event	Count all snoop responses that trigger data transfer read or write.
20	8	Active OTT entries	Number of active OTT entries
21		Reserved	
22	3	Captured SMI packets	Number of SMI packets Captured
23	3	Dropped SMI packets	Number of SMI packets dropped
24	1	Address Collisions	Count number of address collisions on incoming transactions
25	3	Interleaved Data	Count max number of active interleaved data transactions
26	1	Agent event counter	Counts number of events triggered by the native agent
27	1	Noc evet counter	Counts number of events triggered by the Noc
28		Reserved	
29		Reserved	
30	1	Div 16 counter	Divide by 16 free running counter
31	1	Number of QoS starvations	Number of times QoS starvations occurred

Event #	Width	Name	Description
1	1	SMI 0 Tx Stall event	Counts every cycle when valid is set and ready is low
2	1	SMI 1 Tx Stall event	Counts every cycle when valid is set and ready is low
3	1	SMI 2 Tx Stall event	Counts every cycle when valid is set and ready is low
4		Reserved	
5	1	SMI 0 Rx Stall event	Counts every cycle when valid is set and ready is low
6	1	SMI 1 Rx Stall event	Counts every cycle when valid is set and ready is low
7	1	SMI 2 Rx Stall event	Counts every cycle when valid is set and ready is low
8		Reserved	
9	1	ACE-Lite/AXI AW stall event	Counts every cycle when valid is set and ready is low
10	1	ACE-Lite/AXI W stall event	Counts every cycle when valid is set and ready is low
11	1	ACE-Lite/AXI B stall event	Counts every cycle when valid is set and ready is low
12	1	ACE-Lite/AXI AR stall event	Counts every cycle when valid is set and ready is low
13	1	ACE-Lite/AXI R stall event	Counts every cycle when valid is set and ready is low
14	1	ACE-Lite AC stall event	Counts every cycle when valid is set and ready is low
15		Reserved	
16	1	ACE-Lite CR stall event	Counts every cycle when valid is set and ready is low
17	1	CmdReq WR event	Count all write commands that are associated with data, refer CCMP for all related commands.
18	1	CmdReq RD event	Count all read commands that are associated with data, refer CCMP for all related commands.
19	1	SnpRsp event	Count all snoop responses that trigger data transfer read or write
20	8	Active OTT entries	Number of active OTT entries
21		Reserved	
22	3	Captured SMI packets	Number of SMI packets Captured
23	3	Dropped SMI packets	Number of SMI packets dropped
24	1	Address Collisions	Count number of address collisions on incoming transactions
25		Reserved	
26	1	Agent event counter	Counts number of events triggered by the native agent
27	1	Noc evet counter	Counts number of events triggered by the Noc
28		Reserved	
29		Reserved	
30	1	Div 16 counter	Divide by 16 free running counter
31	1	Number of QoS starvations	Number of times QoS starvations occurred

4893

13.4.3 Proxy Performance events

Event #	Width	Name	Description
1	1	Cache read hit	
2	1	Cache write hit	
3	1	Cache snoop hit	
4	1	Cache eviction	
5	1	Cache no ways to allocate	

Event #	Width	Name	Description
6	1	Cache fill stall	
7	1	Cache read stall	
8	1	Cache write stall	
9	1	Cache replay	
10	1	Cache read miss	
11	1	Cache write miss	A write hit with an update is counted as a write miss
12	1	Cache snoop miss	
13		Reserved	
14		Reserved	
15		Reserved	
16		Reserved	
17		Reserved	
18		Reserved	
19		Reserved	
20		Reserved	
21		Reserved	
22		Reserved	
23		Reserved	
24		Reserved	
25		Reserved	
26		Reserved	
27		Reserved	
28		Reserved	
29		Reserved	
30		Reserved	
31		Reserved	

4896

13.4.4 DMI Performance events

Event #	Width	Name	Description
1	1	SMI 0 Tx Stall event	Counts every cycle when valid is set and ready is low
2	1	SMI 1 Tx Stall event	Counts every cycle when valid is set and ready is low
3	1	SMI 2 Tx Stall event	Counts every cycle when valid is set and ready is low
4	1	SMI 3 Tx Stall event	Counts every cycle when valid is set and ready is low
5	1	SMI 0 Rx Stall event	Counts every cycle when valid is set and ready is low
6	1	SMI 1 Rx Stall event	Counts every cycle when valid is set and ready is low
7	1	SMI 2 Rx Stall event	Counts every cycle when valid is set and ready is low
8	1	SMI 3 Rx Stall event	Counts every cycle when valid is set and ready is low
9	1	AXI AW stall event	Counts every cycle when valid is set and ready is low
10	1	AXI W stall event	Counts every cycle when valid is set and ready is low
11	1	AXI B stall event	Counts every cycle when valid is set and ready is low
12	1	AXI AR stall event	Counts every cycle when valid is set and ready is low
13	1	AXI R stall event	Counts every cycle when valid is set and ready is low

Event #	Width	Name	Description
14		Reserved	
15		Reserved	
16		Reserved	
17	1	DtwReq event	Count all DtwReqs that come into DMI
18	1	DtrReq event	Count all DtrReqs that are issued by DMI
19		Reserved	
20	8	Active WTT entries	Number of active WTT entries
21	8	Active RTT entries	Number of active RTT entries
22	4	Captured SMI packets	Number of SMI packets Captured
23	4	Dropped SMI packets	Number of SMI packets dropped
24	1	Address Collisions	Count number of address collisions on incoming transactions
25	1	Number of Merge events	Count number of DtwMergeMrds
26	1	Number of system visible Txn	Count number of system visible transactions
27		Reserved	
28		Reserved	
29		Reserved	
30	1	Div 16 counter	Divide by 16 free running counter
31	1	Number of QoS starvations	Number of times QoS starvations occurred

4899

13.4.5 SMC Performance events

Event #	Width	Name	Description
1	1	Cache read hit	
2	1	Cache write hit	
3	1	Cache CMO hit	Operations like cleanInvalidate etc
4	1	Cache eviction	
5	1	Cache no ways to allocate	
6	1	Cache fill stall	
7	1	Cache read stall	
8	1	Cache write stall	
9	1	Cache replay	
10	1	Cache read miss	
11	1	Cache write miss	
12	1	Cache CMO miss	
13		Reserved	
14		Reserved	
15		Reserved	
16		Reserved	
17		Reserved	
18		Reserved	
19		Reserved	
20		Reserved	
21		Reserved	

Event #	Width	Name	Description
22		Reserved	
23		Reserved	
24		Reserved	
25		Reserved	
26		Reserved	
27		Reserved	
28		Reserved	
29		Reserved	
30		Reserved	
31		Reserved	

4902 13.4.6 DII Performance events

Event #	Width	Name	Description
1	1	SMI 0 Tx Stall event	Counts every cycle when valid is set and ready is low
2	1	SMI 1 Tx Stall event	Counts every cycle when valid is set and ready is low
3	1	SMI 2 Tx Stall event	Counts every cycle when valid is set and ready is low
4		Reserved	
5	1	SMI 0 Rx Stall event	Counts every cycle when valid is set and ready is low
6	1	SMI 1 Rx Stall event	Counts every cycle when valid is set and ready is low
7	1	SMI 2 Rx Stall event	Counts every cycle when valid is set and ready is low
8		Reserved	
9	1	AXI AW stall event	Counts every cycle when valid is set and ready is low
10	1	AXI W stall event	Counts every cycle when valid is set and ready is low
11	1	AXI B stall event	Counts every cycle when valid is set and ready is low
12	1	AXI AR stall event	Counts every cycle when valid is set and ready is low
13	1	AXI R stall event	Counts every cycle when valid is set and ready is low
14		Reserved	
15		Reserved	
16		Reserved	
17	1	DtwReq event	Count all DtwReqs that come into DII
18	1	DtrReq event	Count all DtrReqs that are issued by DII
19		Reserved	
20	8	Active WTT entries	Number of active WTT entries
21	8	Active RTT entries	Number of active RTT entries
22	3	Captured SMI packets	Number of SMI packets Captured
23	3	Dropped SMI packets	Number of SMI packets dropped
24	1	Address Collisions	Count number of address collisions on incoming transactions
25		Reserved	
26		Reserved	
27		Reserved	
28		Reserved	
29		Reserved	

30	1	Div 16 counter	Divide by 16 free running counter
31		Reserved	

4905

13.4.6.1 DCE Performance events

Event #	Width	Name	Description
1	1	SMI 0 Tx Stall event	Counts every cycle when valid is set and ready is low
2	1	SMI 1 Tx Stall event	Counts every cycle when valid is set and ready is low
3	1	SMI 2 Tx Stall event	Counts every cycle when valid is set and ready is low
4		Reserved	
5	1	SMI 0 Rx Stall event	Counts every cycle when valid is set and ready is low
4	1	SMI 1 Rx Stall event	Counts every cycle when valid is set and ready is low
7	1	SMI 2 Rx Stall event	Counts every cycle when valid is set and ready is low
8		Reserved	
9		Reserved	
10		Reserved	
11		Reserved	
12		Reserved	
13		Reserved	
14		Reserved	
15		Reserved	
16		Reserved	
17		Reserved	
18		Reserved	
19		Reserved	
20	8	Active ATT entries	Number of active ATT entries
21		Reserved	
22		Reserved	
23		Reserved	
24	1	Address Collisions	Count number of address collisions on incoming transactions
25	1	SF hit	Snoop filter hit (either owner or sharer) count
26	1	SF miss	Snoop filter miss (neither owner nor sharer) count
27	1	SF recall	Snoop filter recall transaction count
28	1	Snoop rsp miss	Snoop response reports miss
29	1	Snoop rsp Owner transfer	Snoop response Ownership transfer
30	1	Div 16 counter	Divide by 16 free running counter
31	1	Number of QoS Starvations	Number of times QoS starvations occurred

4908

13.4.7 DVE Performance events

Event #	Width	Name	Description
1	1	SMI 0 Tx Stall event	Counts every cycle when valid is set and ready is low
2	1	SMI 1 Tx Stall event	Counts every cycle when valid is set and ready is low
3	1	SMI 2 Tx Stall event	Counts every cycle when valid is set and ready is low
4		Reserved	
5	1	SMI 0 Rx Stall event	Counts every cycle when valid is set and ready is low
4	1	SMI 1 Rx Stall event	Counts every cycle when valid is set and ready is low
7	1	SMI 2 Rx Stall event	Counts every cycle when valid is set and ready is low
8		Reserved	
9		Reserved	
10		Reserved	
11		Reserved	
12		Reserved	
13		Reserved	
14		Reserved	
15		Reserved	
16		Reserved	
17		Reserved	
18		Reserved	
19		Reserved	
20	8	Active STT entries	Number of active STT entries
21		Reserved	
22	1	Captured DtwDbgReq packets	Number of DtwDbg packets captured
23	1	Dropped DtwDbgReq packets	Number of DtwDbg packets dropped
24		Reserved	
25		Reserved	
26		Reserved	
27		Reserved	
28		Reserved	
29		Reserved	
30	1	Div 16 counter	Divide by 16 free running counter
31		Reserved	

4911

13.5 Master Trigger

4914

This acts as a single trigger to start/stop all performance counters in Ncore at approximately the same time. This is achieved by adding a Master count enable bit in DVE. When the bit is set it must be propagated to all Ncore units via a single wire. This signal is expected to be active high asynchronous signal, which is synchronized by the receiving Ncore unit. The Ncore unit will detect rising edge to start the counters and falling edge to stop the counters.

4917

It is expected that SW will set this control register bit then read it to verify that it is set, wait from some x amount of time, and then reset it.

4920

13.6 Bandwidth Counters

Ncore provides Bandwidth counters in AIUs, DMIs and DIIIs. These counters count in 64Byte data accuracy and at divided by 16 accuracies of the clock frequency. BW counting can be filtered based on FunitID or user bits, this can be configured in CSRs xBCNTFR and xBCNTMR

In AIUs they count following

- Read data bandwidth, this refers to data being read into the master/cache
- Write data bandwidth, this refers to data being written out of the master/cache, this may include evicted data.
- Snoop data bandwidth, this refers to data being moved out of the master/cache due to snoops

In DMIs/DIIIs the count following

- Read data bandwidth, this refers to data being read from DMI/DII. In the case of DMI the data maybe read from SMC if present.
- Write data bandwidth, this refers to data being written into DMI/DII. In the case of DMI the data maybe written into SMC if present.

BW counting is achieved by setting xCTCR0 as follows:

- **Counter control** to 3b100 i.e., use as 32 bit counter
- **SSR count** to 3b100 i.e., use as 32 bit counter
- **Count first event** to one of the following events depending on what is to be counted
 - CmdReq WR event: to count AIU write BW
 - CmdReq RD event: to count AIU read BW
 - SnpRsp event: to count Snoop BW
 - DtwReq event: to count DMI/DII write BW
 - DtrReq event: to count DMI/DII read BW
- **Count Second event** to divide by 16 clock cycle event

Once the counter is enabled following is reported

- xCNTSR: number of divide by 16 clock cycles
- xCNTVR: in the unit of data beats

The above information can be used to calculate the effective BW. The counter must be disabled before reading them to get correct BW.

Note that this will be approximate BW as all transactions that were counted may necessarily not be 64 bytes transactions and the time accuracy is divided by 16.

4953 13.7 Latency Histogram Counters

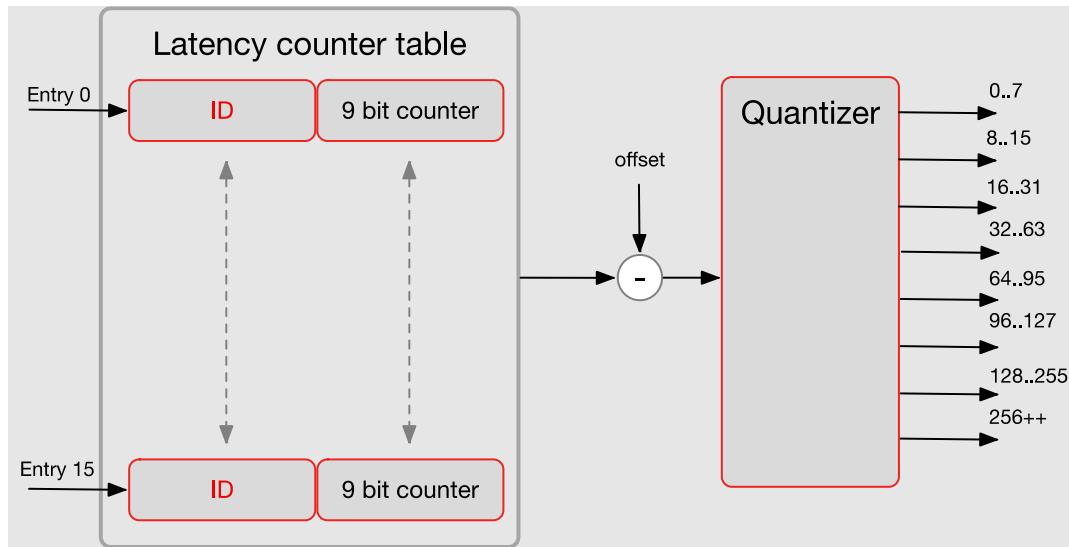
Ncore provides latency counters in AIUs, DMIs and DIIIs for either reads or writes. Latency is reported back as a binned histogram. It is an optional feature that is controlled via a unit level parameter as described in Parameters section. At any given time, it can be configured to report only one type of latency i.e., read latency or write latency. The latency reported at AIUs is from Ncore system preceptive i.e., it is reporting the complete lifetime of the transaction within Ncore. The latency reported at DMI/DII is more of a closer representation of latency seen at the Native AXI interface.

Read latency includes all transitions defined by CCMP/Native interface as a read transition that provides data to the requester. Write latency includes all transactions defined by CCMP/Native interface as a write transaction that provides data to be written at the slave. Stash transactions are not included.

4962 Logic for generating the latency histogram is implemented as separate block as shown in Figure 13-1. In AIUs when the selected type of transaction is allocated to the transaction table (OTT) it is also allocated to the latency counter table, whereas in the case of DMI/DII it is allocated when the transaction is ready to be issued on the Native interface. The ID represents the transaction table (OTT/WTT/RTT) ID and counter is a 9-bit counter. The counter is started as soon as the entry is allocated. If all entries within the 4965 latency counter table are taken, then any new qualified transaction just does not participate in the latency histogram.

4971 The counter increments every 2, 4, 8 or 16 clock cycle based on CSR configuration. If the counter hits its max value, then it stays saturated until deallocation and the saturated value is used for latency histogram binning.

4974 In the case of an AIU an entry in latency counter table is deallocated at approximately the same time the corresponding entry is deallocated from the transaction table. In the case of DMIs/DIIIs an entry in latency 4977 counter table is deallocated at approximately the same time corresponding response is received from the native interface. The deallocated entry counter value is then subtracted by the configured 8-bit offset, if the offset corrected value is negative then it is saturated downwards to zero. The quantizer takes the offset corrected value and increment appropriate histogram bin.



4980

FIGURE 13-1 LATENCY HISTOGRAM BLOCK

4983

To create a single histogram first 4 consecutive counter registers xCNTCR must be configured as follows

4986

- **Counter control** to 3b100 i.e., bit bin counter
- **SSR count** to 3b100 i.e., 32 bit bin counter
- **Count first event** is don't care in this case
- **Count Second event** is don't care in this case

4989

xLCNTCR must be configured as follows

4992

- **Latency pre scale** to desired pre scale value
- **Read/Write latency** to desired read or write latency to be counted
- **Latency bin offset** to desired offset value
- **Latency count enable** to enable latency counting

4995

xMCNTCR must be configured as follows

- **Local Count Clear** to 1b1 and clear the all local counters (this will clear all local counters other than the histogram counters)
- **Local Count Enable** to 1b1 and enable all local counters

4998

After elapsed number of transactions or time or set **Local Count Enable** to 1b0 to stop the counters

8 histogram bins can be read from the 4 consecutive counter registers:

- **xCNTVR0**: Bin 0

- 5001
 - ***xCNTSR0***: Bin 1
 - ***xCNTVR1***: Bin 2
 - ***xCNTSR1***: Bin 3
- 5004
 - ***xCNTVR2***: Bin 4
 - ***xCNTSR2***: Bin 5
 - ***xCNTVR3***: Bin 6
- 5007
 - ***xCNTSR3***: Bin 7

14 System Software Guidelines

The following sections discuss the various requirements for system software.

14.1 Reset and Initialization

Before processing any requests, each Ncore component must be transitioned into the operational state, which is achieved once the following requirements have been met:

- 5013 • The supply voltage has been raised to an operational level
- The clock source is generating a stable clock signal
- The clock frequency is less than or equal to the maximum frequency allowed for the given operational voltage level
- 5016 • The reset signal has been asserted and has been de-asserted after the required minimum number of cycles (16 cycles of the slowest clock in the system) in the case that one or more of the following conditions occurred:
 - 5019 ○ The supply voltage dropped below the logic or memory retention level
 - The clock source was not generating a stable clock signal
 - 5022 ○ The clock frequency was greater than the maximum frequency allowed for a given operational voltage level

NOTE: The reset is asynchronous assert and synchronous de-assert.

5025 Ncore components may be configured to have memories. These memories are initialized by an internal state machine on de-assertion of reset.

5028 Once all Ncore Components are in operational state, the boot/initialization processes described below needs to be followed.

14.1.1 Boot/Initialization

An agent connected to CAIU/NACIU may be designated as boot agent. This agent is expected to make 5031 the first request into the Ncore system. This request is expected to be non-coherent request. Boot-up sequence to be followed are:

- 5034 • Perform CSR access and go through the Ncore component discovery as described in Ncore Component Discovery
- Configure required memory and peripheral address spaces as described in Address space configuration
- 5037 • Configure error registers as needed to enable required error detection and reporting as described in Error Detection and Reporting configuration
- If preset, configure and enable all needed SMCs as described in SMC configuration
- 5040 • If preset, configure and enable all needed Proxy caches as described in Proxy cache configuration
- Transition CAIUs to Coherent state by the SYSCOREQ and SYSCOACK interface if present

- 5043 or Ncore CSRs to trigger the internal mechanism, this is described in CAIU Coherence
transition mechanism.
5046 If the Ncore system is configured with a BR then the above steps can be part of the boot code, in this case
BR can be the first access to load the boot code.

14.1.2 Ncore Component Discovery

5049 Ncore component discovery involves following steps at the designated CAIU/ NCAIU. All read & write
operations here are at the NRS base address.

- Read register at RP 0x0 and register address offset 0x0 i.e. at address bits [19:0] as zero; this will
read xIDR register of the AIU providing following information.
 - AIUs register page number (RPN)
 - Ncore register region identifier (NRRI), currently set to zero
 - Ncore unit ID, this uniquely identifies an Ncore unit within its type
- Read register GRBUNRRUCR at NRRI identified in the previous register, RP 0xFF and address
offset 0xFF8. This register will identify number of different Ncore components which include
AIUs, DCEs, DMIs, DIs and DVEs. RPs to Ncore component mapping is shown in NRS section
- Step through all Ncore component xIDR registers (register address offset 0x0) and xINFO
registers (register address offset 0xFFC) starting from RPN 0.

Note:

- 5061 1. registers access is restricted to address aligned, 8 byte non-coherent device access. Any other
access format will return an error.
- 5064 2. access to an undefined RPN will return an error.
3. Reserved registers within a valid RPN are treated as read as zero and write ignore.

14.1.3 Address space configuration

5067 All AIUs and DCEs in the Ncore system must be configured with the same peripheral and memory
address space configuration. This involves two main configuration steps as following:

- DMI interleaving configuration, this requires configuring following 2 registers⁵³
 - xAMIGR must be configured to select desired MIGS, by default MIGS0 is selected
 - xMIFSR must be configured to select desired interleaving function i.e., address bits used for DMI interleaving, by default option 0 is selected
- GPAS configuration, this requires configuring following 3 registers per address region
 - xGPRAR must be configured with attributes of the address region, these include
- Home unit type (HUT), this specifies type of memory. System memory is mapped to a DMI and peripheral memory is mapped to a DI.

⁵³ Applicable to both regular memory spaces and the boot space if it is configured

- 5076 • Home unit identifier (HUI), this specifies target DMI or DII. In the case of DII the Nunit ID must be specified and in the case of DMI MIG number within the selected MIGS in xAMIGR must be specified.
- 5079 • Size, this is specified as a binary number from 0 to 31 from which the region size is calculated as (size of IG) * 2^(size+12) bytes. Here size of IG is the number of DMIs within the selected MIG, it is always 1 for DII.
 - 5082 ○ xGPRBLR must be configured with lower order address bits 51:12 of the base address of the region
 - 5085 ○ xGPRBHR must be configured with higher order address bits of the base address of the region
- 5088 • ReadID/WriteID, this is applicable only to NCAIUs and specifies ordering override. When these bits are set individually or together respective read or write channel Same AXI-ID ordering is ignored when transactions are issued into the Ncore system by the AIU. AXI-ID ordering protocol at the Native interface is honored
- 5091 • Policy, this is applicable only to NCAUs and specifies the ordering policy followed by DMI/DII at the bottom of the Ncore. For details on the policies, refer to the section 4.14.5
- 5091 • If present, configure address translation registers <specify register name> in DMI/DII.

5094 14.1.4 Error Detection and Reporting configuration

Following steps must be followed to configure error detection and reporting for each Ncore unit/component

- 5097 • Enable uncorrectable error detection by setting the appropriate error detection enable bits in xUEDR register of all Ncore units
- 5100 • If desired enable uncorrectable error interrupts by setting the appropriate error interrupt enable bit in xUEIR register of all Ncore units
- 5103 • Configure the correctable error control register xCECR to enable correctable error detection, interrupt and update the threshold as needed
- 5103 • If desired timeout error threshold can be updated or disabled at xTOCR register of all Ncore units

14.1.5 Proxy cache configuration

5106 Following steps must be followed to configure and enable proxy cache

- 5109 • Read register XAIUPCISR to verify both tag and data RAM are initialized
- 5109 • Configure register XAIUPCTCR to enable the proxy cache in two steps
 - Enable cache look up by setting LookupEn
 - Enable cache allocation by setting AllocEn

14.1.6 SMC configuration

5112 Following steps must be followed to configure and enable SMC

5115

- Read register DMIUSMCISR to verify both tag and data RAM are initialized
- Configure register DMIUSMCAPR to specify desired cache allocation policy
- If the DMI was configured with scratchpad support, then as desired enable the scratchpad as described in Scratchpad configuration
- If the DMI was configured with way partitioning capability configure registers DMIUSMCWPCR x to setup way partitioning
- Configure register DMIUSMCTCR to enable the SMC in two steps:
 - Enable cache look up by setting LookupEn
 - Enable cache allocation by setting AllocEn

5118

5121

14.1.7 Scratchpad configuration

Following steps must be followed to configure and enable the scratchpad

5124

- Configure DMIUSMCSPBR0/1 with desired scratchpad base address
- Configure DMIUSMCPCR0 with desired number of ways minus 1 to be used as scratchpad. Maximum value is limited by the total number of ways configured in the cache
- Configure DMIUSMCPCR1 with scratchpad size. The size is to be specified in number of cachelines and must be an integer multiple of number of sets in the cache times the desired number of ways for scratchpad size minus 1
- Configure DMIUSMCPCR0 to enable scratchpad by setting ScPadEn

5127

5130

14.1.8 CAIU Coherence transition mechanism

There are two ways to transition a CAIU into coherent state.

5133

CHI CAIU can transition to coherent state via the SYSCOREQ and SYSCOACK protocol signaling as specified by ARM.

5136

CHI CAIU agent that does not have the SYSCO singling, ACE CAIU, Proxy cache NACIU and DVM capable NCAIU can transition to coherent state via the provided NCORE CSRs in the AIUs as defined in Table 14-1 and Table 14-2.

TABLE 14-1 : TRANSACTION ACTIVITY REGISTER (xTAR):

Bit	Name	Description	Access	Reset Value
0	TransActv	This bit is set when there is one or more active transactions inside the Unit.	Read Only	0x0
3:1	Rsvd	Reserved	Read Only	0x0
4	SysCoConnecting	1 indicates that SysCo is in the process of connecting.	Read Only	0x0
5	SysCoAttached	1 indicates that SysCo is Attached; 0 indicates it is detached.	Read Only	0x0
6	SysCoError	1 indicates Error was detected during previous or current SysCo event. This bit clears itself when the SysCo process triggers next time.	Read Only	0x0

31:7	Rsvd	Reserved	Read Only	0x0
------	------	----------	-----------	-----

5139

TABLE 14-2 : TRANSACTION CONTROL REGISTER (xTCR):

Bit	Name	Description	Access	Reset Value
0	RDisable	This controls whether new requests can be accepted inside AIU	Read Only	0x0
3:1	Rsvd	Reserved	Read Only	0x0
4	EventDisable	Setting this disables Event handling.	Read Only	0x0
5	SysCoDisable	Setting this disables SysCo.	Read Only	0x0
6	SysCoAttach	Writing 1 to this bit when the status register bit SysCoAttached is 0 starts an attach sequence. Writing 0 to this bit when the status register bit SysCoAttached is 1 starts a detach sequence.	Read Only	0x0

5142

Transition to attached state use the following steps:

- Read the xTAR register to confirm the current state of the AIU
- Set SysCoAttach in xTCR to start the transition of the AIU into coherent state
- Poll the xTAR register SysCoAttached field to confirm that the AIU is in the coherent state.

5145

Transition to the detached state using CSR must follow the following steps:

- Read the xTAR register to confirm the current state of the AIU
- Set SysCoAttach to '0' in xTCR to start the transition of the AIU into detached / Non-coherent state
- Poll the xTAR register SysCoAttached field to confirm that the AIU is in the detached/Non-coherent state.

5148

5151

14.1.9 Snoop enabling configuration

5154

Cache and DVM agents that can be snooped by each DCE and DVE respectively have to be configured correctly during initialization through xSER register as shown in Table 14-3 :

TABLE 14-3 : SNOOP ENABLE REGISTER (xSER)

Bit	Name	Description	Access	Reset
6:0	SnpsEnb	Snoop Enable bits for agents 0..31. If a bit is set for an agent, snoop messages are enabled for that agent; otherwise, disabled.	Read/Write	0x0
31:7	Rsvd	Reserved	Read-Only	0x0

5157

14.2 Q channel clock gating sequence

5160

The Q channel clock gating sequence is as follows:

1. Software must go through the processes of turning off all traffic to the Ncore components that are within the clock domain and are going to be clock gated. Steps included are:
 - a. Stop all coherent traffic at the native interface of the target Ncore components.
 - b. Flush and disable all caches above the native interface or within the target Ncore components.
 - c. Any CAIUs, Proxy cache and DMV capable NCAIUs must be transitioned to non-coherent/detached state either via SYSCOREQ/SYSCOACK interface signaling or via xTAR/XTCR registers.
 - d. Stop all at the native interface of the target Ncore components.
2. Trigger the CMU (Clock gating Management Unit) to send a Q channel request which includes the following:
 - a. REQn is asserted on the Q Channel Interface.
 - b. Ncore component will assert ACCEPTn and accept the request once it is not busy (no active transactions are pending in the Ncore component).

5175

The software or CMU is required to implement a timeout counter to cover cases where the Ncore component may not accept the power down request. In this case ACCEPTn will not be asserted, at timeout REQn must be de-asserted (Clock gating aborted) and that Ncore component stays in up state.

5178

In the Clock gated state the Ncore components will not block any transactions and have no special behavior. Depending on the system design on successful completion of Q channel request the Ncore subsystem clock can be turned off.

5181

The ACTIVE signal indicates if the block is busy and this signal can toggle at any time during normal operation.

5184

The bring back sequence is as follows:

1. Enable the clock.
2. De-assert REQn.
3. Go through the process of transitioning any CAIUs, Proxy cache, and DMV capable NCAIUs to coherent state.
4. Start normal traffic.

5190

Initial system power up with Ncore clock domains in state is not supported.

15 PPA

This section provides the Ncore 3.6 power, performance, area goals.

5193 15.1 Performance goals

Overall, Ncore 3 aims to sustain the maximum theoretical memory bandwidth with hardware coherency without preventing the agents to use their full cache and without limiting their message throughput.

The theoretical aggregate (simultaneous read plus write) bandwidth for a 256-bit wide ACE or CHI interface is 32 Bytes x 1,6Ghz x 2 = 102,4 GB/s.

- 5199 Ncore 3.6 shall sustain the max theoretical bandwidth for reads: 32 Bytes x 1,6Ghz = 51,2GB/s per AIU.
Ncore 3.6 shall sustain the max theoretical bandwidth for writes: 32 Bytes x 1,6Ghz = 51,2GB/s per AIU.
It does not sustain the aggregate bandwidth max theoretical bandwidth for a 256-bit wide interface.

- 5202 Ncore 3.6 shall sustain these goals while scaling the number of agents participating. The round trip latency is becoming higher with larger system or when using slower memory devices. To sustain the bandwidth the Ncore 3 units CAUI, IOAIU and DMI shall sustain a large number of inflight transactions:
- CAIU and IOAIU supports up to 128 outstanding transactions
 - DMI supports up to 128 outstanding reads and 64 outstanding writes

- 5208 Scenari for performance verification tests include memory stream tests. The simulation results shall match the results obtained high level modelling running the corresponding benchmarks. The memory bandwidth is the bottleneck, the SMI links or Concerto units do not limit the memory bandwidth.

- 5211 Other scenari stress the theoretical bandwidth:
- Agent throughput shall not be limited. It shall saturate its interface both for write data and read data channels
 - Cache utilization of agents shall not be limited by Ncore 3 Snoop Filter size, organization and policy

- 5217 Non coherent traffic performance shall also be optimized. Ncore 3.6 shall provide equivalent performance as FlexNoC for an AXI4 interface.

5223 15.2 Timing goals

The product shall support a system clock frequency up to 1.6 GHz with a SVT, LVT and ULVT mix of transistor gate lengths and worst PVT/ Parasitic corner in 7nm technology node.

5226 Nevertheless, the system Clock target Frequency is 1.3GHz in case of automotive project.

The CHI AIU shall support the option for an asynchronous interface.

5229 15.3 Slow SRAM

Please refer to CCP micro architecture specification on the specific mode parameter (enSRAMPipe) which enables SRAM pipe.

5232 Enabling this will add a cycle latency. The details are described in the micro architecture document. Associated parameters are described in the parameter's specification.

5235 In the case of DMI with SMC, this must be enabled only if enHalfSpeedDataSRAM is set. In the case of DMI this adds two cycles of latency and may affect bandwidth results in partial line access scenario.

16 Glossary

5238

The following terms have a specific meaning in this document.

Term	Definition
Arteris	- A NoC Company
AIU	- Agent Interface Unit
iAIU	- initiator AIU - request is started here
sAIU	- snooped AIU - a transaction may result in one or more AIUs being snooped as part of the coherence protocol
aTag	- Allocation Tag – associated with a memory location, stored in memory
NCore3	- A coherent NoC provided by Arteris with AMBA interfaces and built-in caches.
BR	- Boot Region
CAIU	- Coherent Agent Interface Unit
CDTI	- Control and Data Transport Interconnect
CMD	- Command Message
CSTI	- Control and Status Transport Interconnect
DCE	- Distributed Coherence Engine
DII	- Distributed IO Interface
DMI	- Distributed Memory Interface
DTR	- Data Read Message
DTW	- Data Write Message
DVE	- Distributed Virtual Memory Engine
GPAS	- General Purpose Address Space
MRD	- Memory Read Message
NCAIU	- Non-coherent Agent Interface Unit
NRS	- Ncore Register Space
RB	- Request Buffer
pTag	- Physical Address Tag or Physical Tag , a memory location is accessed, the Requester uses both the address of the location and the tag value that it believes is associated with the location
PoC	- The PoC (Point of [system] Coherency) is the point at which all blocks (for example, CPUs, DSPs, or DMA engines) which can access memory, are guaranteed for a particular address to see the same copy of a memory location. Typically, this will be the main external system memory.
PRD	- Product Requirement Document
SMC	- System Memory Cache
SNP	- Snoop Message
SF	- Snoop Filter
STR	- State Reply Message
TSR	- Technical Safety Requirement
UPD	- Update Message
VC	- Virtual Channel

17 Document References

17.1 Supported standards and specifications

- ⁵²⁴¹
- Arm CHI B⁵⁴/E⁵⁵
 - Arm AXI-4/5

⁵²⁴⁴

 - Arm v8.2A, v8.3A, v8.4A, v8.5, v9, v9.1
 - AMBA CHI Issue-B Specification
 - AMBA CHI Issue-E.c Specification

⁵²⁴⁷

17.2 Relevant documents and specifications

- ⁵²⁵⁰
- ARM document [dsu_trm_100453_0401_03_en](#)
 - Ncore 3.6 Architecture Parameter Specification
 - Arteris Symphony Concerto-C Rev. 0.994
 - [Ncore 3.6 Supplemental Architecture Specification 079](#)

⁵²⁵³

 - [Ncore 3.6 Functional Safety Architecture 055](#)
 - [Ncore 3.6 Connectivity Architecture Specification 092](#)
 - [Ncore 3.6 Error Architecture Specification 057](#)

⁵²⁵⁶

 - [Ncore 3.6 Syscmd Architecture Specification 060](#)
 - Ncore 3.6 Exclusive monitors rev 0.53

⁵²⁵⁹

⁵⁴ ARM CHI 5 CHI Architecture Specification version B – ARM IHI 0050B ID080717

⁵⁵ ARM CHI 5 CHI Architecutre Specification version E.c – ARM IHI 0050E.c ID092622

