Job Title: RTL Design Intern

Duration: 6 months

Job Summary:

1) Strong knowledge of digital design fundamentals (combinatorial circuits, sequential circuits, FSMs, etc.)
2) Basic understanding of simulation, synthesis, FPGA design flow
3) Write synthesizable RTL code using Verilog, VHDL or SystemVerilog
4) Experience with FPGA programming and debugging is a must
5) Hands-on experience with open-source or industry standard tools will be an added advantage
6) Familiarity with computer architecture and memory subsystems
7) Familiarity with different types of memory or IPs such as BRAM, SRAM, DRAM will be an added advantage
8) Good to have knowledge on verification methodologies
9) An ideal candidate should possess analytical skills, problem solving ability and attention to details
10) Good communication skills and ability to work in a team environment