ASIC Internship JD

Opportunity:

- We are looking to hire sharp Engineering minds with excellent communication for ASIC Design and Verification
- You will be part of a fast-paced team responsible for delivering high-speed ASICs for large, complex systems.
- You will have a significant opportunity to interact with system design teams across geographies.

Responsibilities:

- Define and architect high-performance blocks for the latest, most advanced networking ASICs
- Perform micro-architecture and logic design to deliver maximum throughput, while using minimum power
- Collaborate with the verification team in the development of the testplan and assist in debugging test failures
- Collaborate with the physical design team to develop timing constraints, analyze timing violations, and perform timing fixes

Required Skills:

- Strong Verilog RTL coding skills; knowledge of C/C++ coding
- Knowledge of Synopsys Design Compiler, Verplex LEC, and Spyglass is desirable
- Knowledge of high performance memory subsystems
- Knowledge of multi-domain clock synchronization and high-speed serial interfaces
- Strong problem solving and ASIC debugging skills
- Excellent written and verbal communications skills