An H-Bridge Driver Using Gate Bias for DC Motor Control

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ABSTRACT

DC motors are important rotation components for consumer electronics and industry controls, especially, DC motors also play an important role in the development of robot technologies. A design of DC motor driver, based on the H bridge using complementary MOSFET type, is proposed in this paper. Differing from the conventional DC motor driver requiring dead time generation, the proposed driver does not has a dead time generator by using gate bias. Therefore, this proposed H-bridge driver without dead time generation can not only reduce its hardware complexity, but also increase the driving efficiency.

INTRODUCTION

In many control applications, such as motors, DC/DC converters, or class D amplifiers, H bridge is an often-used power device to drive the inductive load. Especially for DC motors, the H-bridge driver can be used to control the direction and speed of DC motors [1]; therefore, it has become an important driving component for motor control. The basic structure of H bridge is constructed by 4 power transistors such as BJT, MOSFET, or IGBT, which they work as electronic switches [2]. When both upper and lower power transistors at the same side turn on concurrently, the shoot-through phenomenon may occur due to the transition delay of power transistors. Consequently, the generation of dead time is necessary and important for the H-bridge driver. However, this will cause a nonlinear output corresponding to the PWM control input. Based on complementary MOSFET structure, a new H-bridge design using gate bias technology is proposed in this paper. Without dead time generation exiting in the conventional H-bridge drivers, therefore, the proposed H-bridge driver can benefit low hardware cost and achieve better linear control.

DEAD TIME IN H BRIDGE

Considering the H-bridge motor driver using complementary MOSFET structure shown in Fig 1., when the lower power MOSFET Q_3 (Q_4) turns on from off state, it must wait for the upper power MOSFET Q_1 (Q_2) turning off from on state in advance for a period of time (called dead time). Similarly, it also needs the dead time to turn Q_3 (Q_4) off from on state in advance when the upper power MOSFET Q_1 (Q_2) turns on from off state. The dead time can avoid the upper and lower transistors at the same side turning on concurrently, such that these transistors are not damaged by the shoot-through current. However, the existence of dead time will limit the minimum rotation speed of DC motor at low speed, especially for high-speed switching of power transistors. Moreover, there exists the voltage error between the control voltage and the actual output voltage, and that will not only incur reducing the output torque of DC motor, but also cause a nonlinear distortion when transferring the control voltage to the corresponding rotation speed [3][4].

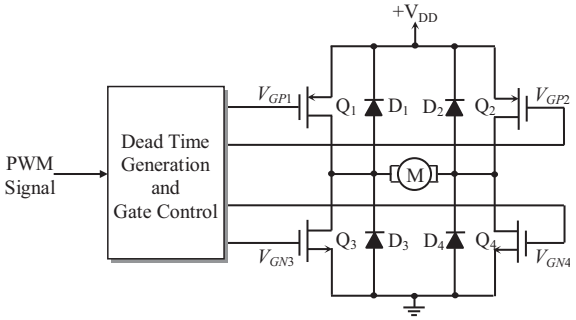

Fig. 1 CMOS H-bridge driver with dead time generation.

PROPOSED H-BRIDGE DRIVER

Our proposed H-bridge driver shown in Fig. 2 is based on a complementary MOS transistor structure [5], where the CMOS H bridge is the same as that of Fig. 1. In this driver no complicated control circuit is required, only four open-collector inverters (U_1~U_4) used as buffers for the logical inputs (A and B) associate with some resistors (R_1~R_6) and capacitors (C_1 and C_2). Here, the outputs of U_1 and U_2 can pull up to the supply voltage (V_{DD}) to turn Q_1 and Q_2 off, respectively. U_3 (U_4) connected to R_3 and R_5 (R_4 and R_6) forms a gate-bias circuit for Q_3 (Q_4), which avoids incurring shoot-through current when the PWM signal inputs to Q_1 and Q_3 (or Q_2 and Q_4) at the same time.

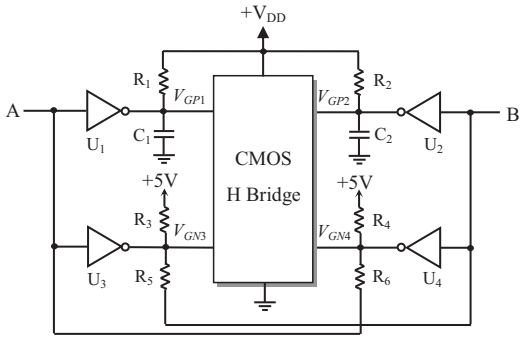

Fig. 2 Proposed H-bridge driver using gate bias.

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For improving the efficiency of the H-bridge driver on PWM control, a gate-bias technology in this paper is proposed to apply to the MOSFET-based H-bridge driver. In our proposed driver circuit, according to the superposition principle at A="Lo" or B="Lo", two gate voltages (V_{GN3} and V_{GN4}) of NMOS transistors (Q_3 and Q_4) can be respectively expressed as [5]:

$$V_{GN3} = \left(\frac{R_5}{R_3 + R_5}\right) \times 5 + \left(\frac{R_3}{R_3 + R_5}\right) \times V_B \quad (1)$$

$$V_{GN4} = \left(\frac{R_6}{R_4 + R_6}\right) \times 5 + \left(\frac{R_4}{R_4 + R_6}\right) \times V_A \quad (2)$$

where V_A and V_B are the logical voltages for A and B inputs, respectively. When both A and B remain "Lo" state (i.e. $V_A = V_B \cong 0$), two PMOS transistors (Q_1 and Q_2) turn off immediately. If R_3, R_5 and R_4, R_6 are appropriately selected to build two gate-bias voltages slightly larger than V_{th} for Q_3 and Q_4, respectively, then Q_3 and Q_4 turn on in this state, where V_{GN3} and V_{GN4} are given by:

$$V_{GN3} = \left(\frac{R_5}{R_3 + R_5}\right) \times 5 \approx V_{th},\ V_{GN4} = \left(\frac{R_6}{R_4 + R_6}\right) \times 5 \approx V_{th} \quad (3)$$

and R_3/R_5 and R_4/R_6 can be found as:

$$\frac{R_3}{R_5} = \frac{R_4}{R_6} \approx \frac{5}{V_{th}} - 1 \quad (4)$$

Considering the PWM signal with period less than R_1C_1 time constant enters into input A and input B remains "Lo", thus Q_1 always turns on and V_{GN4} is modified as:

$$V_{GN4} = V_{th} + \left(\frac{R_4}{R_4 + R_6}\right) \times 5 \times D \quad (5)$$

where D is the duty cycle of the PWM signal and suppose that the high-level voltage of the PWM signal is 5V. Therefore, Q_4 can easily turn on by the PWM signal with less duty cycle. Although the PWM signal also appears at the input of U_3, however, V_{GN3} will vary under V_{th} as the duty cycle of PWM signal increases, and it is given by:

$$V_{GN3} = \left(\frac{R_5}{R_3 + R_5}\right) \times 5 \times (1 - D) \quad (6)$$

Consequently, Q_3 can work from the pinch-off region at D=0 to the cutoff region at D>0 to make sure Q_1 and Q_3 do not turn on concurrently. Therefore, our proposed H-bridge driver can naturally avoid the shoot-through situation without dead time generation. Similarly, when the PWM signal enters into input B at A = "Lo", Q_2 and Q_3 will turn on, and Q_4 works from the pinch-off region to the cutoff region as the duty cycle increases.

EXPERIMENTAL RESULTS

In our experiment, we use two PMOS (IRF9540) and two NMOS (IRF540) transistors to implement the H bridge, where their threshold voltage V_{th} is about 3V, and select $R_3 = R_4 = 1K\Omega$ and $R_5 = R_6 = 1.8K\Omega$ to build two gate biases: $V_{GN3} = V_{GN4} = 3.2V$ according to Eqs. (1) and (2). Besides, this driver offers the voltage range: 5V~24V for DC motor and the maximum supply current: 10A. For verifying and measuring the proposed driver, we try to input the PWM signal with 15.625KHz to one control node of H bridge, and the another node keeps low level. The measured waveforms shown in Fig. 3 [5] include a low-level voltage at node A (CH1), a PWM signal of 50% duty cycle at node B (CH2), and two gate voltages: V_{GN3} (CH3) and V_{GN4} (CH4), respectively. From Fig. 3, we find that the average voltage of V_{GN3} increases to 4.09V from the gate-bias voltage 3.2V for 50% duty cycle, and even Q_2 keeps on, the average voltage of V_{GN4} decreases to 1.61V from 3.2V to always make Q_4 cutoff. Therefore, no dead time is required in the proposed driver.

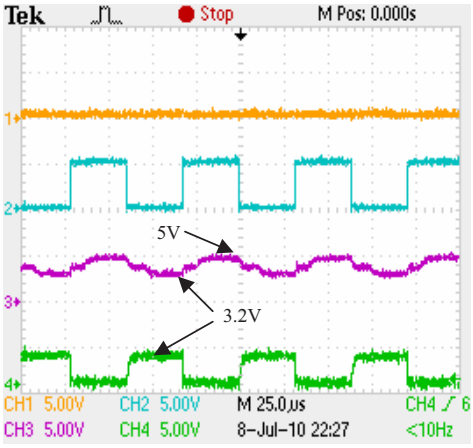

Fig. 3 The measured voltage waveforms for 50% duty cycle.

CONCLUSION

A design of DC motor driver, based on the H bridge using MOSFET type, is proposed in this paper. Unlike the conventional DC motor driver requiring dead time generation, the proposed driver does not has a dead time generator by using gate bias, and it can successfully adjust the speed range of DC motor by the PWM signal from duty cycle: 8% to 100% in our experiment. Therefore, the proposed H-bridge driver indeed improves its driving efficiency for DC motors and provides a low cost design compared with the other drivers with dead time generation.

REFERENCES

[1] N. Mohan, T .M. Undeland and W. P. Robbins, *Power Electronics: Converters, Applications, and Design*, 2nd ed., John Wiley & Sons, Inc., 1995.

[2] J. Brown and B. Jordan, "Brief H-Bridge Theory of Operation", *http://www.dprg.org/tutorials/1998-04a/*, August 2002.

[3] T. J. Summers, and R. E. Betz, "Dead-Time Issues in Predictive Current Control", *IEEE Transactions on Industry Applications*, Vol. 40, No. 3, pp.835-844, May/June 2004.

[4] N. Urasaki, T. Senjyu, K. Uezato, and T. Funabashi, "Adaptive Dead-Time Compensation Strategy for Permanent Magnet Synchronous Motor Drive", *IEEE Transactions on Energy Conversion,* Vol. 22, No. 2, pp.271-280, June 2007.

[5] H.C. Chen and J.C. Chen, "Design of H-Bridge Driver without Dead Time for DC Motors", *Proc. The 9th Taiwan Power Electronics Conference and Exhibition*, pp. 118-121, Sept. 2010.