VLSI LAB PROJECT REPORT

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MAGIC LAYOUT OF THE 4x4 VEDIC MULTIPLIER BASED ON THE URDHVA-TIRYAGBHYAM SUTRA

Objective:

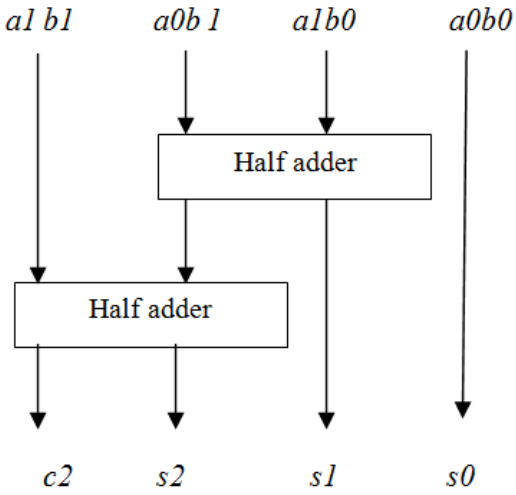
In this project, I explore the Magic layout for multiplication of 4 bit numbers using the Vedic multiplication technique known as the Urdhva-Tiryagbhyam sutra. Urdhva Tiryagbhyam means vertically and cross-wise.

The advantage of the Vedic multiplier over other techniques is the partial products are parallelly computed and hence there's a saving of time as well as area.

Block Diagram and Description of The Circuit:

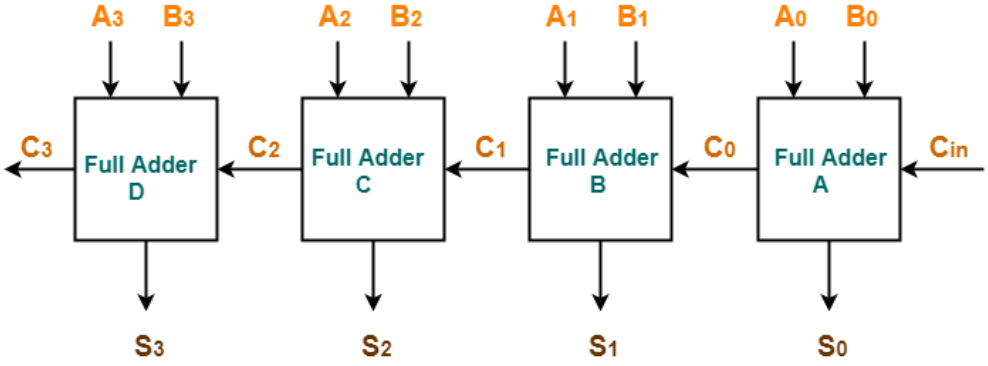
I proceed to build the 4x4 Vedic Multiplier by using 2x2 Vedic multipliers and ripple carry adders using a hierarchical modular approach.

The structure of a 2x2 vedic multiplier is as follows:



I use 4 AND gates and 2 Half adders to build a 2 by 2 Vedic Multiplier. Half adder is built using 1 XOR gate and 1 AND gate.

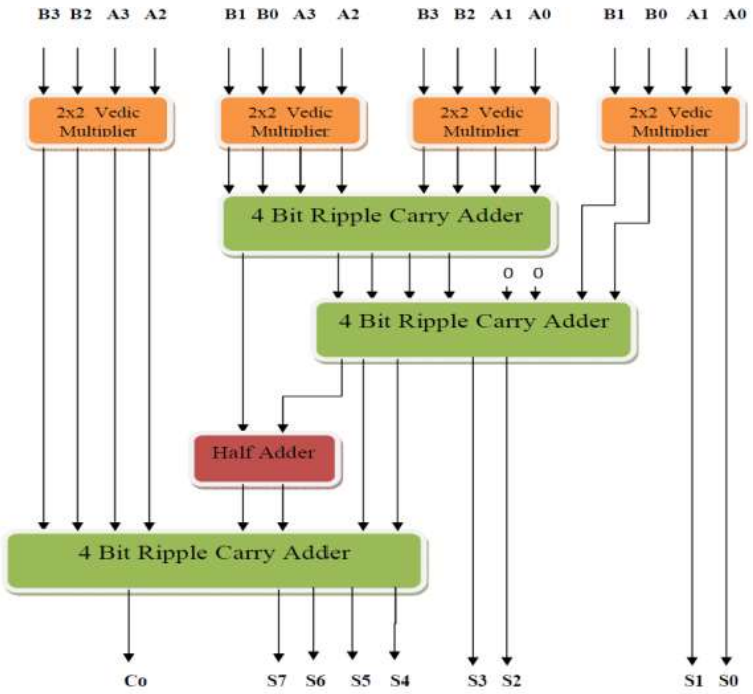
I also used three 4-bit Ripple Carry Adder Units. These are in turn built with four Full adders, which are in-turn made of 2 Half adders and an OR Gate.



4-bit Ripple Carry Adder

I then proceeded to make our 4x4 Vedic Multiplier circuit.

The block diagram of the circuit is as follows:



Implementation Details:

The layout is implemented using the pharosc standard cell library obtained from the vlsitechnology.org. A hierarchical structure is followed to make the multiplier. I first create Half Adders using the standard XOR2 and AND2 gate of version 0 with a drive strength of 1. All the gates used are from the version 0 and have a drive strength of 1.

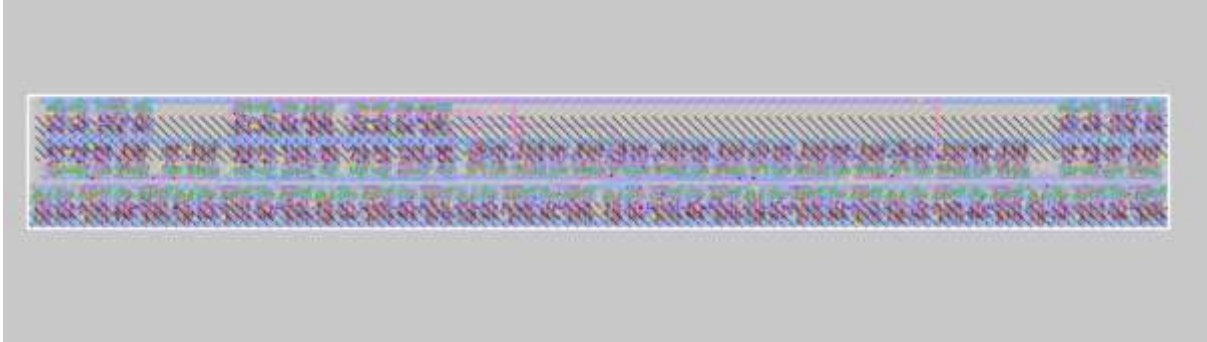
I then proceeded to build the full adders, using which I make the 4-bit Ripple Carry Adder. Blocks of 2by2 Vedic Multipliers are made using AND gates and Half Adders.

I used over the cell routing technique to route as it consumes less area when compared to channel routing. Vedic Multiplier by the virtue of its technique itself provides us with a faster speed, hence I went after optimizing the area for the layout.

Test Strategy:

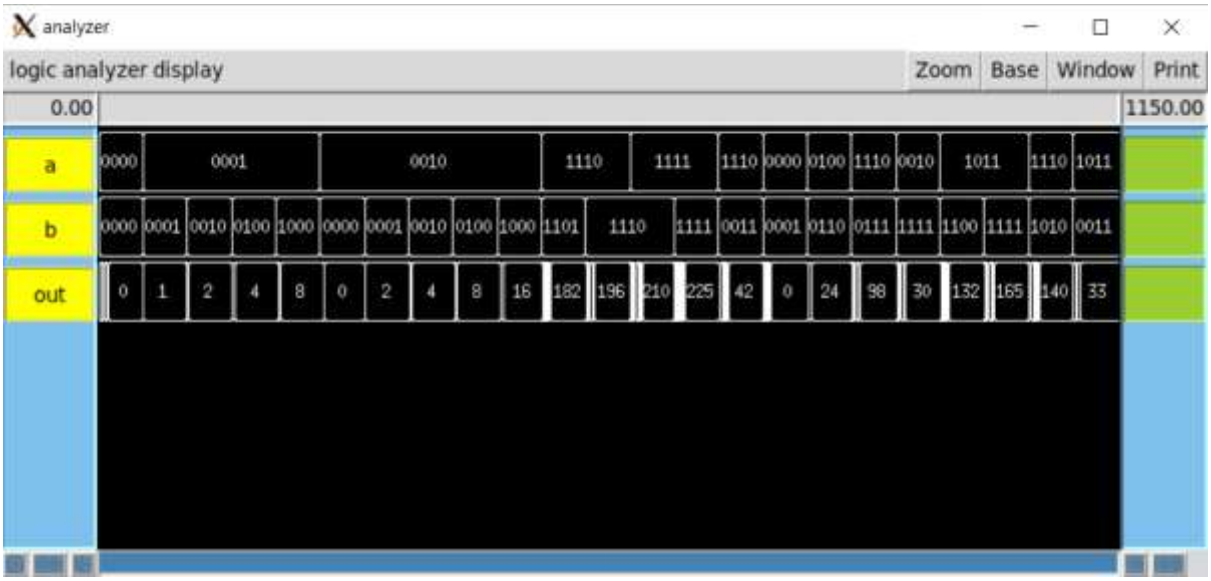
I used a combination of random number generation and specific test patterns to test the results of the circuit. A test was performed at every level of hierarchy first to ensure that each sub component was working well. I performed an exhaustive test of the truth table for testing the subcomponents. However, since the multiplier needs 256 test patterns to test exhaustively, I used the random number + specific test pattern strategy.

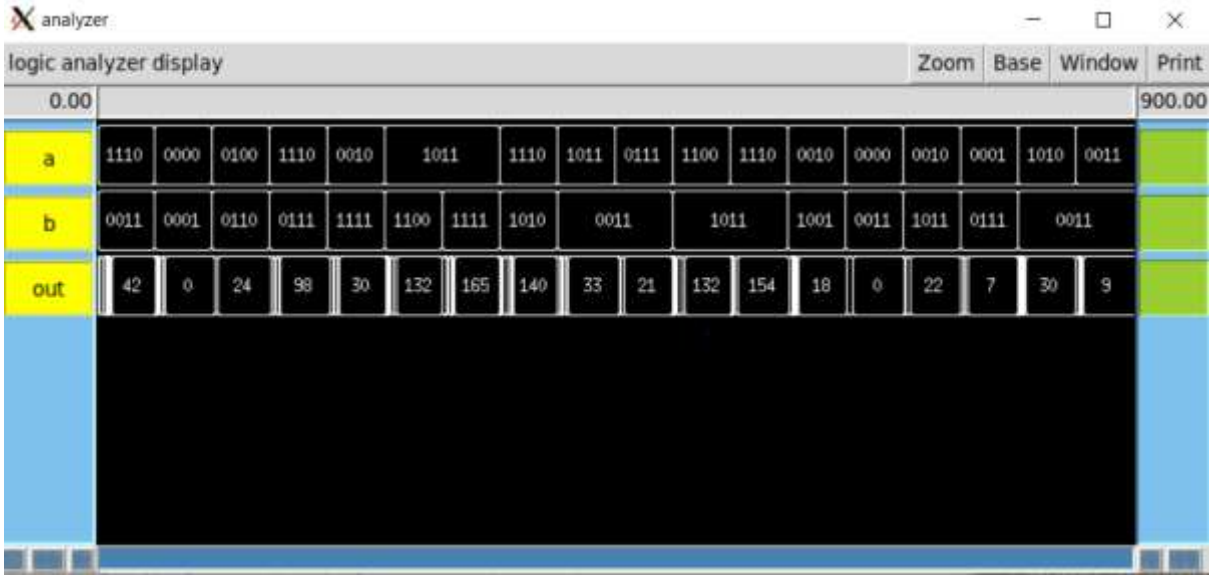
Top Level Layout:



Layout of the 4x4 Vedic Multiplier

Simulation Results:





Component	Area
Half Adder	9430 lambda^2
Full Adder	21663 lambda^2
2x2 Vedic Multiplier	33110 lambda^2
4-bit Ripple Carry Adder	85805 lambda^2
4x4 Vedic Multiplier	478608 lambda^2

The total delay of the Vedic Multiplier is obtained to be 12.32 ns.

For the 4x4 Vedic multiplier

The total number of gates used are 94.

The total number of n-channel MOSFETs used are 348.

The total number of p-channel MOSFETs used are 315.

The sum of nodal capacitances = 19.549274 pF