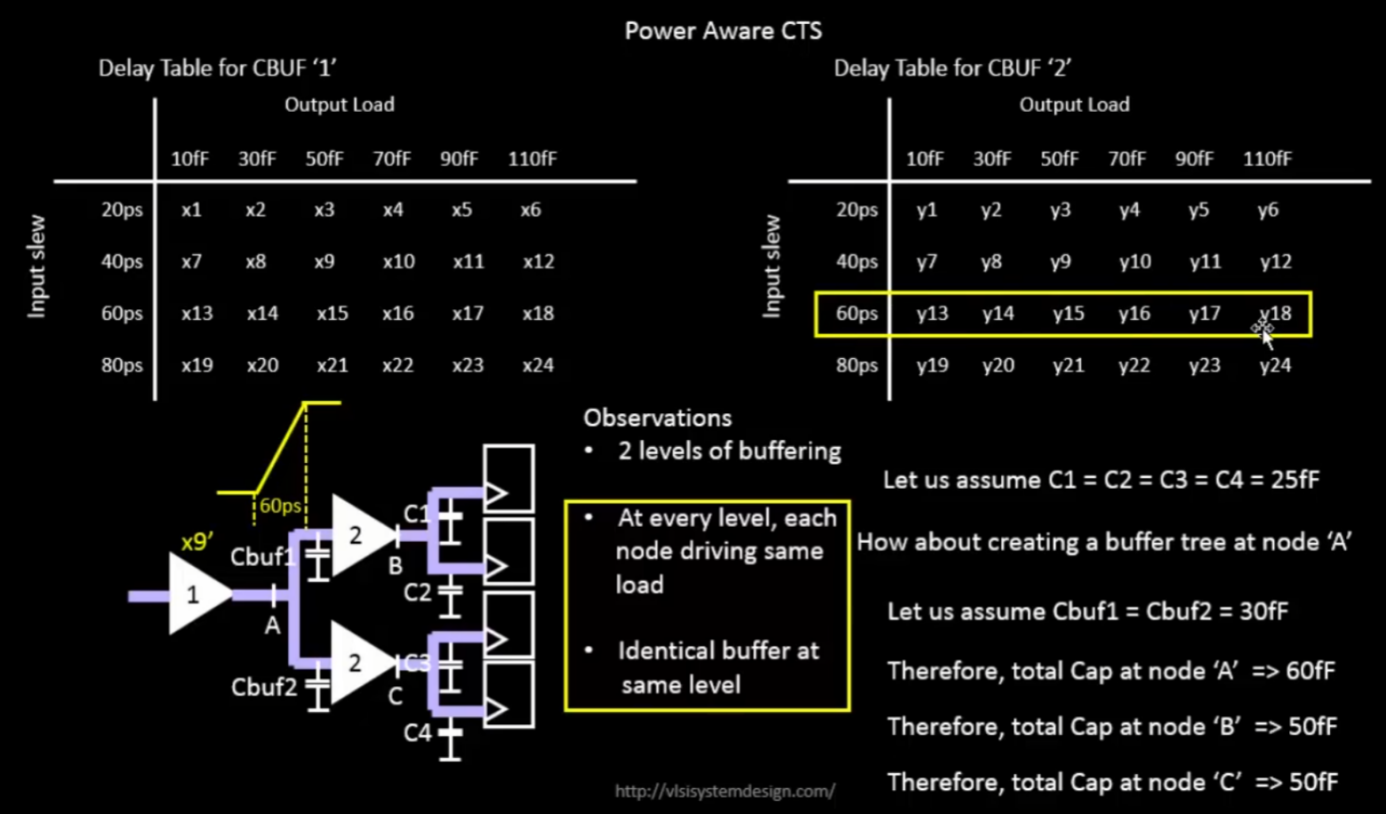
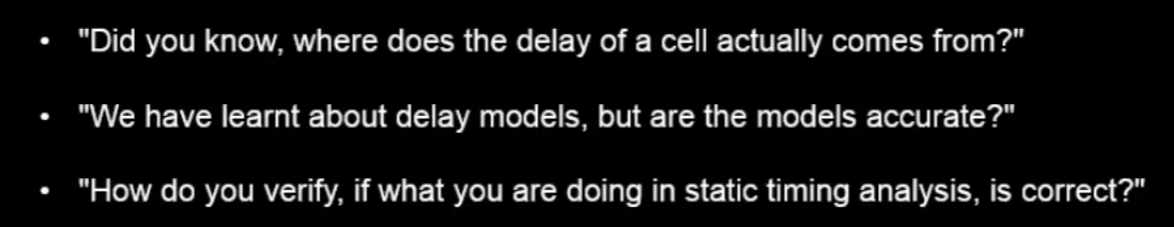
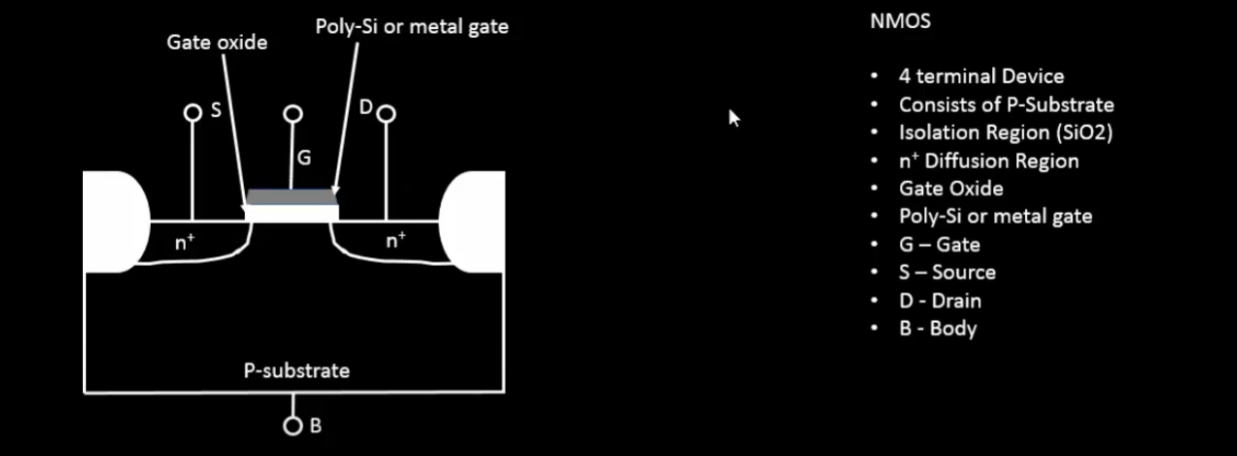
Example of Spice simulation applications. A LUT can be generated from SPICE simulations to generate Delay tables as shown below:

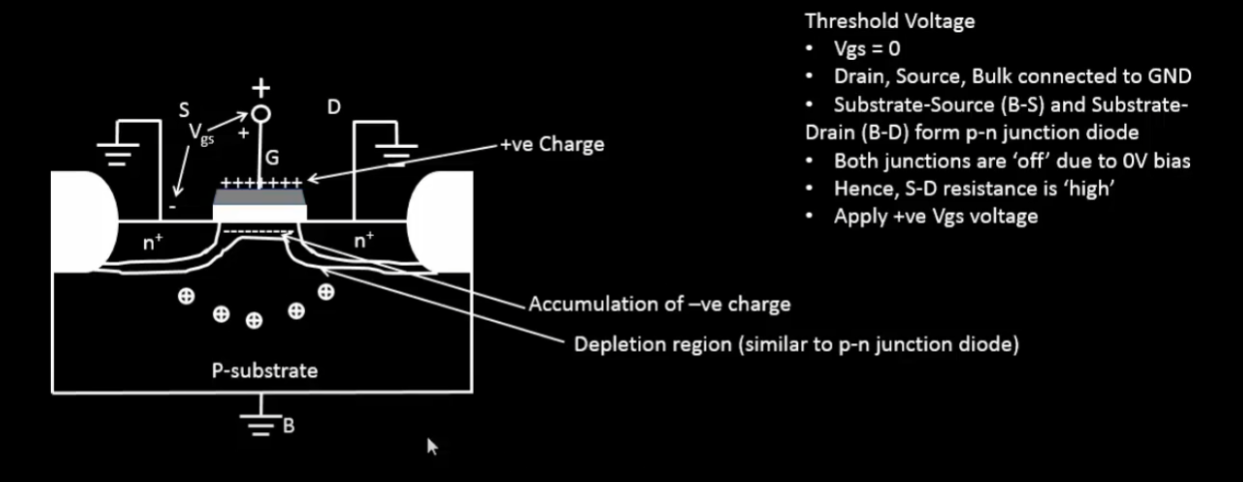


Spice simulation is the answer to the following questions:

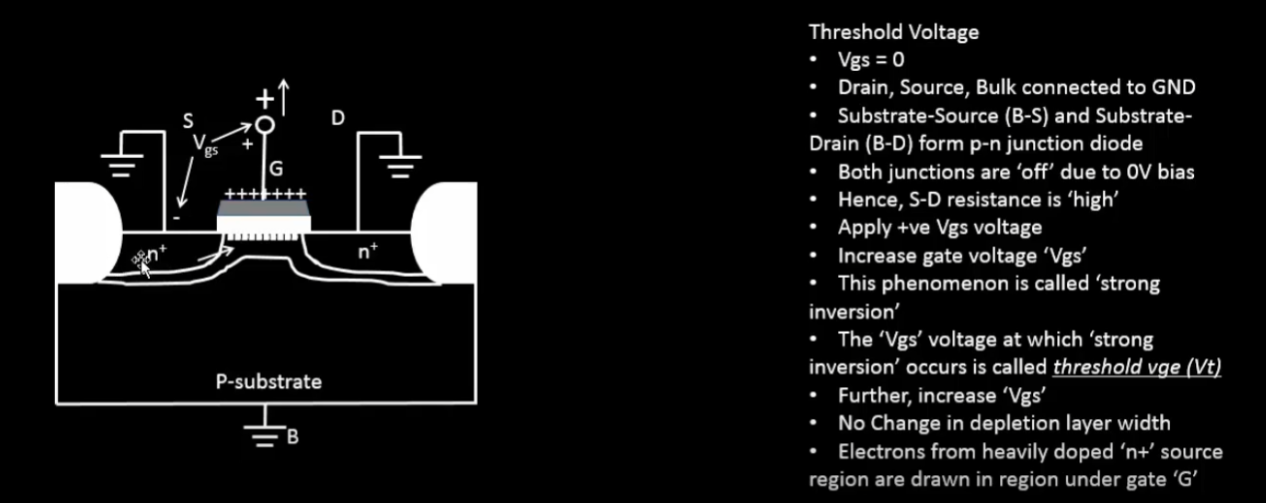




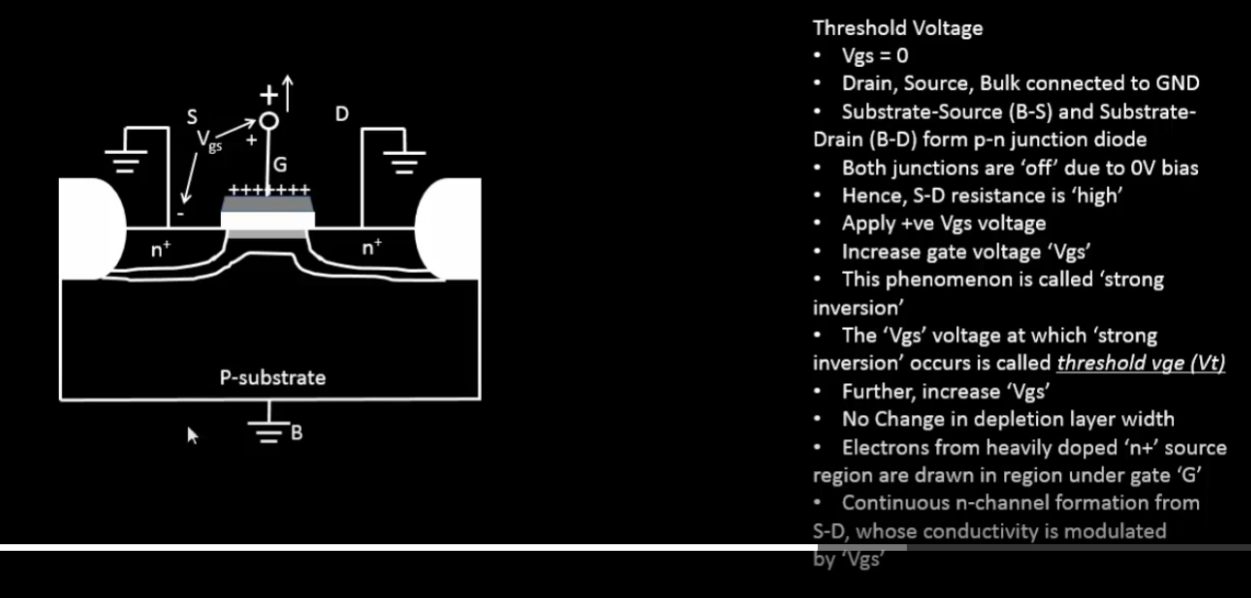
Normally PDK models often categeorized with threhsold votlage of the MOS devices like low Vt, high Vt



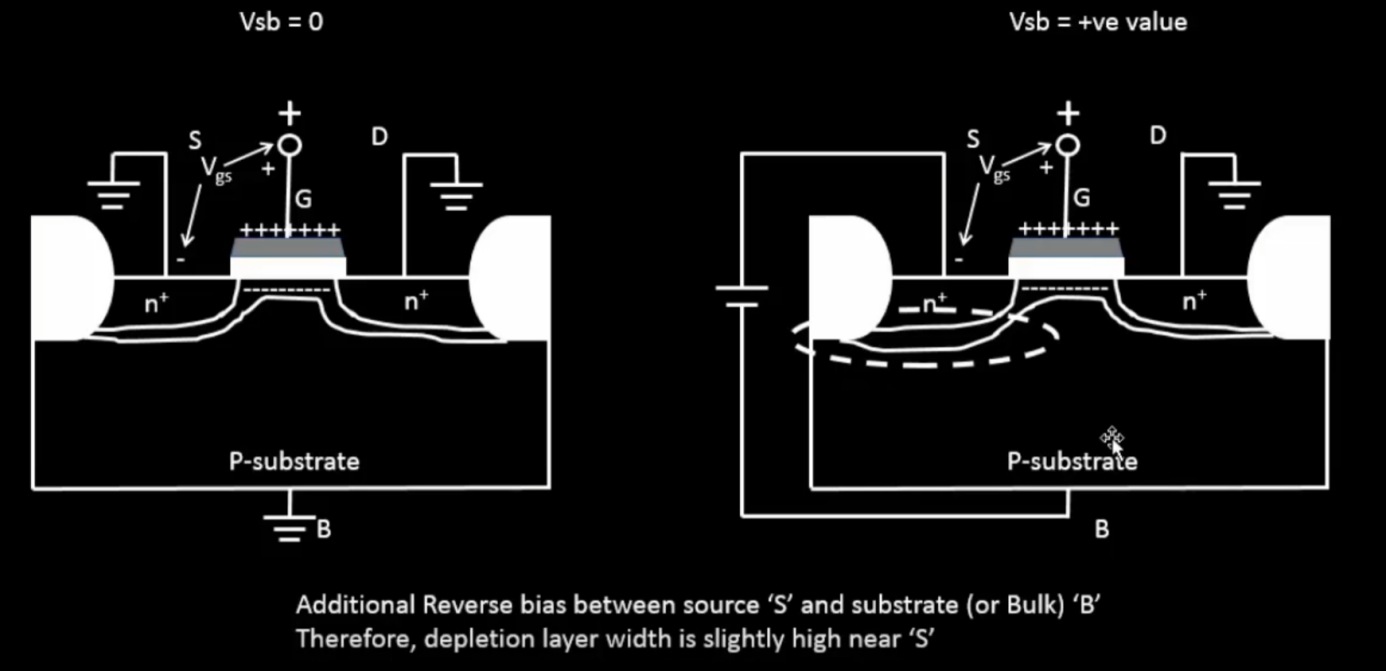
Generally, when there is a PN junction there is a depletion region automatically formed due to diffusion of majority carriers. Holes from P-substrate go into n+ region and electroncs from n+ region come into p-substrate. Now when gate is applied with a positive potential, this depletion region is further enhanced as if a diode is reverse biased. A continuous depletion region will be formed under this gate as shown in the above figure.

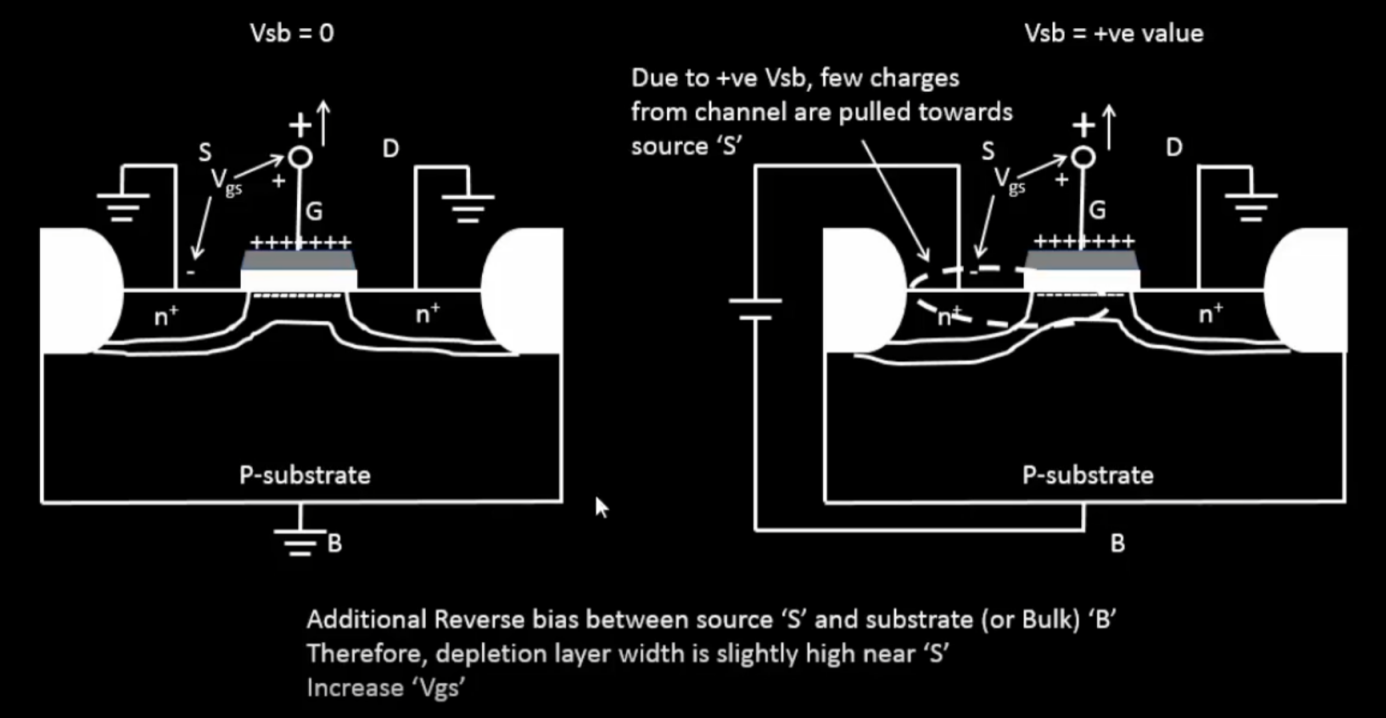


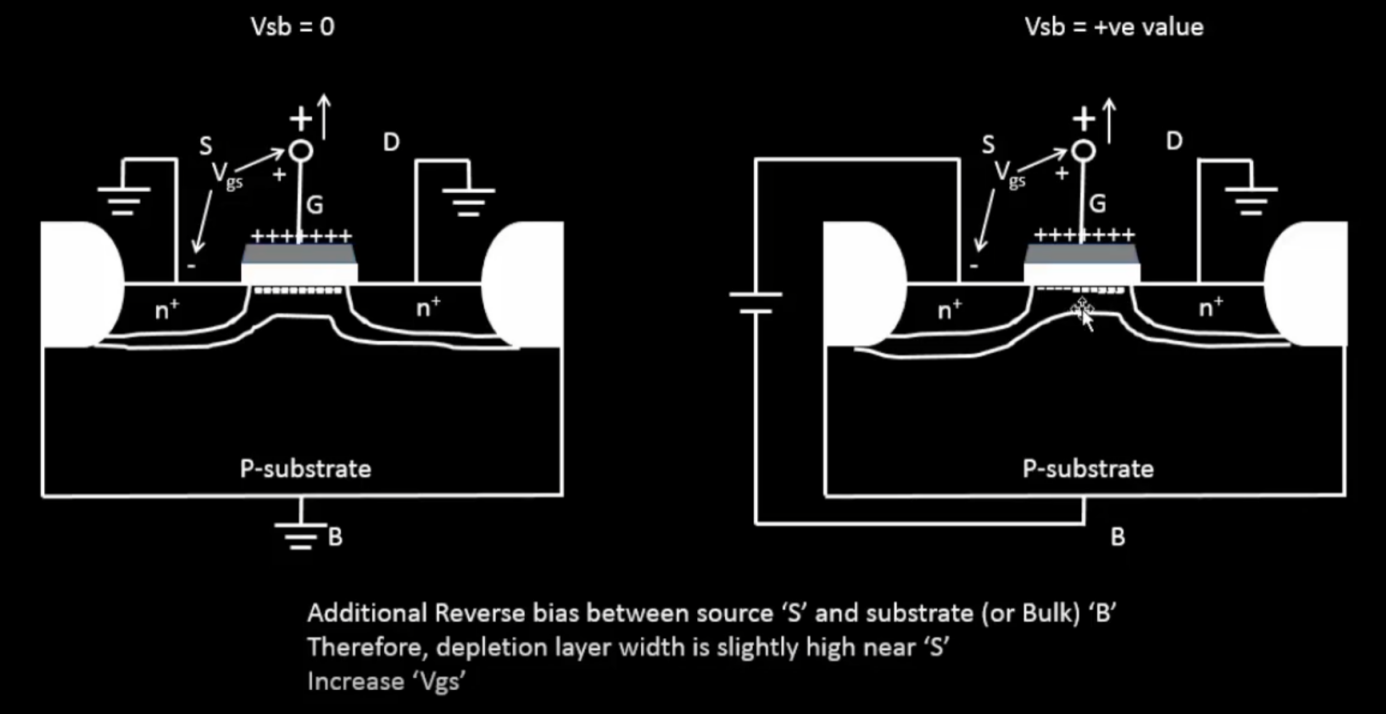
As the gate voltage increases, the depletion region is depleted of all of its negative charges/electrons/minority carriers etc. At this point there are no more negative charges left for the positive potential. At this point the n+ doped region start providing the negative charges. This point of inversion is called strong inversion and hence there will be a conduction between the two n+ regions. The voltage at which this phenomenon happens is called threshold region. After crossing the threshold region we get the following n-channel

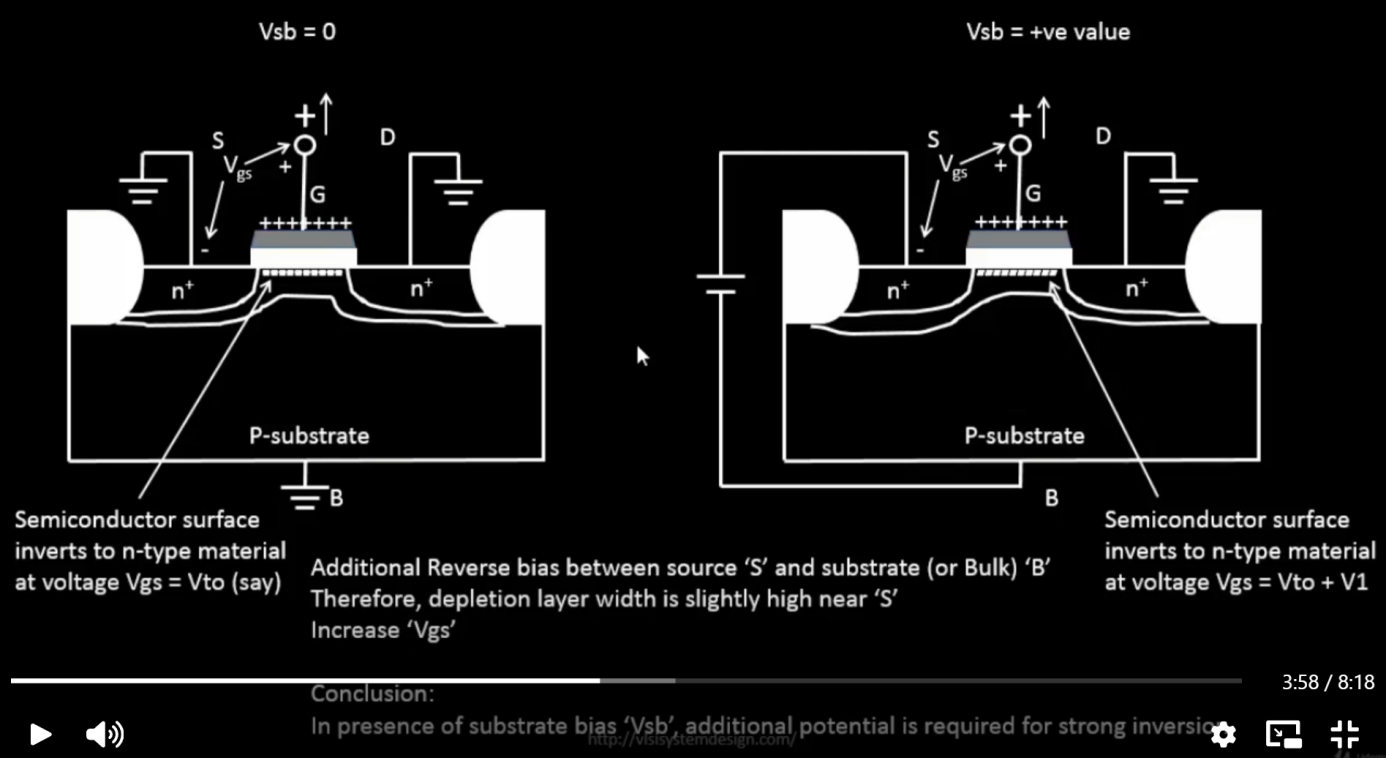


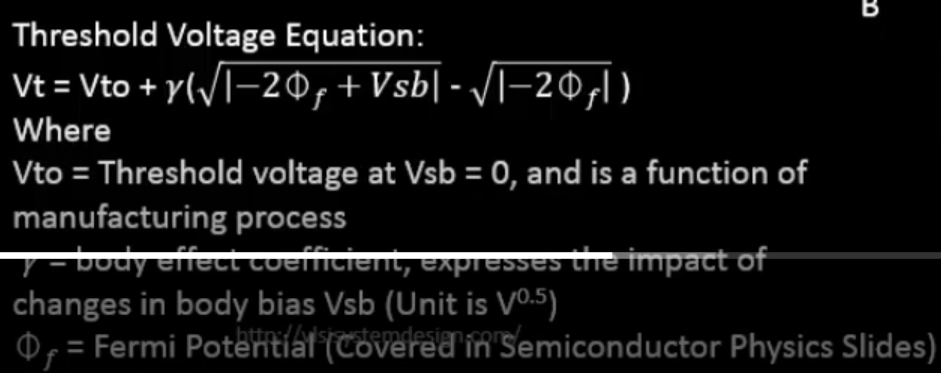
Effect driving the body terminal at a potential:

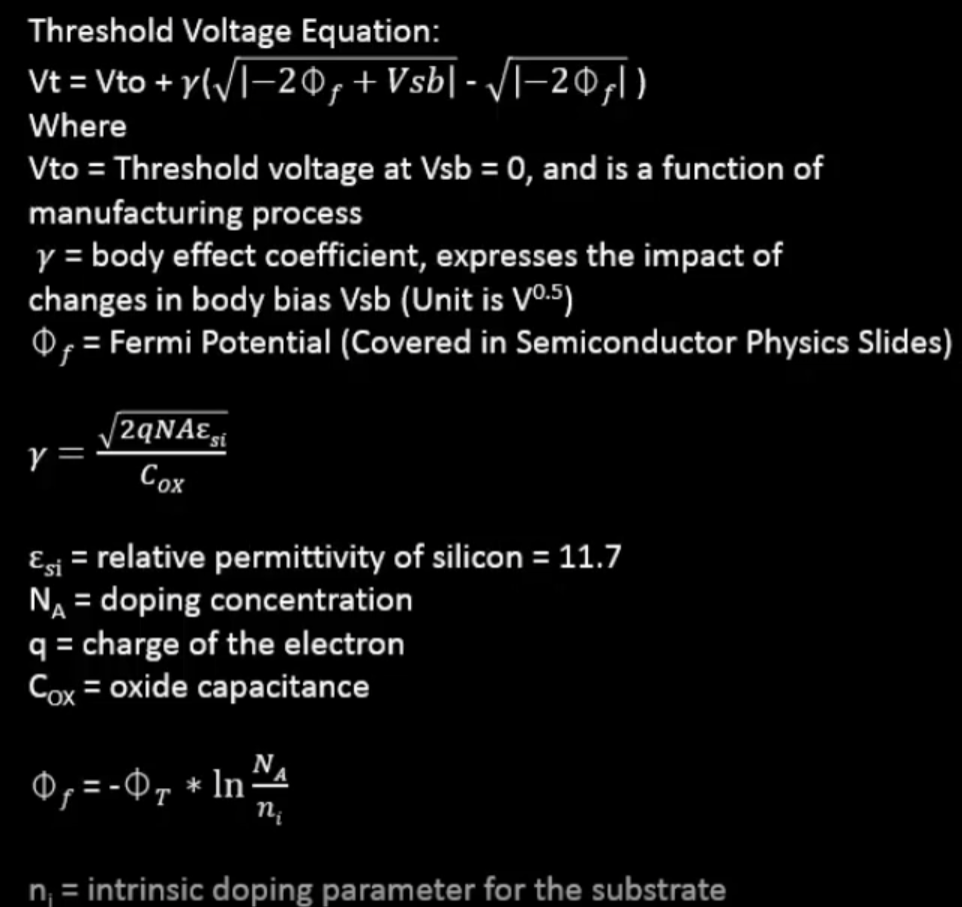


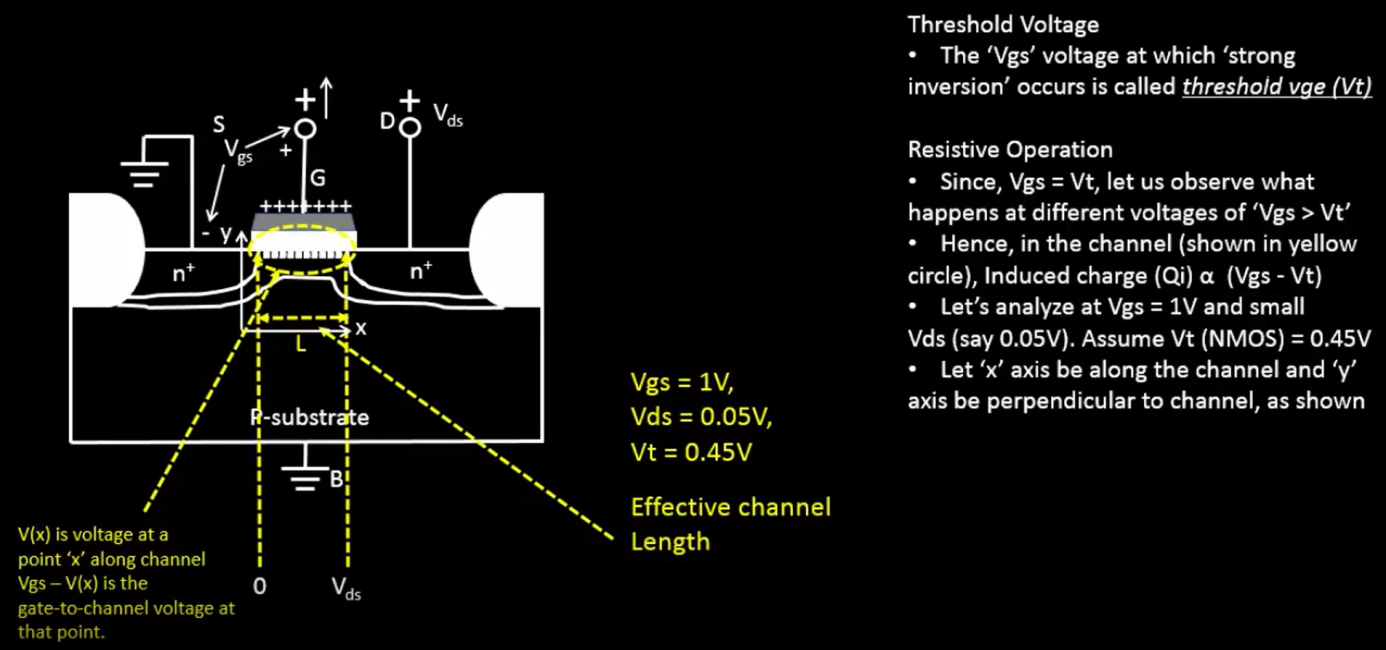




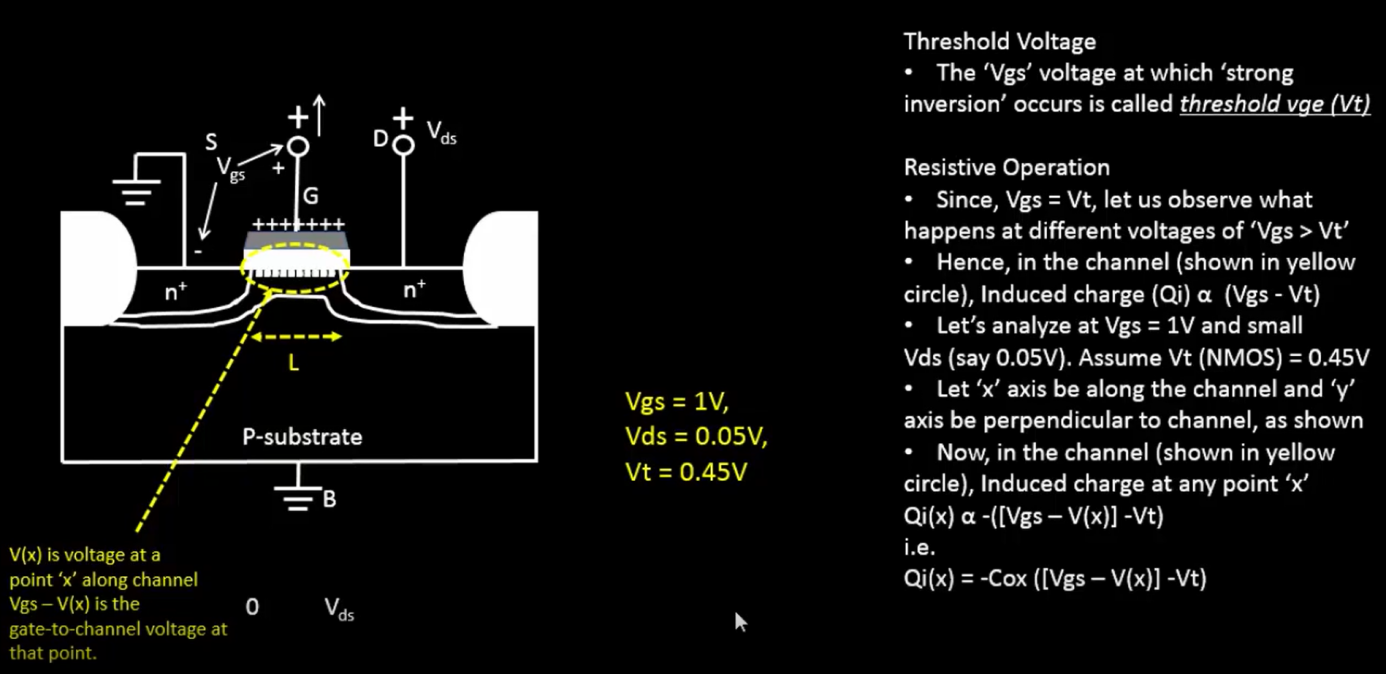


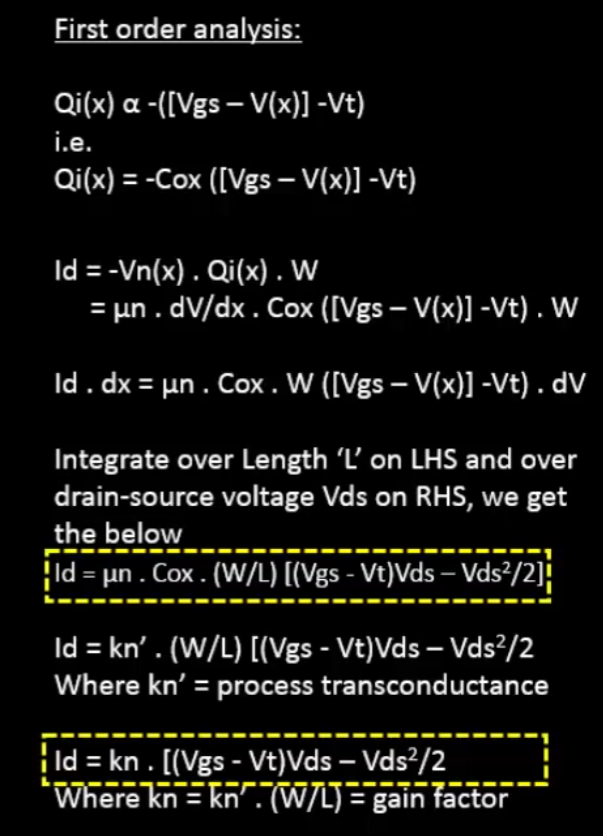
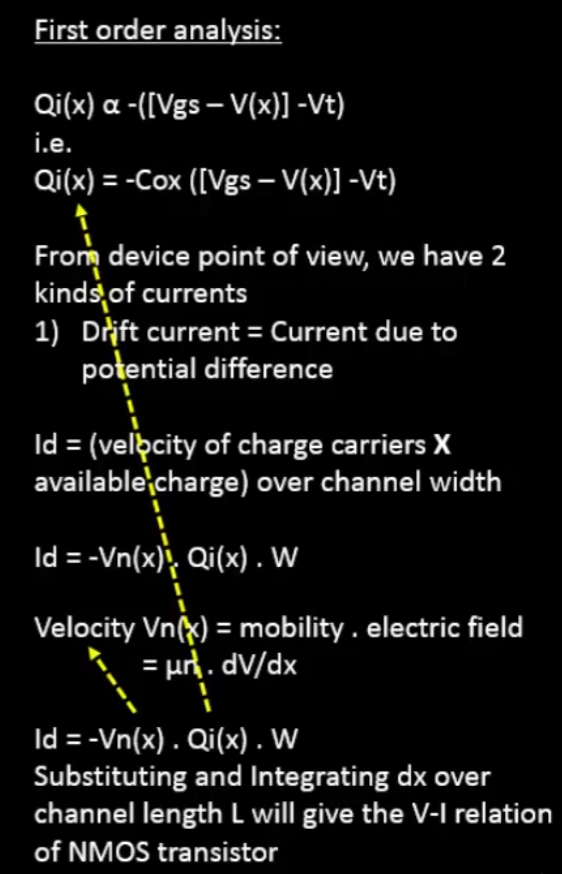
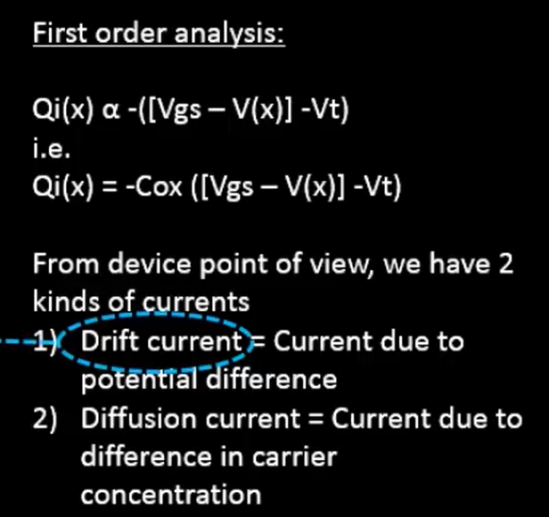




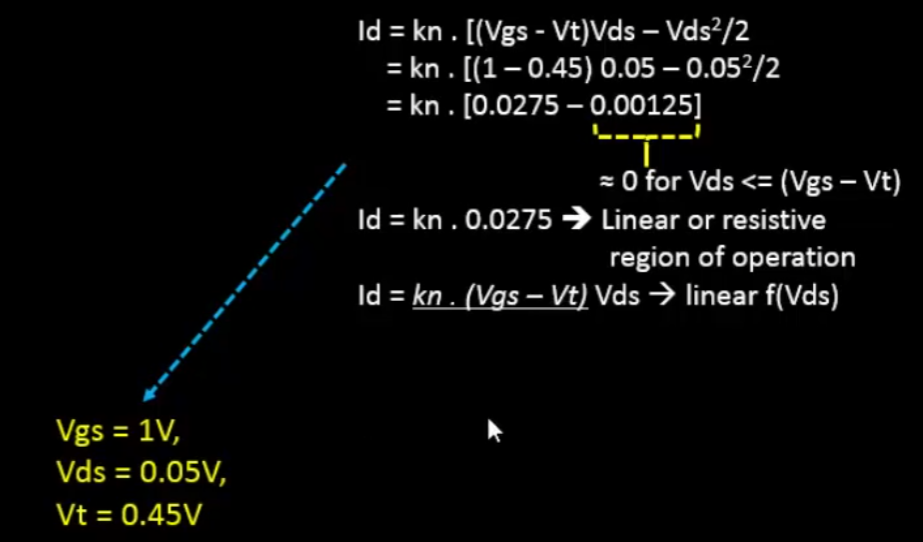


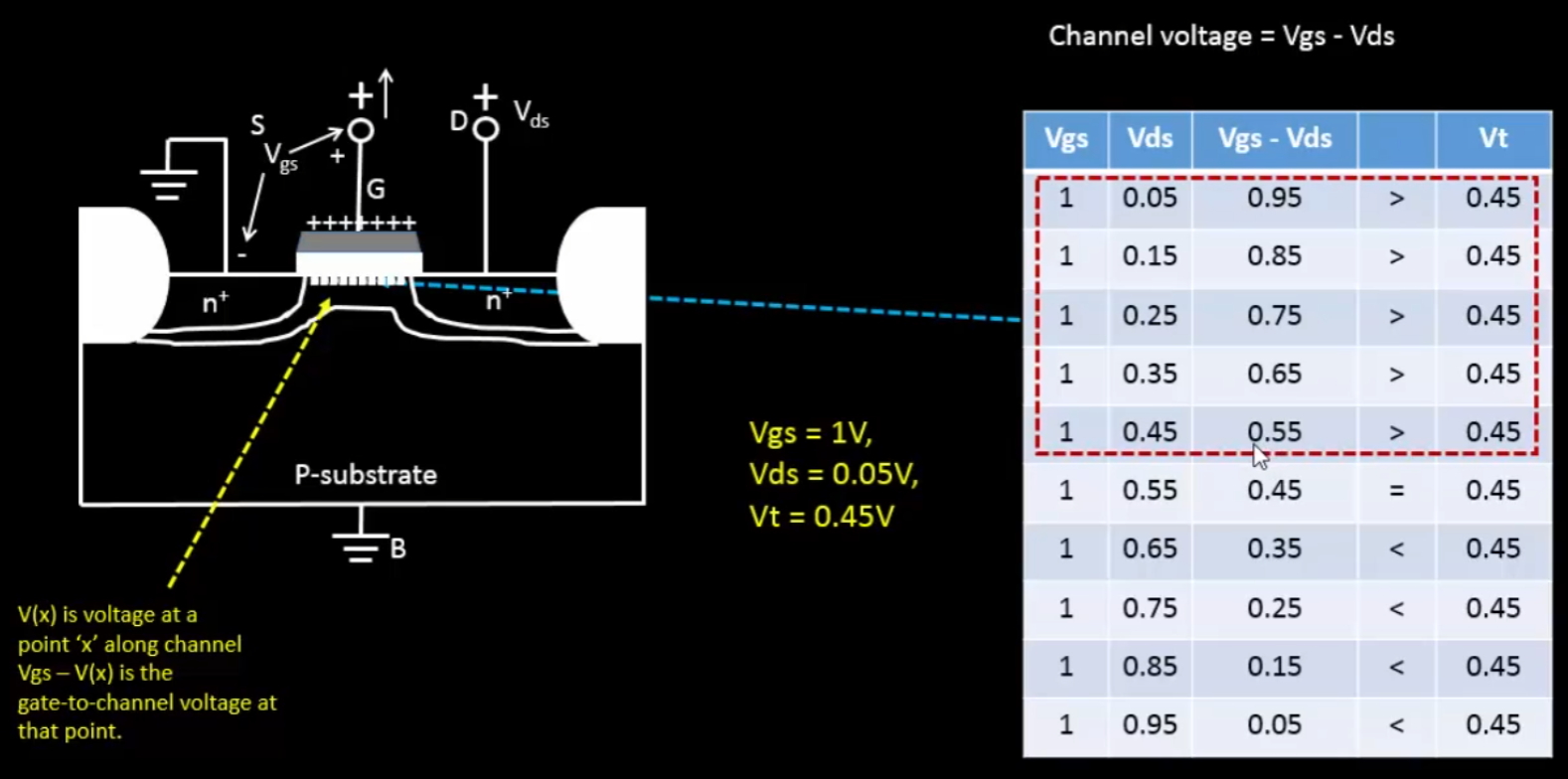
Just like body effect on the threshold voltage we also have the effect of vds. The depletion layer is bigger/wider near the drain because drain-body diode junciton is reverse biased even further. With a wider depletion region, it is natural that the channel formed in the srtrong inversion is narrower near the drain

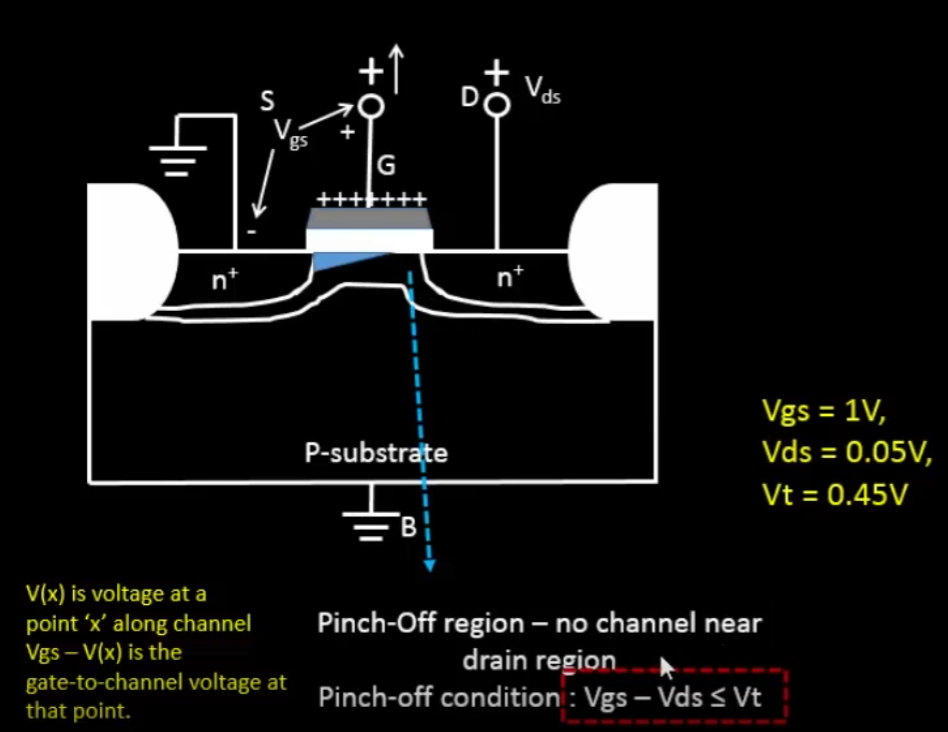
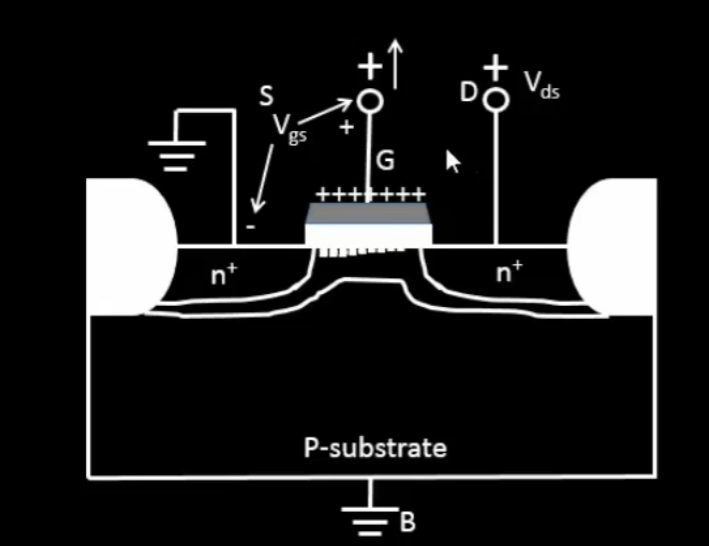




This is being integrated over the comlete channel width because till now all the understanding of the mechanics was done from a cross-sectionaly point of view where the we assumed the carriers were passing through an infitisimally small width of the channel



  
So the channel voltage across the whole length is not the same. Therefore we see an un-even inversion in the channel as shown below:



The channel is getting disappeared at the end near the drain and this gets worse when Vds increases. This means at the end of the channel near the drain, the current/# of carriers will be less but does not mean the current disappears. It just means the current will not follow the same model. In saturation region, after the strong inversion, while deriving using the first order analysis, you do not derive for the whole length of the channel votlage for V I.e. 0 -> Vds, rather you will derive from 0 to Vgs-Vt because there is a pinch of region as well where there is no channel left and this point can be assumed to be at a voltage= Vgs-Vt since this is the Vds value at which pinch off occurs. Hence Vds can be substituted with Vgs-Vt in the drain current equation

