CMPEN 331 – Computer Organization and Design Project

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Date: 12/16/2020

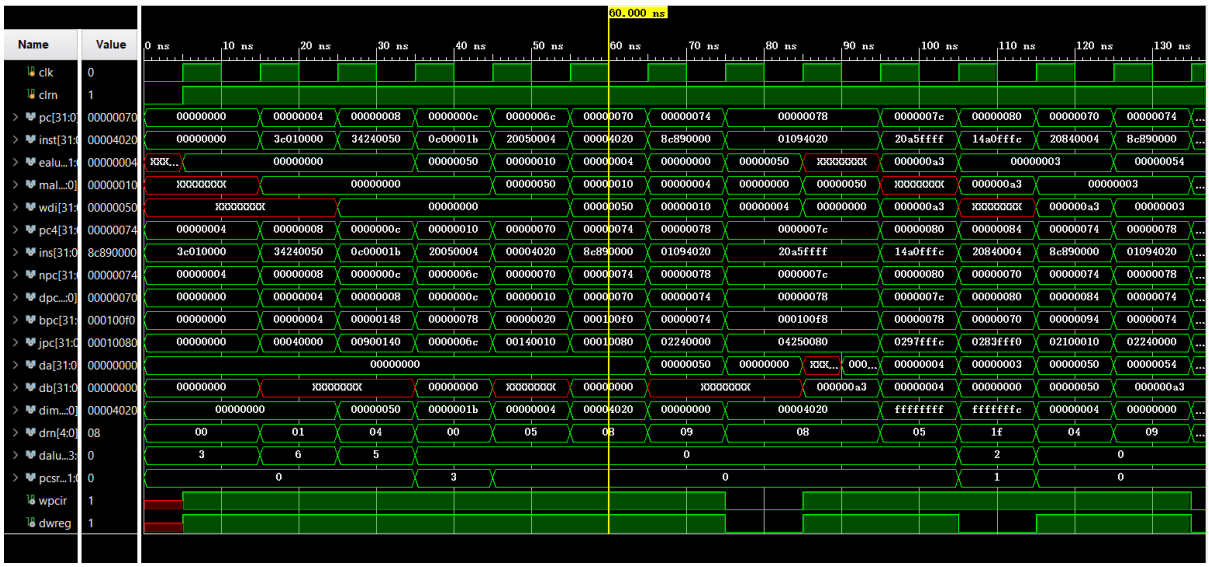
Abstract:

The main objective of the project involves implementing pipeline stalls, which ensure data hazards to avoid at given instructions that could induce them. In order to implement a stall, we first check if the new operand registers, rs and rt, of the new instruction are equivalent to the destination register of the previous two instructions. As inputs have the clock, which replaces our implemented clock from previous labs, and the switch, which once flipped, initiates our program counters and instructions. The outcome is to find an output, which lights up the processer once we reach the end of our instructions.

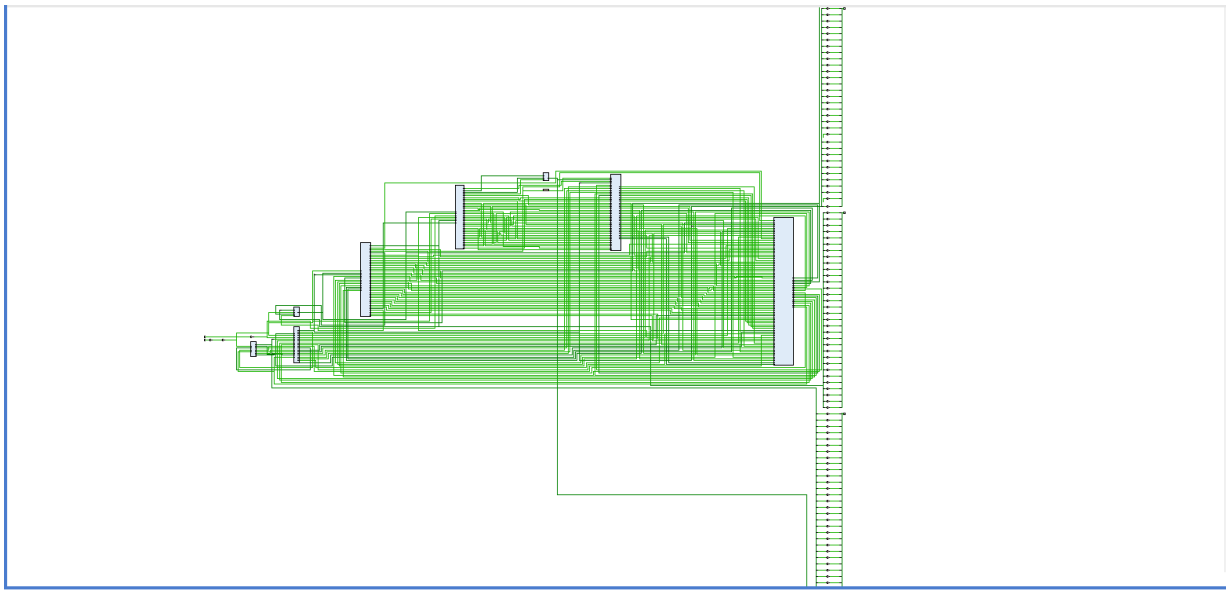
Introduction:

The final project is the culmination of the previous three labs, labs 3, lab 4 and lab 5. Our processor works by having stages, which are our instruction fetch (IF), instruction decode (ID), execution (EXE), memory access (MEM), and write back (WB), In each stage registers that take in the outputs of the stage before it and delivers the values for the inputs for the stage after it. Essentially, what this is doing is storing the previous stage's output values so it can feed it to the next stage. This is beneficial, since this is needed in order to have an implementation that uses several clock cycles per instruction. As one instruction is in the IF stage, another instruction is in the ID stage and another in the EXE stage. This allows five instructions to be running at the same time, which allows our program to run faster, taking advantage of parallelism. This is possible due to the values being stored in the registers so they can be used by the next stages.

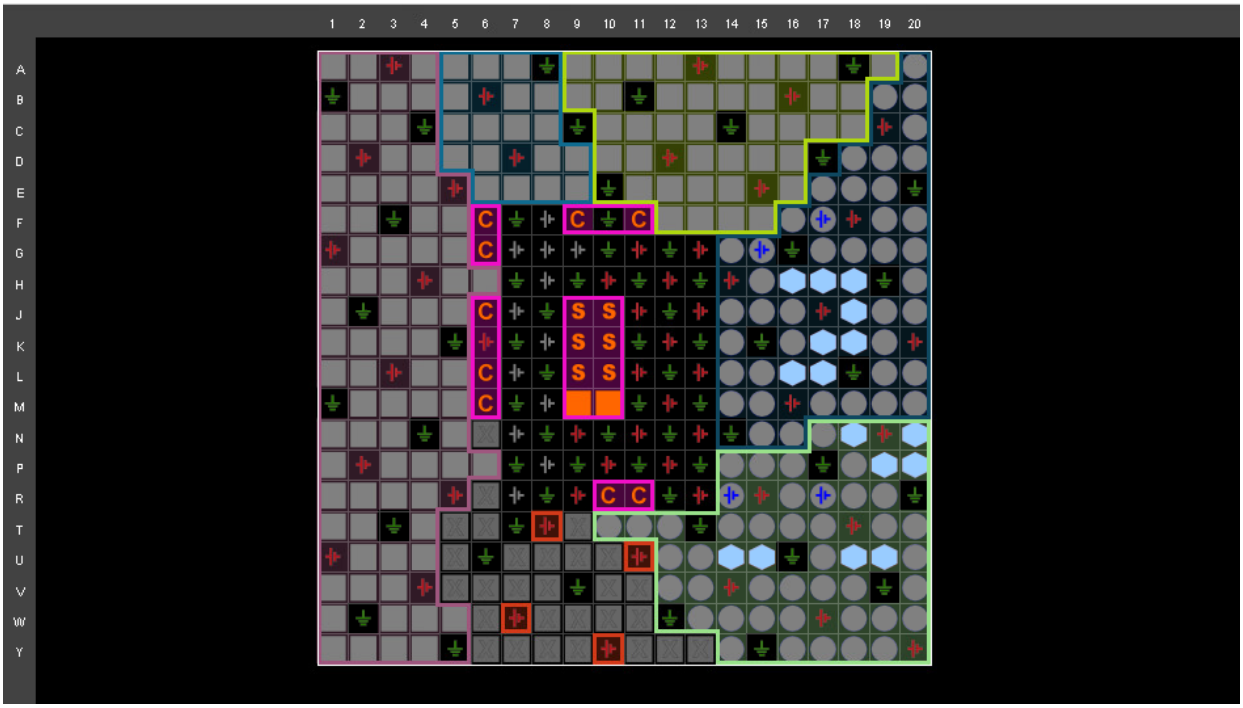
1. Waveforms screen



2. Schematics screen



3. I/O Planning screen



2. Floor planning screen