7. CMOS Inverter and Ring Oscillators

Warning: Be very careful in using the multimeter. You will burn the fuse if you don't pay extra attention.

Learning Objectives

Characterize basic digital circuits, such as CMOS inverter.

Build ring oscillators and adjust frequency.

Build D-flip flop using NAND gates.

Assignments Before the Laboratory Session

Review or search information about "logic gates," "D flip flop."

Search information about "ring oscillator." Study the circuit diagram.

Parts needed include CD4007 CMOS inverter and two 74LS00 IC chips containing low-power Schottky NAND gates. Read data sheet.

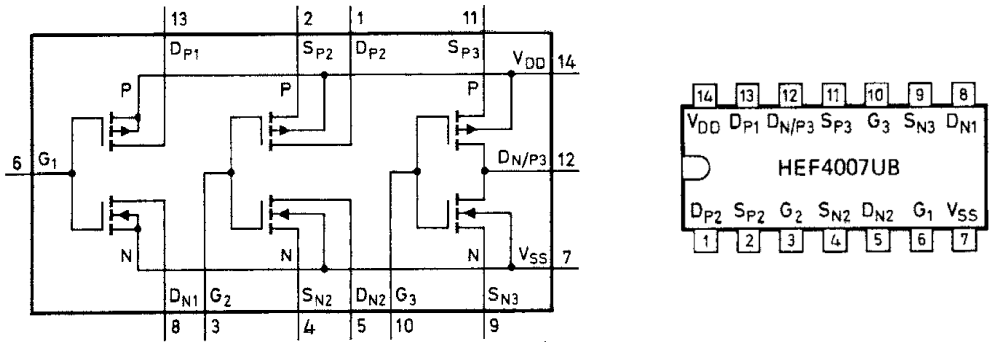

Fig. 1. The diagram and the pin configuration of CD4007. There are three n-MOS and three p-MOS devices in the DIP package. For p-MOS, source nodes are located at pins 14, 2, 11; drain nodes at pins 13, 1, 12. For n-MOS, source nodes are located at pins 7, 4, 9; drain nodes at 8, 5, 12. Gate nodes are at pins 6, 3, 10.

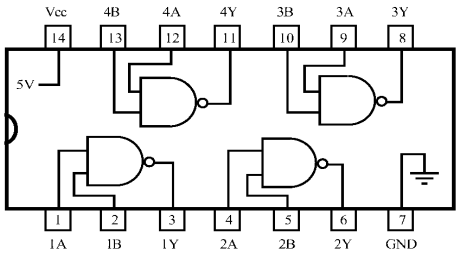

Fig. 2. 74LS00

Background

Logic gates are building blocks of digital integrated circuits. Basic logic gates include AND, OR, NAND, NOR, exclusive OR, exclusive NOR, buffer, and inverter. Their logic symbols and truth tables are well defined and can be found in any textbook of digital electronics. By combining multiple gates, field-programmable gate arrays can provide a great variety of functions. According to the physical circuits used, logic gates developed over the years can be categorized into transistor-transistor logic (TTL), low-power Schottky logic (LS), emitter coupled logic (ECL), complementary MOS (CMOS) and the high speed or advanced versions of them. CMOS operates with very low power consumption. It is the fundamental building block of very large-scale integrated circuits.

Activities During the Laboratory Session

Turn on the power supply. Adjust the voltage to 5 V and current limit to 0.18 A. Do not use the 5 V port because it has no current limiting feature. If there is any error in circuit connection, you can burn components or fuse of the multimeter. Connect the positive output (red) to the power supply bus and connect the ground (black) to the ground bus on the prototype circuit board. Place CD4007 on the prototype circuit board. Connect pin 14 which is the source node of the p-MOS to the 5-V power supply bus through a multimeter in dc current setting. In other words, connect a jumper wire between the power supply bus on the prototype circuit board to the digital meter current (I) probe. Connect the digital meter common (black) probe to pin 14 of CD4007. Connect pin 7 which is the source node of the n-MOS to the ground bus. Connect two drains at pin 13 and 8 together as the output of the CMOS inverter. The common gate node, pin 6, is the input. Logic 0 or LO corresponds to 0 V and logic 1 or HI corresponds to 5 V. As the input switches from low to high, the p-channel MOSFET switches off while the n-channel MOSFET switches on, hence, the output switches from high to low. Therefore, the circuit is an inverter.

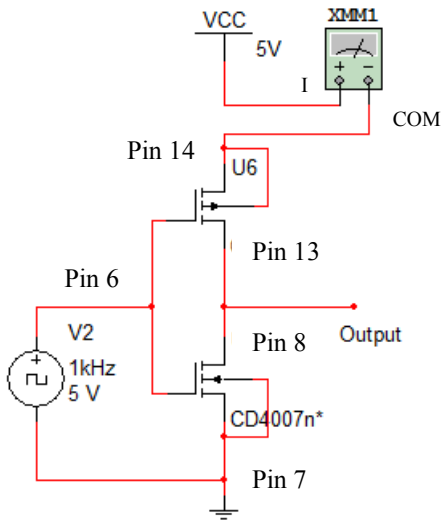

Fig. 3. The schematic diagram of the CMOS inverter. A multimeter in the dc current mode is connected in series from the drain node to power supply to determine the power consumption. It is not needed in normal operation. To study the switching characteristics, a function generator generating a 0 to 5 V clock signal is connected at the input. A dual trace oscilloscope is used to determine the rise and fall time as well as the delay.

Operate the function generator to produce a 100-Hz, 0-5 V triangular wave. You need to set the amplitude to 2.5 V and the offset to 1.25 V. There is a factor of two between actual voltage and displayed value. Do you remember why? Connect the output of the function generator to the input of the inverter. Connect both the input and output to the oscilloscope using dc coupling. Adjust the sensitivity, i.e., vertical scale, of the oscilloscope so that waveforms are as tall as possible but not overshooting the screen. Adjust the time base, i.e., horizontal scale, so that you can see no more than 2 cycles. Save the data of both waveforms displayed on the oscilloscope. Open the data in Excel. Insert a scatter plot. Plot the transfer function, i.e., the output voltage versus the input voltage. Save the Excel file.

The two MOSFETs are in series and at least one of them is in the off state. The steady-state current is almost zero, hence, there is no power consumption during the steady state. A transient current, however, does flow during switching. Therefore, there is energy dissipation but only during switching. The faster the switching rate, the more is the power consumption. This is the reason why a faster cpu would require a better cooling solution and one can extend the battery of a notebook computer by slowing down the cpu clock.

Apply power to the CMOS inverter being tested. Make sure that the multimter only measures the current of this specific inverter, not other circuits on the prototype circuit board sharing the same power bus. Drive the input gate with a 1-kHz square wave. The low and high

levels should be 0 and 5 V, respectively. This can be achieved by properly selecting the amplitude and the offset of the function generator. Attach a 0.1-μF capacitor between the power supply line and the ground on the circuit board to reduce any transient voltage spike due to switching. Use a dual trace oscilloscope to monitor waveforms and confirm that the circuit functions as an inverter. Record the power consumption by measuring the dc current as a function of frequency from 100 Hz to 15 MHz. Power is calculated as the product of current and power supply voltage, i.e., 5 V. At high frequencies, the power may not increase further. In fact, it may slightly decrease. Why? Observe the input and output waveforms at high frequencies. Is the 0-5 V switching complete? Does the output faithfully follow the input as an inverter? At very low frequencies, the power should be nearly zero. If not, check the multimeter connection. Make sure that you are not measuring the current of other circuits on the prototype circuit board.

High linearity is important for analog circuits. On the other hand, timing is crucial for digital operations. The delay between the input and output and the speed of switching are important considerations. Set the frequency of the square wave generated by the function generator to 1 MHz. Record the 10%-90% rise and 90%-10% fall time of the CMOS inverter. Record the delay between the input and output waveforms at the 50% point. Because of bandwidth limitation, the measured data may be longer than the timing information in data the sheet.

Remove the multimeter from the CMOS inverter circuit. Place 74LS00 on the prototype circuit board. Connect pin 14 to the 5-V power supply bus through the multimeter in dc current setting. Connect pin 7 to the ground bus. Tie two input nodes, pins 1 and 2, together forming an inverter. The output node is pin 3. Similarly to the CMOS measurement, measure the power consumption as a function of the clock frequency. Make sure that you are not measuring the power consumption of other chips. Plot power versus frequency. Compare the power consumption of CMOS and low-power Schottky inverters. Which one requires much more power to operate? Remove the multimeter from the low-power Schottky inverter. Disconnect the red probe from the current socket. Reconnect it to the voltage socket.

Turn off and disconnect the function generator. Build three CMOS inverters by connecting pins 1 and 5; pins 8 and 13; pins 2, 11, 14 to 5 V; pins 4, 9, 7 to ground. Cascade three CMOS inverters in series by connecting pins 8 and 3; 5 and 10. Connect the output of the third inverter to the input of the first inverter, i.e., pin 12 to 6. The circuit diagram is shown in Fig. 4. Do not connect any capacitor at this time.

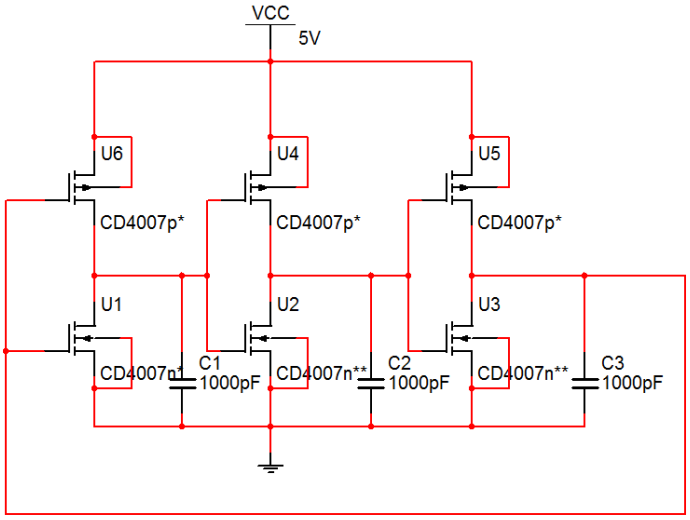

Fig. 4 CMOS ring oscillator. The frequency can be adjusted by loading each inverter with a capacitor.

The circuit oscillates as you activate the power supply. Record the waveform. Measure the frequency of the ring oscillator. The frequency of the ring oscillator is determined by the propagation delay of each inverter and the number of stages used. Please look into the Sedra & Smith book for details. Please note that only odd number of inverters can form a ring oscillator. As discussed previously, it is difficult to measure the intrinsic propagation delay accurately. Furthermore, each inverter has an input capacitance. It becomes a capacitor load to the previous stage. Therefore, don't expect that the theoretical formula will match the experimental data exactly.

The frequency of the ring oscillator can be lowered by loading each inverter with a capacitor. Start with just one capacitor with a moderate capacitance, for example, 100 pF. Increase the capacitance of this capacitor to see how low the frequency can become before oscillation stops. To reach even lower frequencies, you can try adding one capacitor to each inverter. Record the capacitance added to each inverter and the oscillation frequency. Record the waveform of the oscillator at the lowest frequency that you have tried. Can you build an oscillator at a specific frequency during the in-lab test?

Activities After the Laboratory Session

Prepare and submit a Powerpoint presentation file. Include the scoring sheet. Check the scoring sheet so that you won't leave any data out.

Self Study

1. What is CMOS? What is the main advantage of CMOS?

2. What is an inverter?
3. Can you explain the frequency dependence of the power consumption of a CMOS inverter?
4. What is the delay time of the CMOS inverter? Why do cascaded inverters with feedback oscillate? Does the number of cascaded stages play any role?
5. What are differences between CMOS and low-power Schottky gates?

Cover and Score Sheet

Experiment 7 – CMOS Inverter and Ring Oscillators

Author:_____ Partner:_____

Score

Item	Credit	Score
Data	5	
CMOS Inverter Circuit		
Transfer Function		
Acquired Waveforms With Rise and Fall Time, Delay		
Plot of Power Consumption as a Function of Frequency		
Low-Power Schottky Inverter Circuit		
Plot of Power Consumption as a Function of Frequency		
Ring Oscillators		
Acquired Waveform; Oscillation Frequency - CMOS		
Table of Frequency Versus Capacitance		
Acquired Waveform at Low Frequency		
Format and Contents	3	
Total	**8**	

TA Signature:_____ Date:_____