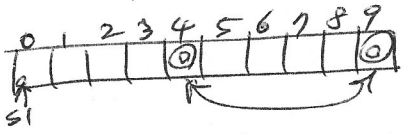
Assign 4 Key

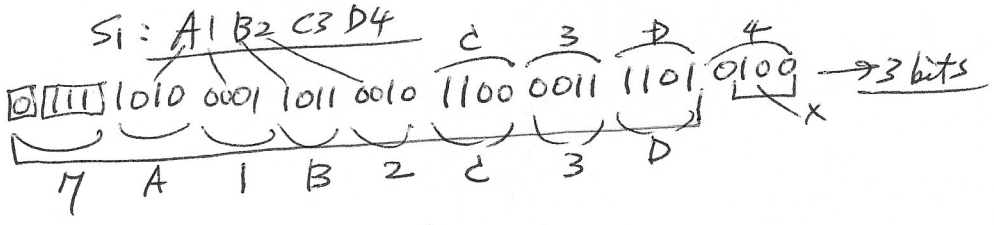
#1.




```
lw $t1, 16($s1);   A[4] → t1
lw $t2, 36($s1);   A[9] → t2
sw $t1, 36($s1);   t1 → A[9]
sw t2, 16($s1);    t2 → A[4]
```

#2.

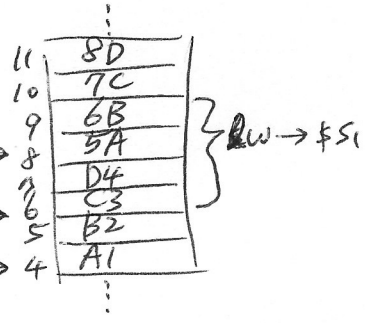
```
sar $t1, $s1, 3
slr $t2, $t1, 1
```



7A1B2C3D

#3.

```
sw $s1, 4($zero);   ①
sw $s2, 8($zero);   ②
lw $s1, 6($zero);   ③
```



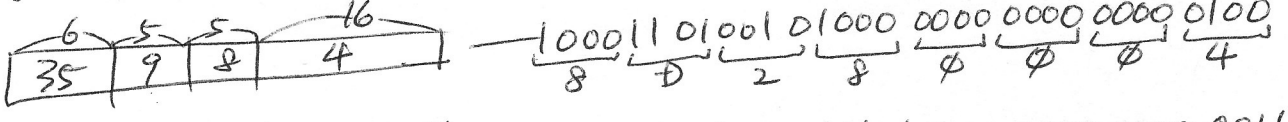
⇒ $s1 : C3 D4 5A 6B

⇒ 4 memory accesses.

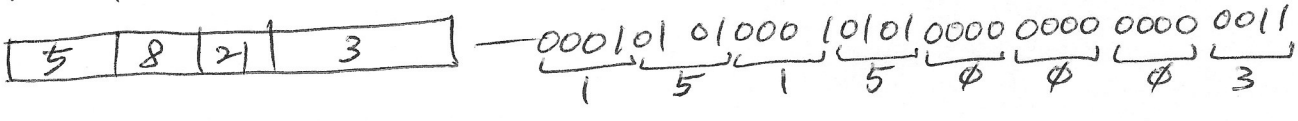
#4. (a)

```
add $t1, $s2, $s1;   — R — register addressing mode
lw  $to, 4($t1);     — I — base/displacement "
bne $to, $s5, End;   — I — pc-relative "
addi $s1, $s1, 2;    — I — immediate "
subi $s1, $s1, 1;    — I — immediate "
j start;             — J — pseudo-direct "
```

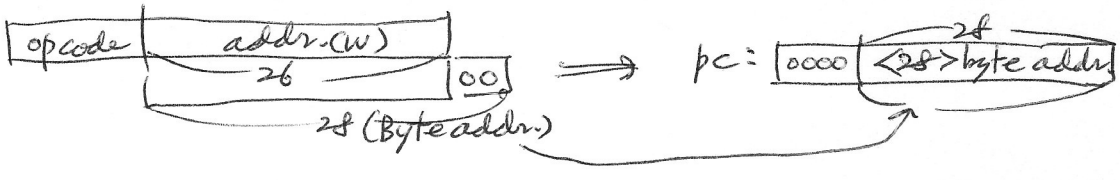
(b)



(c)



#5.



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