Memory hierarchy simulation programming

0. Prepare data structures for register_file, cache, and main_memory modules;

Logic:

1. Read a machine instruction from input data file;
2. Decode (analyze) the instruction:
   - determine opcode (lw: 35, sw: 43);
   - determine rs and rt register numbers;
   - determine byte_offset value;
3. Compute effective memory address (byte address) and convert it to a word address;
4. From the word address, compute cache index and tag values using MOD and DIV;
5. Search cache and do read/write operation, i.e., one of
   {read_hit, read_miss, write_hit, write_miss};
6. repeat step 1~5 for each instruction in the input data file (while loop until EOF).