

A

Major Project Report on

TITLE OF THE THESIS

Submitted in the Partial Fulfillment of the

Requirements

for the Award of the Degree of

BACHELOR OF TECHNOLOGY

in

Electronics and Communication Engineering

Submitted by

STUDENT 1 NAME STUDENT 1 Roll Number

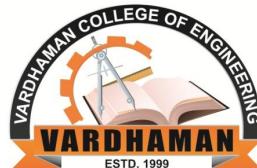
STUDENT 2 NAME STUDENT 2 Roll Number

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Under the esteemed guidance of

NAME OF SUPERVISOR

DESIGNATION

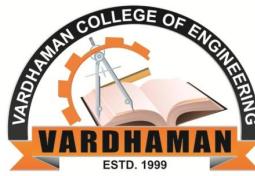


Department of Electronics and Communication Engineering

VARDHAMAN COLLEGE OF ENGINEERING, HYDERABAD

An Autonomous Institute Affiliated to JNTUH

2020-21



VARDHAMAN COLLEGE OF ENGINEERING, HYDERABAD
An Autonomous Institute Affiliated to JNTUH

Department of Electronics and Communication Engineering

CERTIFICATE

This is to certify that the project titled **TITLE OF THE THESIS** is carried out by

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STUDENT 2 NAME STUDENT 2 Roll Number
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in partial fulfillment of the requirements for the award of the degree of **Bachelor of Technology in Electronics and Communication Engineering** during the year 2020-21.

Signature of the Supervisor
NAME OF SUPERVISOR
DESIGNATION

Signature of the HOD
Dr. G.A.E. Satish Kumar
Professor and Head, ECE

Project Viva-voce held on _____

Internal Examiner

External Examiner

ACKNOWLEDGMENT

The satisfaction that accompanies the successful completion of the task would be put incomplete without the mention of the people who made it possible, whose constant guidance and encouragement crown all the efforts with success.

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STUDENT 1 NAME
STUDENT 2 NAME
STUDENT 2 NAME

ABSTRACT

The Department of Electronics and Communication Engineering has been playing a vital role in producing quality engineers ever since it was established in the year 1999. The department runs one under graduate program and two post graduate programs to cater to the ever – changing needs of technical excellence in all areas of Electronics and Communication Engineering such as VLSI Design, Embedded Systems, Telecommunications, Signal Processing etc. The intake for undergraduate Program (B. Tech) is 240. The department also offers Post Graduation programs with specialization in Digital Electronics and Communication Systems (DECS) and Embedded Systems (ES) with an intake of 18 each.

The Department is headed by Dr. G.A.E Satish Kumar having vast teaching experience and ably supported by highly qualified faculty with an unparallel level of expertise in their field. The Department constitutes 10 Professors, 12 Associate Professors and 30 Assistant Professors.

The UG Program has been accredited by the National Board of Accreditation (NBA) till the year 2021.

Keywords: ky1; ky2; ky3; ky4

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ABBREVIATIONS

Abbreviation	Description
VCE	Vardhaman College of Engineering
CMOS	Complementary Metal Oxide Semiconductor

CHAPTER 1

INTRODUCTION

1.1 A Section

Lorem ipsum[1] Binary addition is the single most important operation that a processor performs. Most of the adders have been designed for synchronous circuits even though there is a strong interest in clockless/asynchronous processors/circuits. Asynchronous circuits do not assume any quantization of time. Therefore, they hold great potential for logic design as they are free from several problems of clocked (synchronous) circuits. In principle, logic flow in asynchronous circuits is controlled by a request-acknowledgment handshaking protocol to establish a pipeline in the absence of clocks. Explicit handshaking blocks for small elements, such as bit adders, are expensive. Therefore, it is implicitly and efficiently managed using dual-rail carry propagation in adders. A valid dual-rail carry output also provides acknowledgment from a single-bit adder block. Thus, asynchronous adders are either based on full dual-rail encoding of all signals (more formally using null convention logic that uses symbolically correct logic instead of Boolean logic) or pipelined operation using single-rail data encoding and dual-rail carry representation for acknowledgments. While these constructs add robustness to circuit designs, they also introduce significant overhead to the average case performance benefits of asynchronous adders. Therefore, a more efficient alternative approach is worthy of consideration that can address these problems.

1.1.1 Part of a section

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1.1.2 How to insert a image

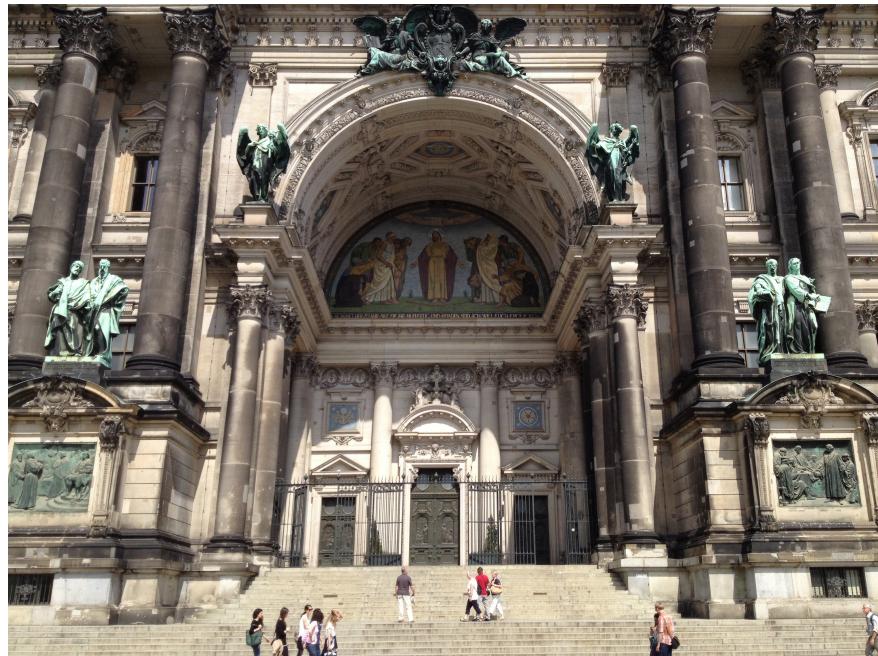


Figure 1.1: Give Figure Caption here

FIRST PUT YOUR FIGURE(JPG FORMAT) IN FIGURES FOLDER.
COPY THE ABOVE LINES. PASTE IT WHERE YOU WANT TO INSET
THE FIGURE.REPLACE BERLIN BY THE FIGURE NAME

1.2 Equation Inserting

Open the word file. Click on the equation written in MathType. Go to Mathtype Tab at the top. You will find a option ToggleTex. Click and copy the codes here.

$$I = -C_{out} \frac{dV_{out}}{dt} = \frac{\beta_n}{2} (2(V_{DD} - V_{Tn}) V_{out} - V_{out}^2)$$

$$\int \frac{dV_{out}}{2(V_{DD} - V_{Tn})V_{out} - V_{out}^2} = - \int \frac{\beta_n}{2C_{out}} dt$$

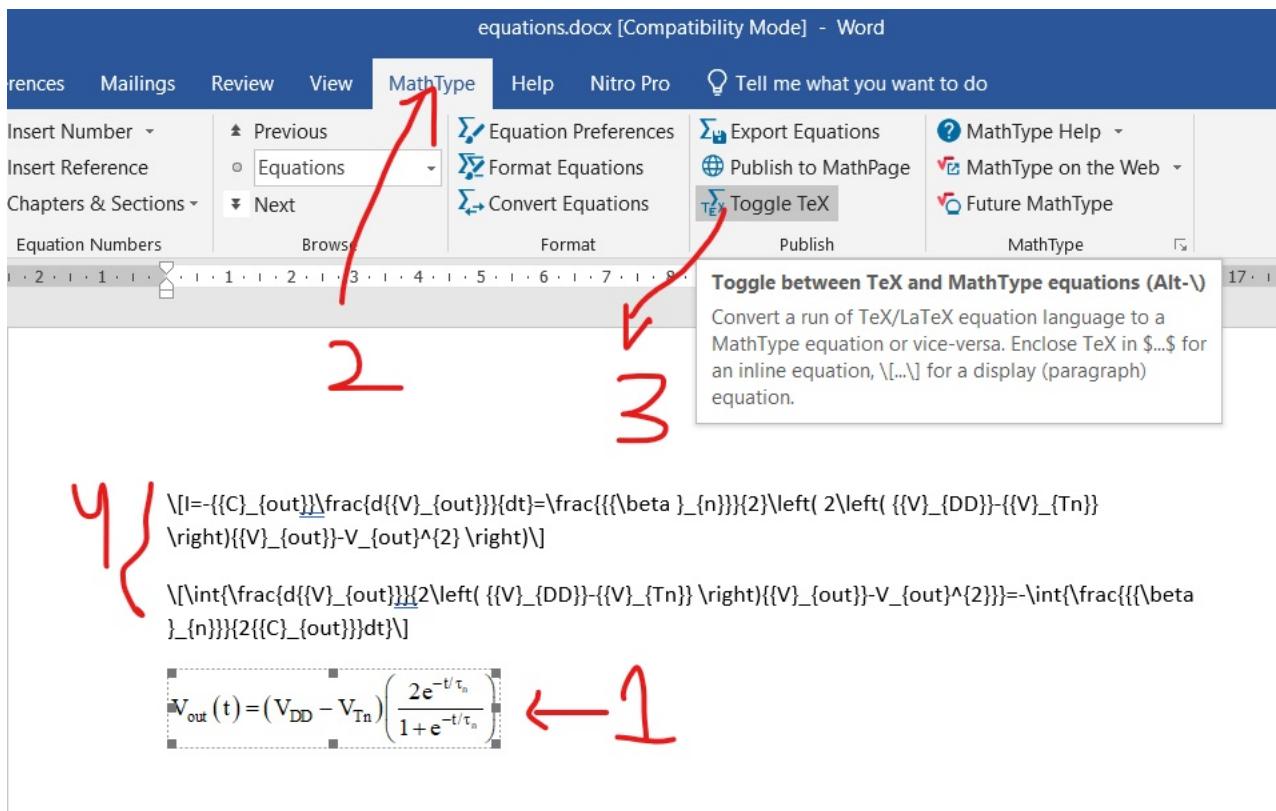


Figure 1.2

$$V_{out}(t) = (V_{DD} - V_{Tn}) \left(\frac{2e^{-t/\tau_n}}{1 + e^{-t/\tau_n}} \right)$$

Table 1.1: Table Caption

Sr No	Multicolumn Header		
	DataHeader1	DataHeader2	DataHeader3
1	data1	data2	data3
2	data1	data2	data3
3	data1	data2	data3
4	data1	data2	data3

Table 1.2: Table Caption

Surface	Material	Hardness					
		Soft		Medium		Hard	
		Factors					
		A	B	A	B	A	B
Base Metal	Cast Iron	10	20	30	40	50	60
	Steel	70	80	90	100	110	120
Base Metal	Cast Iron	10	20	30	40	50	60
	Steel	70	80	90	100	110	120
Base Metal	Cast Iron	10	20	30	40	50	60
	Steel	70	80	90	100	110	120

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