

# CSCE 616: Introduction to Hardware Design Verification

Lab-10: HTAX Regression

Bug Report

Name: Sai Surendra Reddy Yaraballi

UIN: 333002926

The vmanager regression result is shown below:

The screenshot shows the vManager Regression Center interface. The top navigation bar includes 'vManager', 'Regression', 'Analysis', 'Planning', and 'Tracking'. The 'Regression' tab is active. Below the navigation bar, there are several toolbars for session management and analysis. The main area displays a table of regression sessions. The session 'htax\_regres.sai\_surendra.23\_12\_05\_16\_48\_46...' is highlighted, showing a status of 'completed' and a progress bar. The table columns include Session Status, Name, Total Runs, #Passed, #Failed, #Running, #Waiting, #Other, Start Time, and Owner. The session has 250 total runs, 244 passed, and 6 failed. The start time is 12/5/23 4:48 PM, and the owner is sai\_surendra.

Session Status	Name	Total Runs	#Passed	#Failed	#Running	#Waiting	#Other	Start Time	Owner
completed	htax_regres.sai_surendra.23_12_05_16_48_46...	250	244	6	0	0	0	12/5/23 4:48 PM	sai_surendra

Showing 1 out of 678 items

The svseed number for the failed test case is taken from xlog file

The screenshot shows the vManager Analysis Center interface. The top navigation bar includes 'vManager', 'Regression', 'Analysis', 'Planning', and 'Tracking'. The 'Analysis' tab is active. Below the navigation bar, there are several toolbars for analysis and session management. The main area displays a table of test runs. The test case 'ASRST.assert\_eot\_timeout\_check' is highlighted, showing a status of 'failed' and a duration of 8 seconds. The test case description is 'Assertion top\_inst\_htax\_rx\_inf[3].assert\_eot\_timeout\_check has run 86 script exited with exit status 2. See /home/gr...'. The log file 'xrun.log' is open, showing the test case details and the svseed number 212585452.

Index	Name	Status	Duration (sec)	Top Filter
229	/all_test/test9	passed	16	n/a
230	/all_test/test9	passed	16	n/a
231	/all_test/test9	passed	15	n/a
233	/all_test/test9	passed	17	n/a
234	/all_test/test9	passed	16	n/a
235	/all_test/test9	passed	16	n/a
236	/all_test/test9	passed	15	n/a
237	/all_test/test9	passed	15	n/a
238	/all_test/test9	passed	15	n/a
239	/all_test/test9	passed	14	n/a
240	/all_test/test9	passed	16	n/a
241	/all_test/test9	passed	15	n/a
242	/all_test/test9	passed	15	n/a
243	/all_test/test9	passed	16	n/a
244	/all_test/test9	passed	15	n/a
245	/all_test/test9	passed	16	n/a
246	/all_test/test9	passed	15	n/a
247	/all_test/test9	passed	16	n/a
248	/all_test/test9	passed	16	n/a
249	/all_test/test9	passed	15	n/a
250	/all_test/test9	passed	16	n/a
86	/all_test/test9	failed	8	n/a
97	/all_test/test9	failed	17	n/a
155	/all_test/test9	failed	9	n/a
196	/all_test/test9	failed	11	n/a
222	/all_test/test9	failed	16	n/a

Showing 250 items

ASRST.assert\_eot\_timeout\_check

Assertion top\_inst\_htax\_rx\_inf[3].assert\_eot\_timeout\_check has run 86 script exited with exit status 2. See /home/gr...

svseed set randomly from command line: 212585452

vm\_brn.log xrun.log local\_log.log

286 xmsim: \*W.DLCVAR (/home/grads/s/sai\_surendra/cds.lib.13): cds.lib invalid environment var

287 Loading snapshot worklib.top.v Done

288 SVSEED set randomly from command line: 212585452

289 xmsim: \*W.DSEM2009: This SystemVerilog design is simulated as per IEEE 1800-2009 SystemV

290 Writing initial vsf to /home/grads/s/sai\_surendra/csc616/HTAX/lab-10-saisurendra96/lab1t

291 xcellum- source /opt/coe/cadence/XCELLUM/tools/xcellum/files/xmsimrc

292 xcellum- source /opt/coe/cadence/XCELLUM/tools/methodology/UVM/CDNS-1.1d/sw/files/t

293 xcellum- database -open waves -into waves.shm -default

294 Created default SHM database waves

295 xcellum- probe -create top-all -memories -depth all -tasks -functions -all -database waves -w

296 xmsim: \*W.PFRFTNEV: (-FUNCTION) Database must be opened in -EVENT mode to capture c

297 Created probe 1

298 xcellum-

299 xcellum- run

300 -----

301 CDNS-UVM-1.1d (22.09-s004)

302 (C) 2007-2013 Mentor Graphics Corporation

303 (C) 2007-2013 Cadence Design Systems, Inc.

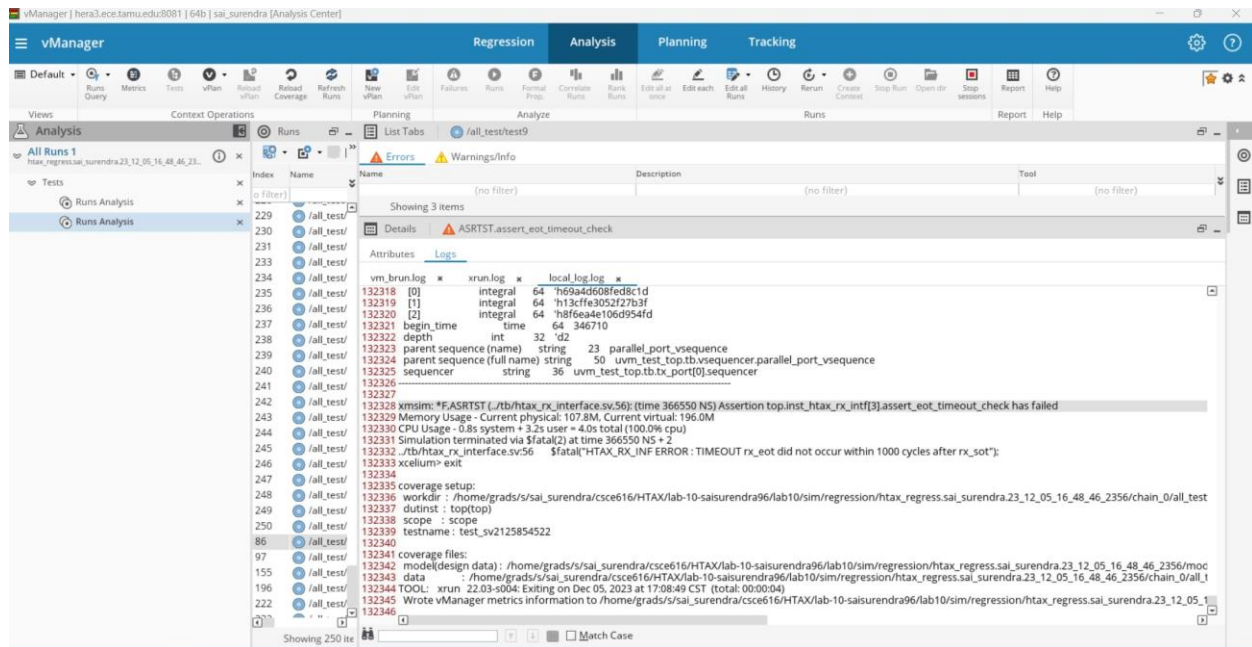
304 (C) 2006-2013 Synopsys, Inc.

305 (C) 2011-2013 Cypress Semiconductor Corp.

306 -----

307 \*\*\*\*\* IMPORTANT RELEASE NOTES \*\*\*\*\*

308 -----



After taking the seed number enter the command

`irun -f run.f +UVMTESTNAME=parallel_port +svseed [seednumber]`

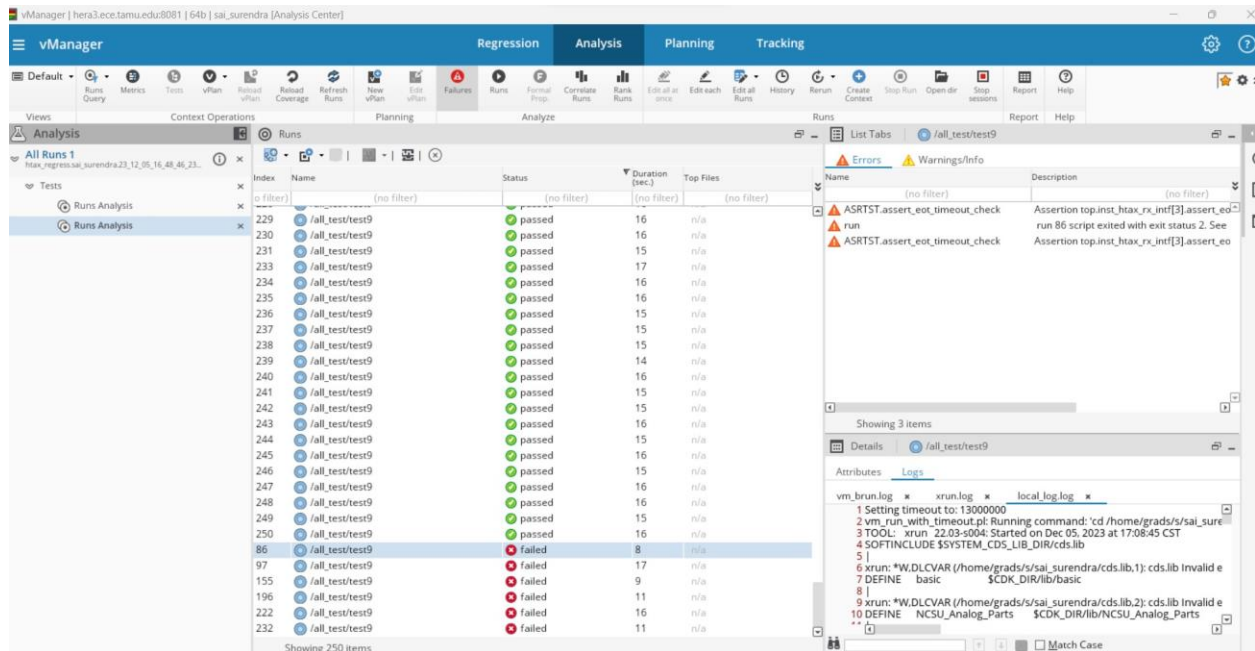
then we can see the logs more clearly for that particular testcase.

The error is shown below:

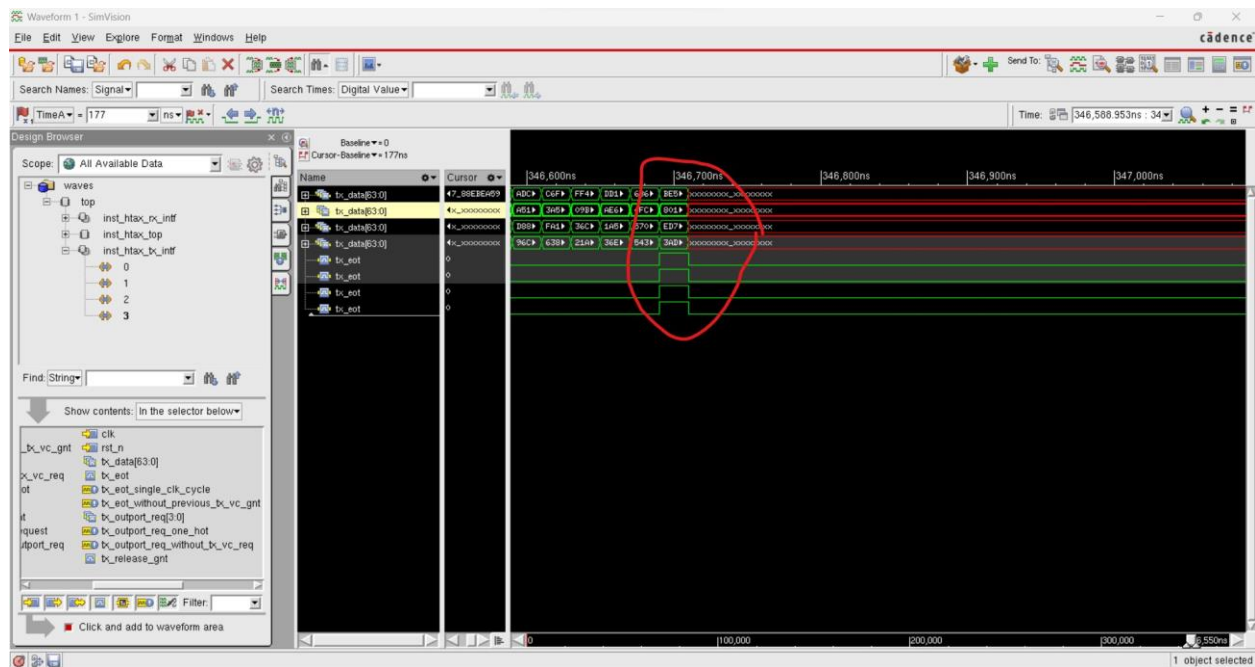
```
xmsim: *F,ASRTST (../tb/htax_rx_interface.sv,56): (time 366550 NS) Assertion top.inst_htax_rx_intf[3].assert_eot_timeout_check has failed
Memory Usage - Current physical: 105.9M, Current virtual: 192.1M
CPU Usage - 1.6s system + 3.5s user = 5.1s total (99.7% cpu)
Simulation terminated via $fatal(2) at time 366550 NS + 2
../tb/htax_rx_interface.sv:56 $fatal("HTAX_RX_INF ERROR : TIMEOUT rx_eot did not occur within 1000 cycles after rx_sot");
xcelium> exit

coverage setup:
workdir : ./cov work
```

After the regression test and after running the failure testcase, I can see that there is an error in the tx\_eot signal.



After opening the waveform, I found the issue.



In the above waveform, I can see that when tx\_eot is one at the same time for different ports, the data packet is getting corrupted.

For the fix, I have checked the design where the tx\_eot signal is evaluated. In design/htax\_outport\_data\_mux.sv file, selected\_eot is assigned to eot when if condition is true.

```

sot_out <= {VC{1'b0}};
if (!inport_sel_reg && !eot_out || (!selected_sot && (!inport_sel && !any_gnt) )))
    eot_out <= selected_eot;

```

Backtraced the code and find the issue in the line

```
assign selected_eot = |(eot_in & inport_sel_reg) & ~(&(eot_in));
```

I removed the `& ~(&(eot_in))` part in the above line.

The fixed code line for the bug fix is

```
assign selected_eot = |(eot_in & inport_sel_reg);
```

After bug fix, the waveform is

