Digital-FIR-Filter-Design-Using-FPGA

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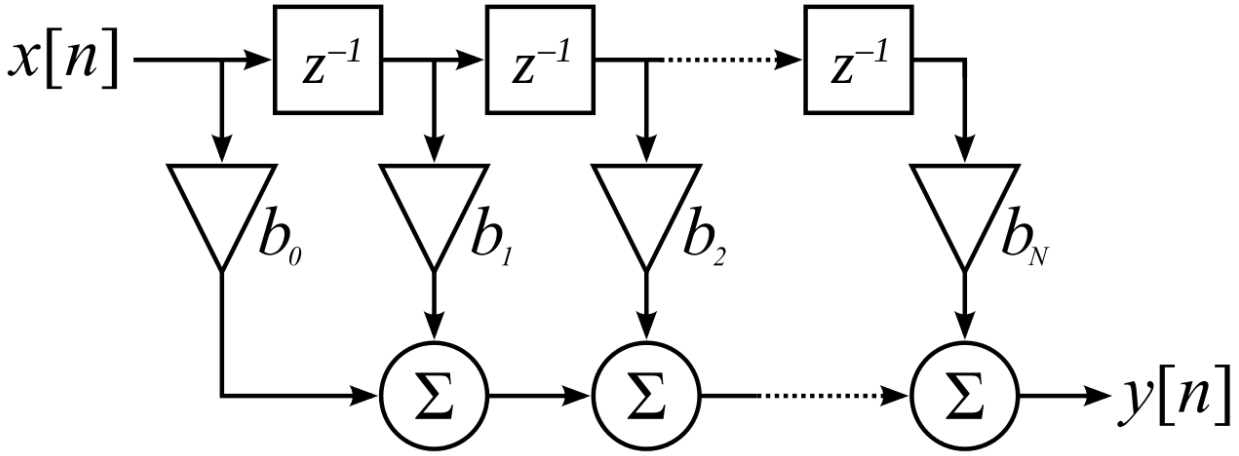
Introduction and Equations

In signal processing, a finite impulse response (**FIR**) **filter** is a **filter** whose impulse response (or response to any finite length input) is of finite duration, because it settles to zero in finite time.



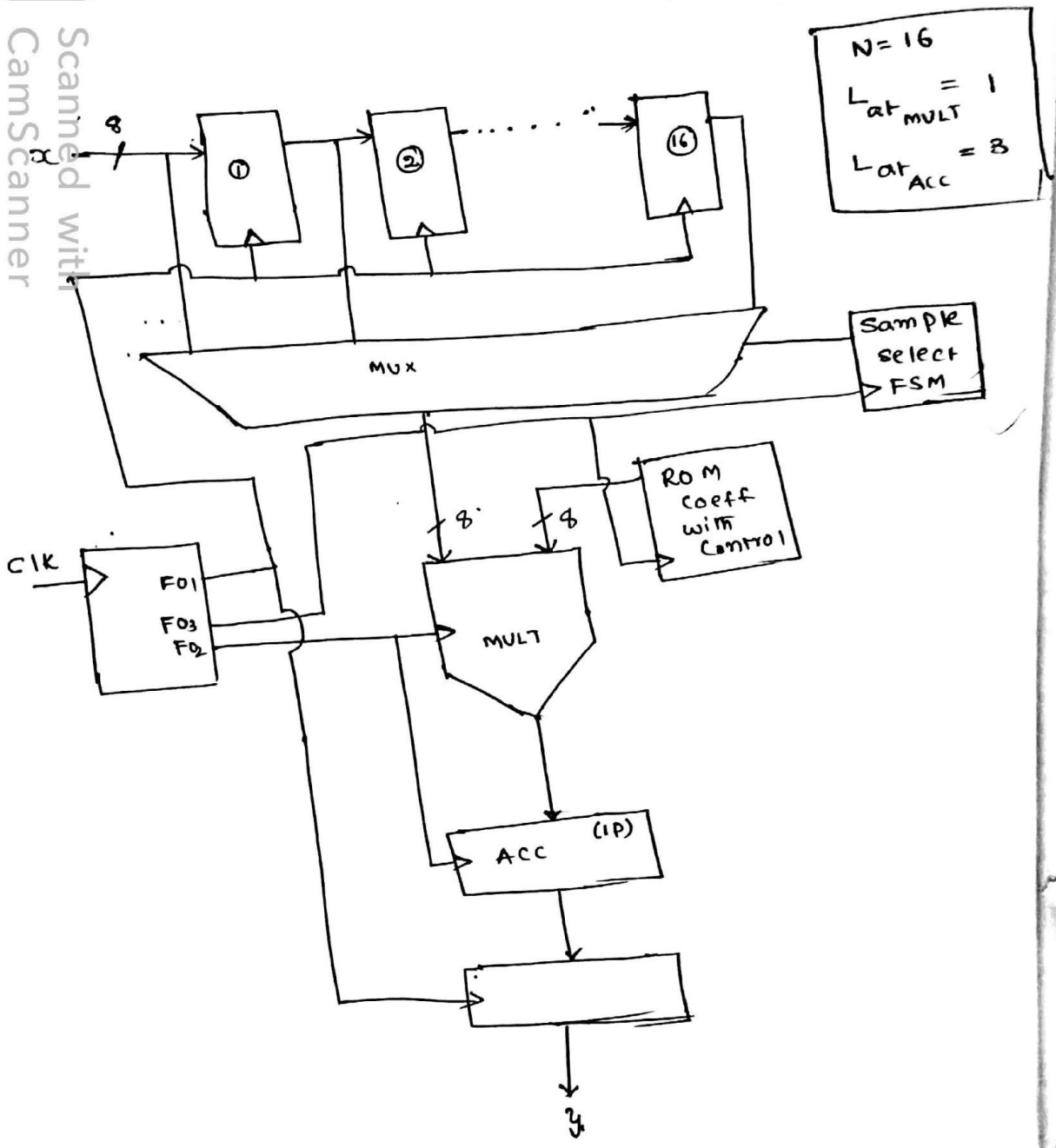
From the above image it follows that:

$$y[n] = b_0 x[n] + b_1 x[n-1] + \cdots + b_N x[n-N]$$
$$= \sum_{i=0}^{N} b_i \cdot x[n-i],$$

Architecture

To implement the above equation in verilog we came up with the following architecture.Inputs are taken in a shift register which are the inputs to a 16x1 Mux. Then the filter coefficients are stored in a ROM, and using a counter suitable input is multiplied with the corresponding filter coefficient and then these products are added using an accumulator. After all the products are added the output is taken from the accumulator and the accumulator is reset for calculating the next filtered value.The following image outlines the above description.

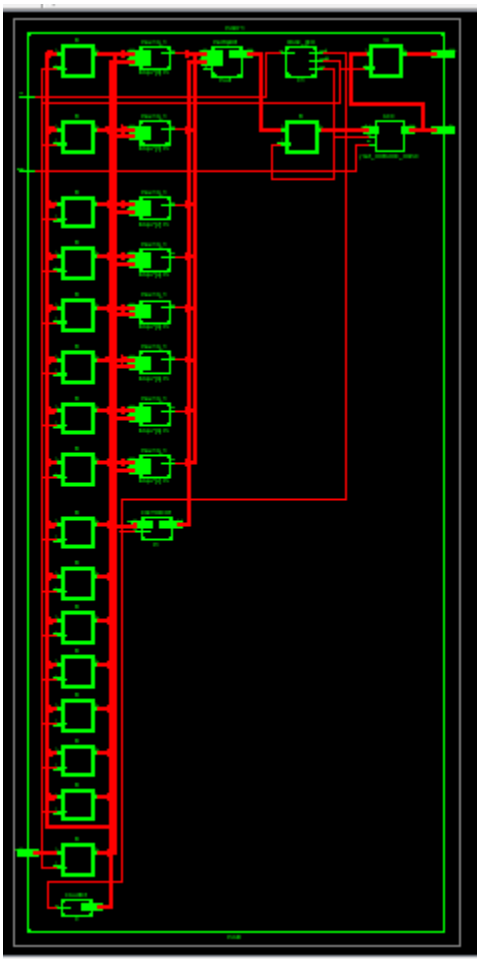
FIR FILTER USING MAC



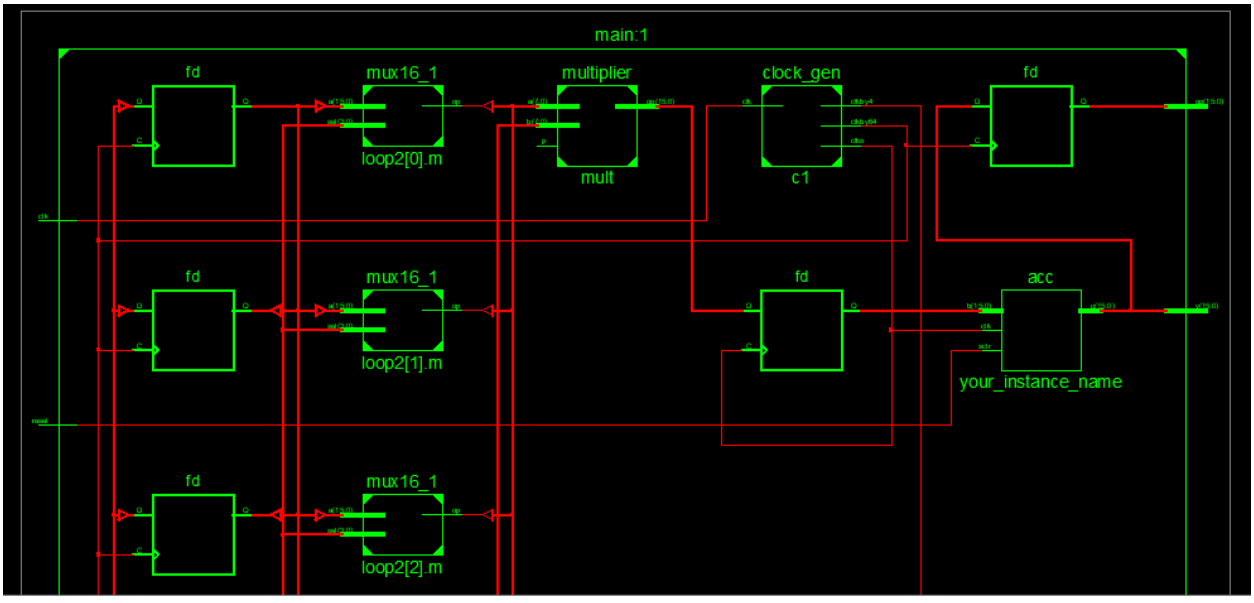
$$y = a_0 x(n) + a_1 x(n-1) + a_2 x(n-2) + \cdots + a_{15} x(n-15)$$

$$FO_2 = F_{CLK}\ ;\quad FO_3 = \frac{F_{CLK}}{L_{at_{MULT}} + L_{at_{ACC}}}\ ;\quad FO_1 = \frac{F_{CLK}}{N\left[L_{at_{MULT}} + L_{at_{ACC}}\right]}$$

RTL Schematic



Magnified view



Modules used:-

- Multiplexer 16x1
- Baugh Wooley Multiplier: Used for signed multiplication.
- Accumulator: From IPCORE
- Counter: To keep track of input from shift register
- Clock generator
- ROM : To store FIR filter coefficient. Also implemented from IPCORE

Simulation Results:-

Hardware utilization:-

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Device utilization summary:
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Selected Device : 6slx16csg324-2


Slice Logic Utilization:
 Number of Slice Registers:             211  out of  18224     1%
 Number of Slice LUTs:                  153  out of   9112     1%
    Number used as Logic:               153  out of   9112     1%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    294
   Number with an unused Flip Flop:      83  out of    294    28%
   Number with an unused LUT:           141  out of    294    47%
   Number of fully used LUT-FF pairs:    70  out of    294    23%
   Number of unique control sets:         4

IO Utilization:
 Number of IOs:                         42
 Number of bonded IOBs:                 42  out of    232    18%
    IOB Flip Flops/Latches:             16

Specific Feature Utilization:
 Number of Block RAM/FIFO:               1  out of     32     3%
    Number using Block RAM only:         1
 Number of BUFG/BUFGCTRLs:               2  out of     16    12%
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=========================================================================
HDL Synthesis Report

Macro Statistics
# Registers                                          : 13
 1-bit register                                      : 10
 128-bit register                                    : 1
 16-bit register                                     : 2
# Multiplexers                                       : 20
 1-bit 2-to-1 multiplexer                            : 20
# Xors                                               : 122
 1-bit xor2                                          : 122

=========================================================================
=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# Registers                                          : 170
 Flip-Flops                                          : 170
# Multiplexers                                       : 20
 1-bit 2-to-1 multiplexer                            : 20
# Xors                                               : 122
 1-bit xor2                                          : 122

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Timing and speed results:-

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Timing Summary:
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Speed Grade: -2

   Minimum period: 3.002ns (Maximum Frequency: 333.111MHz)
   Minimum input arrival time before clock: 3.654ns
   Maximum output required time after clock: 4.202ns
   Maximum combinational path delay: No path found

Timing Details:
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All values displayed in nanoseconds (ns)

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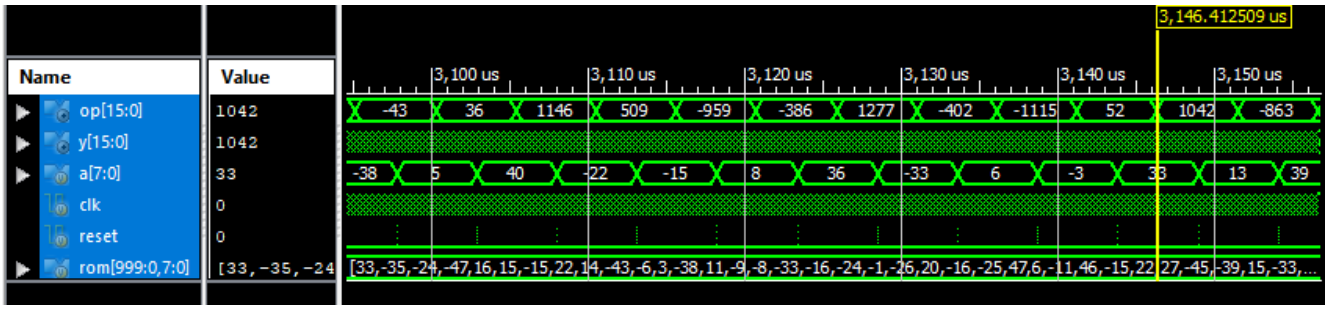
Timing constraint: Default period analysis for Clock 'c1/j6/q'
  Clock period: 1.324ns (frequency: 755.287MHz)
  Total number of paths / destination ports: 120 / 120
-------------------------------------------------------------------------
Delay:               1.324ns (Levels of Logic = 0)
  Source:            ip_0_0 (FF)
  Destination:       ip_0_8 (FF)
  Source Clock:      c1/j6/q rising
  Destination Clock: c1/j6/q rising
```

Simulation output example:



Discussion:-

This whole project was designed using a structural coding approach. For example to design a 16x1 Mux, 4x1 Muxes were used which were also designed using 2x1 Muxes. Even the clock generator and counter were generated using sequential logical circuits using JK Flip-Flops as the building blocks.

To reset the accumulator after taking the output, a reset input pulse was generated in the test bench as the synchronous clear(Sclr) input of the accumulator was level triggered and not edge triggered.

All the given inputs and coefficients were converted to Binary using Matlab. To initialize inputs in ROM the binary values were written in .coe format. Input is read from a text file and output is written into one for further analysis.

Reference:

- Zhou Yajun, Pingzheng Shi, "Distributed Arithmetic for FIR Filter implementation on FPGA", *Multimedia Technology (ICMT) 2011 International Conference*, 2011.
- A. T. Erdogan and T. Arslan "Low Power FIR Filter Implementations Based on Coefficient Ordering Algorithm". IEEE Computer Society Annual Symposium on VLSI Emerging Trends in VLSI Systems Design, 2004 IEEE.