AIC-project (neural amplifier)

2020102024

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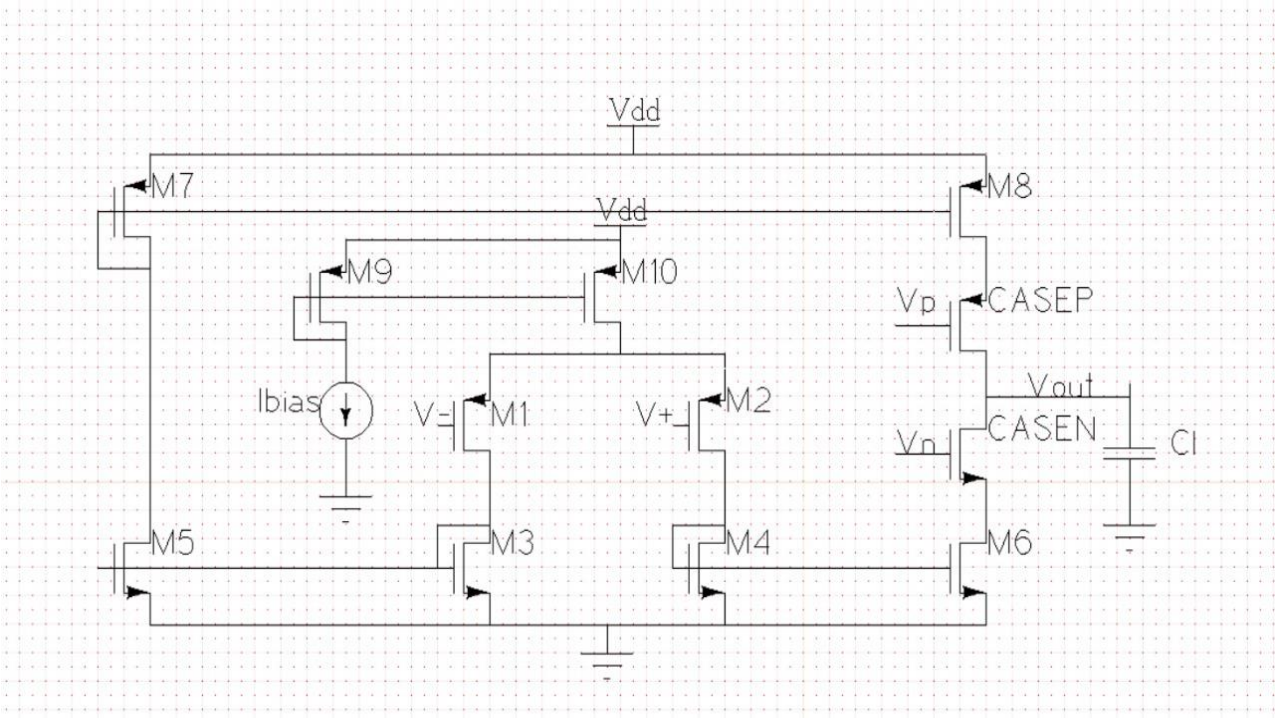
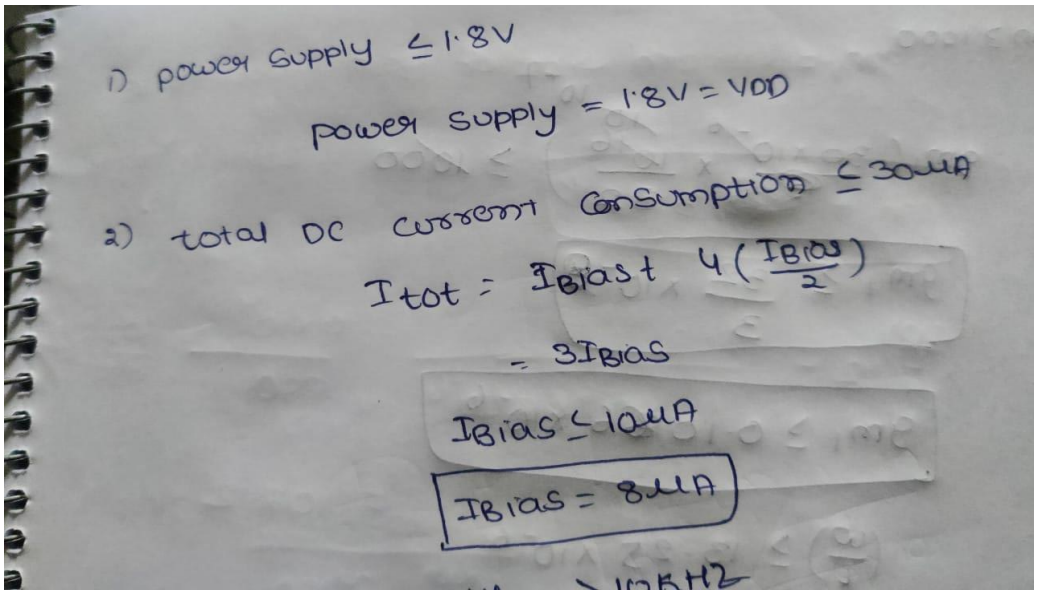
(a) Clearly draw the OTA schematic (Fig. 4 in the paper) using xcircuit or some other drawing software and label the transistors, resistors, and capacitors.

by using the x-circuit I have drawn Ota with a load capacitance 'CL'

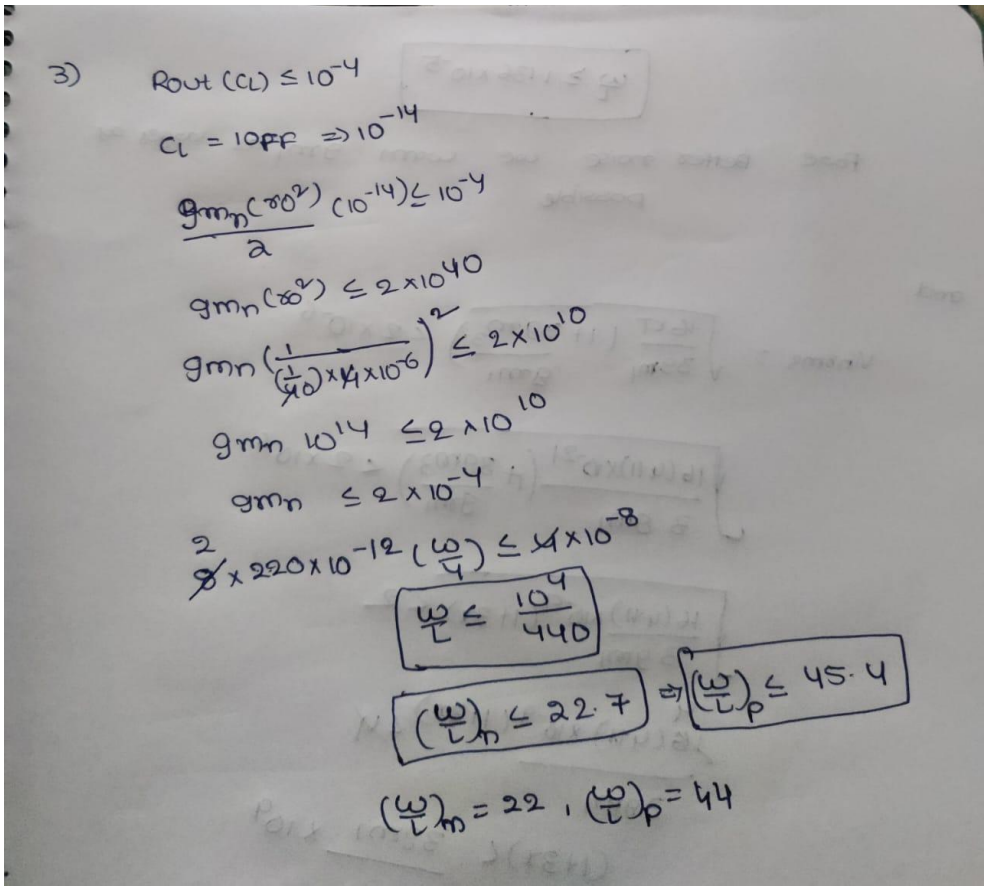


The naming of the transistors is same the naming shown in the paper.

(b) Show the step-by-step procedure and calculations for OTA design.

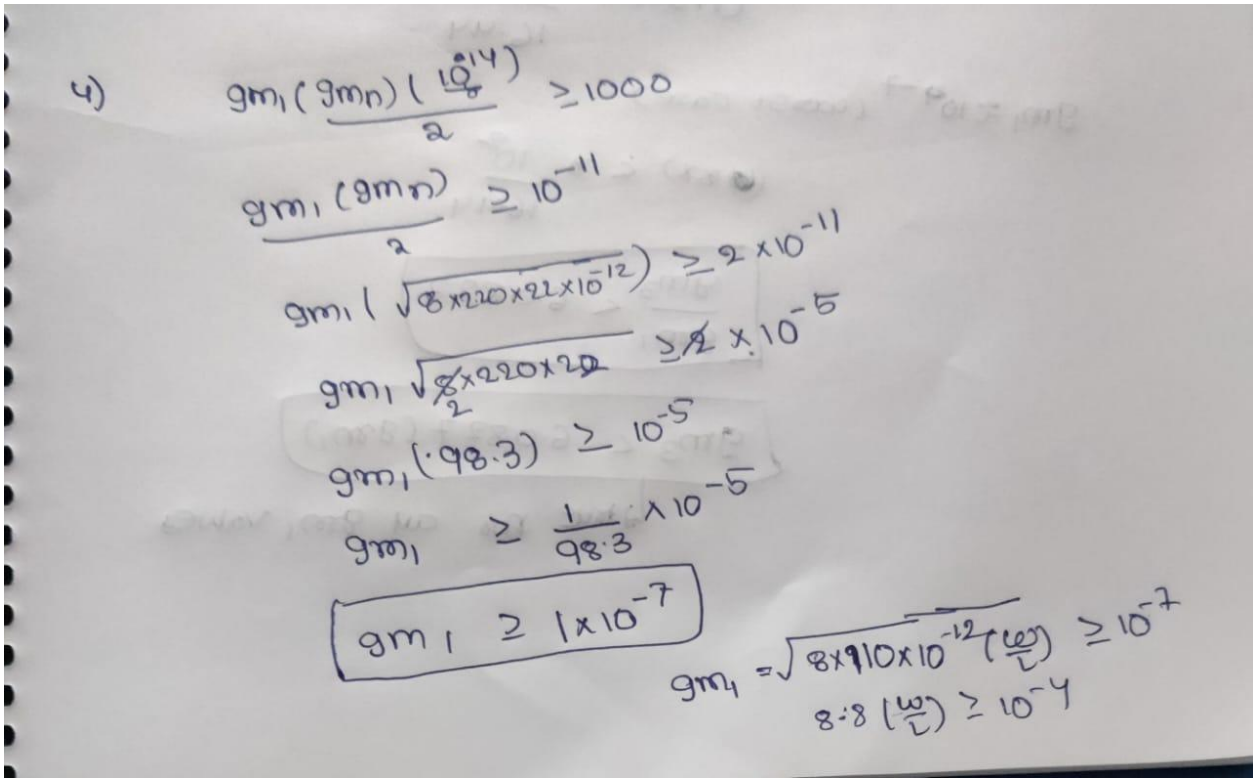


Calculation of gmn and gmp of capcodes form bandwidth



from above calculations we have calculated w/L of caseN ,caseP transistors and also we have taken $\lambda = 0.025$, and load capacitance to be 10fF.

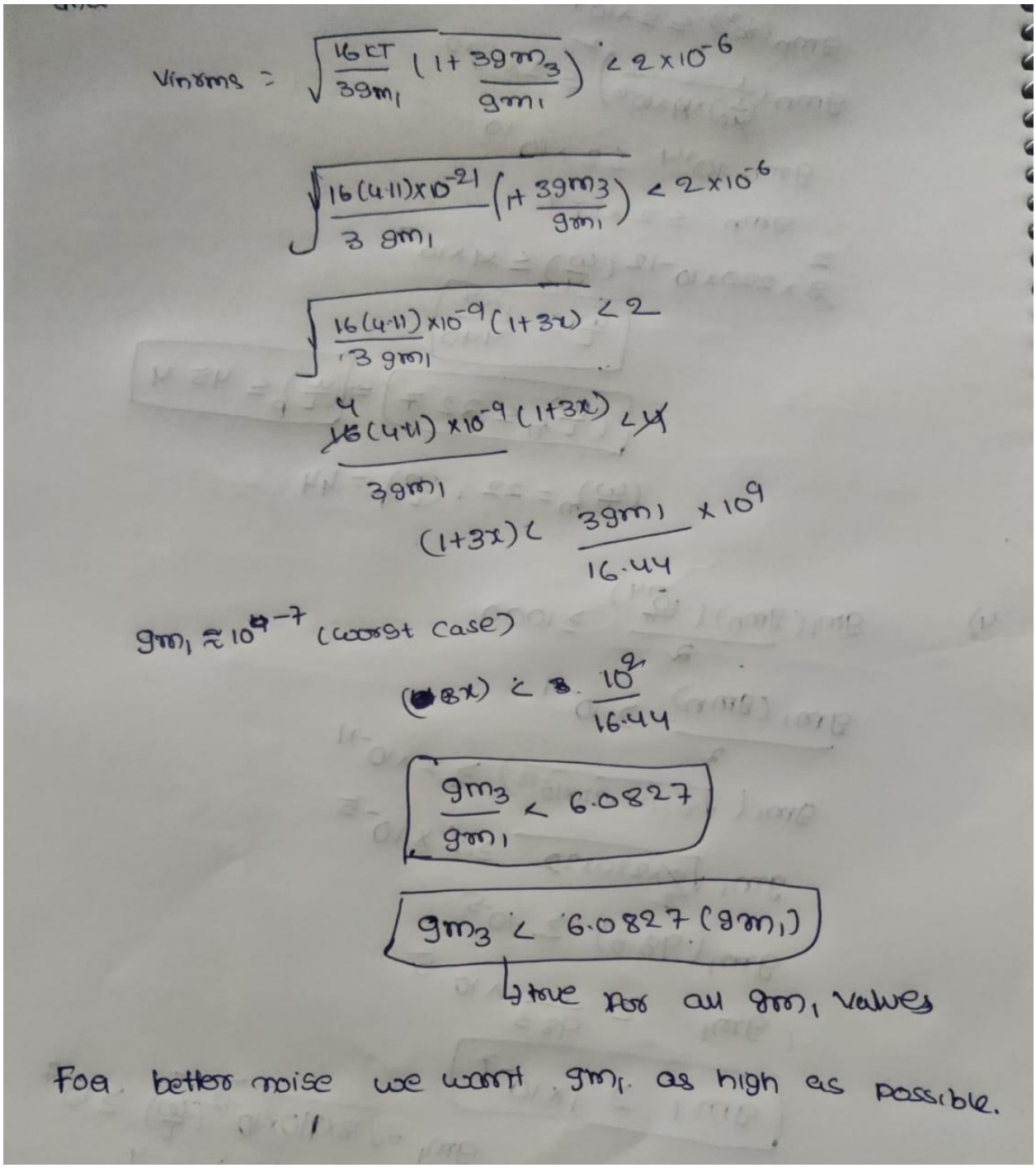
calculation of the gm for the Mosfets M1, M2 from gain:-



Here we have calculated the gm for M1 and M2 using the dc gain of the amplifier and the current through these mosfets the UnCox is 220U(simulations) and UpCox is 110U.

From above we will get $\frac{W}{L} \geq 1.136 * 10^{-5}$

Then we will calculate the NEF which for these calculations is 3.7822 this can be decreased increasing the bandwidth which can be done by decreasing the capacitance to half the given value.



And by using the input referred noise we can calculate the gm3, gm7 for simplification we have taken gm3=gm7 but when we are trying to find w/l we can use range to find those values.

When we convert $gm3 < 6.0827 \cdot gm1$ to W/l then we will get

$$\left(\frac{w}{l}\right)_3 \leq 18 \cdot \left(\frac{w}{l}\right)_1$$

$$\left(\frac{w}{l}\right)_7 \leq 36 \cdot \left(\frac{w}{l}\right)_1$$

If we want better input referred noise,
we must reduce gm3 and increase gm1 this way input referred noise is decreased.

(c) Tabulate the design parameters (W, L, R, C, I).

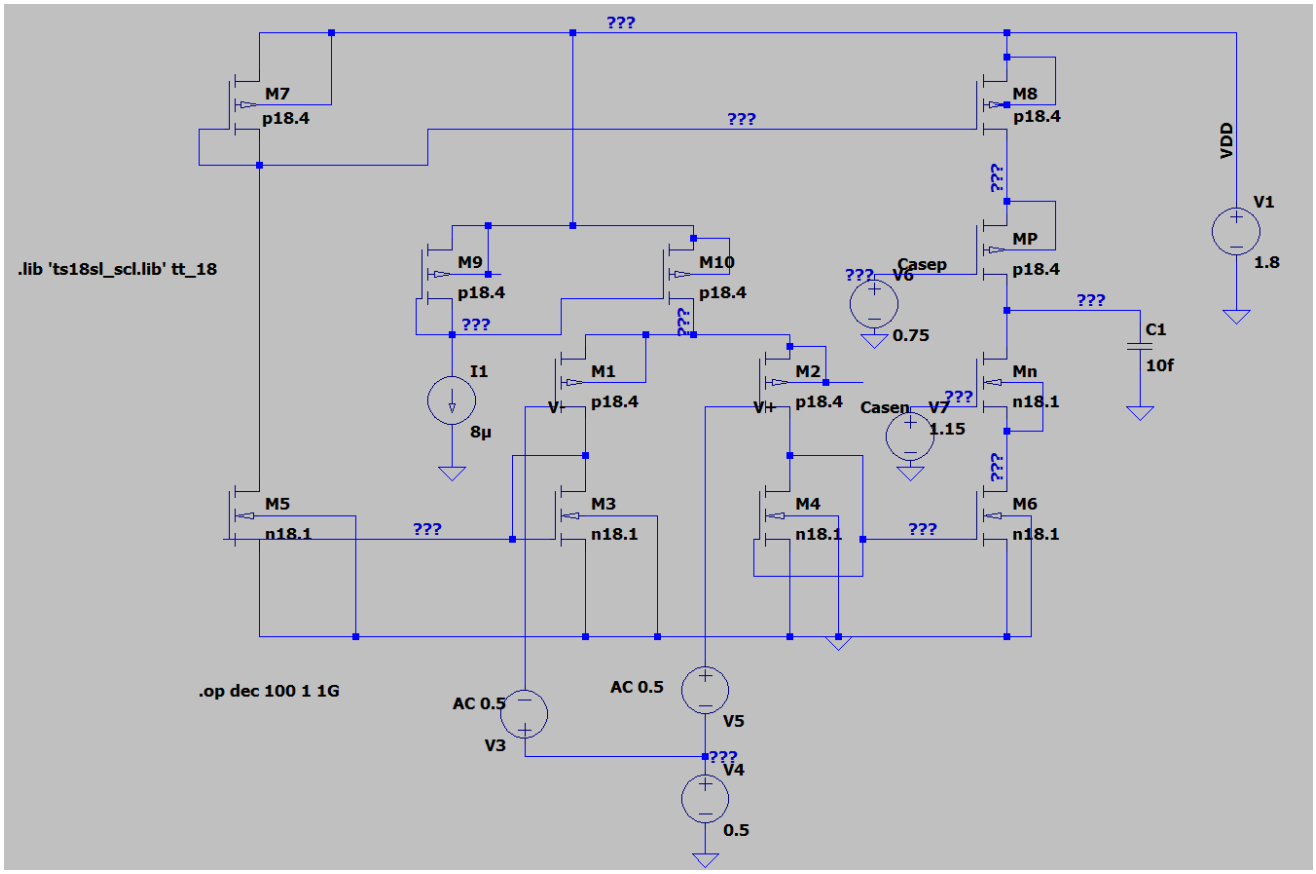
$\left(\frac{w}{l}\right)_{1,2}$	100
$\left(\frac{w}{l}\right)_{3,4,5,6}$	2.5
$\left(\frac{w}{l}\right)_{7,8}$	5
$\left(\frac{w}{l}\right)_{n}$	22
$\left(\frac{w}{l}\right)_{p}$	44
$\left(\frac{w}{l}\right)_{9,10}$	1
I_{bias}	$8\mu A$
C_L	10fF

(d) Tabulate the calculated specifications (gain, unity gain bandwidth, slew rate, phase margin) for the OTA

$\boldsymbol{A_v}$	$131db$
Unity gain bandwidth	$A_v \cdot BW \approx 389.85 \cdot 10^8$
Slew rate	$800\, V/\mu s$
Phase margin	
BW	$\approx 10^4$

3)

(a) Use LTSPICE and SCL 180 nm model file and report the drawn circuit with chosen MOSFETs



(b) Tabulate the design parameters (W, L, R, C, I etc) and compare with the hand calculate values.

$\left(\frac{W}{l}\right)_{1,2}$	$\frac{100\mu}{1\mu}$
$\left(\frac{W}{l}\right)_{3,4,5,6}$	$\frac{20\mu}{5\mu}$
$\left(\frac{W}{l}\right)_{9,10}$	$\frac{90\mu}{90\mu}$

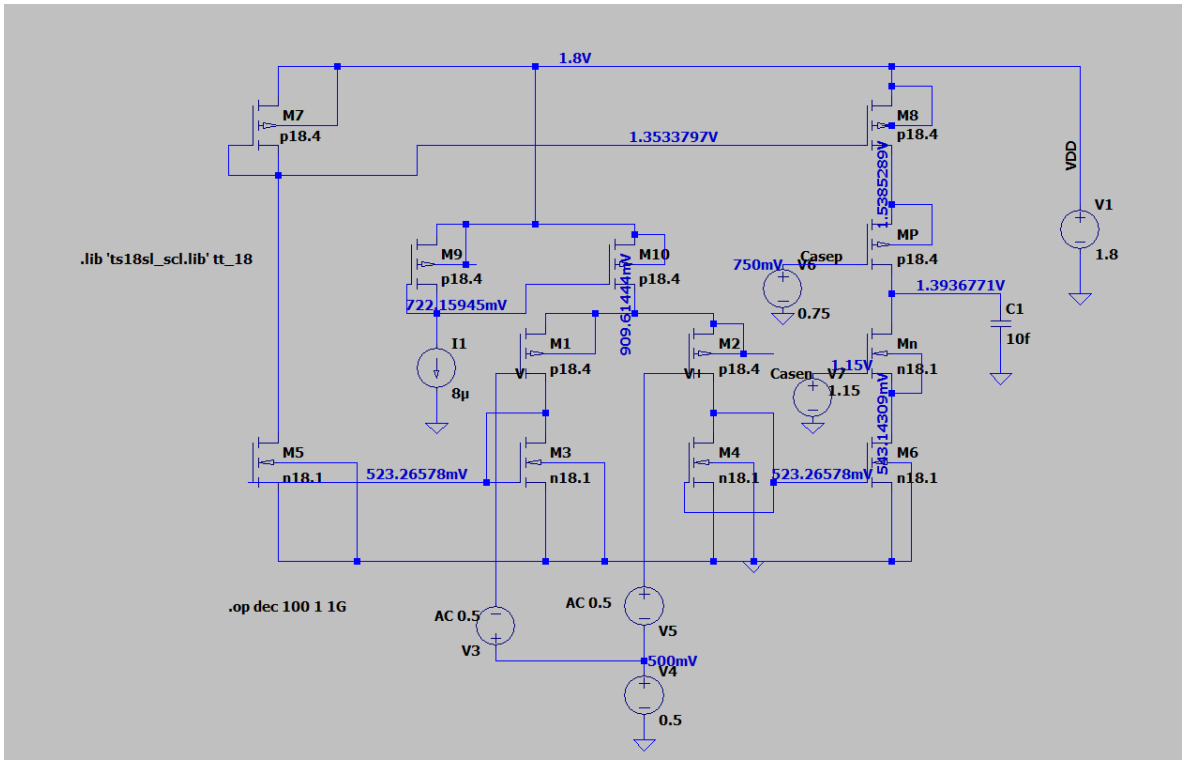
$\left(\frac{w}{l}\right)_n$	$\frac{1.075\mu}{1\mu}$
$\left(\frac{w}{l}\right)_p$	$\frac{12.9\mu}{6\mu}$
$\left(\frac{w}{l}\right)_7$	$\frac{320\mu}{8\mu}$
$\left(\frac{w}{l}\right)_8$	$\frac{290\mu}{7.25\mu}$
I_{bias}	$8\mu A$
C_L	10fF

(c) OPERATING POINT [5] Perform the dc operating point analysis with the OTA. Clearly annotate and report the dc operating point voltages at every node on the schematic. Ensure that your circuit is biased as desired.

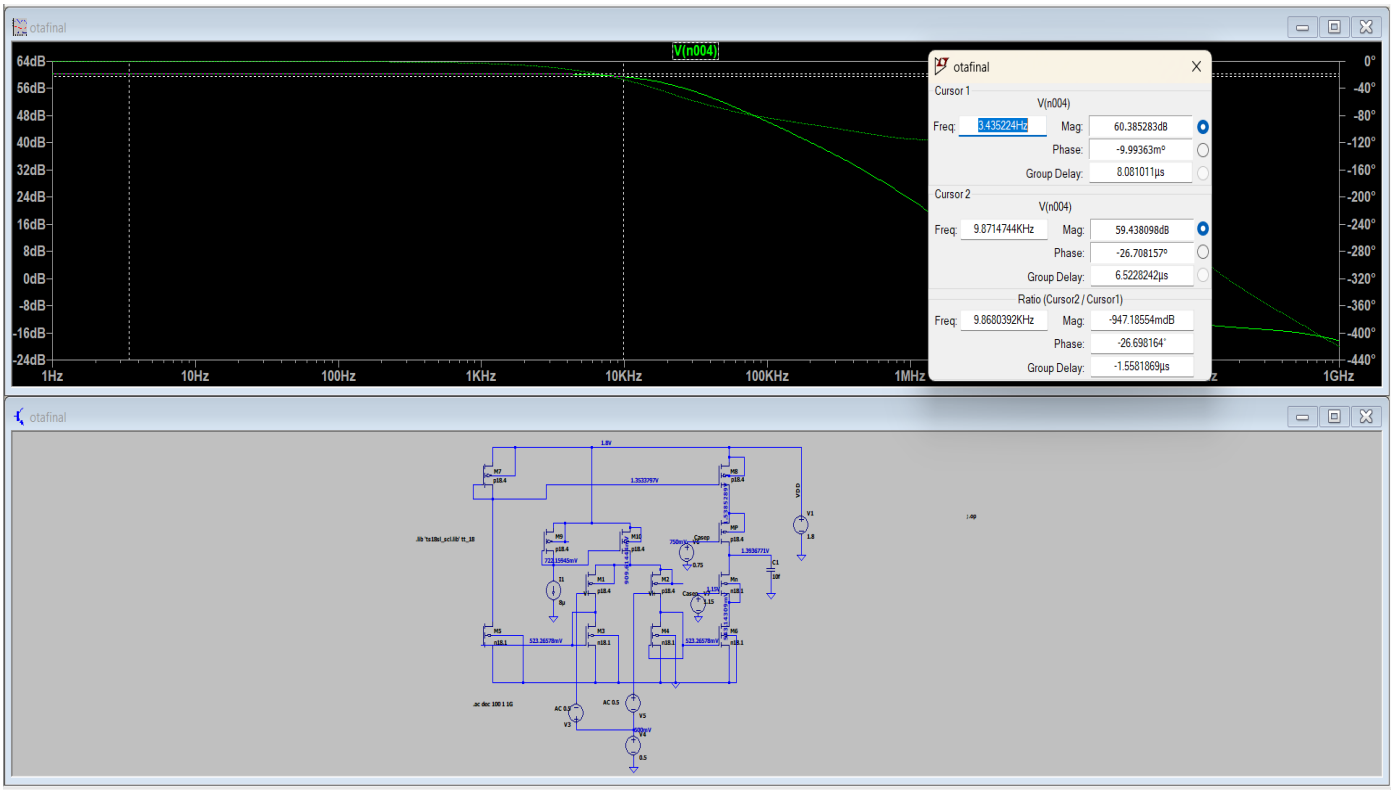
V(vdd):	1.8	voltage
V(n001):	1.35338	voltage
V(n002):	1.53853	voltage
V(n003):	0.722159	voltage
V(n005):	0.909614	voltage
V(casep):	0.75	voltage
V(n004):	1.39368	voltage
V(n007):	0.523266	voltage
V(n008):	0.523266	voltage
V(v-):	0.5	voltage
V(v+):	0.5	voltage
V(n006):	0.543143	voltage
V(casen):	1.15	voltage
V(n009):	0.5	voltage

These are the dc operating voltages at nodes and the circuit is biased as we desire, which can be said by looking at the currents in the each transistor we want 8μA in M9,M10 and 4μA in the remaining transistors

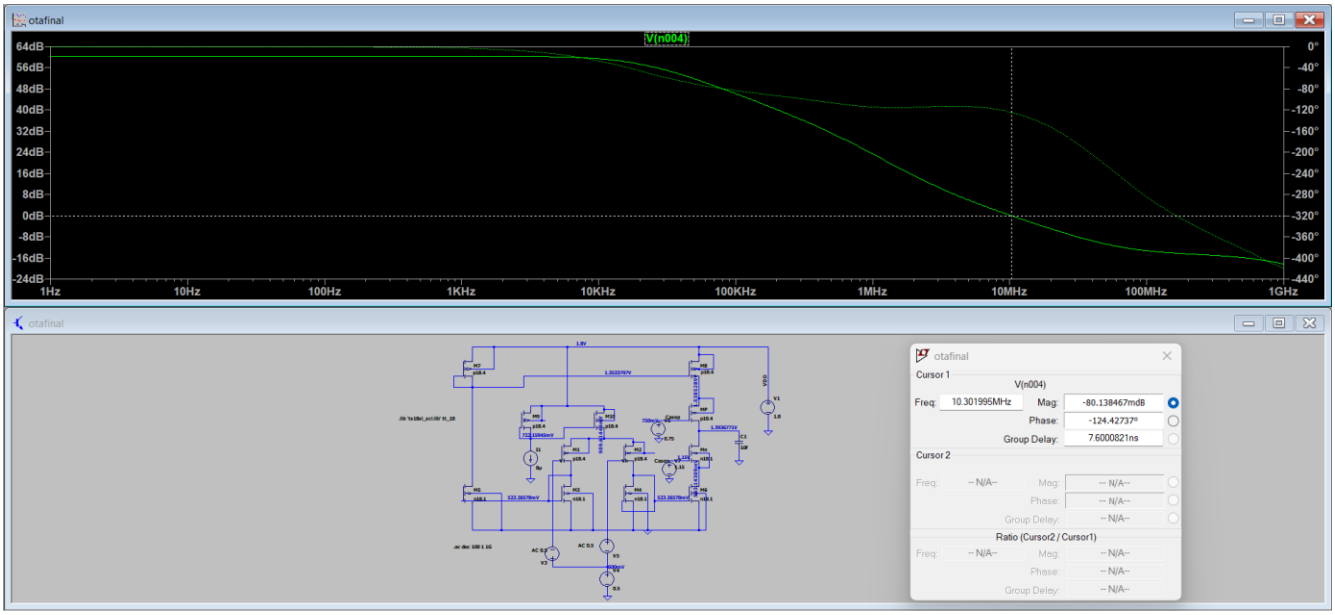
Below picture shows the values of voltages at the each node.



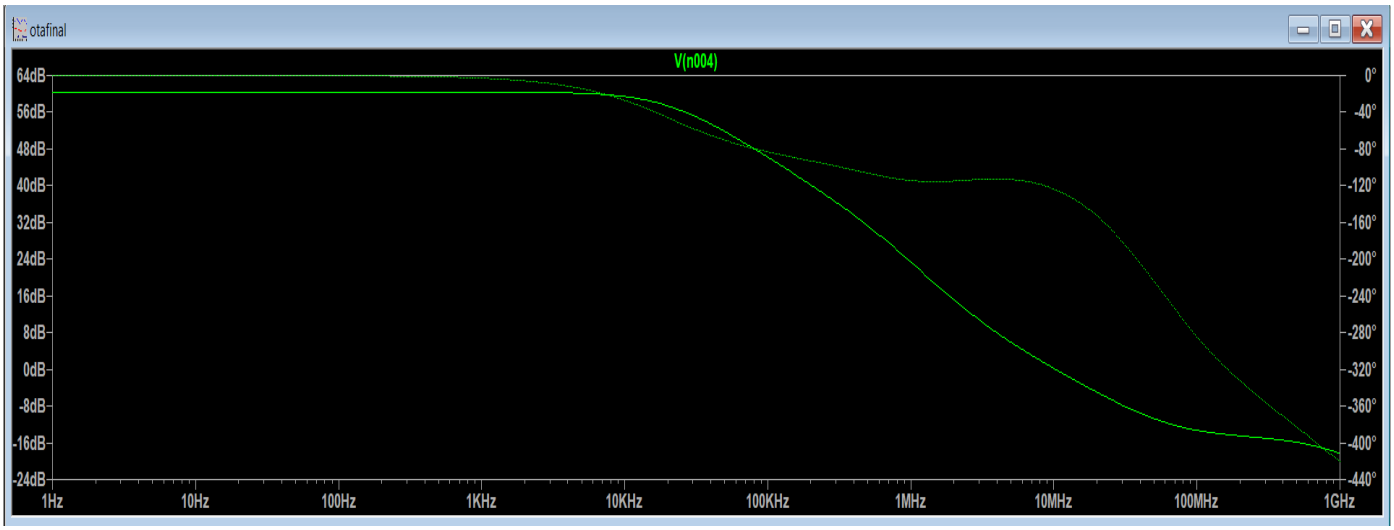
(e) STB ANALYSIS: [5] report the DC gain, unity gain frequency and the phase margin. Also show the magnitude and phase plot.



From the above plot we can clearly say that the gain is 60.38db and the band width is greater than 10Khz

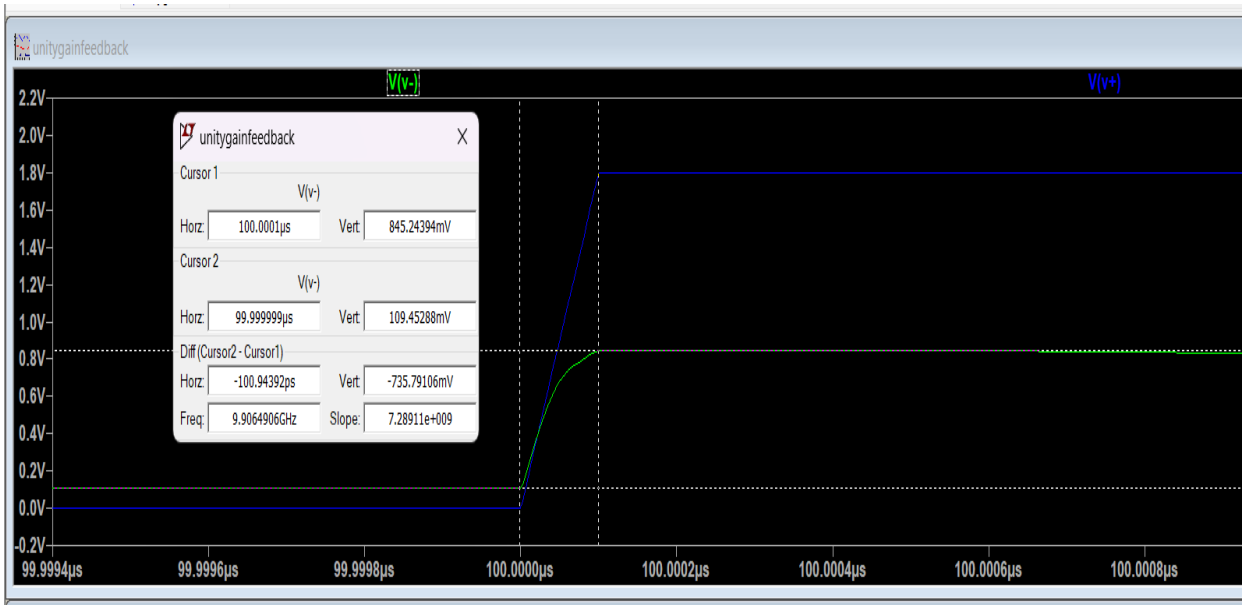


Here the unity gain frequency is 10MHz and the phase margin is 55.6^{o} and this says that the OTA is a stable amplifier.



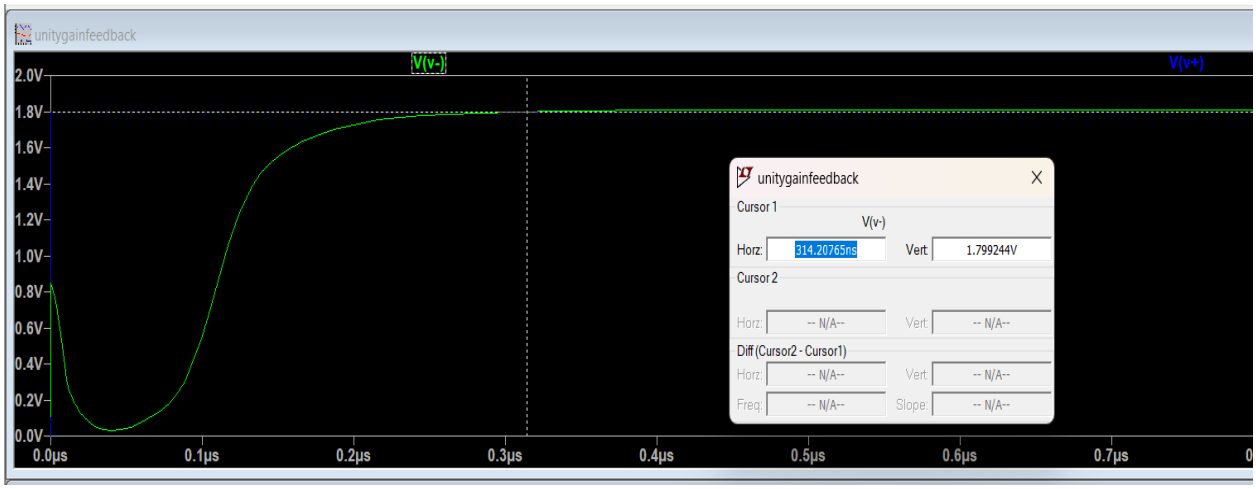
Unity gain frequency	10Mhz
Dc gain	60.38db
bandwidth	20KHz
Phase margin	55.6^{o}

(f) SLEW RATE: [5] With the OTA in unity gain feedback mode, apply a positive step from 0 to 1.8V with a rise time of 100 ps. Measure the slew rate and clearly show the output plot in the slewing region with cursors.



The slew rate is the rate of change of output voltage when a step is given. Here the slew rate is $7.29 \cdot 10^3 \frac{V}{\mu s}$.

(g) SETTLING TIME: [5] With the OTA in unity gain feedback mode, apply the same step input as above. Measure and report the settling time, ts for 2% accuracy.



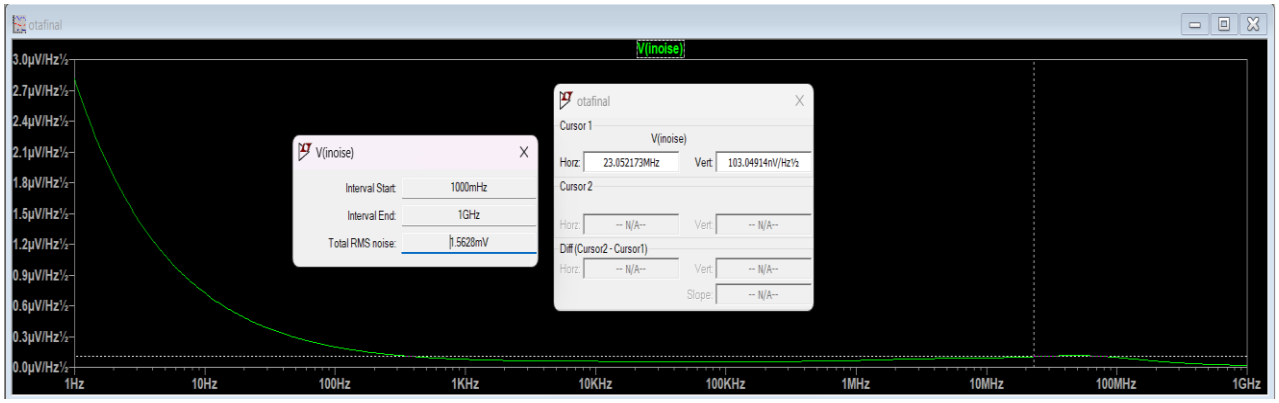
The settling time is 314ns after this time the circuit reaches to steady value of 1.8v at output.

(h) SYSTEMATIC OFFSET: [5] With the OTA in unity gain feedback mode, measure and report the systematic offset value using dc analysis. Clearly show the output node voltage on the schematic.

V(vdd) :	1.8	voltage
V(n001) :	1.36197	voltage
V(n002) :	1.43716	voltage
V(n003) :	0.722159	voltage
V(n004) :	0.540736	voltage
V(casep) :	0.75	voltage
V(v-) :	0.109453	voltage
V(n006) :	0.513825	voltage
V(n007) :	0.531917	voltage
V(v+) :	0	voltage
V(n005) :	0.0837849	voltage
V(casen) :	1.15	voltage

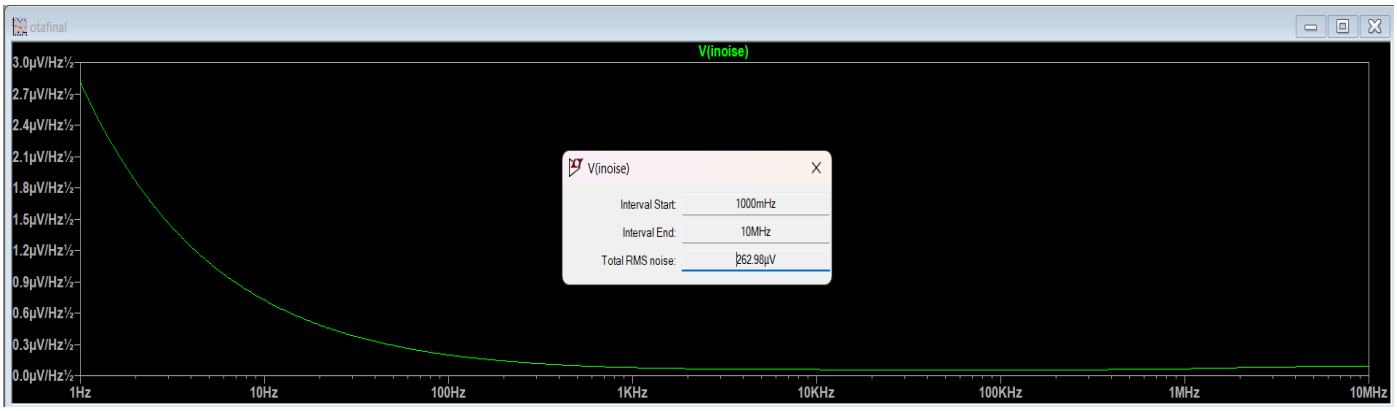
Here the value of offset is 0.1V which is V(v-) shown in the above picture from dc operating point analysis. This done when the v+ is grounded.

(i) NOISE: [5] Show the input referred noise PSD from 1Hz to 1GHz band. Clearly show the RMS thermal noise voltage in the plot (with cursor). Report the integrated noise voltage over the unity gain bandwidth.



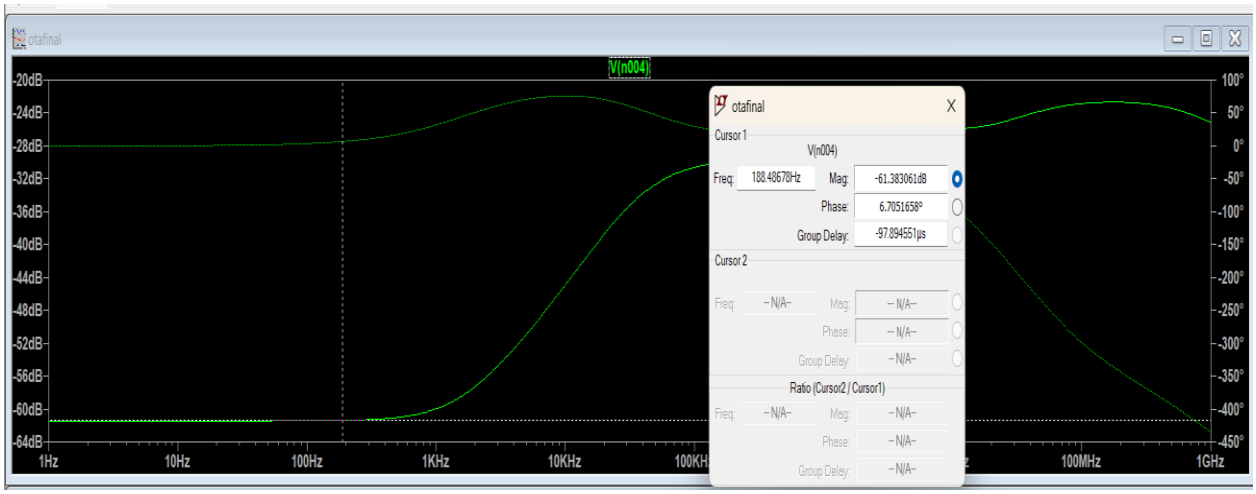
Here the input referred noise is 1.5mV.

RMS thermal noise is 103.049nV(by checking the noise value at higher frequency)



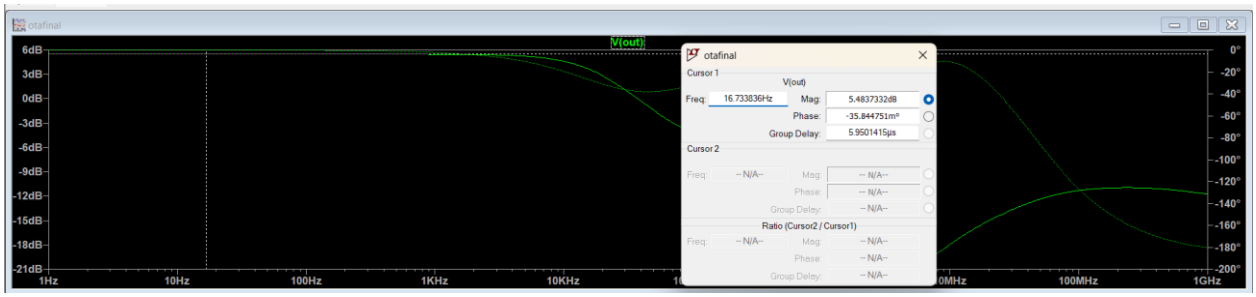
Total noise is 830mV

(j) CMRR: [5] Plot the open loop CM gain of the OTA with clear labels. Report the CMRR of the OTA.



Here the common mode gain is -61.38db and the differential mode gain is 61.3db so the total CMRR in db. is 122.76db

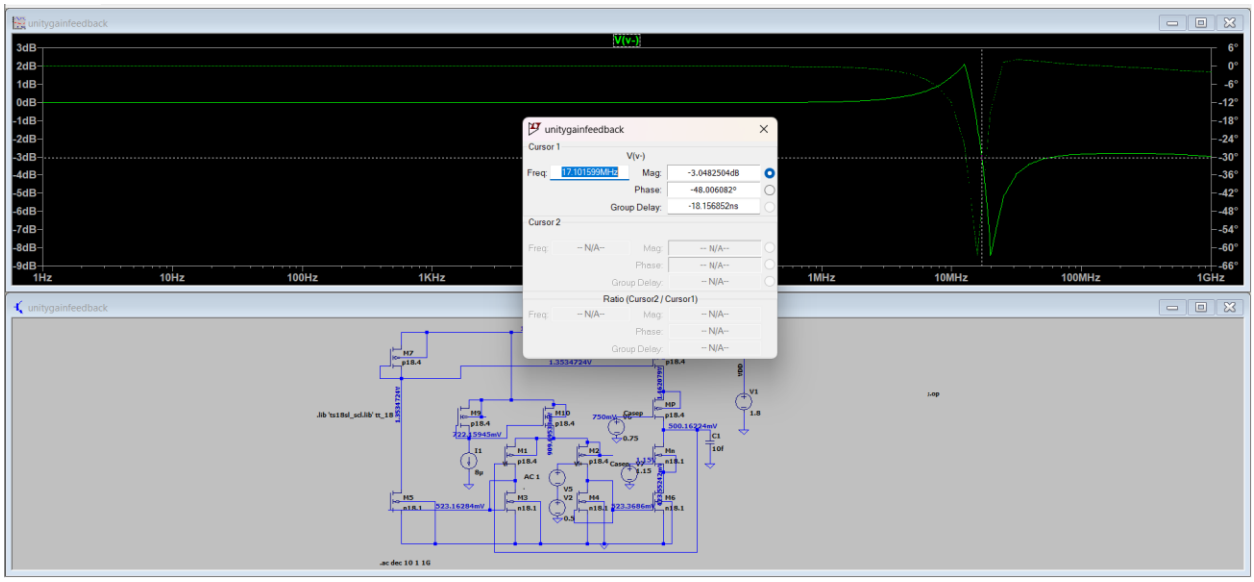
(k) PSRR: [5] Perform the PSRR simulation by adding a small signal component only on the voltage supply of the OTA. Plot and report the PSRR value with clear labels (Open loop).



Here the ps gain is 5.4db and DM is 61.3db so the PSRR is 61.38-5.48=55.9db.

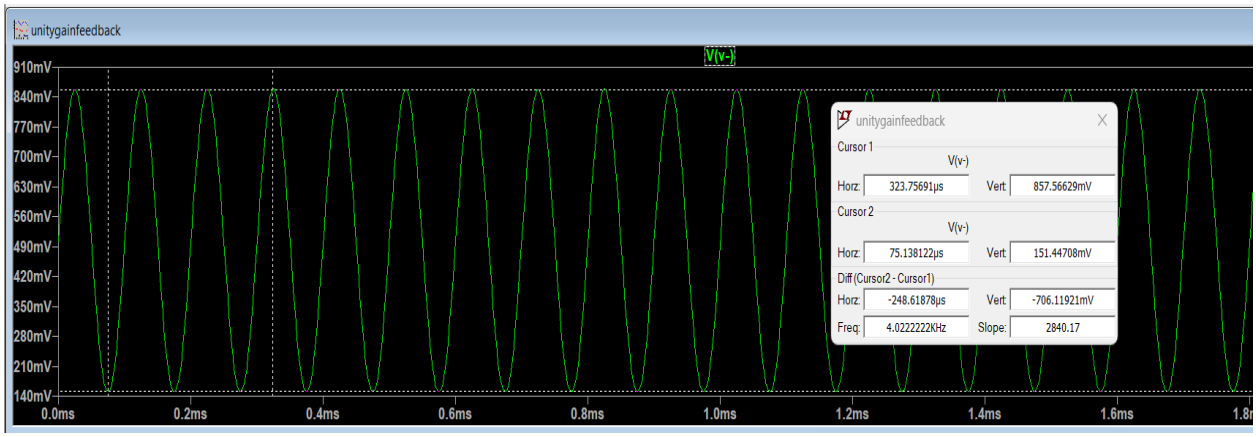
(l) INPUT COMMON MODE RANGE: Sweep the input common mode voltage in the unity gain configuration and report the maximum input common mode range of the OTA. [5]

(m) CLOSED LOOP GAIN: With the OTA in unity gain feedback mode, perform ac analysis and report the DC gain and the -3dB frequency. [5]



As we expected the gain in closed loop is 0db and the bandwidth is 17.101MHz.

(m) CLOSED LOOP TRANSIENT ANALYSIS: [5] With the OTA in unity gain feedback mode, apply a sinusoidal signal of 10KHz frequency for maximum signal swing at the output without distortion.



The maximum amplitude is 360mV if we increase this value then we will observe sinusoid, but the positive half cycle amplitude and the negative half amplitude is different after some point sinusoidal shape gets distorted.

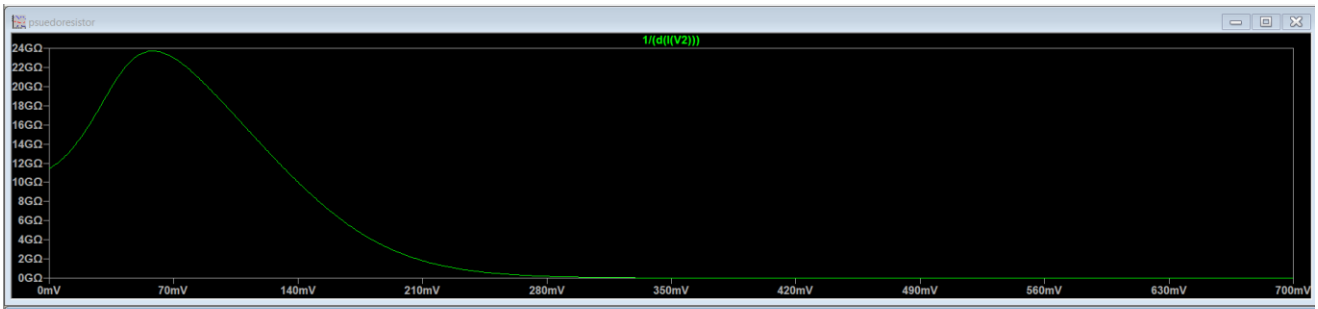
(n) POWER CONSUMPTION: [5] Report the total current and power consumption of the OTA.

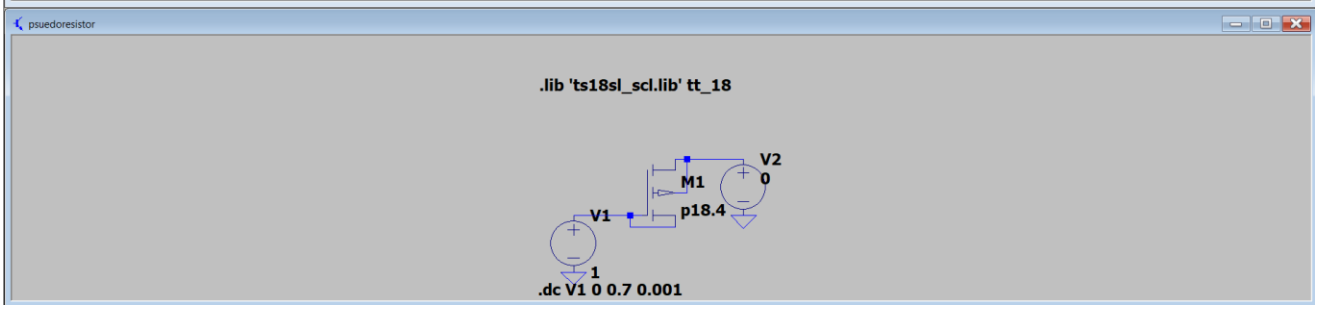
```
Is(Mp):         -3.99869e-006 device_current
Id(M10):        7.99558e-006  device_current
Ig(M10):        -0            device_current
Ib(M10):        9.00386e-013  device_current
Is(M10):        -7.99558e-006 device_current
Id(M9):         8e-006        device_current
Ig(M9):         -0            device_current
Ib(M9):         1.08784e-012  device_current
Is(M9):         -8e-006       device_current
Id(M8):         3.99869e-006  device_current
Ig(M8):         -0            device_current
Ib(M8):         2.7147e-013   device_current
Is(M8):         -3.99869e-006 device_current
Id(M7):         4.02e-006     device_current
Ig(M7):         -0            device_current
Ib(M7):         4.5662e-013   device_current
Is(M7):         -4.02e-006    device_current
```

Here the total current is $Id_{10} + Id_9 + Id_8 + Id_7 = 24.00985 \cdot 10^{-6} A$

Total power consumer = $43.21773 \cdot 10^{-6}$W

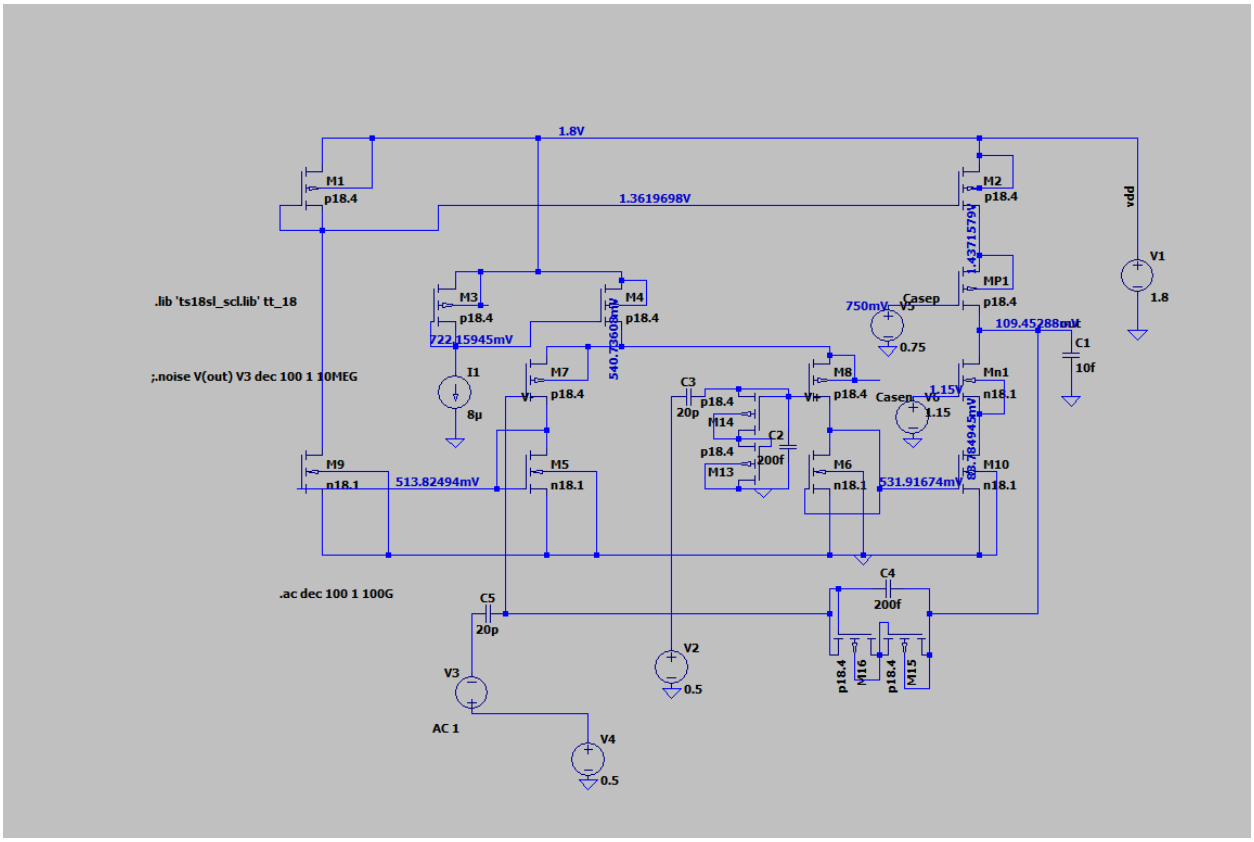
4.Pseudo resistor design [20] Design the pseudo PMOS resistor shown in the Fig. 1 in the paper. Simulate and plot its I-V characteristics and incremental resistance vs incremental voltage across it.

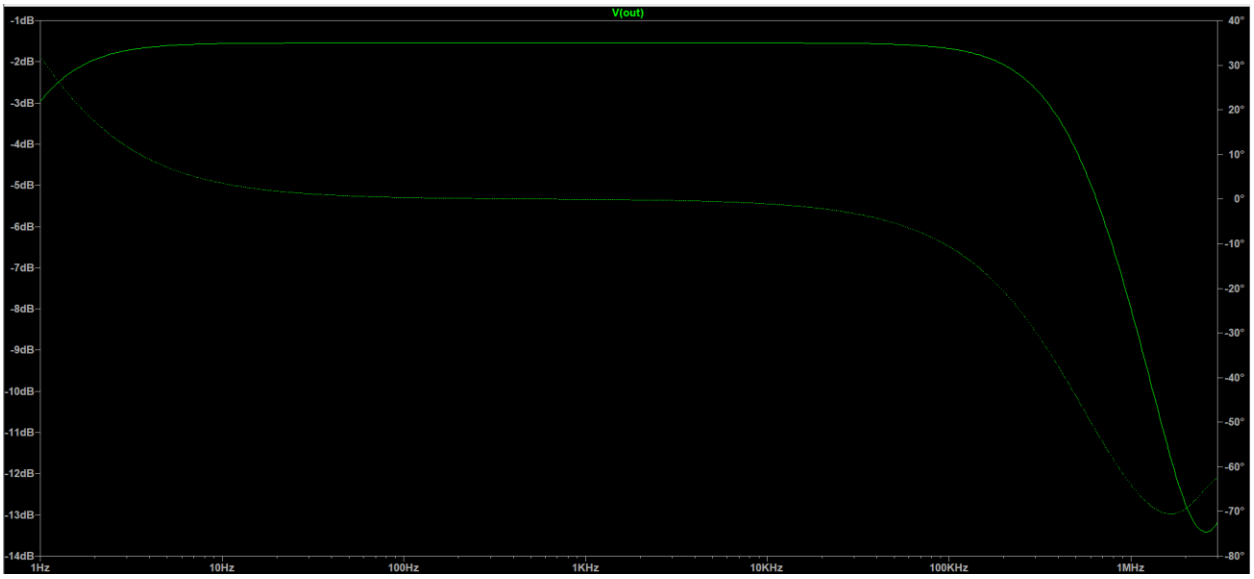




Both the graphs are same the graphs mentioned in the paper and are same as expected.

5.Neural amplifier design [30] Use the OTA and pseudo resistor to build the neural amplifier (Fig. 1 in the paper). Report capacitor values (C1, C2), sizing for pseudo PMOS resistor. Run necessary simulations (DC, AC, transient, noise, CMRR, PSRR etc.) and report the achieved specifications





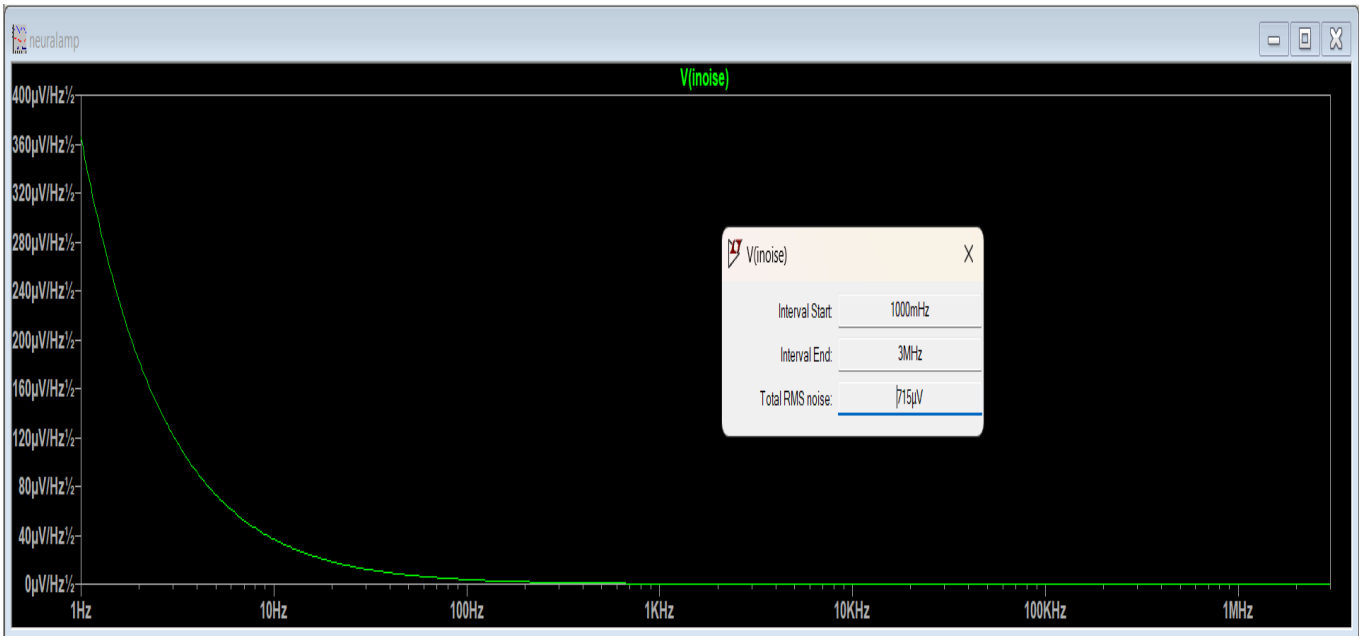
The values of C1 = $20pF$ and C2=200fF

And the W/L for pseudo resistor is 1u/1u.

From the above ac simulations, the value of the dc gain is -6.11db

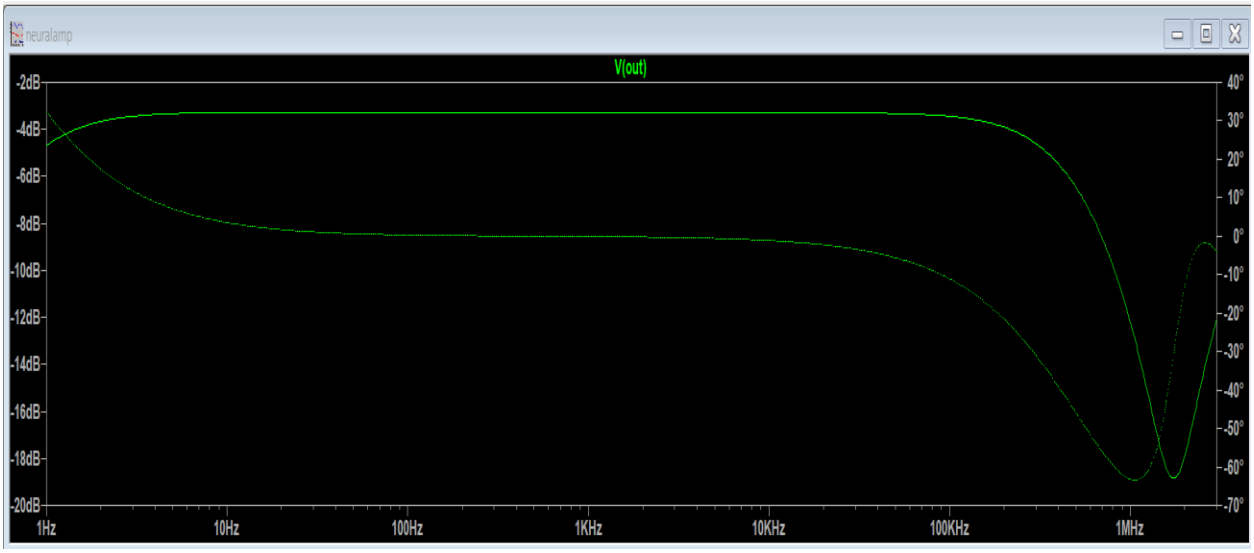
DC:-

NOISE: -



RMS input referred noise is 715μV

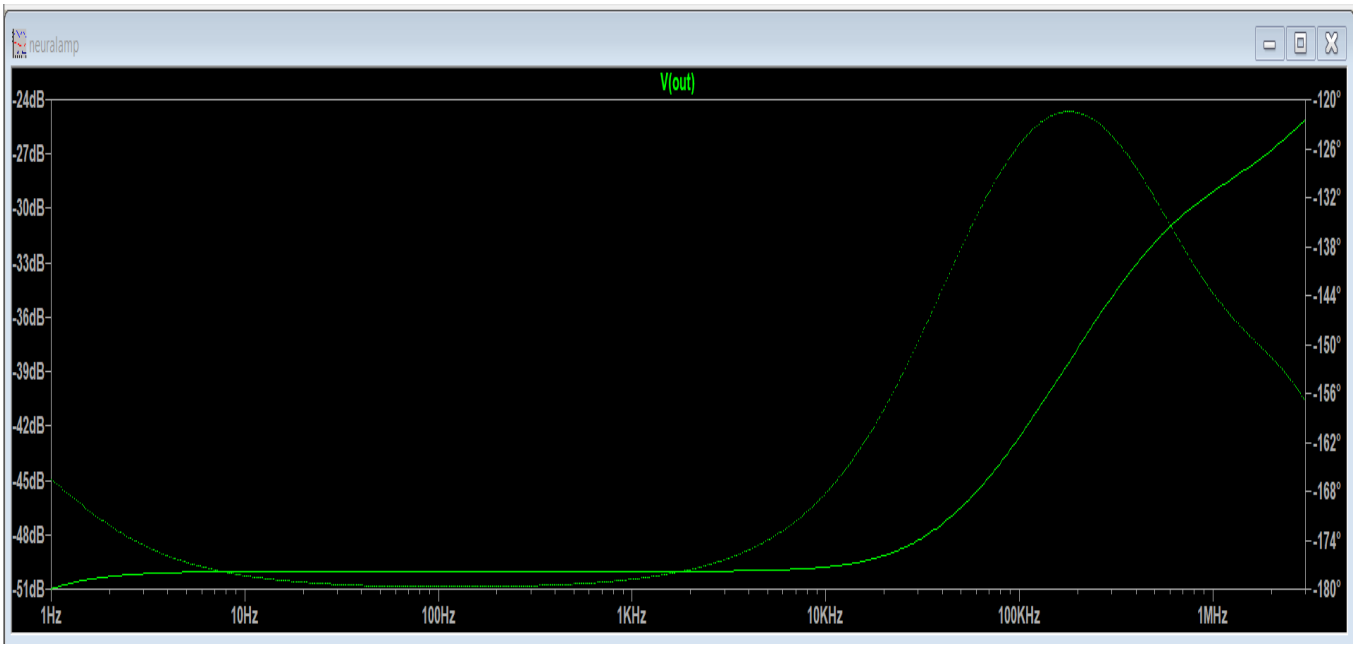
CMRR:-



Above graph is the common mode gain of the -3.2db

So the cmrr is 3.2-6.11=-2.91db (which is a very bad value)

PSRR: -



to ps gain is -50.02db so the psrr =-6.11+50.02=43.91db.

we got cmrr less than which we don't want.

Slew rate is $1.4254 \cdot 10^{10} \frac{V}{s}$

```
I(V1):          -2.28489e-005  device_current
```

The power is $=4.1128 \cdot 10^{-5} W$

From the schematic simulations, tabulate the OTA and neural amplifier performance (DC gain, unity gain frequency, phase margin, ICMR, CMRR, PSRR, slew rate, output swing (peak to peak), RMS thermal noise, power) and compare with the required specifications. (Table columns - specifications — Schematic)

	OTA	NEURAL AMPLIFIER
power	**43.21μW**	**41.128μW**
CMRR	**122.76db**	**-2.91db**
PSRR	**55.9db**	**43.91db**
Phase margin	**55.06^{o}**	**-**
Dc gain	**60.38db**	**-6.11db**
Unity gain frequency	**17.101MHz**	**-**
Output swing	**0.65V-1.25V**	**0.65V-1.25V**