REPORT
ECE 506 – Machine Problem 2

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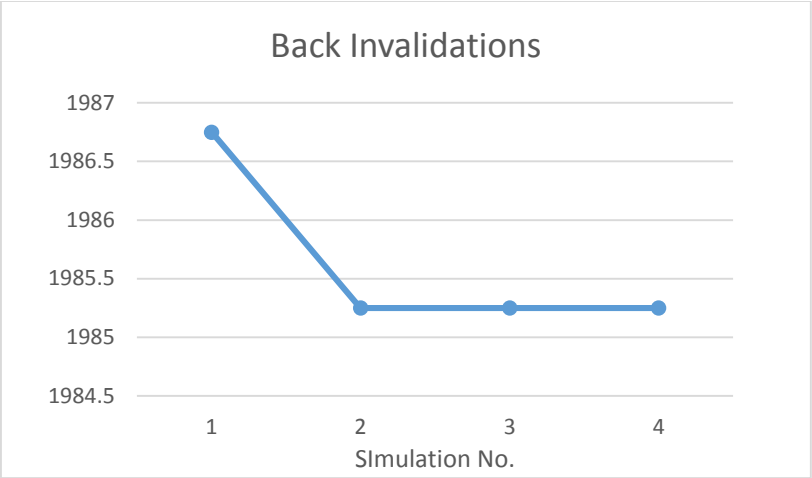
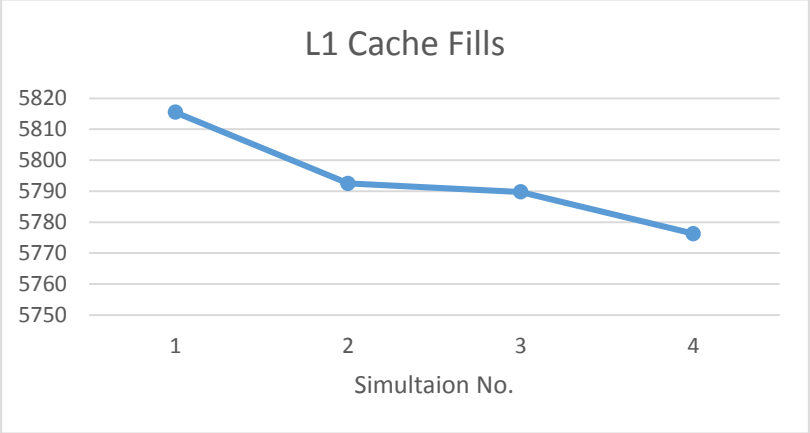
Varying cache sizes:

Stats

L1/L2 size						
1. L1 - 256 kb, L2 - 512 Kb, L1 assoc - 4 way, L2 assoc - 8 way, Blocksize - 64						
L1 read misses -		5798	- Proc 0			
L1 write misses -		46	- Proc 0			
total miss rate -		4.69%	- Proc 0			
L2 coherence miss:		2014	- Proc 0			
Back invalidatiions:		1986.75	- Avg. of 4 procs			
L1 fills:		5815.5	- Avg. of 4 procs			
2. L1 - 512kb, L2 - 1Mb, L1 assoc - 4 way, L2 assoc - 8 way, Blocksize - 64 by						
L1 read misses -		5774	- Proc 0			
L1 write misses -		46	- Proc 0			
total miss rate -		4.67%	- Proc 0			
L2 coherence miss:		2014	- Proc 0			
Back invalidatiions:		1985.25	- Avg. of 4 procs			
L1 fills:		5792.5	- Avg. of 4 procs			
3. L1 - 1Mb, L2 - 2Mb, L1 assoc - 4 way, L2 assoc - 8 way, Blocksize - 64 byte						
L1 read misses -		5771	- Proc 0			
L1 write misses -		46	- Proc 0			
total miss rate -		4.67%	- Proc 0			
L2 coherence miss:		2014	- Proc 0			
Back invalidatiions:		1985.25	- Avg. of 4 procs			
L1 fills:		5789.75	- Avg. of 4 procs			
4. L1 - 2Mb, L2 - 4Mb, L1 assoc - 4 way, L2 assoc - 8 way, Blocksize - 64 byte						
L1 read misses -		5754	- Proc 0			
L1 write misses -		46	- Proc 0			
total miss rate -		4.65%	- Proc 0			
L2 coherence miss:		2014	- Proc 0			
Back invalidatiions:		1985.25	- Avg. of 4 procs			
L1 fills:		5776.25	- Avg. of 4 procs			

Graphs:





Inference:

1) Back Invalidations:

As we can see from the above statistics and figures, increasing the sizes of the L1 and L2 caches has an effect on the number of back invalidations. This is because as the two caches get large enough, the possibility of a capacity miss reduces drastically. As a result, after a certain point, the number of unique blocks that can be accommodated in the L2 cache is no longer limited by the cache size. Hence we see a sharp decline after the cache sizes are increases to 512Kb and 1Mb for the L1 and L2 caches respectively; upon further increase in cache size, the no. of back invalidations remains constant.

2) L1 Cache Fills:

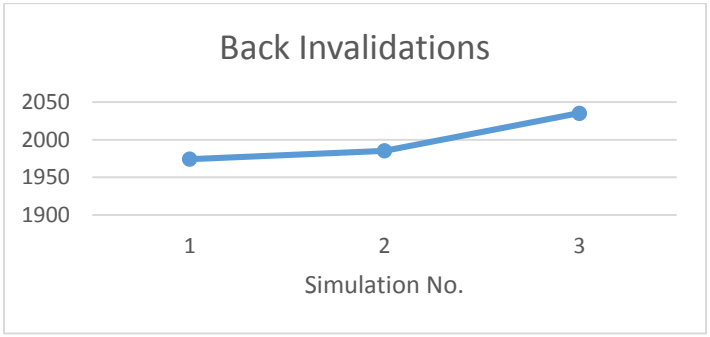
The number of L1 cache fills is indicative of the number of read misses suffered by the L1 cache as, in the WTNA policy, a block is only filled if there is a read miss. As the cache sizes increase, the number of read misses proportionately decrease since there is now more place to accommodate more blocks. Hence, the number of L1 fills also decreases gradually.

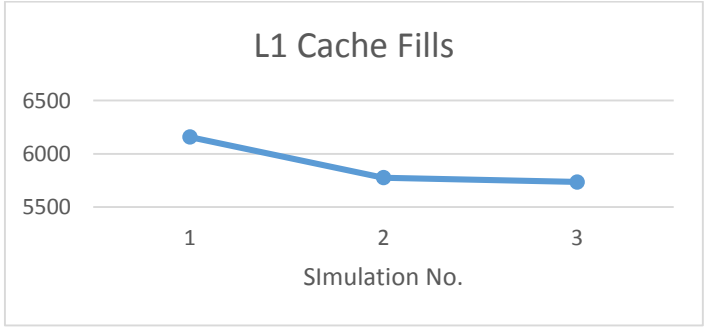
Varying Blocksize:

Stats

4. L1 - 2Mb, L2 - 4Mb, L1 assoc - 4 way, L2 assoc - 8 way, Blocksize - 32 byte		
L1 read misses -	6149	- Proc 0
L1 write misses -	49	- Proc 0
total miss rate -	4.97%	- Proc 0
L2 coherence miss:	2006	- Proc 0
Back invalidatiions:	1974.25	- Avg. of 4 procs
L1 fills:	6156.75	- Avg. of 4 procs
4. L1 - 2Mb, L2 - 4Mb, L1 assoc - 4 way, L2 assoc - 8 way, Blocksize - 64 byte		
L1 read misses -	5754	- Proc 0
L1 write misses -	46	- Proc 0
total miss rate -	4.65%	- Proc 0
L2 coherence miss:	2014	- Proc 0
Back invalidatiions:	1985.25	- Avg. of 4 procs
L1 fills:	5776.25	- Avg. of 4 procs
4. L1 - 2Mb, L2 - 4Mb, L1 assoc - 4 way, L2 assoc - 8 way, Blocksize - 64 byte		
L1 read misses -	5347	- Proc 0
L1 write misses -	46	- Proc 0
total miss rate -	4.33%	- Proc 0
L2 coherence miss:	2066	- Proc 0
Back invalidatiions:	2035.25	- Avg. of 4 procs
L1 fills:	5735.5	- Avg. of 4 procs

Graphs:





Inference:

1) Back Invalidations:

As we can see from the above statistics and figures, increasing the Blocksize gradually increases the number of back invalidations. This is because although the size of the blocks increase, the total cache size remains the same, leading to fewer number of blocks being accommodated. And as the number of blocks decrease, we get commensurately more invalidations from the L2 to the L1 cache. Also, since the number of back invalidations increase, we can conclude that the data being accessed doesn't have very high spatial locality.

2) L1 Cache Fills:

The number of L1 cache fills is indicative of the number of read misses suffered by the L1 cache as, in the WTNA policy, a block is only filled if there is a read miss. As the Blocksizes increase, the number of read misses proportionately decrease since there are now more hits to the same blocks. Hence, the number of L1 fills also decreases gradually.