CMPE 200
Computer Architecture & Design

Final Review
Quiz3 Notes

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Quiz3 Question (1)

1. Which of the following cache configurations would likely have the highest number of conflict misses?

A. 4-way set associative
B. 2-way set associative
C. Fully associative
D. Direct mapped

Quiz3 Question (2)

2. An 8-way set-associative L2 cache of size 512KB data with 64byte block size has X tag bits and Y index bits.

A. X=16, Y=10
B. X=13, Y=10
C. X=13, Y=7
D. X=19, Y=7

512 x 1024 / 64 = 8 x 1024

8 x 1024 / 8 = 1024 sets

2^10

Y = 10

64 = 2^6

32 − Y − 6 = 16 tag

Quiz3 Question (3)

3. What is the size of a 4-way set-associative L1 cache with 512 sets and 16-byte blocks?

A. 32KB
B. 64KB
C. 16KB
D. 256KB

$512 \times 4 \times 16 = 1024 \times 32$

Quiz3 Question (4)

4. Which of the following cache miss types cannot be improved (increase in hit rate) by making the overall cache capacity larger?

A. Conflict miss
B. All can benefit from a larger cache
C. Compulsory miss
D. Capacity miss

Quiz3 Question (5)

5. Below is the sequence of 12 memory address references given as word addresses:

0,1,9,4,1,17,9,7,0,9,12,4

Now assume the cache is of infinite capacity, fully associative and initially empty. What is the miss rate?

A. 10/12
B. 7/12
C. 8/12
D. 12/12

Quiz3 Question (6)

6. Below is the sequence of 12 memory address references given as word addresses:

0,1,9,4,1,17,9,7,0,9,12,4

Assume 2-way associative caches with 1-word blocks and a total cache size of 16 blocks. What is the miss rate assuming the cache is initially empty? Use LRU replacement policy.

A. 1
B. 8/12
C. 10/12
D. 7/12

	0	1
0	0.	
1	1. 9.	9 17
2		
3		
4	4.	12
5		
6		
7	7	

0 % 8 = 0
9 % 8 = 1
17 % 8 = 1
12 % 8 = 4

Quiz3 Question (7)

7. If the hit time, hit rate and miss penalty for the L1 cache are given by 2ns, 0.94 and 10ns, respectively, what is the average access latency for the L1 cache?

A. 2.36
B. 2.60
C. 9.40
D. 2.94

$1 - 0.94 = 0.06$

$AMAT(L1) = 2 + 0.06 \times 10$

$= 2.6$ ns

Quiz3 Question (8)

8. For a byte-addressable machine, let us consider the following trace of addresses and the corresponding cache hit ratios. Assume that the cache is initially empty and uses an LRU replacement policy.

Address Trace	Hit Ratio
0, 2, 4, 8, 16, 32	66.66%

What is the possible block size of the cache?

A. 4B

B. 8B

C. 16B

D. 32B

Quiz3 Question (9)

9. For a byte-addressable machine, let us consider the following trace of addresses and the corresponding cache hit ratios. Assume that the cache is initially empty and uses an LRU replacement policy.

Address Trace	Hit Ratio
0, 512, 1024, 1536, 2048, 1536, 1024, 512, 0	11.11%

What is the possible associativity of the cache, for a cache size of 512B with a block size of 32B?

A. 1 way

B. 2 ways

C. 4 ways

D. 8 ways

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