CMPE 200 – Assignment 7

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Pipelined MIPS Processor, I/O, and Interfacing

Purpose

Convert the fifteen-instruction 32-bit single-cycle MIPS processor into a five-stage, pipelined design. Interface the processor with a factorial accelerator and a general-purpose I/O unit using memory-mapped interface registers.

Description

In this assignment, you are required to complete the design and functional verification of a pipelined MIPS processor. You are further required to complete the design and functional verification of a small system-on-chip (SoC) system which includes the pipelined MIPS processor, a factorial accelerator (you have completed in Assignment 1), and a simple general-purpose IO (GPIO) unit, all connected via direct interface to the MIPS local bus, using memory-mapped interface registers.

Based on the enhanced single-cycle MIPS processor (which supports the additional instructions `multu, mfhi, mflo, jr, jal, sll, slr`) you successfully accomplished in Assignment 6, use the test program (factorial calculation via nested procedure calls) included in the assignment to test the pipelined MIPS processor. Extra credit will be given if your design is enhanced to have control and data hazard handling capabilities.

For the SoC design, requirements include:

1) The factorial accelerator should be able to handle 4-bit input data (n).
2) You should use the simple GPIO for validation. Specifically, the MIPS should read input (n) via GPIO, and return the result (n!) also via GPIO.
3) Your report should include an analytical performance comparison between the software-only and hardware-accelerated execution of the factorial function.

All the information you need (background, methodologies, technical details such as memory space allocation) are discussed in class and available from class Canvas site (e.g., Lecture 3.5: I/O and Interface).

For this assignment, you are also expected to predict the expected performance of factorial computations between the single-cycle MIPS, pipelined MIPS, and SoC designs. Analysis of each design should be graphed, showing the relationship between runtime (e.g., in SoC cycles) and the factorial input parameter.

As always, you should document your work professionally. In addition to the essential sections, your report should include schematics (generated by professional tools) of the pipelined MIPS micro architecture, including the pipelined datapath, the pipelined

control unit, and each of the memory modules. Your report should also include schematics of the SoC top-level, factorial module, and GPIO module. If your design contains hazard handling capabilities, the logic equations used for each function must be included. All source code must be attached and commented.

This is a three week long assignment. The detailed tasks are as follows:

1. Draft of pipelined MIPS microarchitecture schematic (digital copy only)
2. Draft of SoC interface schematic (digital copy only)
3. Tables for MIPS control unit (Microsoft Excel only) and memory maps for SoC interface
4. Performance analysis of hardware accelerated n!
5. Unit-level (with interface wrappers) simulation
6. Completed interface design for the SoC with the pipelined MIPS processor, the factorial unit (from Assignment 1) and the simple GPIO