CMPE 200
Computer Architecture & Design

Final Review
Quiz4 & 5 Notes

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Quiz4 Question (1)

1. Let us consider a paged DRAM, where access to the first word of a row takes 20 cycles and access to any word in the same row takes 5 cycles. For the following sequence of 5 requests in the MC's pending queue given as (row address, column address), what is the total number of memory cycles required to access all the data? (Assume the MC uses FR-FCFS scheduling)

(2, 24), (2, 30), (3, 8), (3, 9), (2, 10).

A. 45 cycles
B. 50 cycles
C. 55 cycles
D. 60 cycles

Quiz4 Question (2)

2. If the size of a memory bank is (16 x 256 x 8) bits, what is the total memory size of a DIMM that consists of 8 DRAM chips, where each chip in turn has 8 banks?

A. 2048KB
B. 256KB
C. 1028KB
D. 512KB

$16 \times 256 \times 8 = 4\,KB$

$4 \times 8 \times 8 = 256\,KB$

Quiz4 Question (3)

3. Assume an HDD has the following configuration: rotation speed 7,500 RPM, average seek time 8 ms, 100MB/sec transfer rate, and 0.2 ms controller overhead. If the measured average seek time is 50% of the advertised average seek time, then what is the average time to read or write a 512B sector from this disk?

A. 0.2 ms
B. 3.2 ms
C. 6.2 ms
D. 8.2 ms ✓

4 ms + 0.5/7500 0.125

+0.5KB/100 + 0.2 = 4 + 4 + 0.005 + 0.2

RPMS = 7,500 / 60,000 = 0.125 RPMS

100MB/sec = 100KB/ms

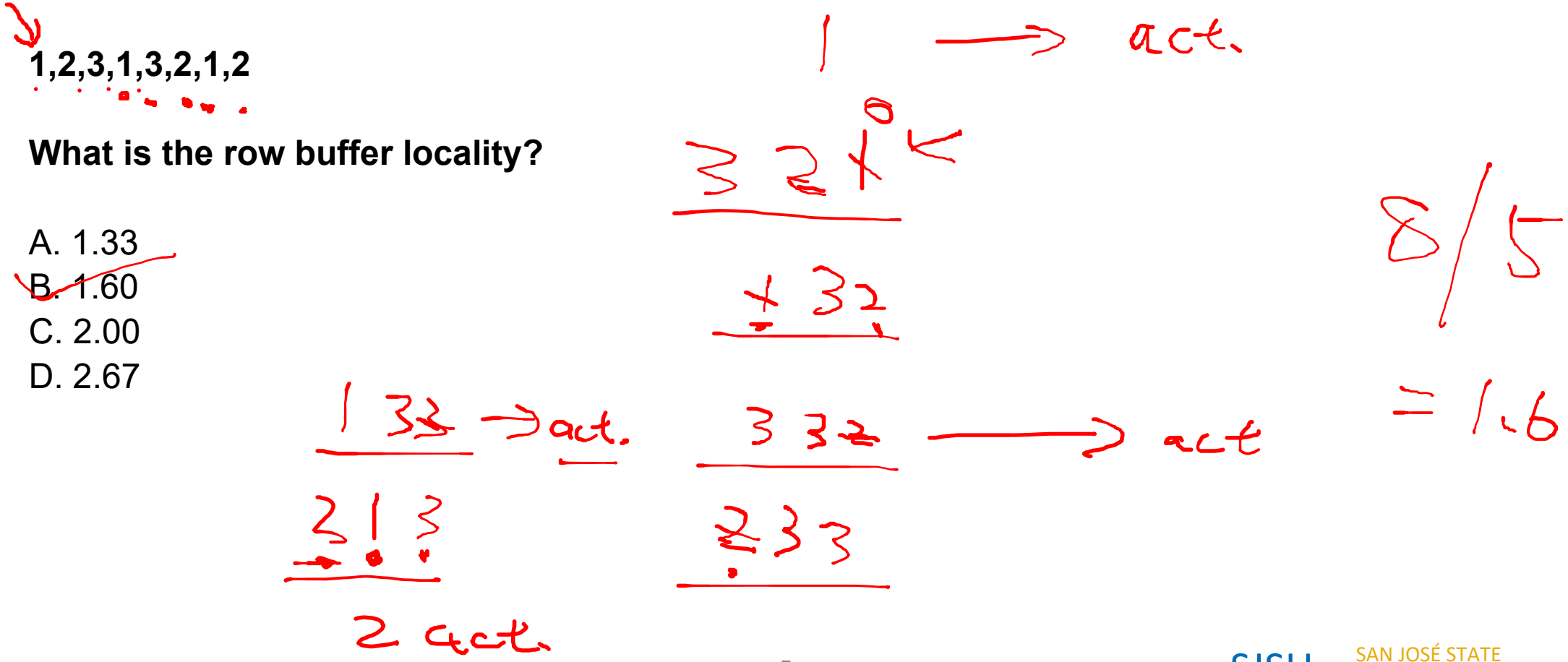
Quiz4 Question (4)

4. Assume the pending queue in the memory controller can hold at most 3 memory requests. With an FR-FCFS memory scheduler and the following memory access sequence (shown as row index):

1,2,3,1,3,2,1,2

What is the row buffer locality?

A. 1.33
B. 1.60
C. 2.00
D. 2.67



Quiz4 Question (5)

5. Which of the following TLB, page table, and cache access status combinations are possible?

A. TLB miss, page table hit, cache miss
B. TLB hit, page table miss, cache miss
C. TLB miss, page table miss, cache hit
D. TLB miss, page table miss, cache miss

Quiz4 Question (6)

6. Which of the following configuration combinations are possible for DDR SDRAM?

A. Core frequency 400 MHz, 2n prefetch, I/O buffer frequency 800 MHz, data frequency 1600 MHz

B. Core frequency 400 MHz, 4n prefetch, I/O buffer frequency 800 MHz, data frequency 1600 MHz

C. Core frequency 800 MHz, 2n prefetch, I/O buffer frequency 800 MHz, data frequency 1600 MHz

D. Core frequency 800 MHz, 4n prefetch, I/O buffer frequency 1600 MHz, data frequency 1600 MHz

Quiz5 Question (1)

1. For the following instruction sequence:

```
lw   $t1, 0($t0)
sub  $t5, $t1, $t3
lw   $t2, 4($t0)
add  $t3, $t1, $t2
sw   $t3, 12($t0)
add  $t1, $t2, $t3
lw   $t0, 0($t3)
lw   $t4, 8($t0)
add  $t5, $t1, $t4
sw   $t1, 16($t0)
```

How many cycles are required to execute these instructions in a 5-stage pipeline MIPS machine with and without code reordering?

A. 14 and 17

B. 15 and 19

C. 14 and 18

D. 15 and 20

10

K + N − 1

5 + 10 − 1 = 14

18

Quiz5 Question (2)

2. Assuming the initial state is 0, how many correct predictions can be generated for a 2-bit branch predictor given the following actual branch outcomes? (T = Taken = 1, N = Not Taken = 0)

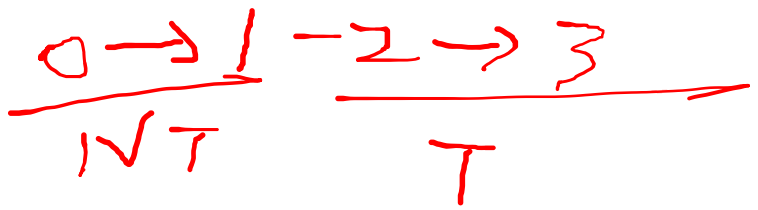
TNNTTTNTTNTNNN

A. 5

B. 6

C. 7

D. 8



OC		T	N	N	T	T	T	N	T	T	N	T	N	N	N
S	0	1	0	0	1	2	3	2	3	3	2	3	2	1	0
P		NT	NT	NT	NT	NT	T	T	T	T	T	T	T	T	NT
		x	√	√	x	x	√	x	√	√	x	√	x	x	x

Quiz5 Questions (3)

3. For the following instruction sequence:

```
lw $5, -16($5)
sub $6, $6, $0
sw $5, -16($5)
add $5, $5, $0
sub $5, $5, $6
```

How many nops have to be inserted to eliminate all data hazards assuming there is no forwarding hardware support?

A. 3

B. 2

C. 1

D. 0

Quiz5 Question (4)

4. Which of the following condition check is related to control hazard?

A. we_regM and (rsE ≠ 0) and (rf_waM = rsE)

B. we_regW and (rsE ≠ 0) and (rf_waW = rsE)

C. ((rsD == rtE) or (rtD == rtE)) and dm2regE

D. we_regM and (rsD ≠ 0) and (rf_waM == rsD)

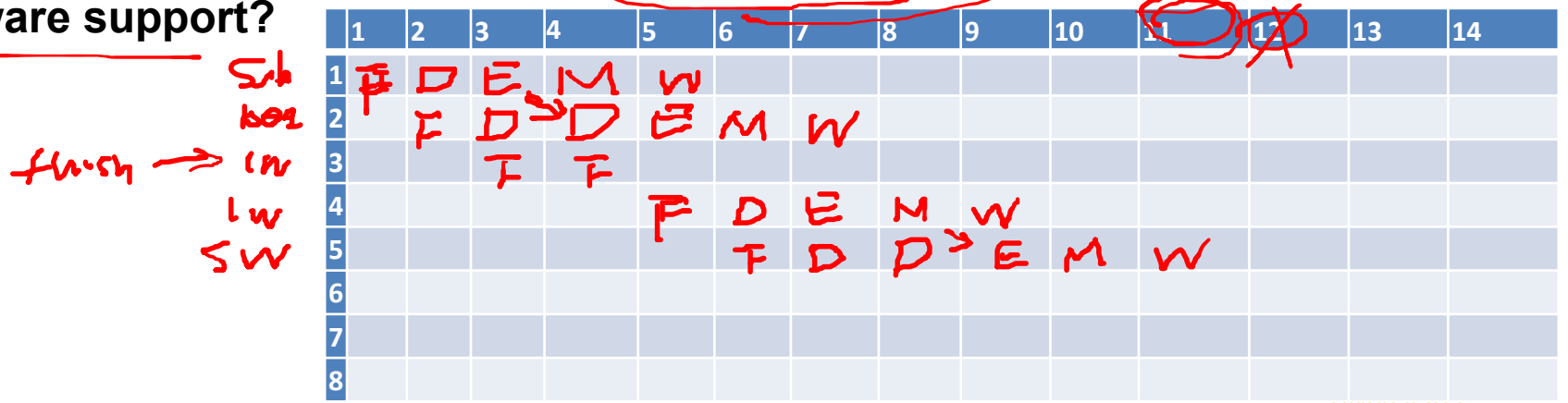
Quiz5 Question (5)

5. Consider the execution of the following code using the 5-stage pipelined MIPS with static branch predictor and early branch determination:

```
sub $t1, $0, $0
beq $t1, $0, Else
lw $t2, 0($s0)
lw $t3, 0($t2)
Else: lw $t4, 8($t2)
sw $t5, 0($t4)
```

How many cycles are required to execute these instructions with and without forwarding hardware support?

A. 11 and 13
B. 12 and 13
C. 11 and 14
D. 12 and 14



Quiz5 Question (5)

5. Consider the execution of the following code using the 5-stage pipelined MIPS with static branch predictor and early branch determination:

```
sub $t1, $0, $0
beq $t1, $0, Else
lw $t2, 0($s0)
lw $t3, 0($t2)
Else: lw $t4, 8($t2)
sw $t5, 0($t4)
```

How many cycles are required to execute these instructions with and without forwarding hardware support?

A. 11 and 13
B. 12 and 13
C. 11 and 14
D. 12 and 14

Quiz5 Question (6)

6. Which of the following condition check is related to the stalling logic in the MIPS pipeline design? (2 possible answers)

A. we_regM and (rsE ≠ 0) and (rf_waM = rsE)

B. ((rsD == rtE) or (rtD == rtE)) and dm2regE

C. branchD and we_regE and ((rf_waE == rsD) or (rf_waE == rtD))

D. branchD and we_regM and (rsD ≠ 0) and (rf_waM == rsD)

Quiz5 Question (7)

7. With static branch predictor but no early branch determination, which of the following CPIs are possible for a branch instruction in the pipelined MIPS machine? (2 possible answers)

A. 1

B. 2

C. 3

D. 4

Quiz5 Question (8)

8. With early branch determination and static branch predictor, which of the following CPIs are possible for a branch instruction in the pipelined MIPS machine?

A. 1

B. 2

C. 3

D. 4

Quiz5 Question (9)

9. Consider the execution of the following code using the MIPS 5-stage pipelined datapath (IF, ID, EX, MEM, WB) with stall and data forwarding logic for data hazard, static branch predictor, and early branch determination logic for control hazard:

```
add, $2, $0, 1
beq $2, $0, Else
lw $3, 4($5)
Else: lw $4, 8($3)
add $5, $3, $4
add $7, $6, $1
add $2, $8, $6
```

During the ninth cycle of execution, what registers are being read, and what registers are being written?

none

Quiz5 Question (9)

9. Consider the execution of the following code using the MIPS 5-stage pipelined datapath (IF, ID, EX, MEM, WB) with stall and data forwarding logic for data hazard, static branch predictor, and early branch determination logic for control hazard:

```
addi $2, $0, 1
beq $2, $0, Else
lw $3, 4($5)
Else: lw $4, 8($3)
add $5, $3, $4
add $7, $6, $1
add $2, $8, $6
```

During the ninth cycle of execution, what registers are being read, and what registers are being written?

None

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	IF	ID	EX	MEM	WB									
2		IF	ID	ID	EX	MEM	WB							
3			IF	IF	ID	EX	MEM	WB						
4					IF	ID	NOP	EXE	MEM	WB				
5						IF	NOP	ID	NOP	EXE	MEM	WB		
6								IF	NOP	ID	EXE	MEM	WB	
7										IF	ID	EXE	MEM	WB
8														

Additional Question

1. Assume a program contains 20 scalar additions and a matrix addition between two matrices. If we want to achieve at least 20x speedup on 50 cores, what could be the dimensions of the matrices?

A. 20 x 20

B. 25 X 25

C. 30 X 30

D. 35 X 35

$$\text{speed w/ E} = \frac{1}{(1-F) + F/S}$$

$$20 < \frac{1}{\frac{20}{20+S} + \frac{S}{(S+20)50}}$$

$$F = \frac{S}{S+20}$$

$S > ?$ X

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