CMPE 200
Computer Architecture & Design

Midterm Review (2)

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Quiz1 Questions

1. What is the function of the following instructions?

```
lw $t0, 32($t1)
sub $t0, $s2, $t0
sw $t0, 32($t1)
```

A. A[8]=h-A[8]

B. h=h-A[8]

C. A[32]=h-A[32]

D. h=h-A[32]

Quiz1 Questions

$2^5 = 32$

$2^3 = 8$

2. Let us assume that we have only 8 registers (instead of 32) for designing a MIPS 32-bit architecture. This would require changes to the I-type instruction format to encode BRANCH instructions. What would be the change to the branch range compared to the original instruction format?

(5-3)

Saved = (2)x(2) = 4 bits

2 regs in I-type

$2^4 = 16$

A. No change

B. Branch range would be 16 times lower

C. Branch range would be 8 times higher

D. Branch range would be 16 times higher

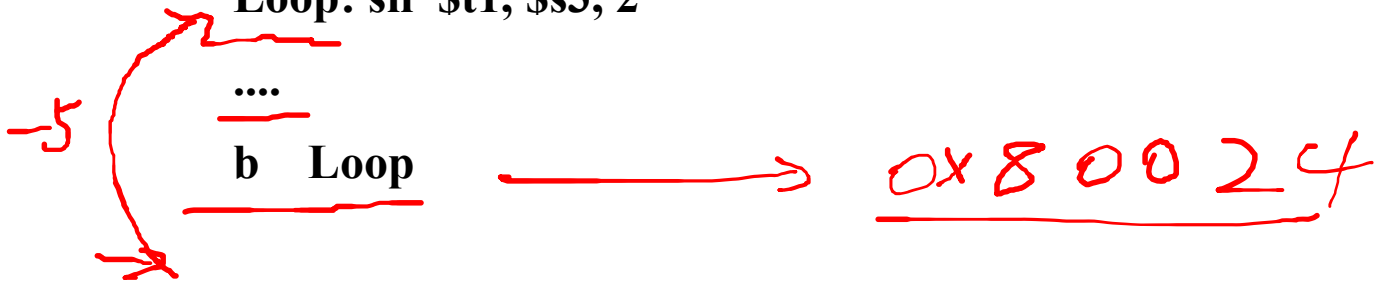
Question & Answer Example

3. For the following instructions:

Loop: sll $t1, $s3, 2

....

b Loop



For the last line of code, if its machine code is 000100 00000 00000 1111111111111011 and address is 0x80024, what is the address of the first line of code?

A. 0x80008

B. 0x8000C

C. 0x80010

D. 0x80014

80028 − 5x4

= 0x80014

Quiz1 Questions

4. Suppose we use 2's complement number system. We have

$t0 = 0xB1C27905

$t1 = 0x1F386420

What is the value of $t2 after the following instructions?

```
slt $t2, $t0, $t1
beq $t2, $zero, ELSE
j DONE
ELSE: addi $t2, $zero, 2
DONE:
```

A. 3

B. 2

C. 1

D. 0

Quiz1 Questions

5. For the following code:

```
sub $t0, $0, $t0
addi $t0, $t0, 1
```

If $t0 stores 1 at the beginning, what is the content of $t0 after executing the instructions above?

A. -1

B. 0

C. 1

D. 2

Quiz1 Questions

6. Computer A executes the MIPS ISA and computer B executes the x86 ISA. On average, programs execute 1.5 times as many MIPS instructions as x86 instructions. Computer A has an average CPI of 1.5 and computer B an average CPI of 3. If computer B runs at a 3GHz clock frequency, what speed does computer A have to run at to be at least as fast as computer B?

A. 1 GHz

B. 1.5 GHz

C. 2.25 GHz

D. 3 GHz

Time_A = Time_B

Time = CPI x # Insty. x 1/freq.

A = 1.5 x 1.5 x X86 x 1/freq.

B = 3 x X86 x 1/3

freq = 1.5^2 = 2.25

Quiz1 Questions

7. Different architecture uses different assembly codes.

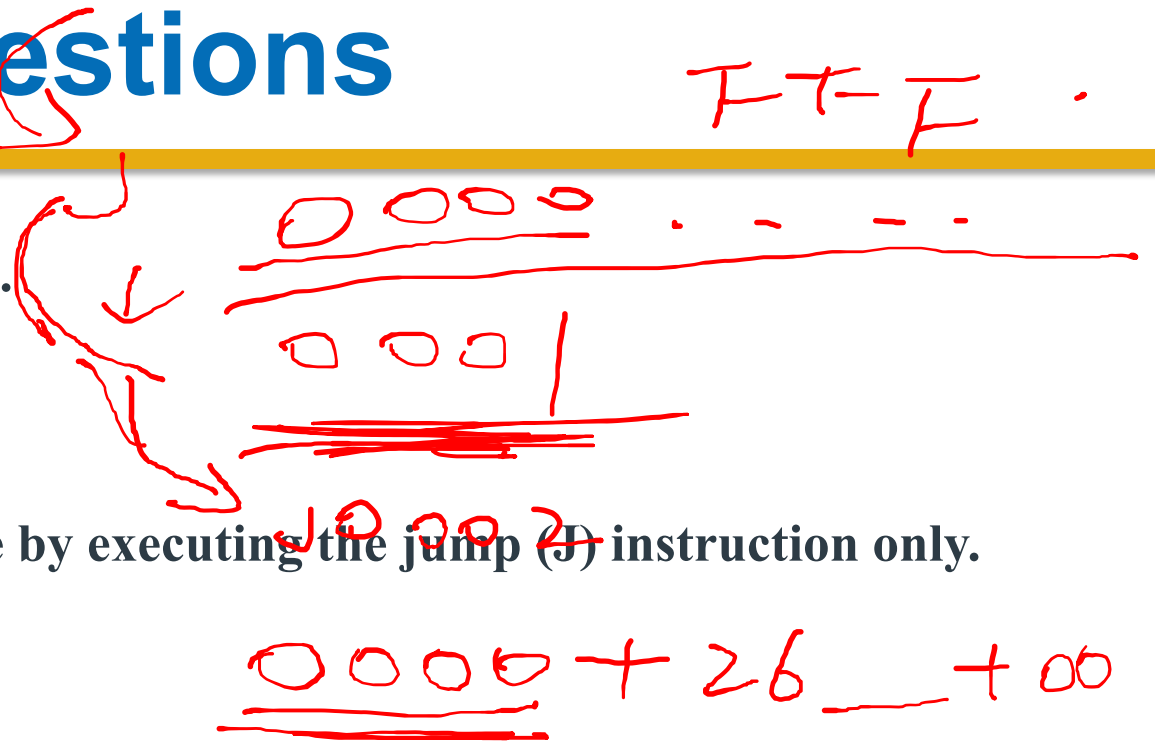
T

8. It is not possible to change the PC to any legal value by executing the jump (J) instruction only.

F

9. Since MIPS use word-oriented memory, we cannot access individual bytes when using MIPS machines.

F



Quiz1 Questions

10. According to Moore's Law, the more transistors we use, the faster our CPUs are.

F

11. Once compiled, the machine code can run on any machine.

F

12. We should increase the voltage of our computer systems to make them more powerful and work at higher frequencies.

F

$C f V^2$

Quiz1 Questions

13. Translate the following C code to MIPS assembly code:

```
int a[10];
int i;
for (i = 0; i < 10; i++){
    a[i] = i;
}
```

```
addi $a0, $0, 0x10
addi $a1, $0, 0
addi $t1, $0, 10
```

```
Forloop:
slt $t2, $a1, $t1
beq $t2, $0, Done
```

```
sll $t2, $a1, 2
add $t2, $t2, $a0
sw $a1, 0($t2)
addi $a1, $a1, 1
```

Quiz2 Questions

1. Let us consider a sequence of procedure calls where procedure A calls procedure B, B calls procedure C, C calls procedure D and D calls procedure E. Each procedure call needs 4 spaces in the stack (including the ra). What would be the overall stack size and how many return addresses are in the stack for this sequence of calls? (The choices are given as stack space size and number of return addresses.)

4 x 4 = 16

A. 16 and 4

B. 16 and 3

C. 12 and 4

D. 12 and 3

Quiz2 Questions

2. In the following MIPS assembler code, how many times is instruction memory accessed and how many times is data memory accessed?

```
Lw $v1,0($a0)
Addi $v0, $v0,1
Sw $v1, 8($a1)
Addi $a0, $a0,1
```

A. instruction memory: 2, data memory: 4

B. instruction memory: 2, data memory: 2

C. instruction memory: 4, data memory: 4

D. instruction memory: 4, data memory: 2

Quiz2 Questions

3. Assume a single-cycle machine has clock cycle 800ps, a 5stage pipeline machine has clock cycle 250ps. How long it will take for this single-cycle machine and pipeline machine to complete 200,000 instructions, respectively?

A. 160,000,000 ps, 50,001,000 ps

B. 200,000,000 ps, 50,001,250 ps

C. 160,000,000 ps, 50,001,250 ps

D. 160,000,000 ps, 250,000,000 ps

$S = 800 \times 200,000$

$P = (K+N-1) = 5 + 200,000 - 1$

$= 200,004 \times 250\ ps$

$=$

Quiz2 Questions

4. After synthesizing a 5-stage pipeline design, the delay for each stage was as follows: IF 200ps, ID 200ps, EX 150ps, MEM 300ps, and WB 250ps. The operating frequency of this pipeline architecture would be:

A. 1.1 GHz

B. 3.33 GHz

C. 6.67 GHz

D. 5 GHz

$$\frac{1}{300\,ps} \approx 3.33\ldots$$

Quiz2 Questions

5. For the following instruction sequence:

addi $3, $0, 5

lw $5, 5($3)

In the single-cycle CPU, what is the ALU's output for the lw instruction?

A. 0

B. 3

C. 5

D. 10

Quiz2 Questions

6. For the following instruction sequence:

lw $5, -16($5)

sw $5, -16($5)

add $5, $5, $5

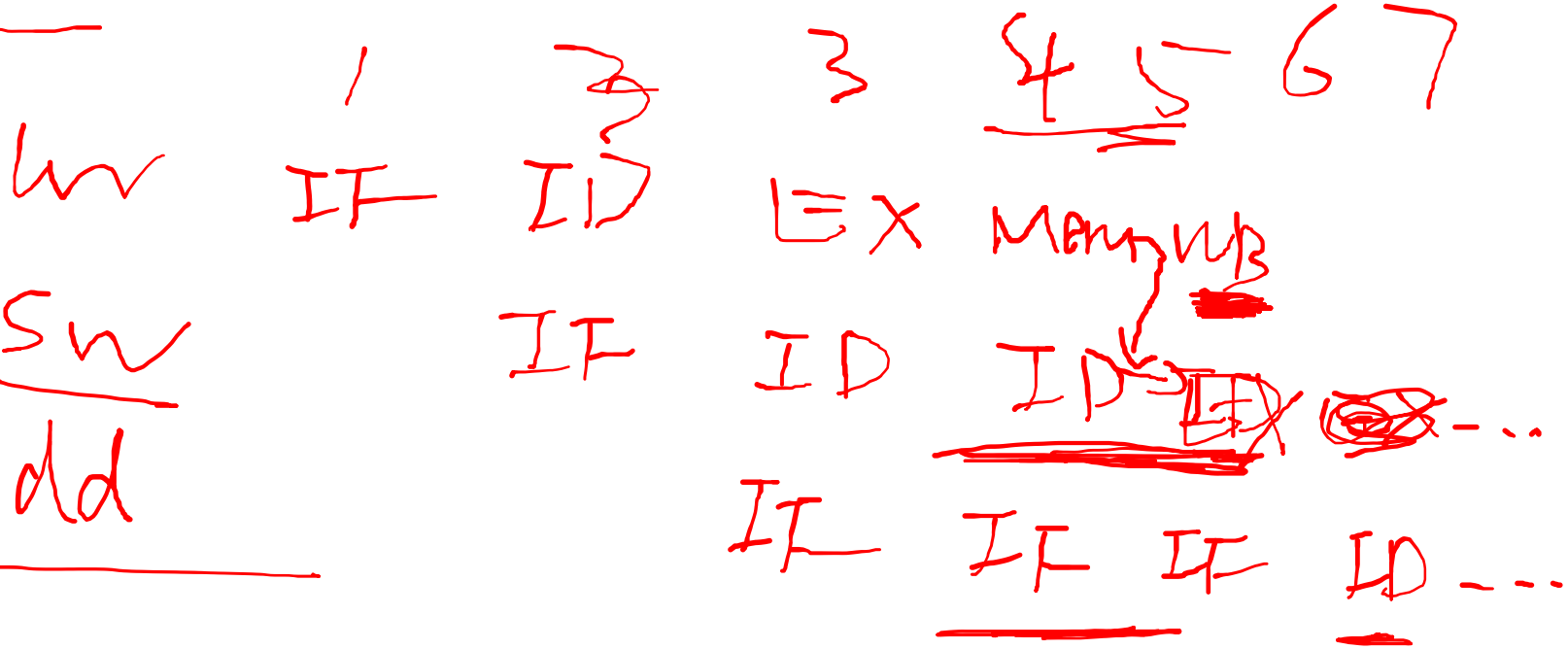
How many nops have to be inserted to eliminate all data hazards assuming there is no forwarding hardware support?

A. 3

B. 1

C. 0

D. 2



Quiz2 Questions

7. Assume a 5-stage pipeline machine has clock cycle 350 ps. Which of the following options are possible for this machine to complete 30,000 instructions?

A. 10,151,400 ps

B. 22,001,400 ps

C. 52,501,400 ps

D. 10,501,400 ps

Worst: 1 + 4 hops = 5 cycles/instr.

5 x 30,000 x 350 = 52,500,000

best: 5 + 30,000 - 1 = 30,004

x 350

= 10,501,400

Quiz2 Questions

8. For pipelined MIPS, LW and SW instructions can stall the pipeline for 2 cycles if there is no data forwarding support.

T / F (F)

9. For a pipelined machine, the structural hazards will not happen if it has a separate instruction cache and data cache.

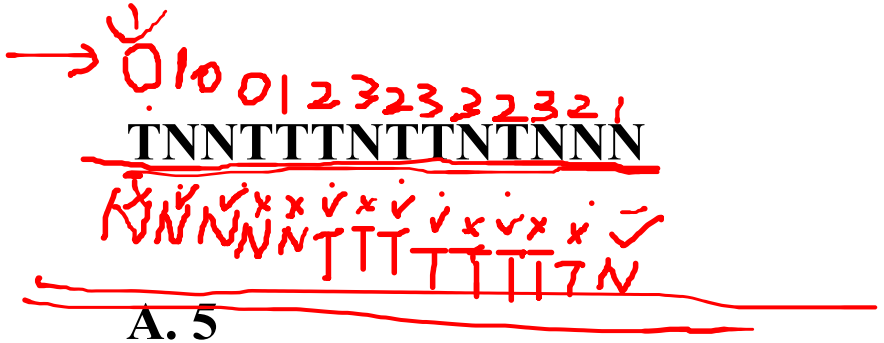
T / F (F)

10. For pipelined MIPS, not all instructions need to use the ALU.

T / F (T)

Processor Example Question

Assuming the initial state is 0, how many correct predictions can be generated for a 2-bit branch predictor given the following actual branch outcomes? (T = Taken = 1, N = Not Taken = 0)



TNNTTTNTTNTNNN

A. 5

B. 6

C. 7

D. 8

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