San José State University
Computer Engineering Department
CMPE 200, Computer Architecture and Design, Section 01, Fall 2022

Course and Contact Information

Instructor(s):	Haonan Wang
Office Location:	ENG 265
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Office Hours:	Mon/Wed 16:15 – 17:15 I welcome you to contact me outside of class and office hours. The best way is to send an email. Individual Zoom meetings can be scheduled if required.
Class Days/Time:	Lecture (Section 01): Mon/Wed 15:00 – 16:15
Classroom:	Clark Building 222
Prerequisites:	CMPE180D or instructor consent. Artificial Intelligence or Computer Engineering or Software Engineering majors only. Students who do not provide documentation of having satisfied the class prerequisite and co-requisite requirements (if any) by the due date will be dropped from the class.

Course Description

Computer design overview, processor instruction set architecture and microarchitecture, instruction-level parallelism, memory hierarchy, storage and I/O systems, multicore/multiprocessor and data/thread-level parallelism, introduction to parallel programming.

Faculty Web Page and MYSJSU Messaging

Course materials such as syllabus, handouts, notes, assignment instructions, etc. can be found on the Canvas Leaning Management System course login website at http://sjsu.instructure.com. You are responsible for regularly checking with the messaging system through MySJSU at http://my.sjsu.edu to learn of any updates.

Course Learning Outcomes (CLO)

Upon successful completion of this course, students will be able to:

1. have an overall understanding of computing systems from architectural and organizational point of view.

2. have an in-depth understanding of RISC processor instruction-set architecture and micro-architecture, as well as memory organization.

3. understand advanced topics such as instruction-level and thread-level parallelism, and multicore/multiprocessor/clustered systems.

Required Texts/Readings

Textbook

Patterson and Hennessy: Computer Organization and Design – the Hardware/Software Interface, 5th Edition or Revised 4th Edition, Morgan Kaufmann (Elsevier).

Other Readings

David and Sarah Harris: Digital Design and Computer Architecture, Morgan Kaufmann (Elsevier), 1st or 2nd Edition.
Hennessy and Patterson: Computer Architecture – A Quantitative Approach, 5th Edition, Morgan Kaufmann (Elsevier).
Michel Dubois, Murali Annavaram, and Per Stenström: Parallel Computer Organization and Design, 1st Edition (Cambridge University Press).

Other technology requirements / equipment / material

1. MIPS assembler and debugger/simulator (http://courses.missouristate.edu/kenvollmar/mars/)
2. Electronics Design Automation (EDA) Tool: Xilinx (http://www.xilinx.com) Vivado Design Suite
3. Miscellaneous simulation tools.

Course Requirements and Assignments

SJSU classes are designed such that in order to be successful, it is expected that students will spend a minimum of forty-five hours for each unit of credit (normally three hours per unit per week), including preparing for class, participating in course activities, completing assignments, and so on. More details about student workload can be found in University Policy S12-3 at http://www.sjsu.edu/senate/docs/S12-3.pdf.

NOTE that University policy F15-12 at https://www.sjsu.edu/senate/docs/F15-12.pdf states that "Students are expected to attend all meetings for the courses in which they are enrolled as they are responsible for material discussed therein, and active participation is frequently essential to ensure maximum benefit to all class members. In some cases, attendance is fundamental to course objectives; for example, students may be required to interact with others in the class. Attendance is the responsibility of the student. Participation may be used as a criterion for grading when the parameters and their evaluation are clearly defined in the course syllabus and the percentage of the overall grade is stated.".

Final Examination or Evaluation

There will be one midterm, one final exam, and up to four pop-up quizzes for this course.

No late Submission will be accepted

An extension will be granted only if a student has serious and compelling reasons that can be proven by an independent authority (e.g., doctor's note if the student has been sick).

All exam dates are final. The only exception is medical emergencies accompanied with doctor's report. The retake of exams may have more difficult set of questions and may not be in the same format.

Grading Information

Assignments: 35%
Midterm: 25%
Final Exam: 35%

Quizzes: 5%
Extra Credit:
Participation: 10% (attendance:6%; asking and answering questions: 4%)
Miscellaneous: 15% (e.g., solving additional questions in assignments and exams)

Determination of Grades

- NO makeup exams will be given. Students will take a full responsibility for not missing any exam.
- Pop-up Quizzes will be used for helping students to earn extra 5% of the total score. There will be up to four quizzes.
- Students can also earn extra credit from assignments and exams. The details will be announced in the classroom.
- The letter grades will be determined like below.

Grade	*Points*	*Percentage*
A plus	*9.6 to 1.00*	*96 to 100%*
A	*9.3 to 9.59*	*93 to 95%*
A minus	*9.0 to 9.29*	*90 to 92%*
B plus	*8.6 to 8.99*	*86 to 89 %*
B	*8.3 to 8.59*	*83 to 85%*
B minus	*8.0 to 8.29*	*80 to 82%*
C plus	*7.6 to 7.99*	*76 to 79%*
C	*7.3 to 7.59*	*73 to 75%*
C minus	*7.0 to 7.29*	*70 to 72%*
D plus	*6.6 to 6.99*	*66 to 69%*
D	*6.3 to 6.59*	*63 to 65%*
D minus	*6.0 to 6.29*	*60 to 62%*

Classroom Protocol

1. Each student is required to engage in classroom activities, submit assignments and reports on time, and take exams and tests on time.
2. Students who disturb the peace and harmony in class, behave disrespectfully to the instructor or his/her fellow students will be immediately dismissed from the class and reported to student affairs for disciplinary action.
3. A student or students involved in a cheating incident in a test, homework, report, or lab project will receive an F in the course and will be reported to the judicial affairs office and subjected to disciplinary action.

University Policies

Per University Policy S16-9 *(http://www.sjsu.edu/senate/docs/S16-9.pdf)*, relevant university policy concerning all courses, such as student responsibilities, academic integrity, accommodations, dropping and adding, consent for recording of class, etc. and available student services (e.g. learning assistance, counseling, and other resources) are listed on Syllabus Information web page (http://www.sjsu.edu/gup/syllabusinfo), which is hosted by the Office of Undergraduate Education. Make sure to visit this page to review and be aware of these university policies and resources.

A student or students involved in a cheating incident involving any homework, quiz, or exam will receive an F on that instrument, and will be reported to the department and related school office. Whether the report will carry a recommendation for disciplinary action will be left to the instructor's judgment.
Please see the University Academic Integrity Policy at http://www.sjsu.edu/senate/docs/F15-7.pdf.

CMPE 200, Section 01, Fall 2022, Course Schedule

The schedule is subject to change with fair notice on the class website.

Course Schedule

Week	Date	Topics	Homework
1	22 Aug.	Course Orientation	Assignment 0 Out
1	24	Computer Architecture Overview – Metrics & Technology Trends (1)	
2	29	Computer Architecture Overview – Metrics & Technology Trends (2)	Prerequisite/ Honesty pledge/ Assignment 1 Out/ Assignment 0 Due
2	31	Processor Instruction Set Architecture & Language (1)	
3	5 Sep.	Labor Day – No Lecture	Assignment 2 Out/ Assignment 1 Due
3	7	Processor Instruction Set Architecture & Language (2)	
4	12	Processor Instruction Set Architecture & Language (3)	Assignment 3 Out/ Assignment 2 Due
4	14	Processor Instruction Set Architecture & Language (4)	
5	19	Processor Instruction Set Architecture & Language (5)	Assignment 4 Out/ Assignment 3 Due
5	21	*Topic Review*	
6	26	Processor Microarchitecture and Design (1)	Assignment 5 Out/ Assignment 4 Due
6	28	Processor Microarchitecture and Design (2)	
7	3 Oct.	Processor Microarchitecture and Design (3)	Assignment 6 Out/ Assignment 5 Due
7	5	Processor Microarchitecture and Design (4)	
8	10	Processor Microarchitecture and Design (5)	Assignment 6 Due/ Assignment 7 Out
8	12	Processor Microarchitecture and Design (6)	
9	17	*Midterm Review*	
9	19	**Midterm Exam**	
10	24	I/O and Interface	
10	26	Memory Hierarchy (1)	
11	31	Memory Hierarchy (2)	Assignment 7 Due/ Assignment 8 Out
11	2 Nov.	Memory Hierarchy (3)	
12	7	Memory Hierarchy (4)	
12	9	Memory Hierarchy (5)	
13	14	Memory Hierarchy (6)	

Week	Date	Topics	Homework
13	16	*Topic Review*	
14	21	Advanced Parallelism, Multicore, Multiprocessors, and GPUs (1)	
14	23	Non-Instructional Day – No Lecture	
15	28	Advanced Parallelism, Multicore, Multiprocessors, and GPUs (2)	Assignment 8 Due
15	30	Advanced Parallelism, Multicore, Multiprocessors, and GPUs (3)	
16	5 Dec.	*Final Exam Review*	
Final Exam		**Thursday, December 8, 12:15 - 14:30**	