CA Assignment - 2

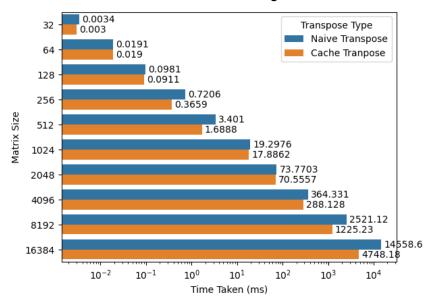
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Question-1 Part-A Single Thread :-

- All graphs are log scaled.
- For sizes :- 16, 4096, 8192, 16384, the program is ran for a total of 3 times for getting stable results.
- The program is ran on dgx server which has Intel(R) Xeon(R) CPU E5-2698 v4 @ 2.20GHz

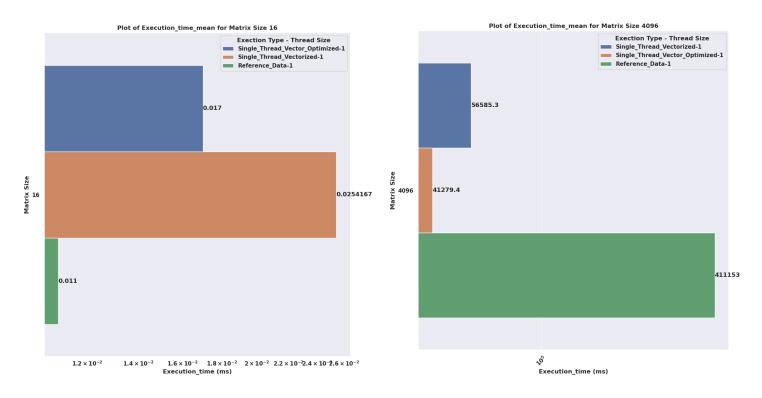
Optimization Process:-

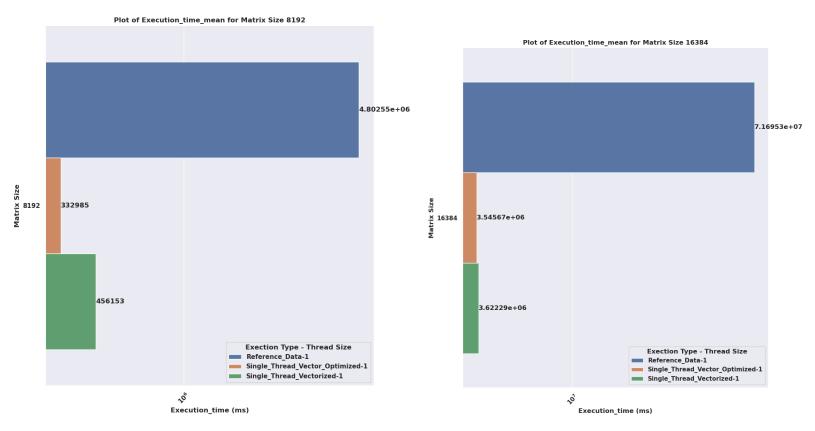
- 1. The very basic optimizations include converting multiplications to right shift and divisions to left shift which doesn't improve performance to a whole lot level but is still taken care of.
- Generally when accessing matrices, fetching the next elements i+1, i+2 (if current index is i) is faster as
 matrices as stored in row-fashion order. Hence with this hunch its better to transpose second matrix
 when performing matrix multiplication to exploit performance.
 - a. 2 different types of transposes methods are used based on the matrix size that is passed to the program.
 - b. Its observed that for smaller matrix sizes naive transpose (get_transpose in code) is same as cache transpose hence for simplicity the former is used.
 - c. But for larger matrix sizes there is an **cache oblivious transpose** approach ("Cache Oblivious Approach", n.d.) which helped achieving speedup of ~3x (-10 secs) for transpose case for matrix size of 16k as can be seen in the below figure.



- 3. The problem statement was to multiply first row and second row of first matrix with first column and second column of second matrix which will be first row and second row of second matrix after transpose of second matrix. In mathematical notation its as follows
 - a. Let f = first, s = second
 - b. Result = A[f] * B[f] + A[f] * B[s] + A[s] * B[f] + A[s] * B[s].
 - c. The above is performing 4 multiplication operations and 3 addition operations which can be reduced as there are some redundant operations.
 - d. The equation in 3b can be reduced using the below equation which is just 2 additions and 1 multiplication.
 - e. Result = (A[f] + A[s]) * (B[f] + B[s])
 - f. This above optimization further helps improve in boosting the performance.
- 4. Further, it was observed that when performing matrix multiplication of A's first 2 rows with B's 2 rows (because of transpose), many computations are getting recalculated again and again. Hence to avoid this 2 new arrays of size N/2 * N are created which will hold the sum of consecutive rows. (0th row of resultant matrix will hold sum of 0th and 1st row of actual matrix, while 1st row of resultant matrix will hold sum of 2nd and 3rd row of actual matrix). Thus whenever matrix multiplication is being done there is no need of performing the addition of consecutive rows everytime.
- 5. Current x86 ISA which is being used in the underlying hardware can only perform an operation on 2 numbers at once. Thus to further exploit performance AVX2 ("Advanced Vector Extensions", n.d.) is being used which can perform same operation on 8 integers at once is being used. There are plots below that show the difference in execution time and other parameters for implementation involving creation of the additional matrices (discussed in the above point 5) along with vectorization does help in improving performance over the implementation where plain vectorization is used.
- 6. The primary disadvantage of it being its not reusable in the sense, if the datatype that operations to be performed changes to floats/double from integer, different methods should be used altogether. Thus a new binary needs to be created altogether by making changes to souce code.
- 7. It was observed that not using vectorization and just interchanging loops (code present in header file) is performing better than the reference function but still slower than the vectorization functions. Its an observation that is made during the initial program building. Hence the data for the same is not captured and thus they will not be seen in any plots.

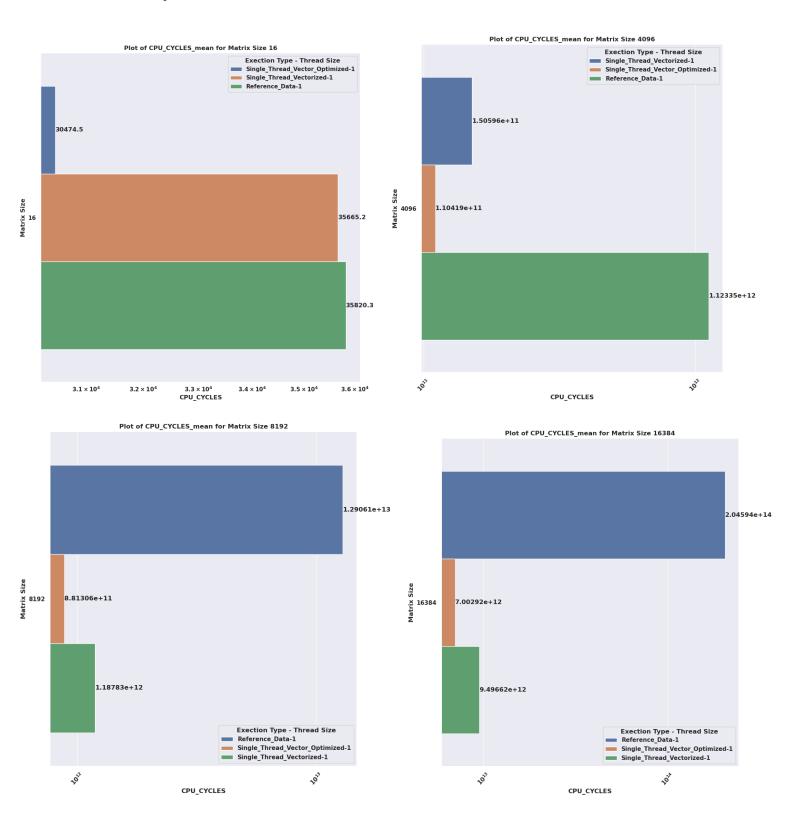
Execution Time



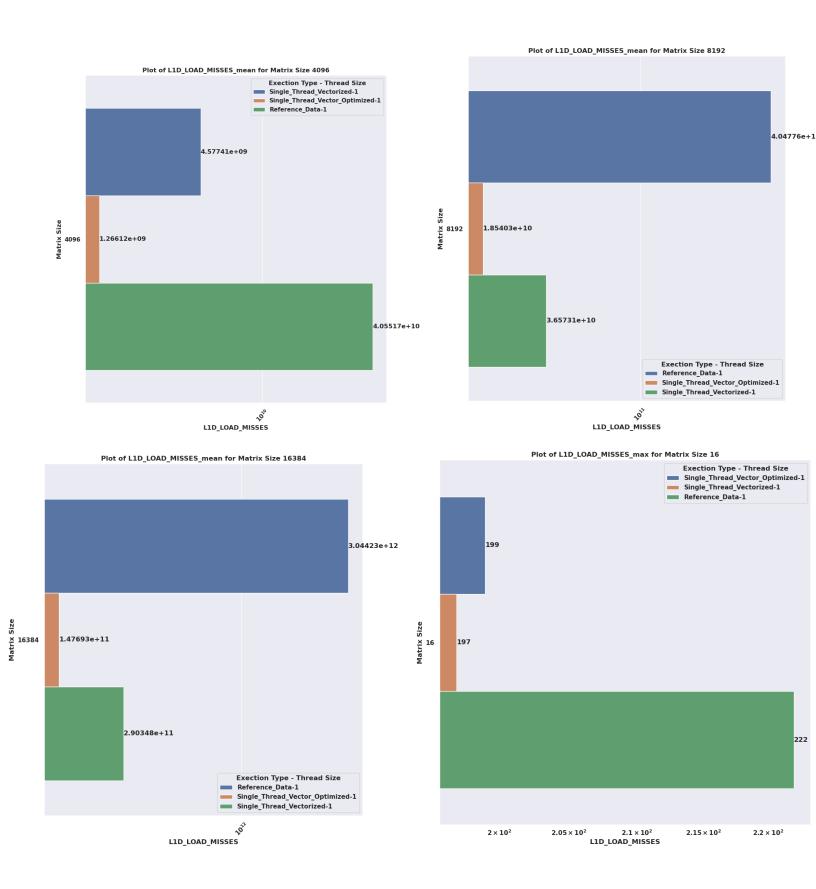


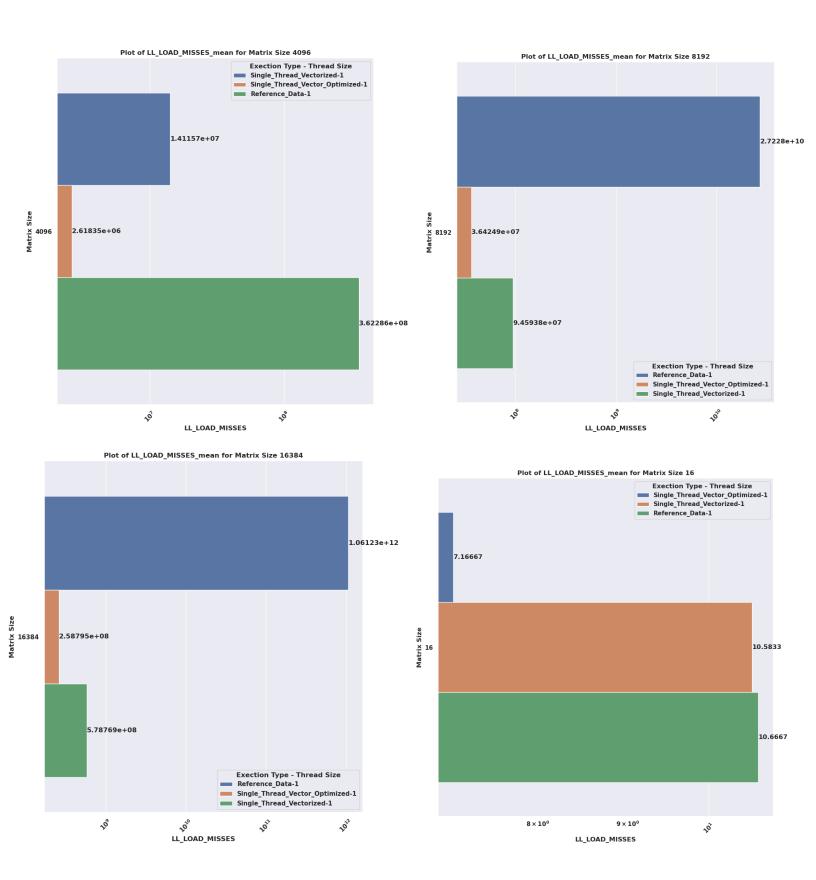
- The above 4 plots show execution time for different matrix sizes (16, 4096, 8192, 16384). Its says
 mean because an average of 3 runs time is captured.
- Reference_Data 1 implies its the time taken by the reference function which uses a single thread to complete execution.
- Single_Thread_Vectorized-1 implies, the matrix multiplication is performed with the help of AVX using a single thread.
- Single_Thread_Vector_Optimized-1 implies before performing matrix multiplication, the optimization mentioned in point 4 is performed which creates 2 N/2*N matrices using vectorization and these matrices are then multiplied using vectorization to produce the final result. (Tranpose of the second matrix is being done in both the optimization types).
- It can be observed from the plots that while vectorization is not ideal for matrices with smaller sizes (still reasonable), but as the size increases, a speedup of ~10x, ~14.5x, ~20.2x for matrix sizes 4096, 8192, 16384 respectively for Single_Thread_Vector_Optimized-1 case and an speedup of ~7.3x, ~10.5x, ~19.8x for matrix sizes 4096, 8192, 16384 respectively for Single_Thread_Vectorized-1 case can be observed, which clearly shows that eliminating the redundant addition operations is indeed helping improve the overall performance. For 16k matrix size, it can be seen that the speedup of the 2 variants were quite close but in general this was not the case. The results that were obtained when running the 16k were contended with processes that were running from other users at the same time hence the slipup in the speedup incase of 16k.

CPU Cycles



om the above plots it can observed that with the help of vectorization the number of cpu cycles are reduced its performing operations on 8 integers at once in this case.
L1 Data and LLC Load misses:





The above plots show the load misses in L1 data and LLC caches. Compared to the misses in smaller sized matrices which are relatively closer, for larger sized matrices it can be clearly seen that the number of misses are not even relatively close because of proper use of locality by using both transpose and vectorization.

Concluding remarks :-

In single threaded version, to achieve as much speedup/performance as possible its better to pre-process few things along with vectorization which helps in performing operations on multiple elements at once.

Question-1 Part-A Multi-Thread:

Implementation Details :-

- Implemented multi-threading using pthreads -
 - Thread Counts ranging from {32, 64, 128, 256}
 - Matrix sizes {16, 4096, 8192, 16384}.
- Implementation:(Optimizations applied in multi-thread as similar to that of the optimization that are applied in single-thread part)
 - Transposed the second matrix (MatB) to convert into row major order to exploit better locality.

```
void get_transpose(int *new_matrix, int *old_matrix, int size)
{
  int diagnol_index, index2, length, shift_factor = (int)(log10(size) / log10(2)), index = 0;
  diagnol_index = (index << shift_factor) + index;
  while (index < size - 1)
  {
    length = size - index;
    index2 = index * (size + 1);
    for (int i = 1; i < length; ++i)
    {
        new_matrix[index2 + (i << shift_factor)] = old_matrix[i + index2];
        new_matrix[i + index2] = old_matrix[index2 + (i << shift_factor)];
    }
    new_matrix[diagnol_index] = old_matrix[diagnol_index];
    ++index;
    diagnol_index = (index << shift_factor) + index;
}
new_matrix[diagnol_index] = old_matrix[diagnol_index];
}</pre>
```

- Below equation is used to reduce the total number of arithmetic operations:
 - $\{Row(i) + row(i + 1)\} \times \{Col(i) + Col(i + 1)\}$

```
// reduce matrix size;
for(int i = 0; i < N; i += 2){
    for(int j = 0; j < N; j++){
        matAG[(i >> 1)*N + j] = matAG[i*N + j] + matAG[(i + 1)*N + j];
        matBG[(i >> 1)*N + j] = matBG[i*N + j] + matBG[(i + 1)*N + j];
    }
}
```

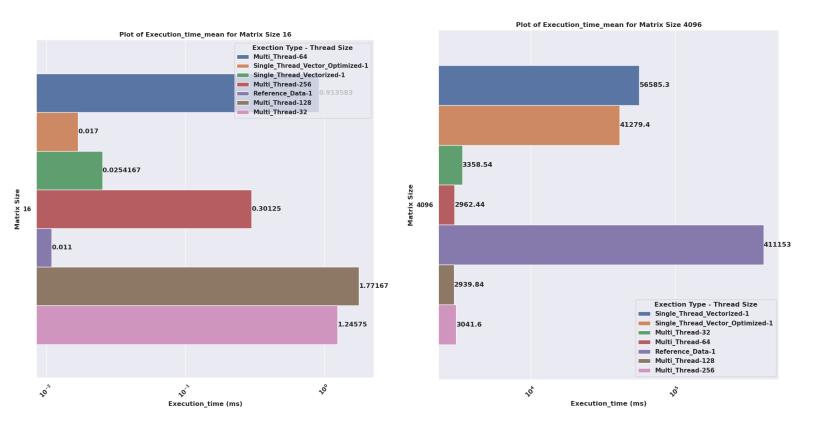
Pre-processed the matrix as above to add two consecutive rows and columns into one, which effectively reduced the matrix sizes to (N / 2) x N and N x (N / 2) respectively

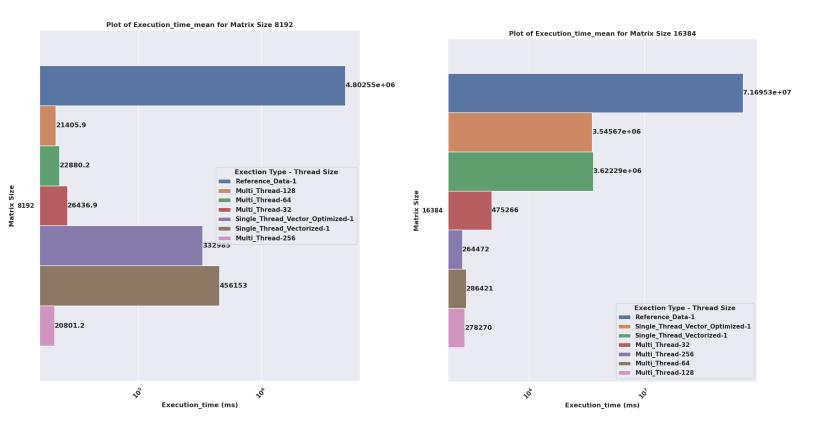
- Sub-divided the matrix multiplication operation as per the
 - load factor(k):- (Input Matrix A rows / # threads)
 - o each thread will be performing (k x (N / 2)) matrix multiplications
- We have keep the input matrices global for better performance, we tried implementing a version where
 for each pthread we sent out the sub-matrix upon which it would operate but yielded results even worse
 than single-thread optimizations.

Performance Report:

• All the results have been averaged over 3 runs for all the combinations of matrix and thread size.

Execution Times



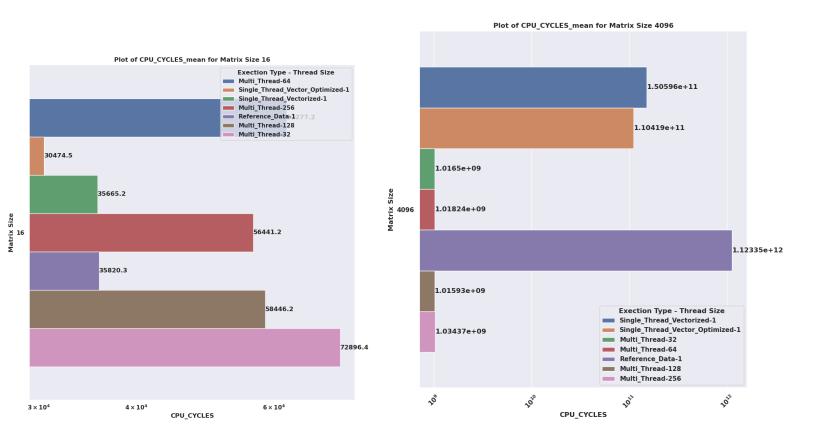


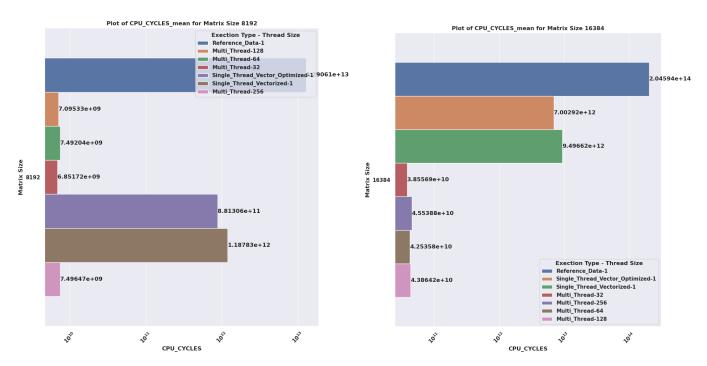
- The above 4 plots show mean execution time for all the matrix sizes along with 4 thread combinations.
- We have compared it with reference time and single thread optimizations.
- From the above plots we can infer that as we gradually increase the thread size from 32 upto 256 we see a gradual decrease in execution times, and thread size 128 yields the best performance.
- We sampled all the params for thread size greater than 256, but either they were giving the same improvement and for larger thread sizes the run times were very high, which is justified as creation of pthreads can add a lot of overhead.
- The threads are able to exploit better parallelism as we have divided the tasks among them in such a way that each thread will operate independently. MatB will shared across all, but since it's a read access there will be no data dependency conflicts.
- As we can see from the plots that multi-threading is not ideal for smaller matrices because of pthread overhead, causing it to perform even worse than base line execution.

Overall we see ~140x, ~224x, ~270x improvements in execution time over baseline and ~14x, ~15x, ~13x improvements in execution time over single-thread for matrices [4096, 8192, 16384]. We can infer that for larger matrix sizes the improvement using multi-threading is significant.

NOTE: While running the execution times for 16k, in some cases we found 540x improvement over baseline,

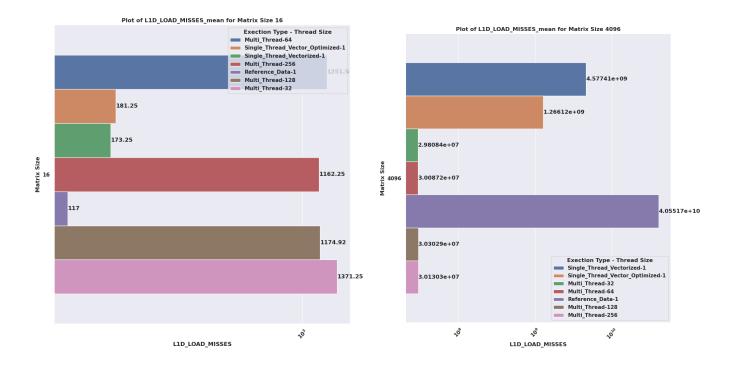
CPU cycles:

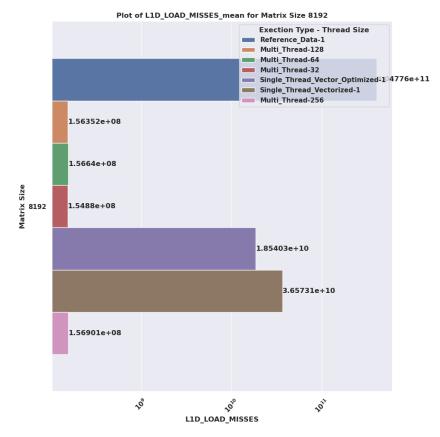


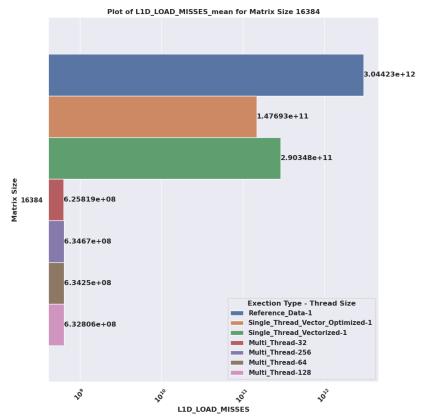


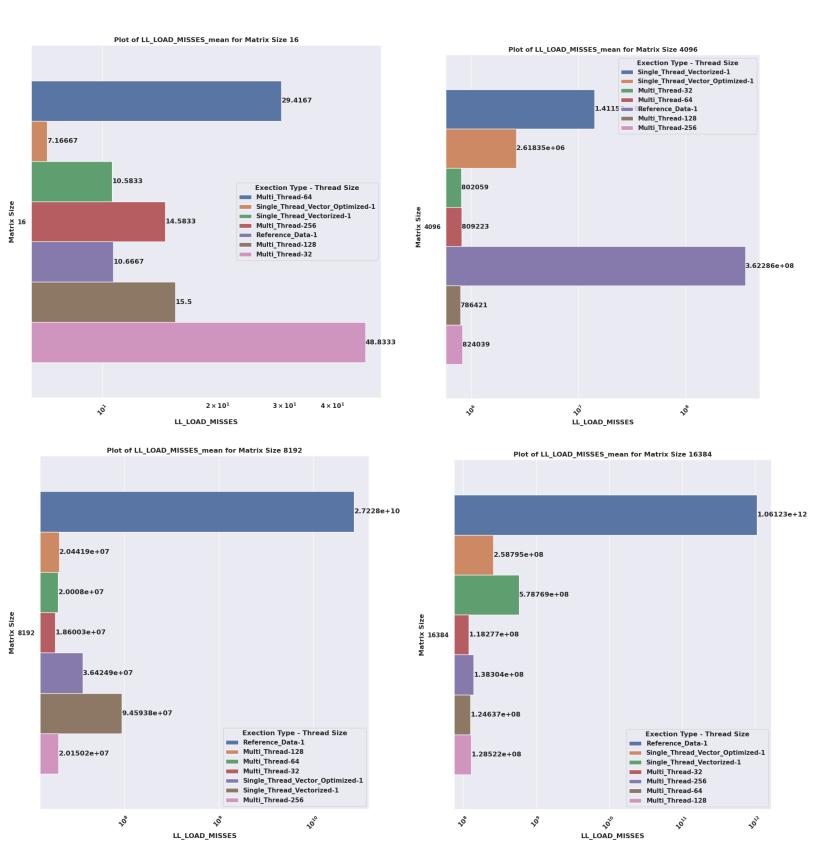
We can clearly see that the number of CPU cycles have substantially reduced in multi-thread variant as compared to others, which justifies the improvement in execution time in the previous plots.

L1 Data and LLC Load Misses:





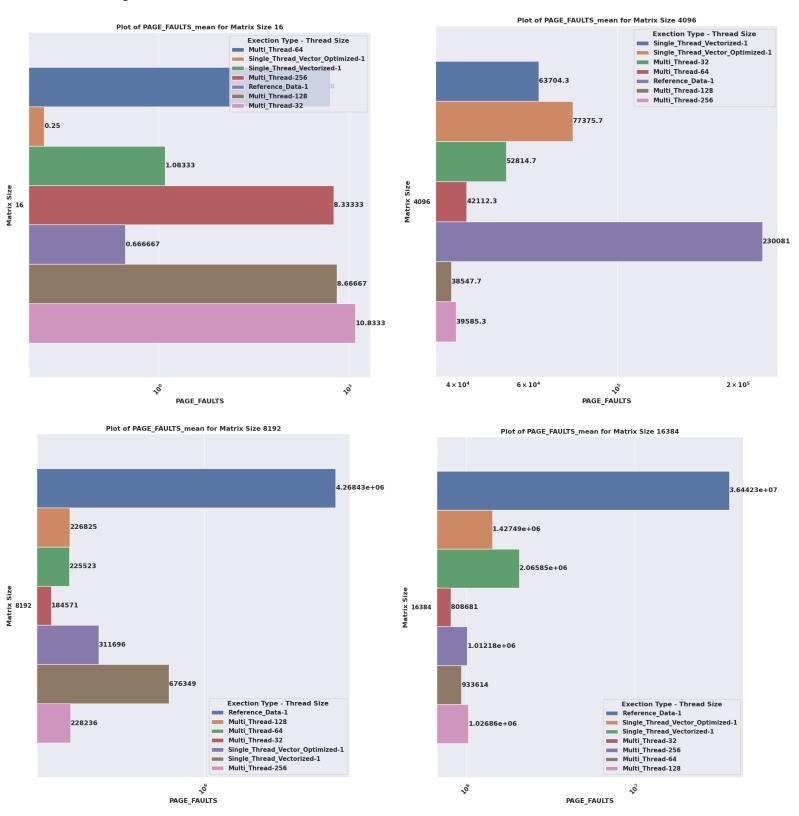




 From above plots we can see a clear reduction in L1D and LLC load misses for multi-thread variant over baseline as well as single thread. This explains multi-threading is exploiting the locality better in

terms of single-thread optimized version as multiple threads are operating on inwhich are already pre-loaded in cache resulting in more cache hits.	dependent sets of data

Page Faults:



- Page-Faults are lower for multi-thread variant than baseline as well as single-thread optimizations.
- Normally, if a thread takes a page fault and must wait for the page to be read from disk, the operating system runs a different thread while the I/O is occurring, this also adds up to improved execution time and hides page-fault latency in case of multi-threading.
- But in our case the overall page-faults are anyways lower, this is because multiple threads are
 operating on different parts of matrix atonce, which leads to lesser page-eviction to disk from
 current process as they are least recently used, unless some-other competing high priority process
 comes into play.

Concluding remarks :-

- In multi-threading we can clearly see a significant improvement in execution times, indicating that the workload we are evaluating has high parallelism.
- Parallelism can be exploited upto a certain extent as spawning very high number of threads(>256) will add to pthread management overhead.
- We are also limited by the logical cores which if not taken care of can yield poor results as most of the time threads will be competing with each other for resources.

Question-1 Part-B:

- Configurations:
 - o NVIDIA Corporation TU104 [GeForce RTX 2080 Rev. A] (rev a1)
 - o **nsight compute** is used to profile the performance counters.
- 1. Optimizations that were used in the previous parts are borrowed and the same are applied in this part aswell.
- Transposing of second matrix is done in GPU only if it exceeds as certain size (32 in out case)
 otherwise the transpose is done in CPU itself as there is no point in allocating cuda memory,
 copying matrix and launching a kernel for smaller sized matrices when the same can be
 achieved in the CPU itself at a similar time.
 - a. Transposing matrix in GPU is done only when matrix size is greater than 32. For the implementation part when coming to sizes greater than 32, its implemented using Coalesced Transpose Via Shared Memory. ("CUDA GPU Transpose", n.d.)
- 3. 2D blocks per grids and 2D threads per blocks are being used for every different matrix sizes for both addition and multiplication of matrices as it helps in better utilization of the overall resources incase the resources are not getting contended.
- 4. For a matrix of size N * N, which creates a resultant matrix of size N/2 * N/2, a total of N/2 * N threads for addition and N/2 * N/2 incase of multiplication are being spawned. so every element of resultant matrix can compute its own value without waiting for any other values. Thus for a matrix size 4096 * 4096, for multiplication phase there will be a total of 4914304 threads.

Results:-

- Nsight cli provides performance counters on a per-kernel basis
- We have used a total of 4 kernel for our implementations and hence in the plotted graphs we will be splitting up the parameters for each kernel.

Execution Times:

We have used nsys for profiling timings and modeled three different times as below:

\$ nsys stats -r cudaapisum,gpukernsum,gpumemtimesum

MAT 128

ime (%)	Total Time (ns)	Num Calls	Avg (ns)) Med	d (ns) M	Min (ns)	Max (ns)	StdDev (ns)	Name
	12,47,98,248		2,07,99,76	98.0 2	,345.5	1,388	12,47,83,669	5,09,41,529.2	cudaMalloc
	72,840		12,14	40.0 1	,781.0	1,271	62,863	24,867.9	cudaFree
	60,610		60,61	L0.0 60	,610.0	60,610	60,610		cudaDeviceSynchronize
	60,024		20,00	08.0 20	,272.0	16,210	23,542	3,673.1	cudaMemcpy
	28,249		7,06	52.3 3	,749.0	2,594			cudaLaunchKernel
	1,153		1,15	53.0 1	,153.0	1,153	1,153		cuModuleGetLoadingMode
	Total Time (ns)								out.sqlite] Name
Time (%)	Total Time (ns)	Instances	Avg (ns)	Med (ns)) Min (n. 	ns) Max	(ns) StdDev (ns)	Name
Γime (%) 65.8	Total Time (ns) 43,508	Instances	Avg (ns) 21,754.0	Med (ns)) Min (n 9 21,5	ns) Max ((ns) StdDev (,962 29	ns) 4.2 _Z7add_gpu	Name iiPiS_ii
Time (%)	Total Time (ns) 43,508 20,046	Instances2 1	Avg (ns)	Med (ns) 21,754.0 20,046.0) Min (n 0 21,5 0 20,0	ns) Max (546 21	(ns) StdDev (,962 29	ns) 4.2 _Z7add_gpu	Name iPiS_ii vly_gpu_less_threadsPiS_S_iii
Fime (%) 65.8 30.3 3.9	Total Time (ns)	Instances 2 1 1	Avg (ns) 21,754.0 20,046.0 2,586.0	Med (ns) 21,754.0 20,046.0 2,586.0) Min (n 0 21,5 0 20,0 0 2,5 rget-linu	ns) Max (546 21 946 20 586 2 ux-x64/rep	(ns) StdDev (ns) 4.2 _Z7add_gpt 0.0 _Z25multip 0.0 _Z13transp	Name uiPiS_ii oly_gpu_less_threadsPiS_S_iii oose_gpuPiS_ii
fime (%) 65.8 30.3 3.9 unning [/	Total Time (ns)	Instances 2 1 1 .7/nsight-s Count Avg	Avg (ns) 21,754.0 20,046.0 2,586.0 systems-2022 g (ns) Med	Med (ns) 21,754.0 20,046.0 2,586.0 2.1.3/tan (ns) M) Min (n 0 21,5 0 20,0 0 2,5 rget-linu in (ns)	ns) Max ((ns) StdDev (,962 29 ,046 ,586 ports/gpumemti StdDev (ns)	ns) 4.2 _Z7add_gpt 0.0 _Z25multip 0.0 _Z13transp mesum.py mat-12 Operation	Name
Time (%) 65.8 30.3	Total Time (ns)	Instances	Avg (ns) 21,754.0 20,046.0 2,586.0 systems-2022 ((ns) Med 974.0 3,9	Med (ns) 21,754.0 20,046.0 2,586.0 2.1.3/tan (ns) M) Min (n 0 21,5 0 20,0 0 2,5 rget-linu	ns) Max ((ns) StdDev (ns) 4.2 _Z7add_gpt 0.0 _Z25multip 0.0 _Z13transp	Name

MAT 4096:

Time (%)	Total Time (ns)	Num Calls	Avg (ns)	Med (ns)	Min (ns)	Max (ns)	StdDev (ns)	Name
75.6	44,03,14,792		44,03,14,792.0	44,03,14,792.0	44,03,14,792	44,03,14,792		cudaDeviceSynchronize
	11,75,20,091		1,95,86,681.8	92,769.0	66,315	11,70,95,270	4,77,69,259.0	cudaMalloc
	1,95,37,493		65,12,497.7	65,80,847.0	63,41,762	66,14,884	1,48,837.6	cudaMemcpy
	52,79,000		8,79,833.3	10,37,652.0	1,22,674	11,17,094	3,80,504.4	cudaFree
	35,818		8,954.5	5,670.5	2,732	21,745	8,948.5	cudaLaunchKernel
	570		570.0	570.0	570	570		cuModuleGetLoadingMode
	usr/local/cuda-11 Total Time (ns)					ernsum.py mat-4 Max (ns)	O96.out.sqlite] Name
ime (%)	Total Time (ns)	Instances	Avg (ns)	Med (ns)	Min (ns)	Max (ns)	StdDev (ns)	Name
ime (%)	Total Time (ns)43,34,25,998	Instances	Avg (ns) 43,34,25,998.0	Med (ns) 	Min (ns) 43,34,25,998	Max (ns)43,34,25,998	StdDev (ns)	Name Z12multiply_gpuPiS_S_iiiii
Γime (%)	Total Time (ns)	Instances	Avg (ns) 	Med (ns) 43,34,25,998.0 33,48,516.0	Min (ns) 43,34,25,998 33,37,264	Max (ns) 	StdDev (ns) 0.0 15,912.7	Name
Fime (%) 98.4 1.5 0.1	Total Time (ns) 43,34,25,998 66,97,032	Instances 1 2 1	Avg (ns) 43,34,25,998.0 33,48,516.0 3,79,376.0	Med (ns)43,34,25,998.0 33,48,516.0 3,79,376.0	Min (ns)43,34,25,998 33,37,264 3,79,376	Max (ns) 43,34,25,998 33,59,768 3,79,376	StdDev (ns) 0.0 15,912.7 0.0	Name
98.4 1.5 0.1	Total Time (ns)	Instances 1 2 1	Avg (ns) 	Med (ns)	Min (ns) 	Max (ns) 43,34,25,998 33,59,768 3,79,376	StdDev (ns) 0.0 15,912.7 0.0	Name
Fime (%) 98.4 1.5 0.1	Total Time (ns)	Instances	Avg (ns) 	Med (ns)	Min (ns) 	Max (ns)	StdDev (ns) 0.0 15,912.7 0.0 1-4096.out.sql	Name Z12multiply_gpuPiS_S_iiiii _Z7add_gpuiPiS_ii _Z13transpose_gpuPiS_ii ite]

MAT 8192

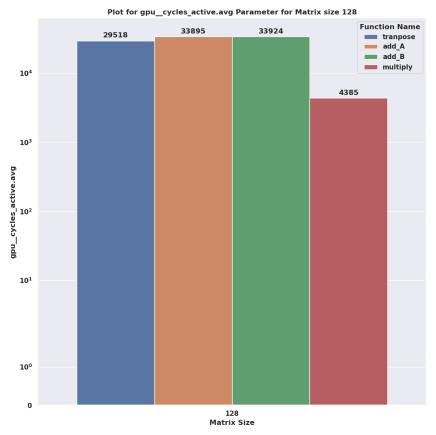
Time (%)	Total Time (ns)	Num Calls		Med (ns)	Min (ns)		StdDev (ns)	
94.3	3,38,25,07,574		3,38,25,07,574.0	3,38,25,07,574.0	3,38,25,07,574	3,38,25,07,574		cudaDeviceSynchronize
	11,79,17,688		1,96,52,948.0	1,99,028.0	90,648	11,70,49,755	4,77,14,524.6	cudaMalloc
	7,72,33,030		2,57,44,343.3	2,61,42,160.0	2,49,12,260	2,61,78,610	7,20,835.7	cudaMemcpy
			12,84,548.5	12,22,664.5	2,96,137	20,13,034	6,27,056.1	cudaFree
	32,081		8,020.3	6,178.5	2,723	17,001	6,743.5	cudaLaunchKernel
	870		870.0	870.0	870	870		cuModuleGetLoadingMode
	usr/local/cuda-11 Total Time (ns)			rget-linux-x64/rep Med (ns)			.sqlite] StdDev (ns)	
							StdDev (ns)	
Time (%) 	Total Time (ns)3,36,80,05,878	Instances	Avg (ns)3,36,80,05,878.0	Med (ns)3,36,80,05,878.0	Min (ns)3,36,80,05,878	Max (ns)3,36,80,05,878	StdDev (ns)	 _Z12multiply_gpuPiS_S_iiii
Fime (%) 99.6 0.4	Total Time (ns) 3,36,80,05,878 1,31,30,814	Instances1 2	Avg (ns) 3,36,80,05,878.0 65,65,407.0	Med (ns) 3,36,80,05,878.0 65,65,407.0	Min (ns) 3,36,80,05,878 65,16,808	Max (ns) 3,36,80,05,878 66,14,006	StdDev (ns) 0.0 68,729.4	 _Z12multiply_gpuPiS_S_iiii _Z7add_gpuiPiS_ii
Γime (%) 99.6	Total Time (ns)3,36,80,05,878	Instances	Avg (ns) 3,36,80,05,878.0 65,65,407.0	Med (ns)3,36,80,05,878.0	Min (ns) 3,36,80,05,878 65,16,808	Max (ns)3,36,80,05,878	StdDev (ns) 0.0 68,729.4	 _Z12multiply_gpuPiS_S_iiii
Fime (%) 99.6 0.4 0.1	Total Time (ns) 3,36,80,05,878 1,31,30,814 17,28,339 usr/local/cuda-11	Instances 1 2 1	Avg (ns) 3,36,80,05,878.0 65,65,407.0 17,28,339.0 systems-2022.1.3/ta	Med (ns) 3,36,80,05,878.0 65,65,407.0 17,28,339.0	Min (ns) 3,36,80,05,878 65,16,808 17,28,339 ports/gpumemtimes	Max (ns) 3,36,80,05,878 66,14,006 17,28,339	StdDev (ns) 0.0 68,729.4 0.0 out.sqlite]	 _Z12multiply_gpuPiS_S_iiii _Z7add_gpuiPiS_ii
99.6 0.4 0.1	Total Time (ns)	Instances 1 2 1	Avg (ns) 3,36,80,05,878.0 65,65,407.0 17,28,339.0 systems-2022.1.3/ta	Med (ns)3,36,80,05,878.0 65,65,407.0 17,28,339.0	Min (ns) 3,36,80,05,878 65,16,808 17,28,339 ports/gpumemtimes	Max (ns) 3,36,80,05,878 66,14,006 17,28,339	StdDev (ns) 0.0 68,729.4 0.0	 _Z12multiply_gpuPiS_S_iiii _Z7add_gpuiPiS_ii
Time (%) 99.6 0.4 0.1	Total Time (ns) 3,36,80,05,878 1,31,30,814 17,28,339 usr/local/cuda-11	Instances 1 2 1 .7/nsight-s	Avg (ns) 3,36,80,05,878.0 65,65,407.0 17,28,339.0 systems-2022.1.3/ta	Med (ns) 3,36,80,05,878.0 65,65,407.0 17,28,339.0 rget-linux-x64/rep	Min (ns) 3,36,80,05,878 65,16,808 17,28,339 orts/gpumemtimes Max (ns)	Max (ns) 3,36,80,05,878 66,14,006 17,28,339 cum.py mat-8192.6	StdDev (ns) 0.0 68,729.4 0.0 out.sqlite]	 Z12multiply_gpuPiS_S_ _Z7add_gpuiPiS_ii _Z13transpose_gpuPiS_i [,]

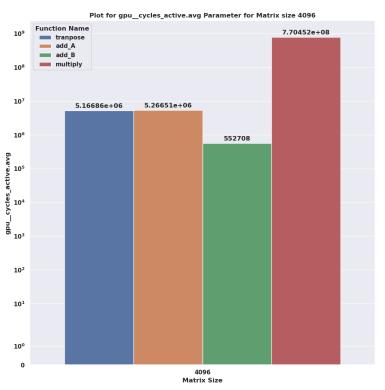
MAT 16384

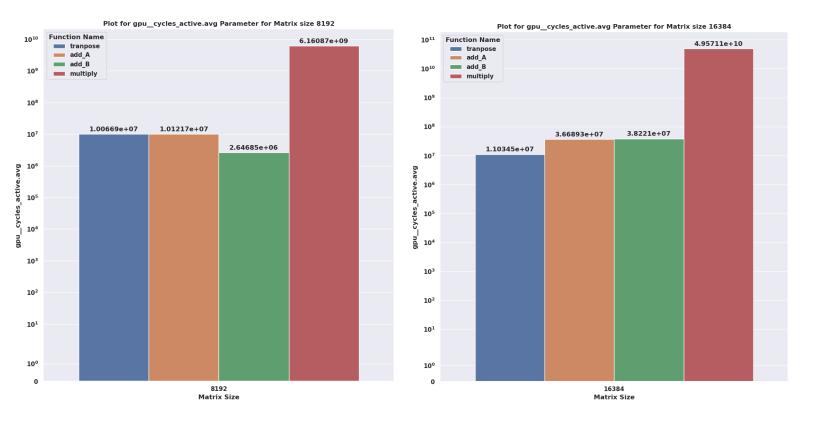
Time (%)		Num Calls						
	30,59,88,426			10,37,99,136.0	9,83,37,871	10,38,51,419		
	11,97,47,489		1,99,57,914.8				1 4,76,71,575.5	
			19,24,411.2		8,38,822	28,43,583		
						22,584		cudaLaunchKernel
	1,099		1,099.0	1,099.0	1,099	1,099		cuModuleGetLoadingMode
	/usr/local/cuda-11		ystems-2022.1.3/tar		ts/gpukernsum.py			
	27,17,24,87,160							_Z12multiply_gpuPiS_S_iii
								_Z7add_gpuiPiS_ii
								_Z13transpose_gpuPiS_ii
nning [/	/usr/local/cuda-11	.7/nsight-s	vstems-2022.1.3/tar	get-linux-x64/repor	ts/gpumemtimesum.	pv mat-16384.ou	t.sqlitel	
ime (%)	Total Time (ns)	Count	Avg (ns) Med	l (ns) Min (ns	s) Max (ns)	StdDev (ns)	Operation	
	20,75,35,914	2 10,	37,67,957.0 10,37	.67,957.0 10,37,63,	440 10,37,72,474	6,388.0	[CUDA memcpy Htol	 D]
	Total Time (ns) 20,75,35,914 9,76,32,460			Min (ns) 67,957.0 10,37,63, 32,460.0 9,76,32,	440 10,37,72,474		Operation [CUDA memcpy Htol	

- ++ The above tables show the bifurcation of the times taken by cuda-api's and kernel's launched by us.
- ++ The majority of time is being consumed by the multiplication kernel itself.
- ++ Whereas the next top consumer is the cudamemcpy operation, in which the host to device copy is the bottleneck.

GPU Cycles:



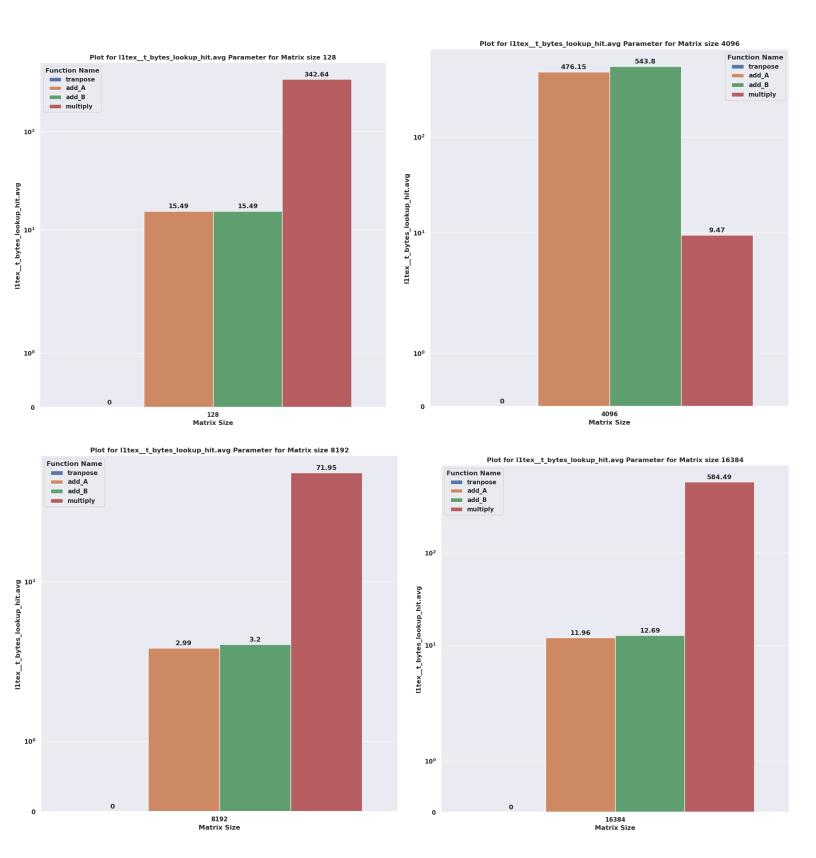




Kernel for matrix multiplication is the top consumer in terms of GPU cycles, which is justified as this where the core logic resides.

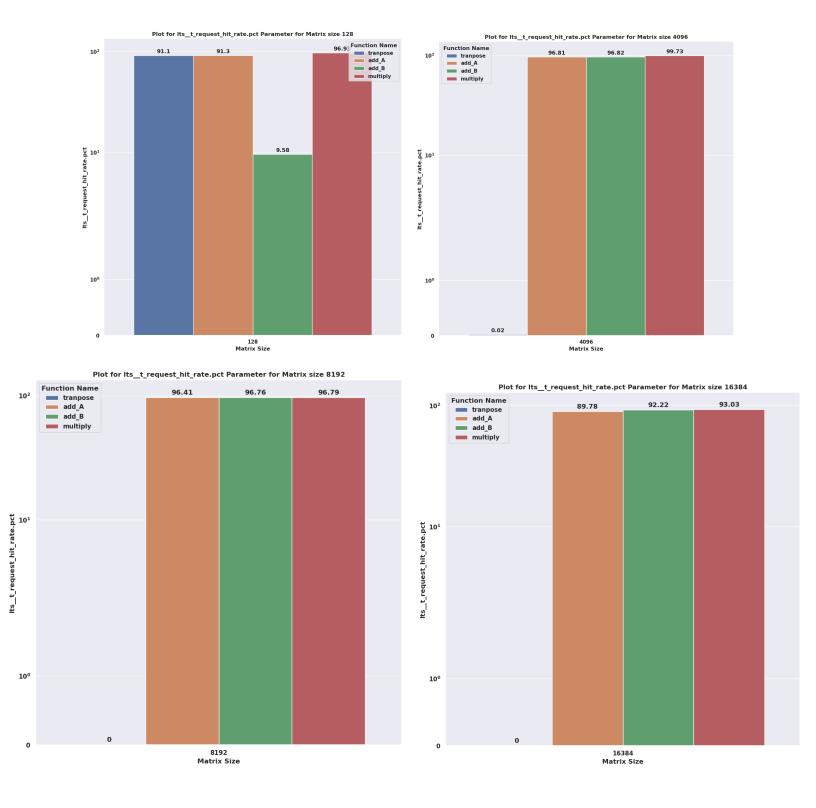
L1 Texture Cache hit rate:

The Level 1 (L1)/Texture Cache is located within the GPC. It can be used as directed-mapped shared memory and/or store global, local and texture data in its cache portion. I1tex__t refers to its Tag stage. I1tex__m refers to its Miss stage. I1tex__d refers to its Data stage.



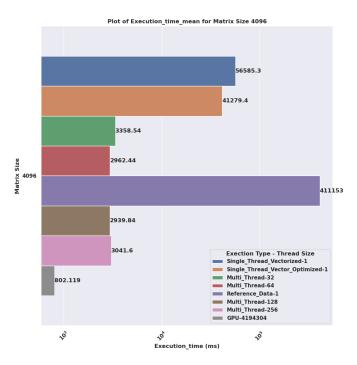
L2 Cache (lts__t):

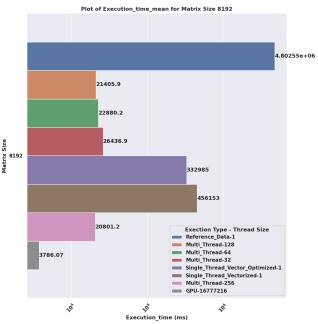
A Level 2 (L2) Cache Slice is a sub-partition of the Level 2 cache. Its_t refers to its Tag stage.

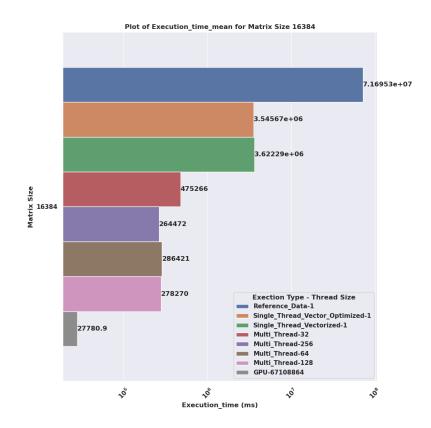


++ We can see all operations except transpose have a hit rate of above 90%.

Concluding remarks :-







It can be observed that with respect to reference execution time the GPU is ~512x, ~1268x, ~2590x faster for matrix sizes of 4096, 8192 and 16384 respectively. It can be observed that the higher the matrix sizes the better its to use GPU because of the number of parallel threads that it can support.

This also supports our previous claim of high parallelism in workload made in multi-threading.

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