

The Evolution and the Future of IBM Quantum Hardware

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IBM Quantum

Outline

- Intro & Building Blocks
- Looking Back 10 Years
- What Has Changed?
 - Control Electronics
 - Wiring
 - Packaging
 - Gate Errors / Chip Performance
- Hardware Innovation Towards Error-Corrected Quantum Computation
 - qLDPC Error Correcting Codes
 - Efforts for Realizing
- Building a Bigger Computer

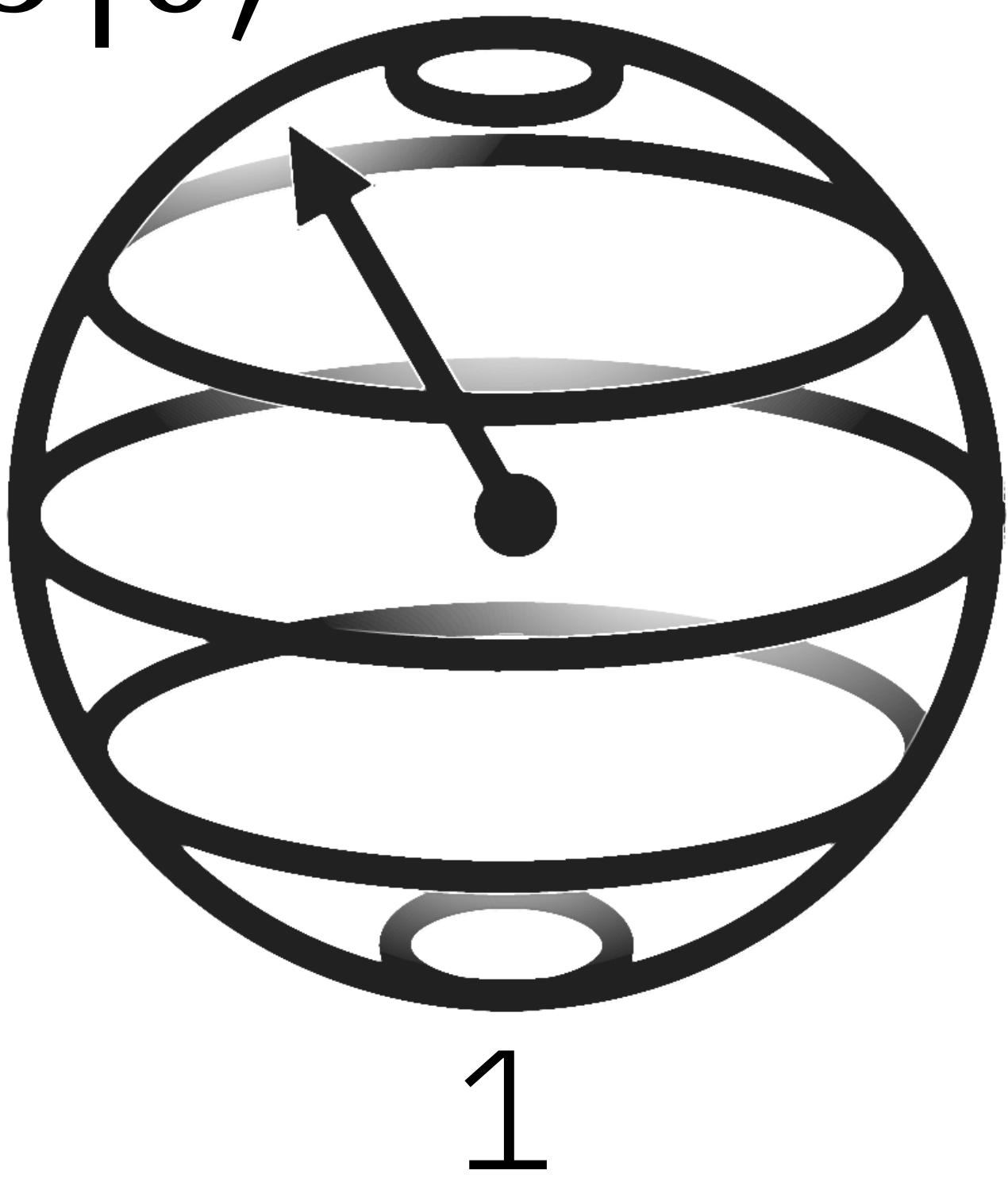
Introduction & Building Blocks

A Classical Bit

1 0

A Qubit

$\alpha|1\rangle + \beta|0\rangle$

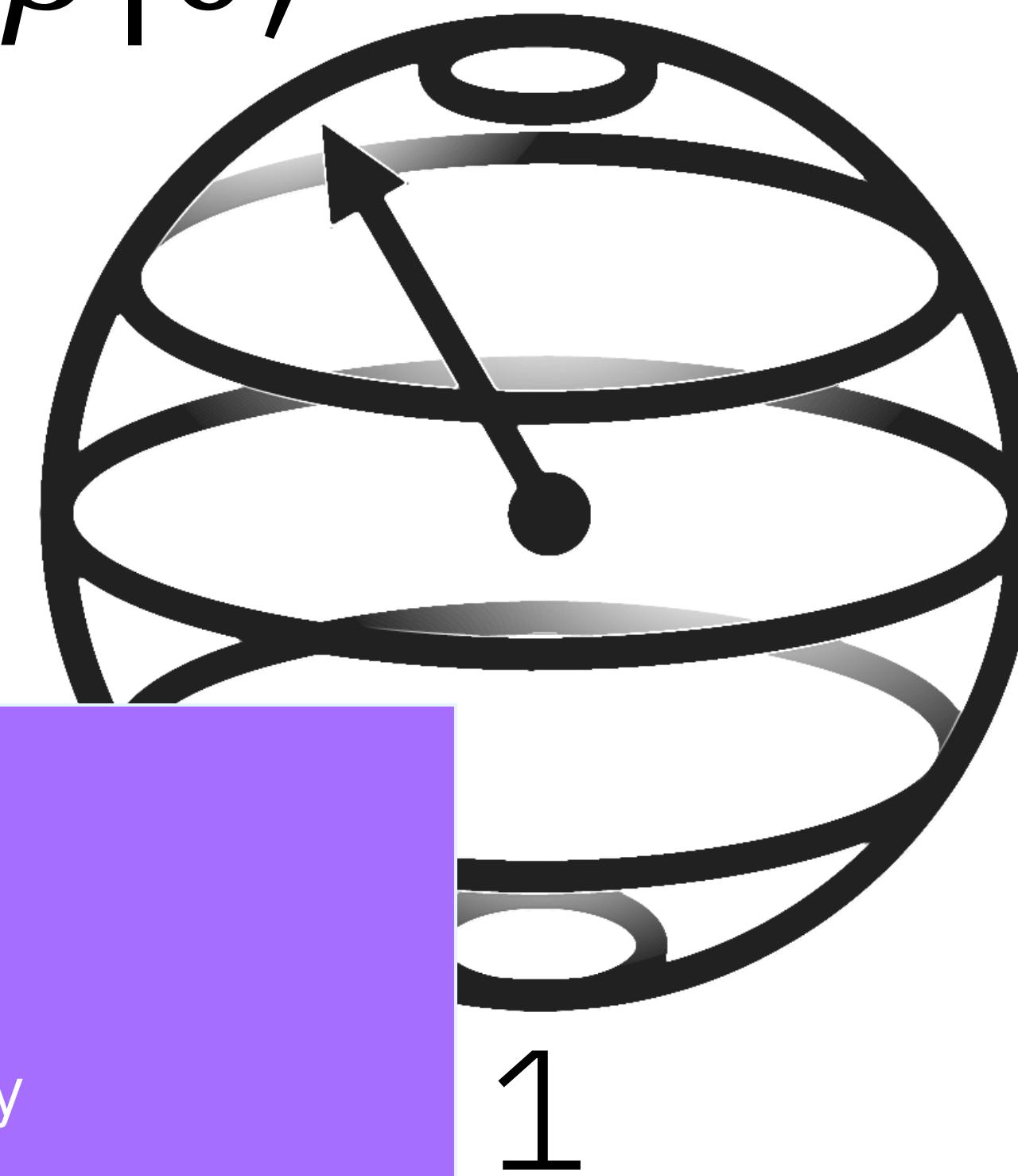


A Classical Bit

1 0

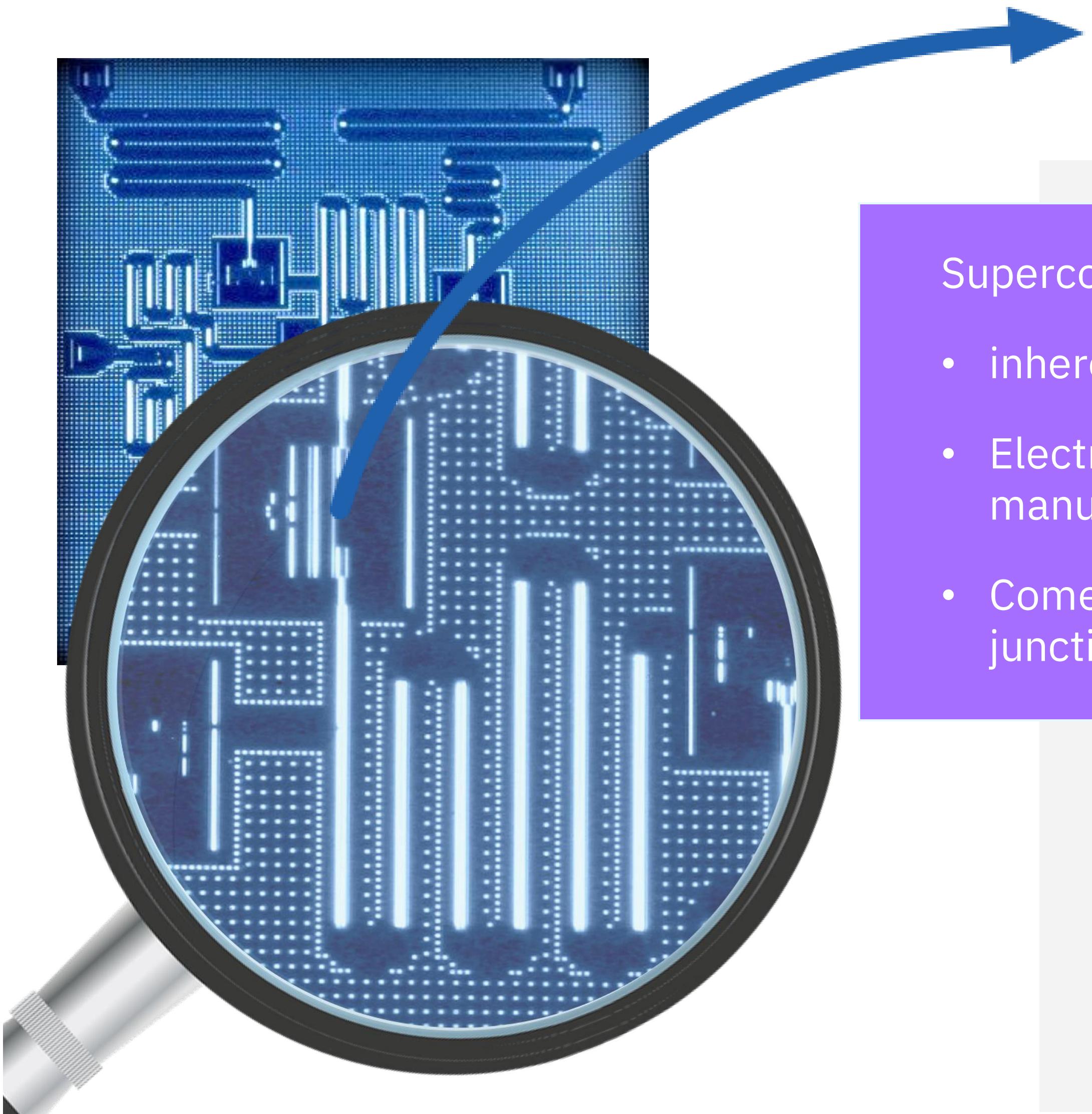
A Qubit

$$\alpha|1\rangle + \beta|0\rangle$$



- Encode any multi-qubit state,
- for long enough
- that we can perform necessary manipulations.
- Also, need a way for measuring the state.

The Transmon



Superconducting Qubit:

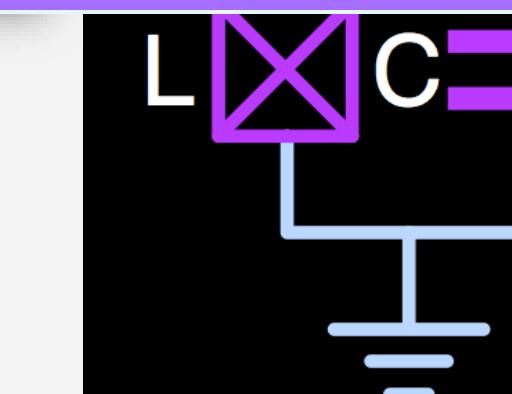
Superconducting circuits:

- inherently low loss.
- Electrical circuits – huge flexibility for design and easy manufacturability.
- Come with a native non-linear element – the Josephson junction.



100 nm
X 100 nm

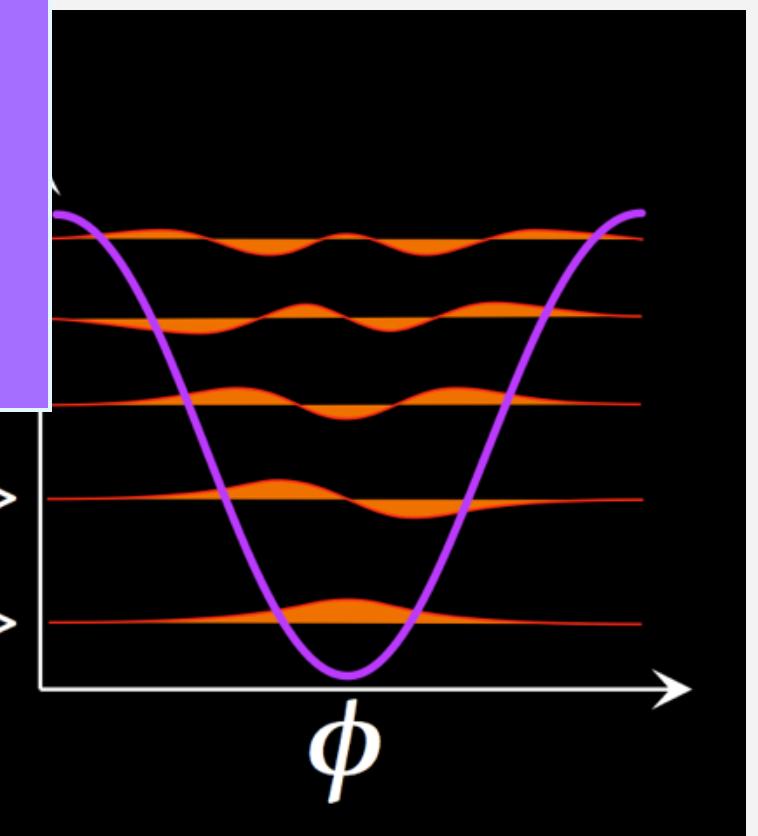
$$H = q^2 + \cos(\Phi)$$



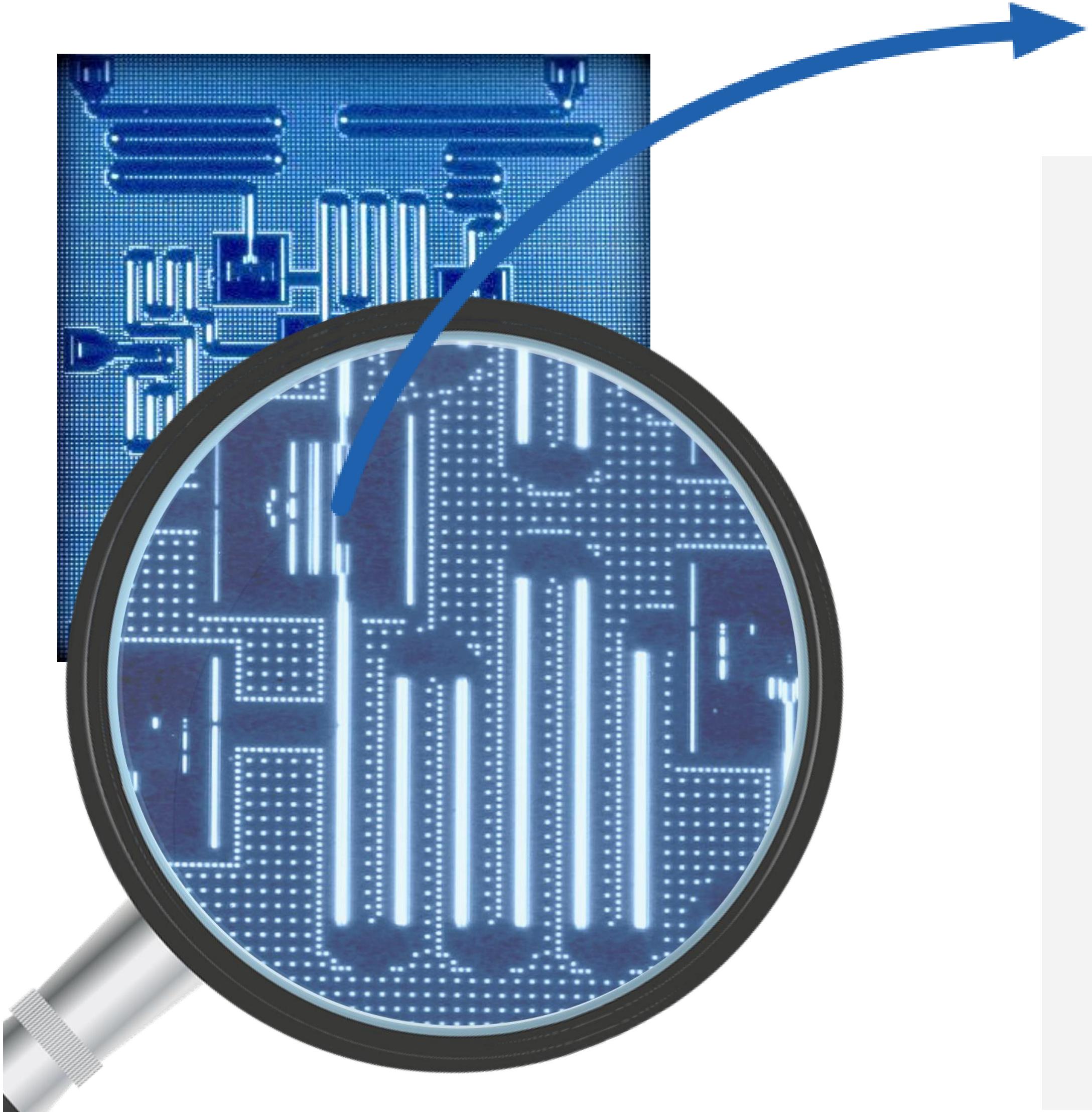
$$E_{01} \approx 5 \text{ GHz} \approx 240 \text{ mK}$$

$$\frac{dI}{dt} = \frac{1}{L} V(t)$$
$$L = \frac{\Phi_0}{2\pi I_0 \cos(\phi)}$$

Non-linear inductor

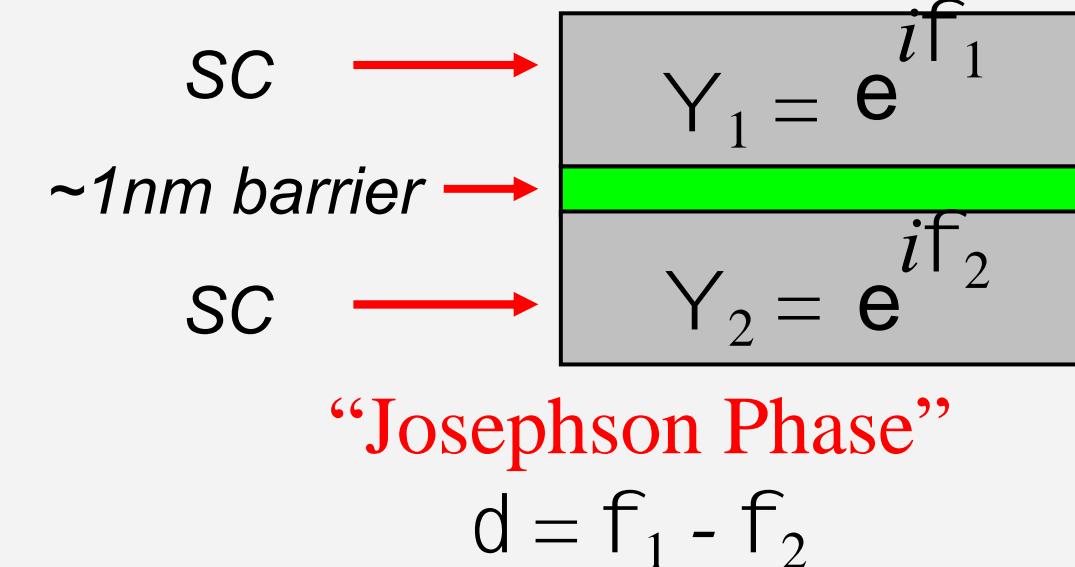


The Transmon



Superconducting Qubit:

Josephson Junction as a non-linear inductor

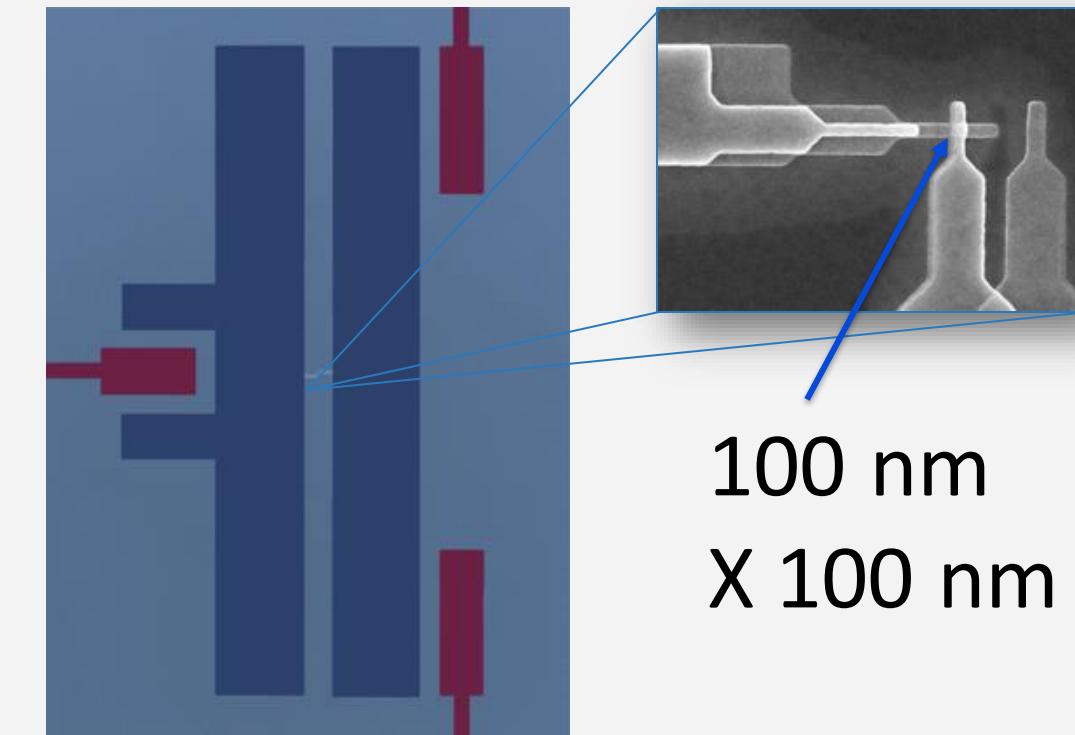


$$V = (F_0 / 2p) \dot{d}$$
$$I_J = I_0 \sin d$$

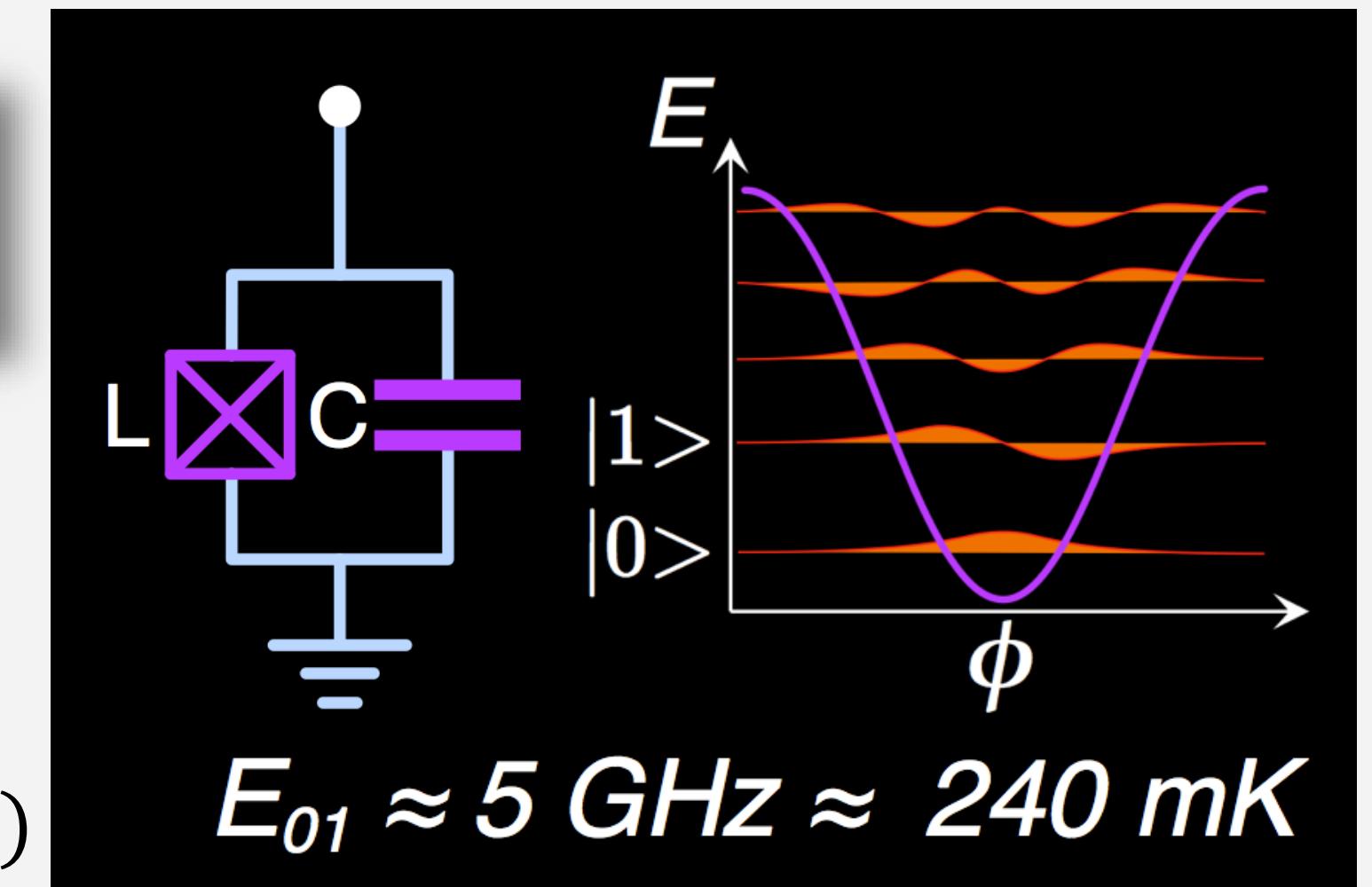
Josephson
Relations

$$\frac{dI}{dt} = \frac{1}{L} V(t)$$
$$L = \frac{F_0}{2pI_0 \cos(d)}$$

Non-linear inductor



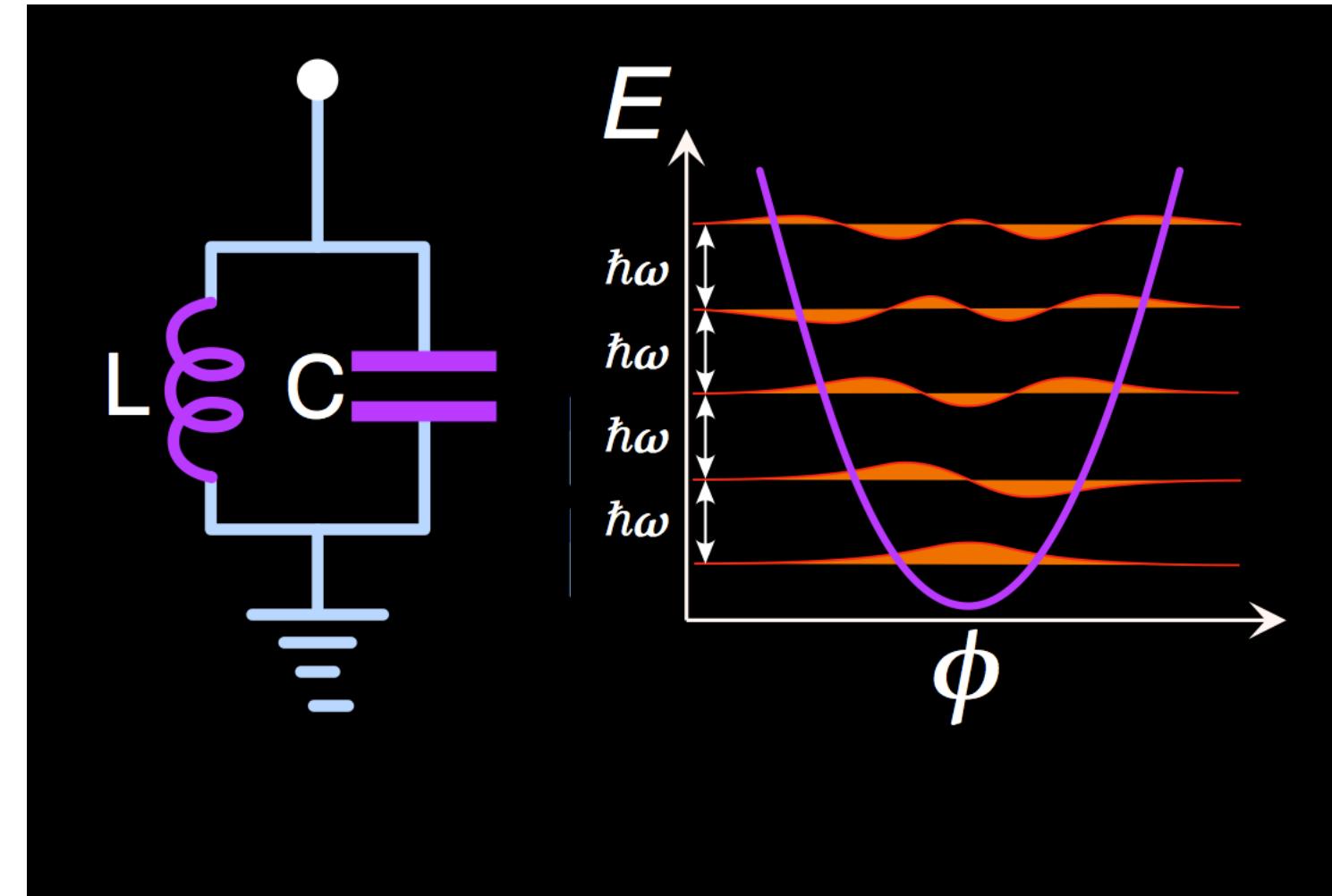
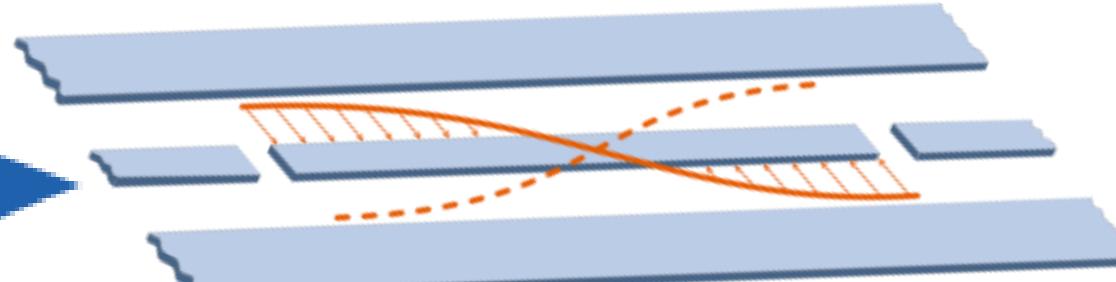
$$H = q^2 + \cos(\Phi)$$



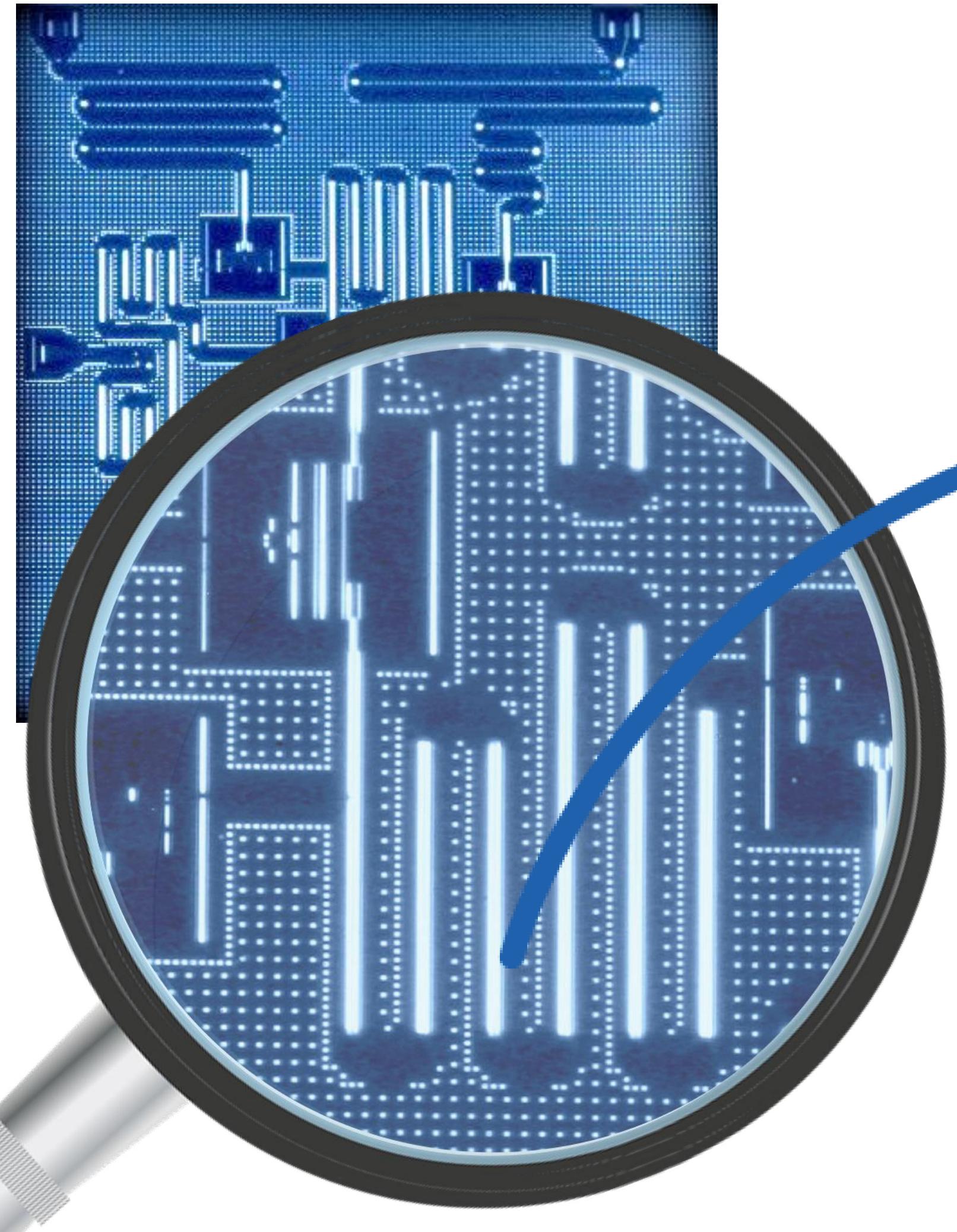
Readout of a Transmon



Readout Resonator

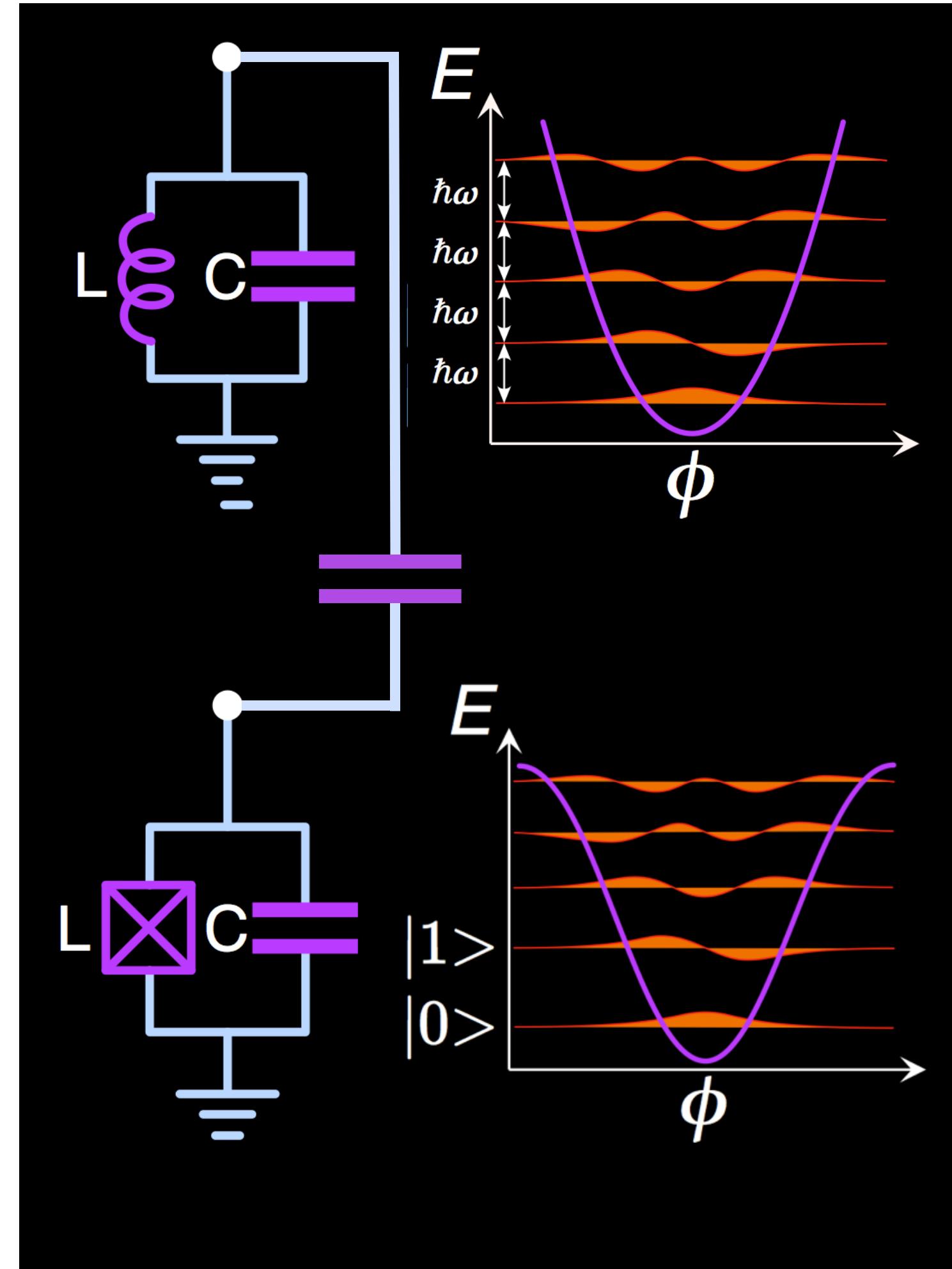


Readout of a Transmon

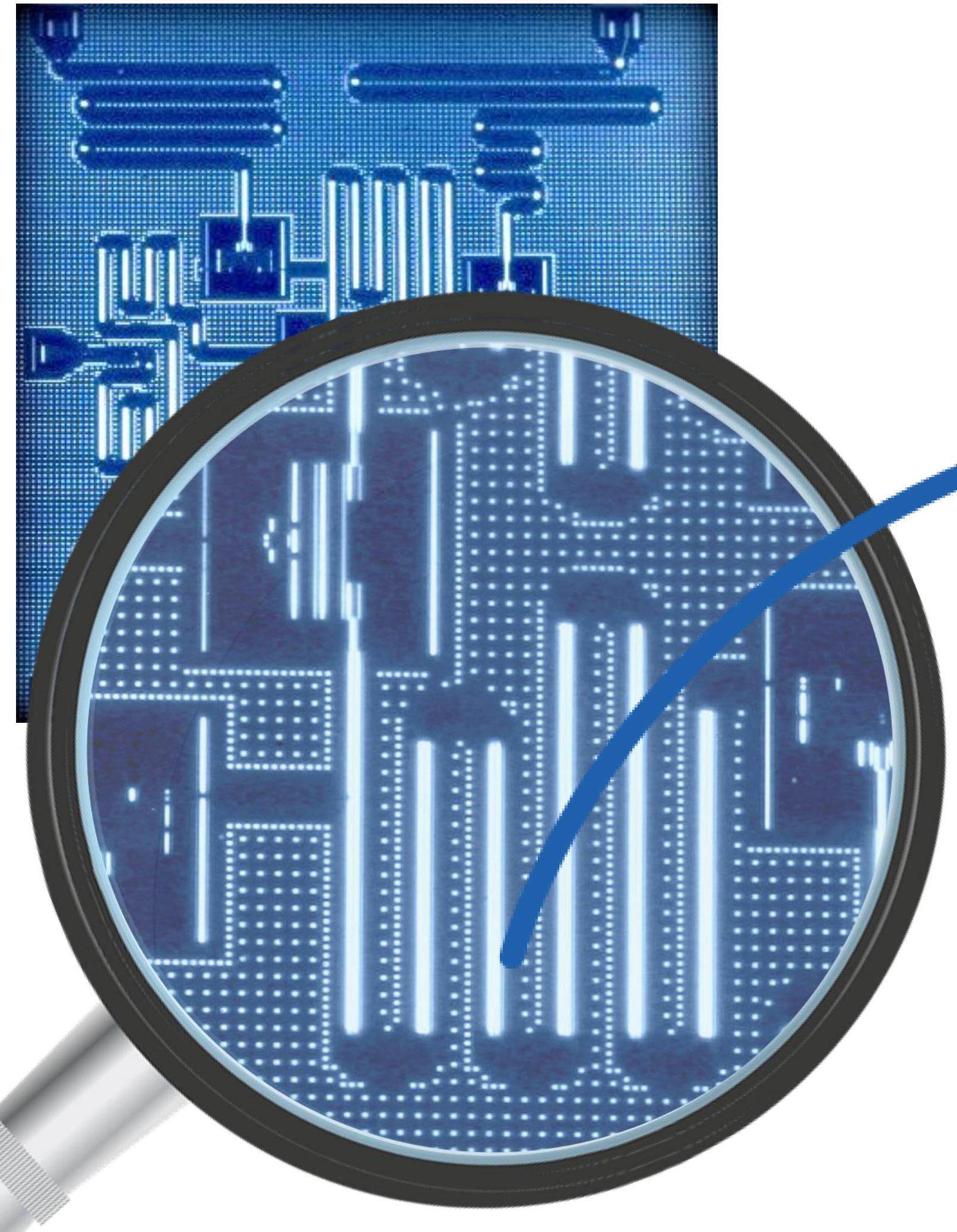


Readout Resonator

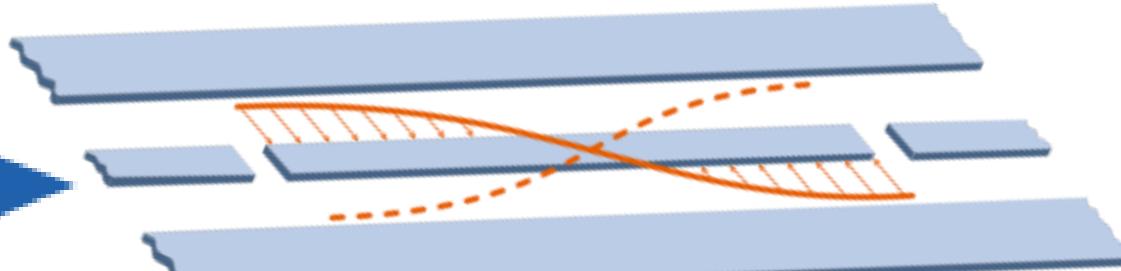
- Resonator frequency depends on transmon state



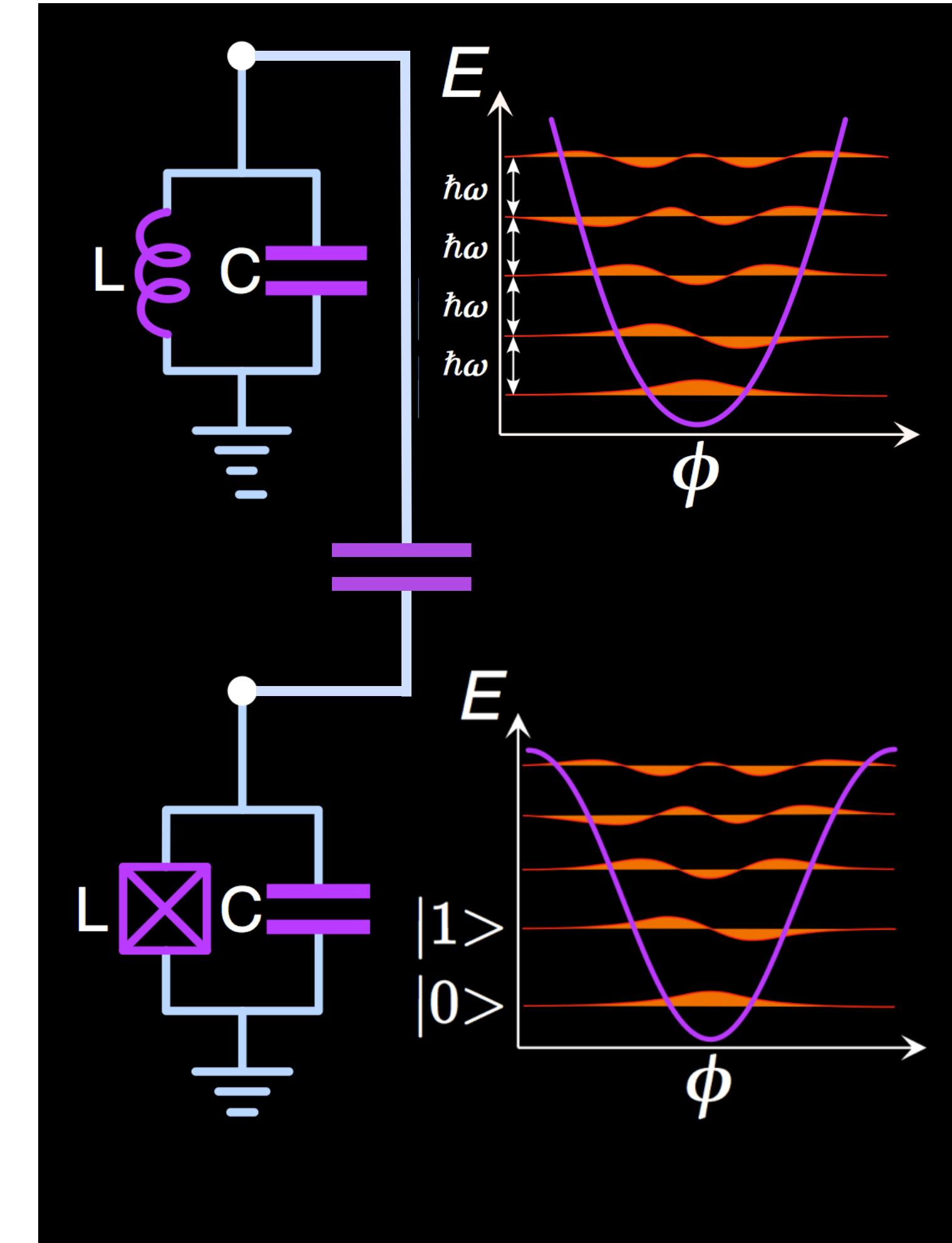
Readout of a Transmon



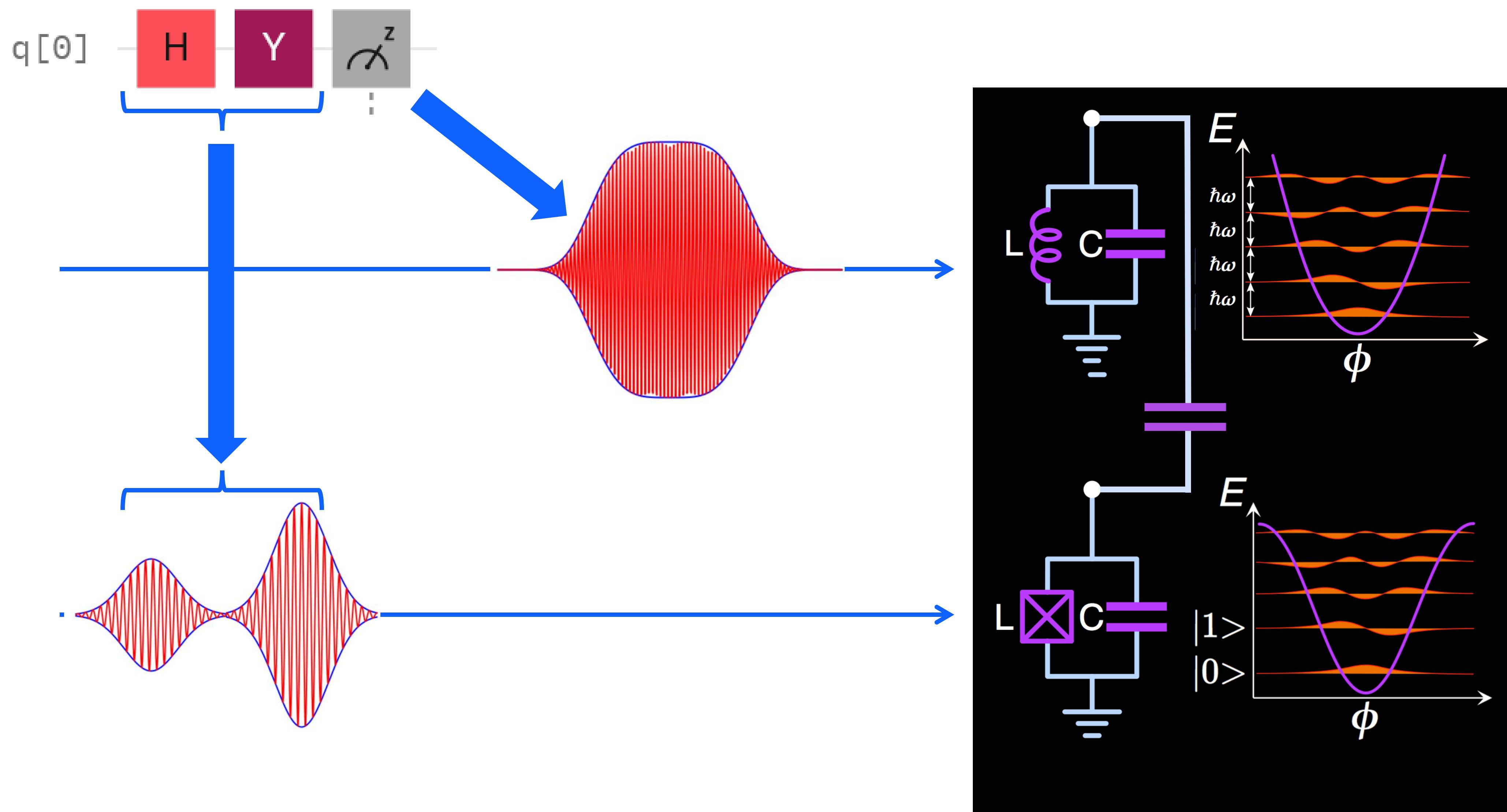
Readout Resonator



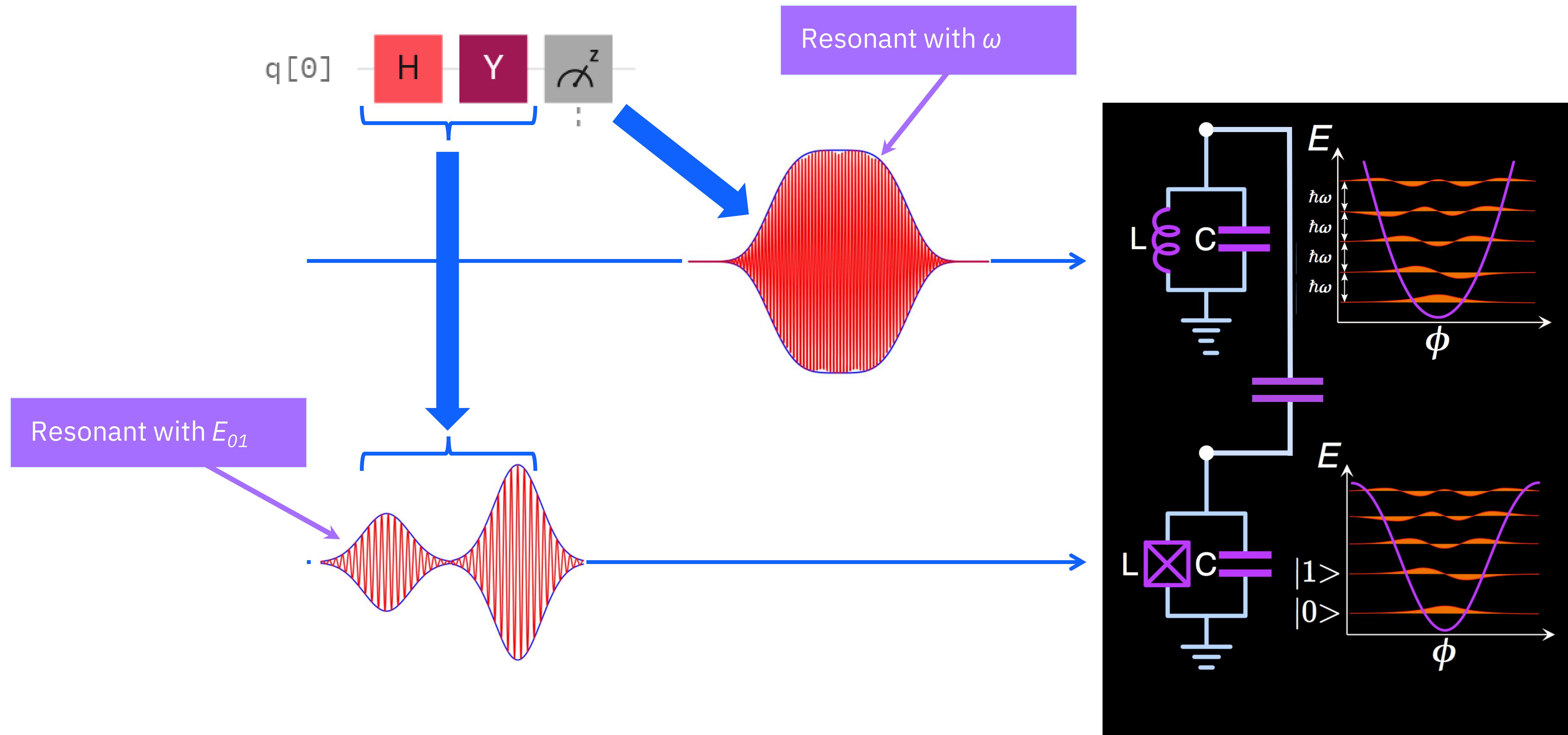
- Resonator frequency depends on transmon state
- Off-resonant: transmon cannot decay
- Use for driving 1Q gates



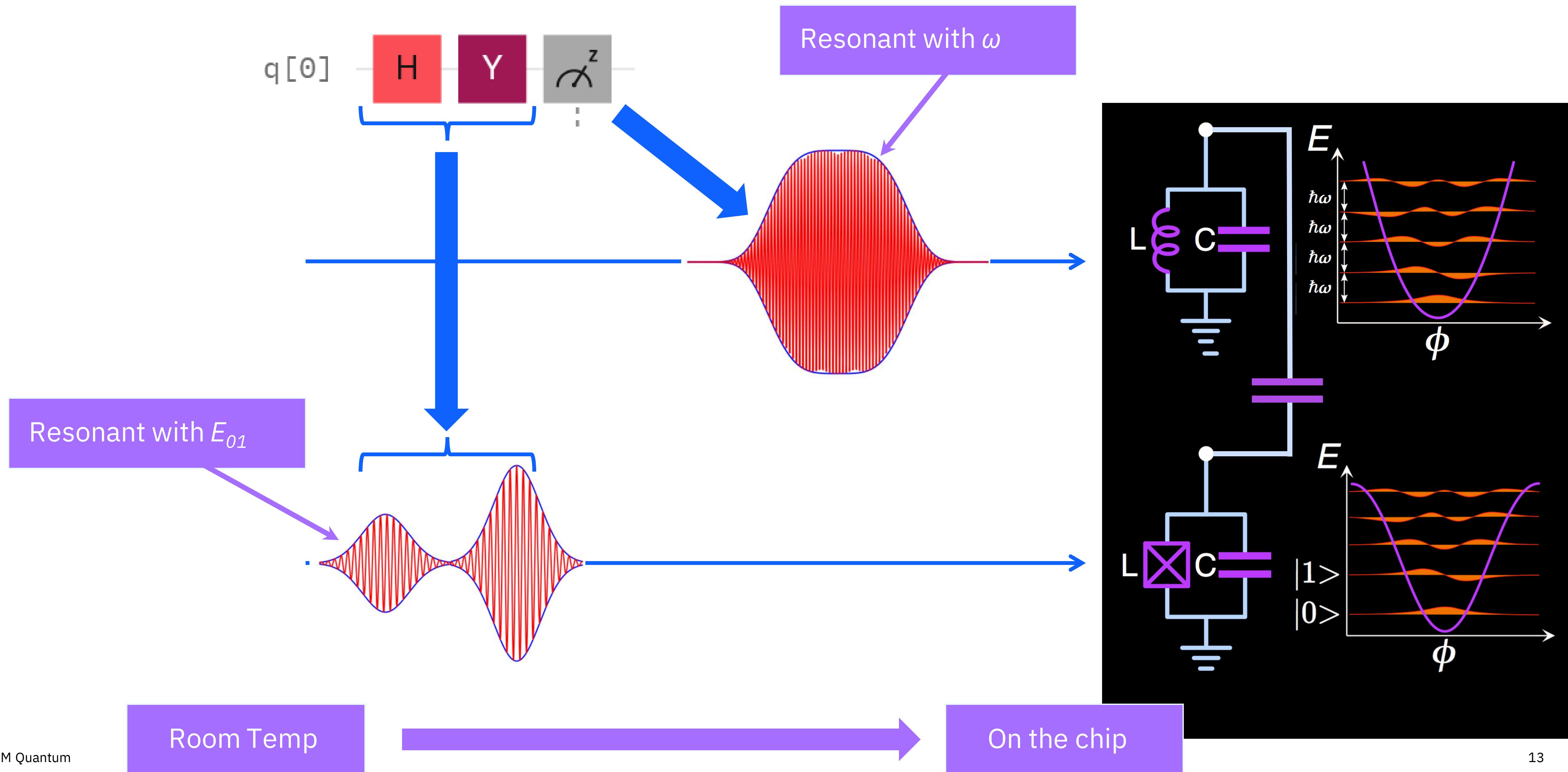
First Experiment



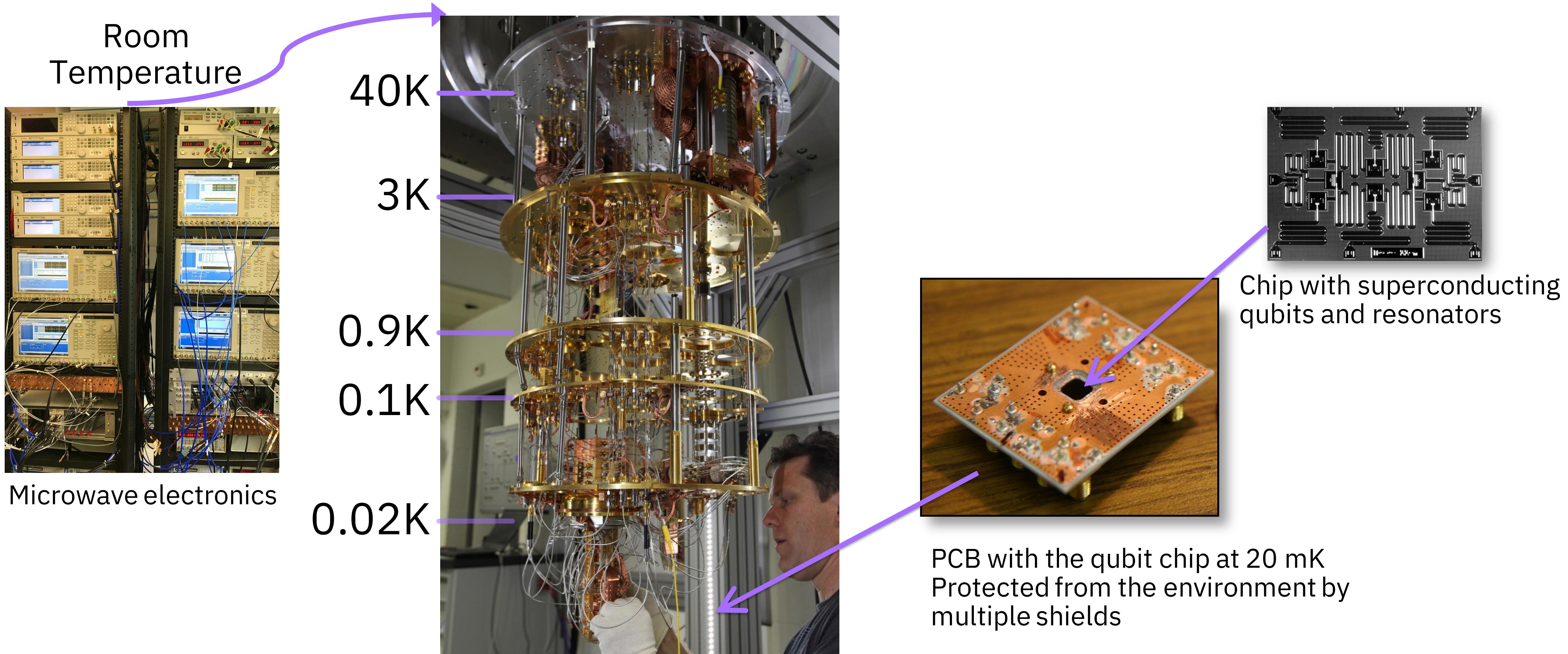
First Experiment



First Experiment



Our Systems 10 Years Ago

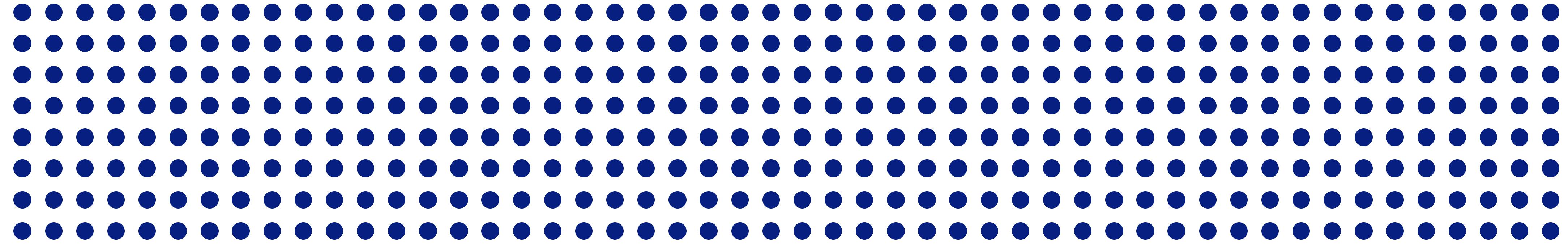
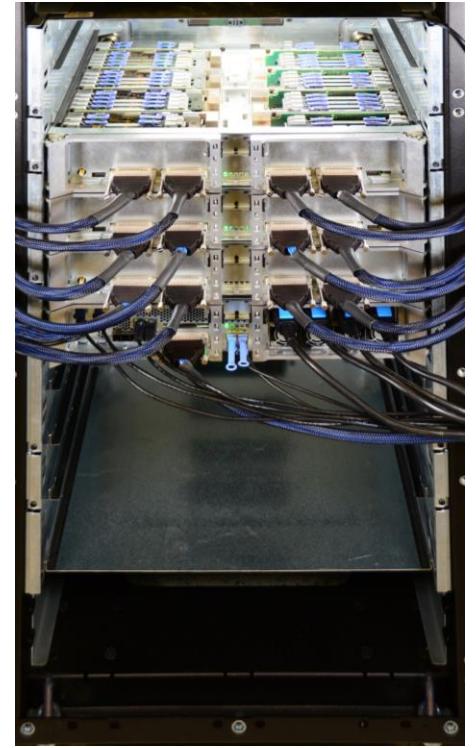


Refrigerator to cool qubits to 20 mK
with a mixture of ^3He and ^4He .

What has changed?

Control Electronics Evolution

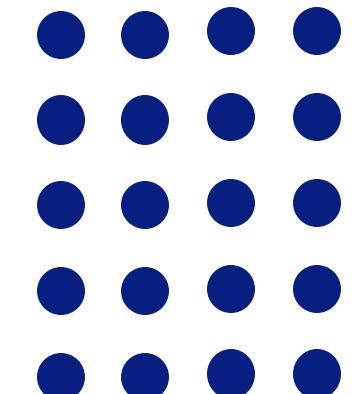
Gen 3
400 qubits



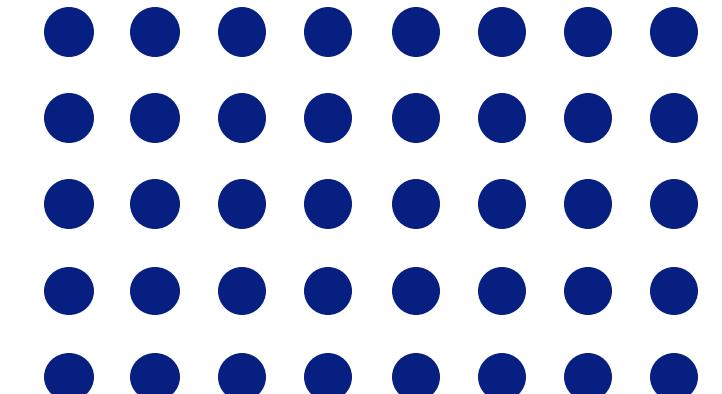
COTS
5 qubits



Gen 1
20 qubits

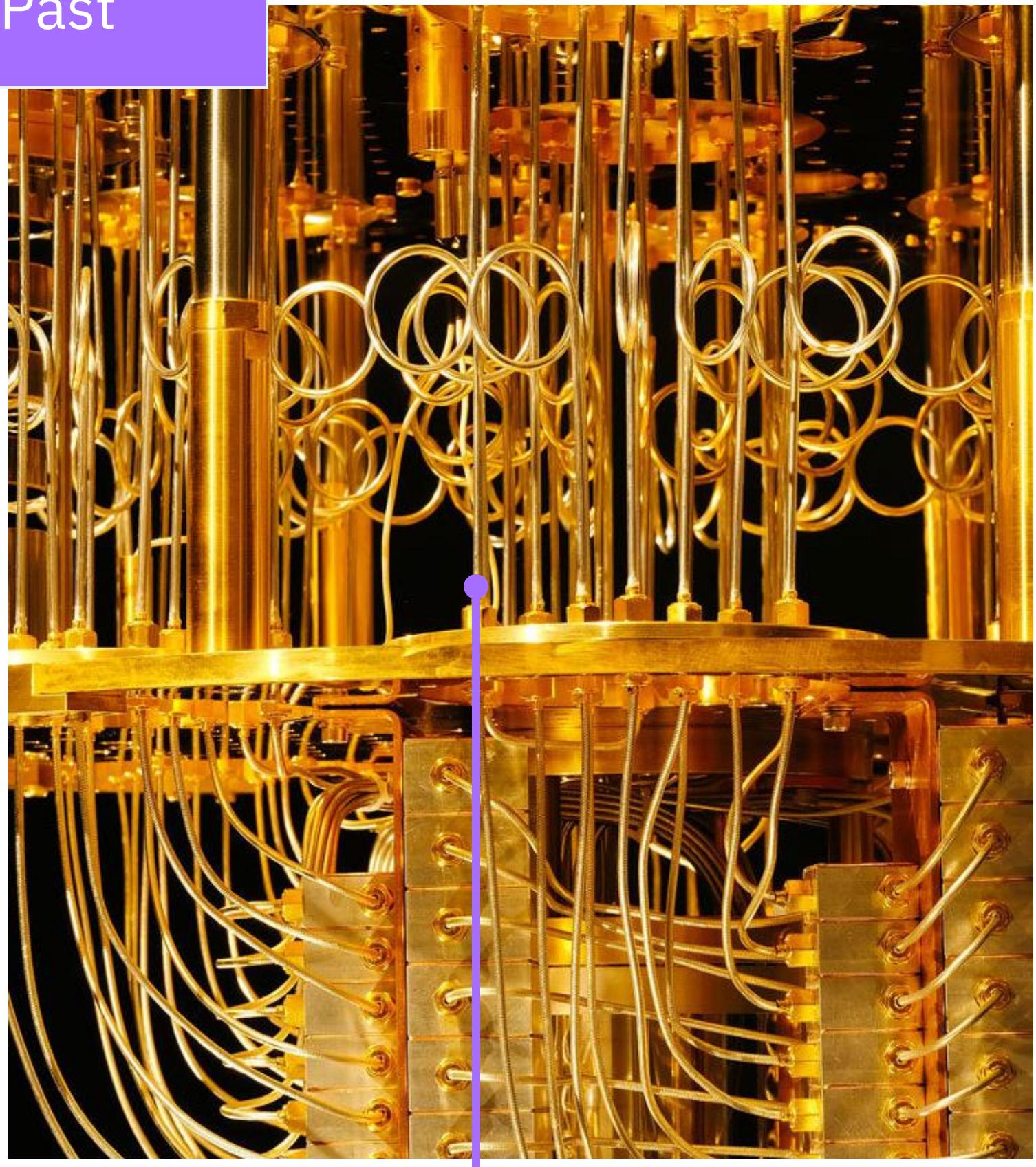


Gen 2
40 qubits



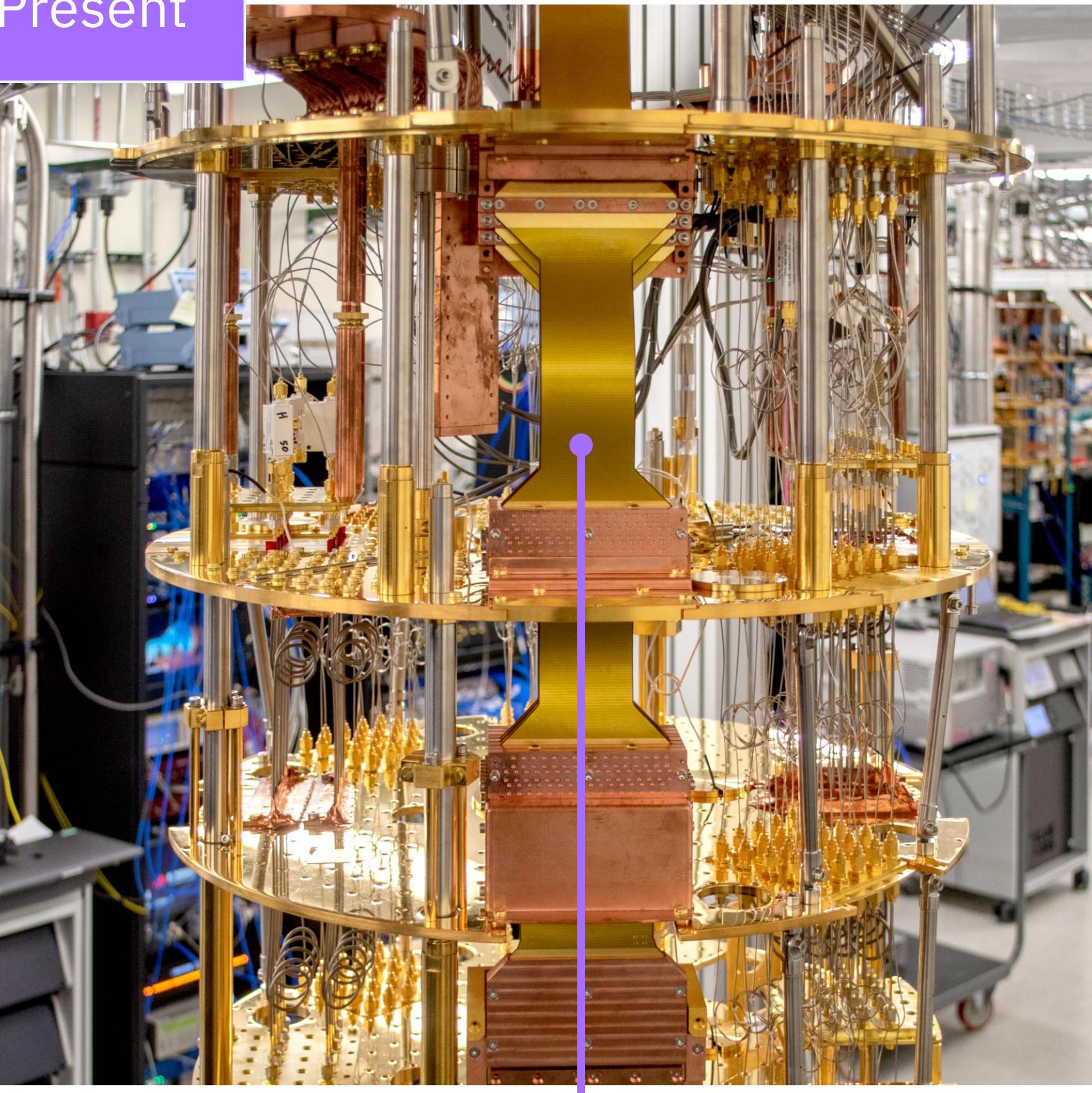
Scaling Input & Output Wiring

Past



High-density coaxial wiring

Present



Cryogenic flexible wiring

Today

- 70% increase in density and a
- 4-5x times reduction in price per line

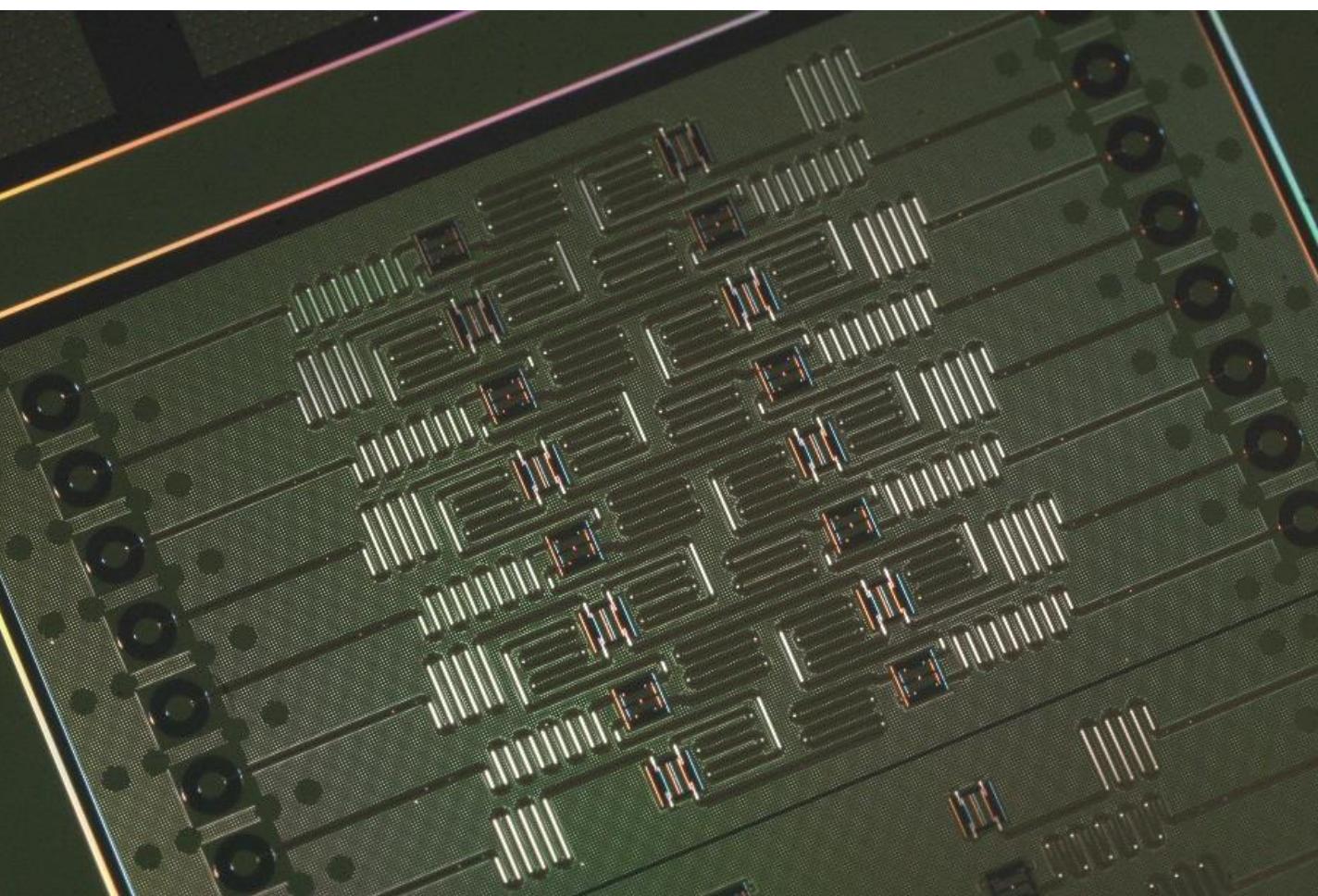
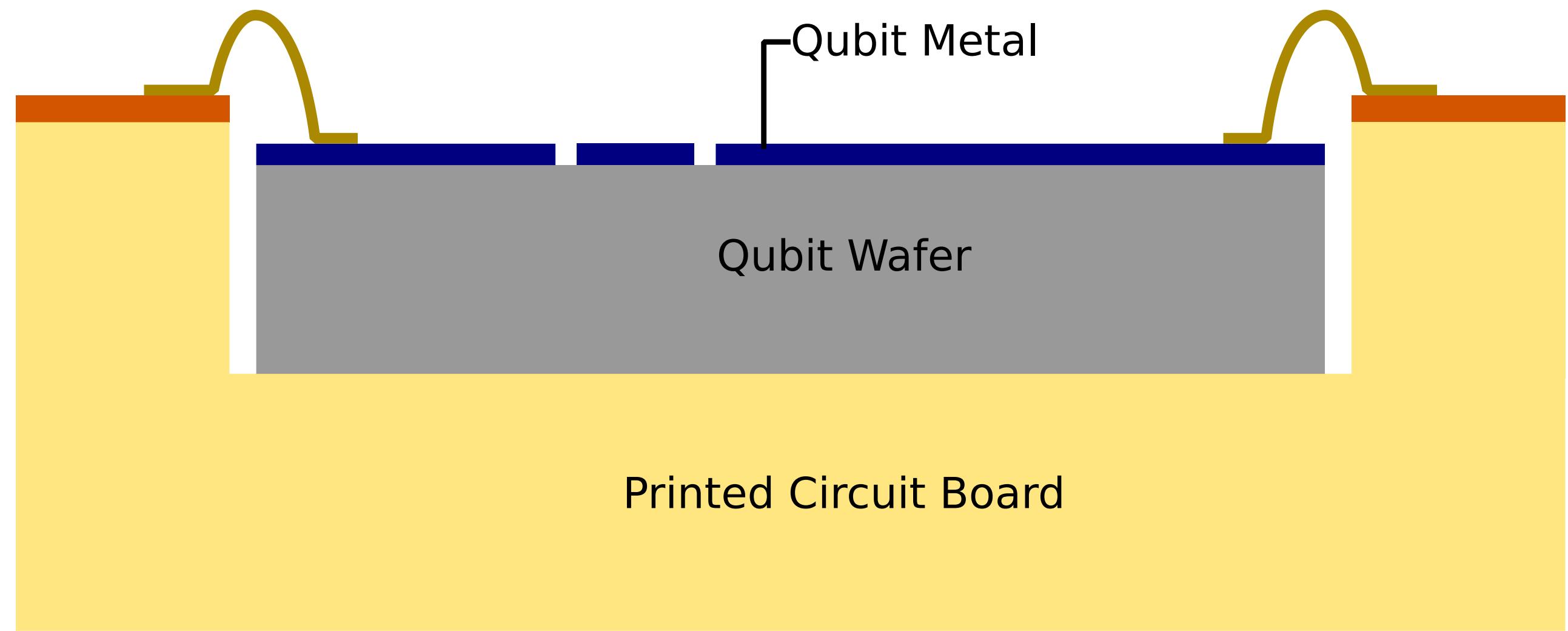
Aiming at further

- 3x density improvement next year

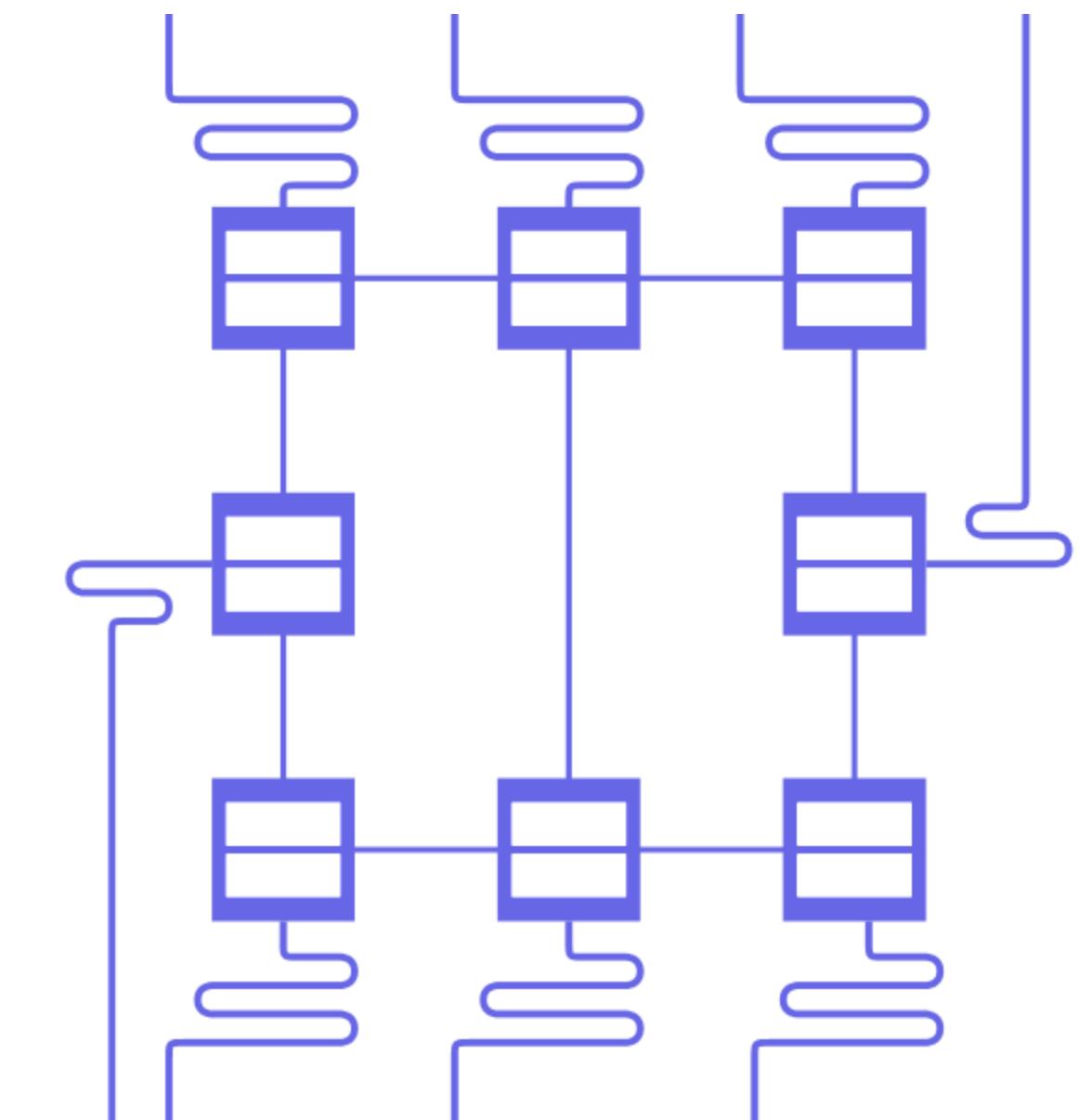
Evolution of Packaging Schemes: Generation 1

Single layer of metal

- Works fine for “ring” topologies.
- Breaks down if there are qubits inside the ring



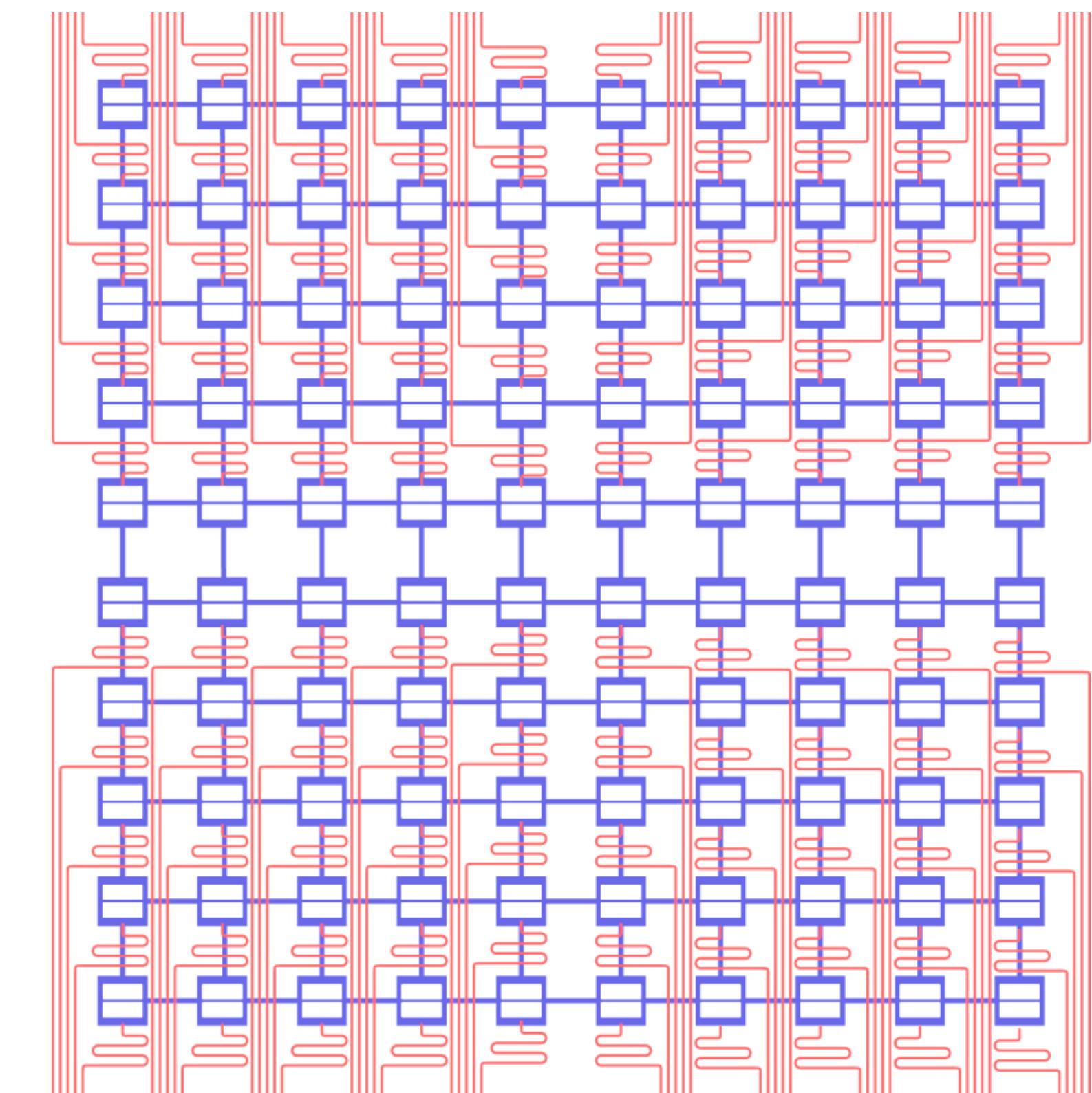
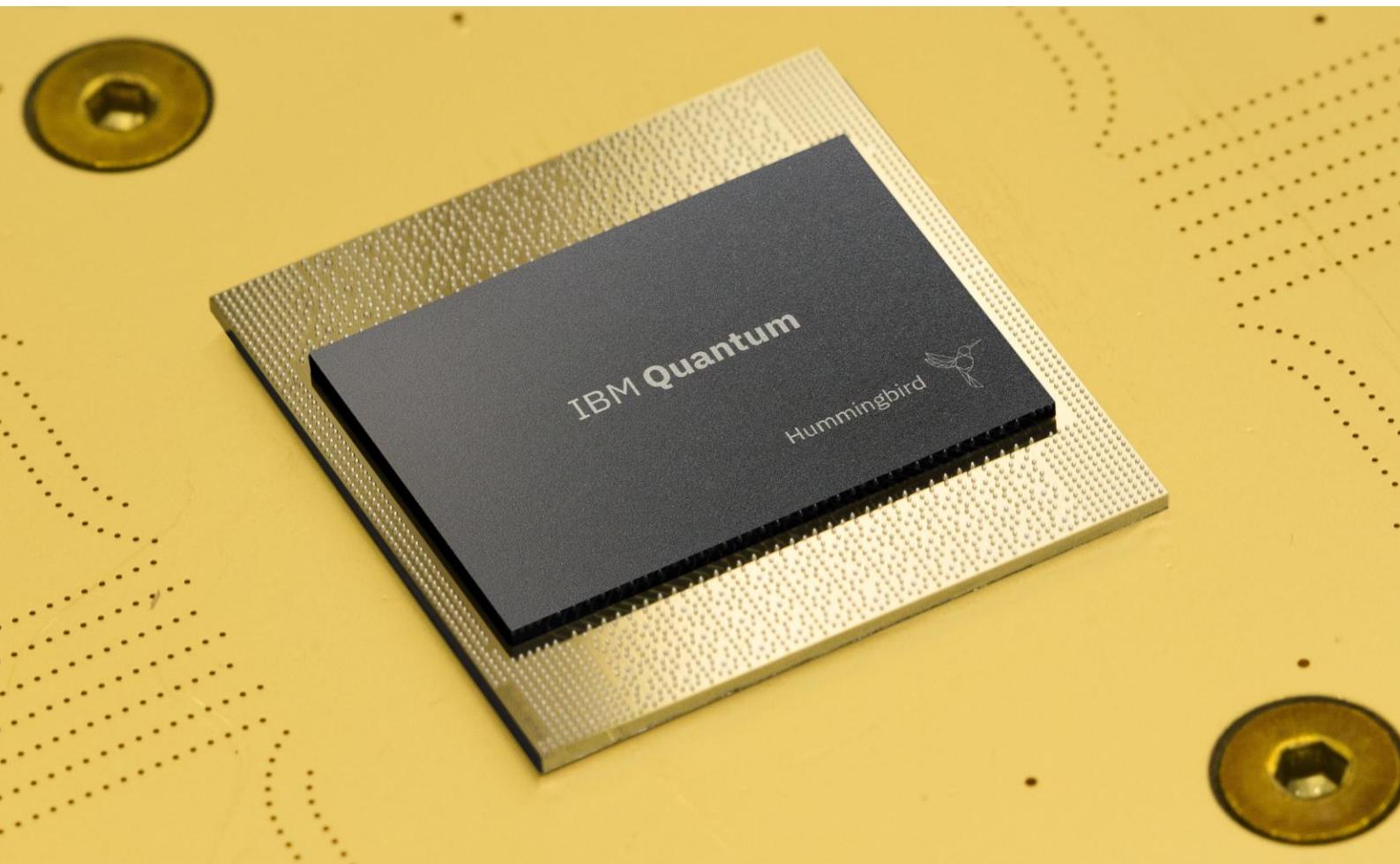
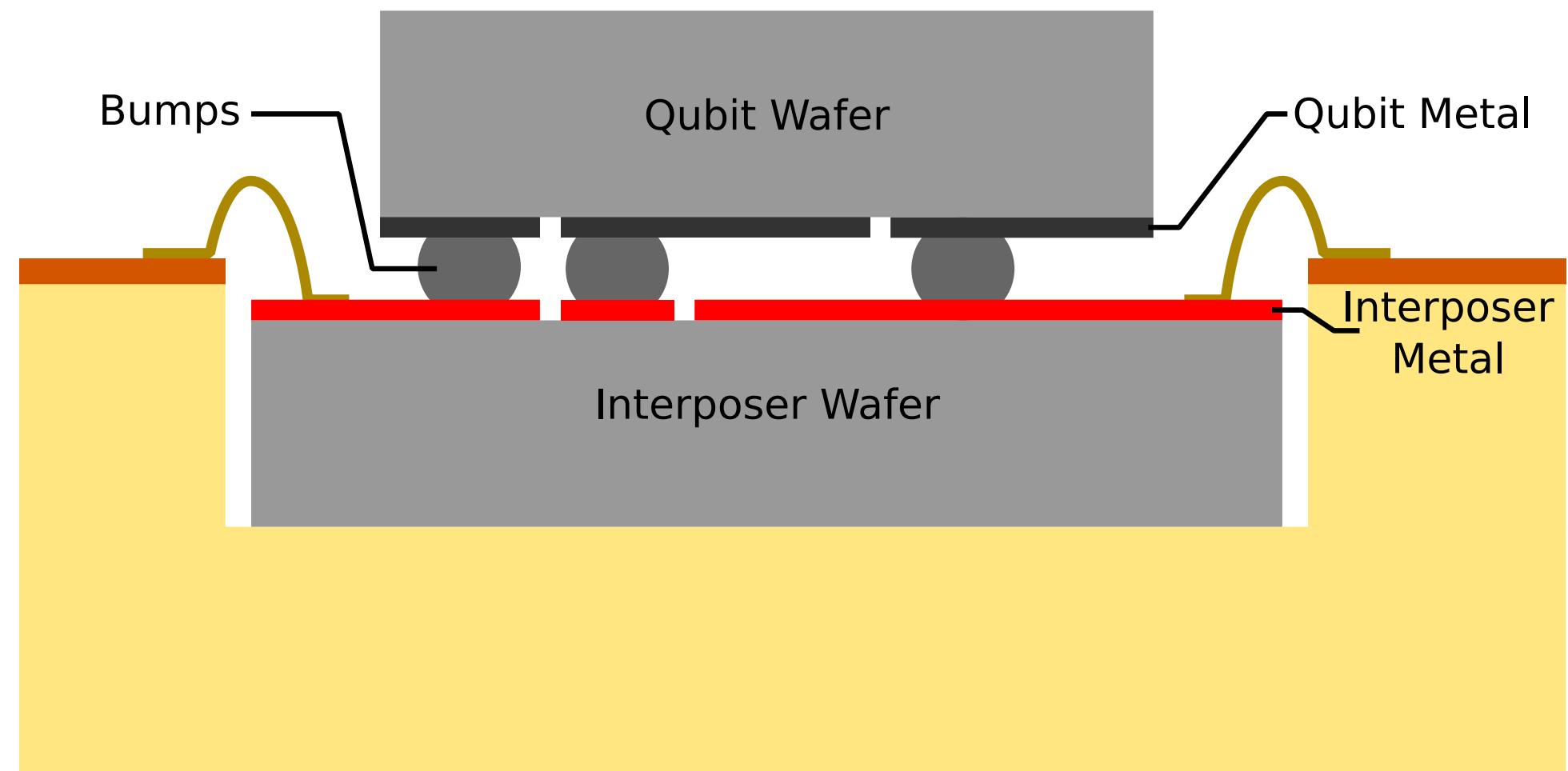
[1] Roushan, P. et al. Science **358**. (2017)



Evolution of Packaging Schemes: Generation 2

Two separate chips, each with one layer of patterned metal

- Joined via superconducting bump bonds
- Allows nearest-neighbor qubit coupling
- All control and readout lines must be routed to periphery of chip
- Metal layers are not isolated from each other

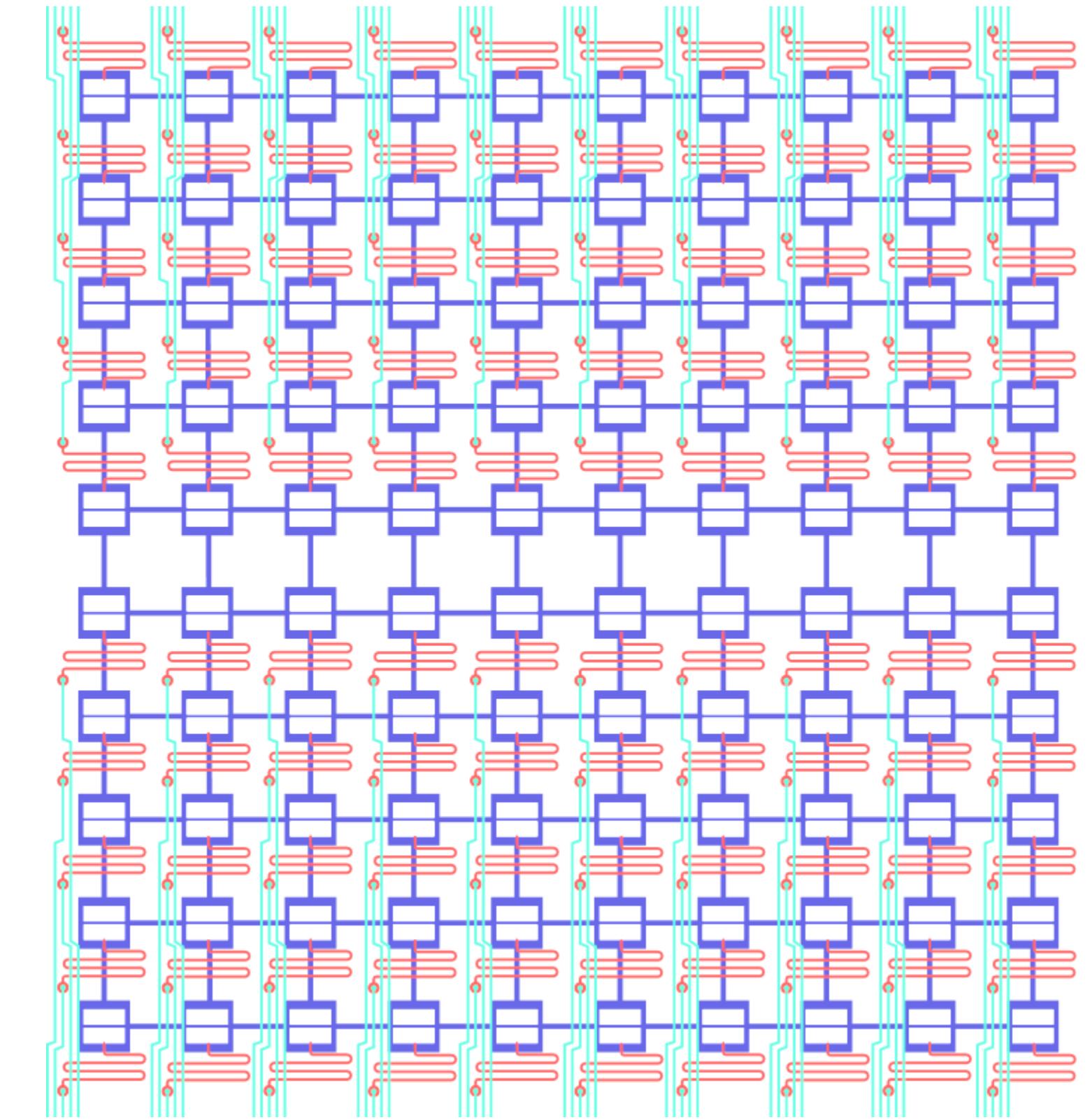
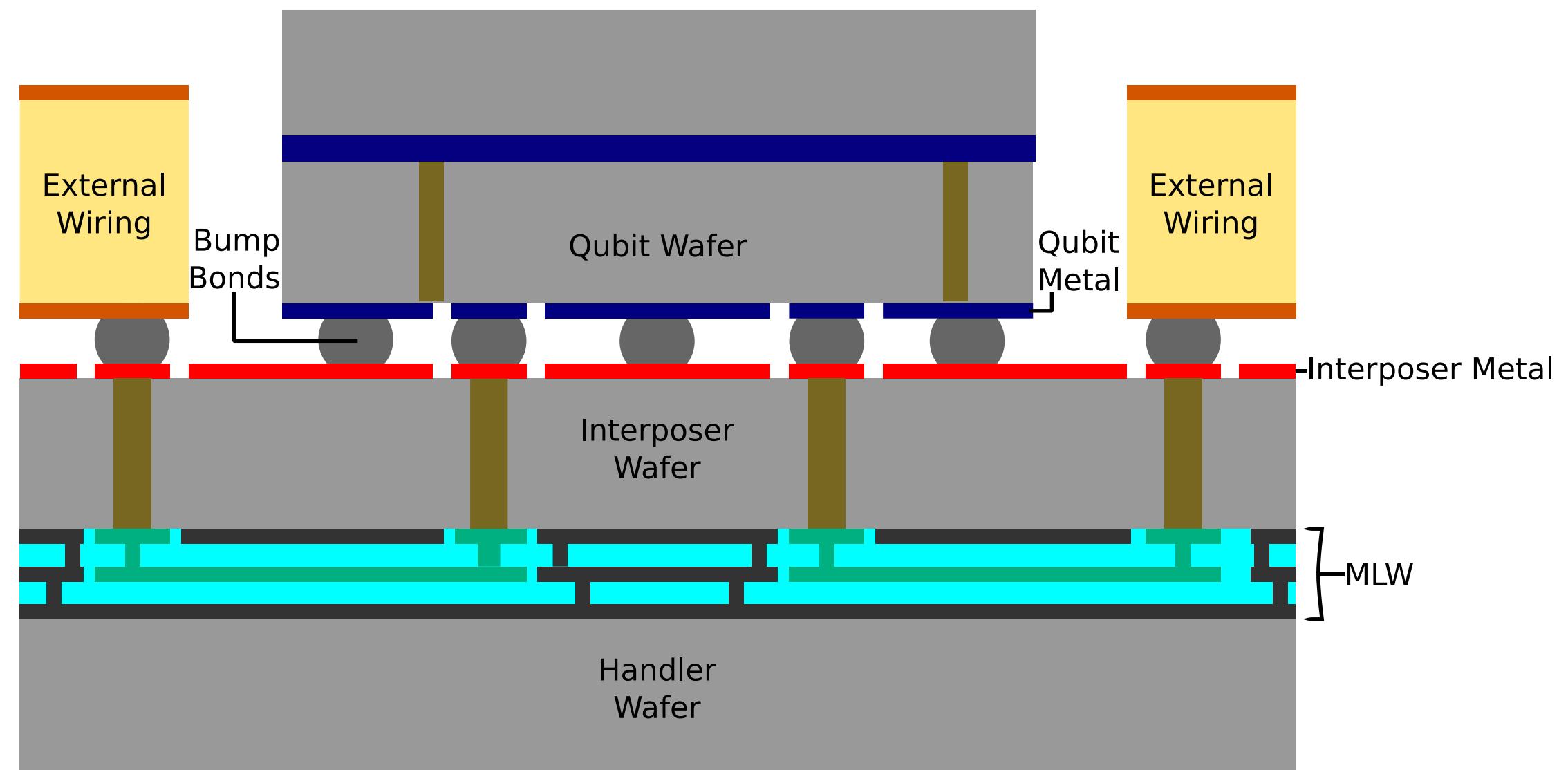


- [1] McRae, C.R.H. et al. arXiv:1705.02435v1 (2017)
- [2] Foxen, B. et al. *Quantum Sci. Technol.* **3** (2018)
- [3] Niedzielski, B. M. et al. *2019 IEEE International Electron Devices Meeting (IEDM)* (2019)
- [4] Jurcevic, P. et al. arXiv:2008.08571v2 (2020)

Evolution of Packaging Schemes: Generation 3

Two chips, as before

- Add “Multi-level Wiring” (MLW) level formed on backside of interposer
- Control and readout signals routed as striplines in the MLW
- Well isolated from Interposer and Qubit metal levels
- Connect to MLW via superconducting Through-Substrate-Vias (TSVs)



[1] Licata, T.J. et al. IBM Journal of R&D **39**. (1995)

[2] Edelstein, D. et al. International Electron Devices Meeting. IEDM Technical Digest (1997)

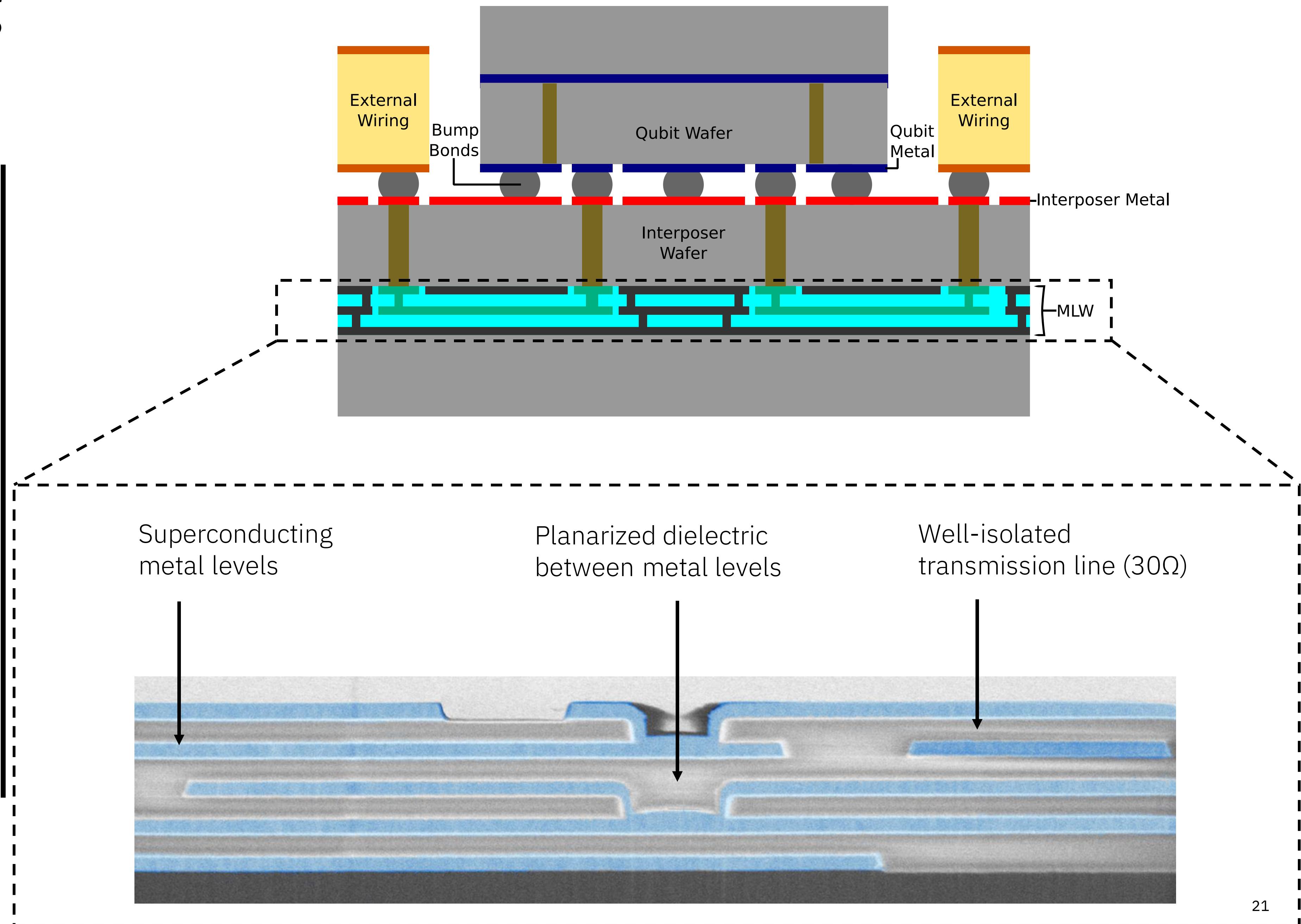
Multi Layer Wiring

5

Superconducting
metal levels

2.5X

The qubit count in
1.7x the space



Scale Solved with MLW and TSV

Qubit plane

Transmon qubits attached to chip via bump bonds.

Readout plane

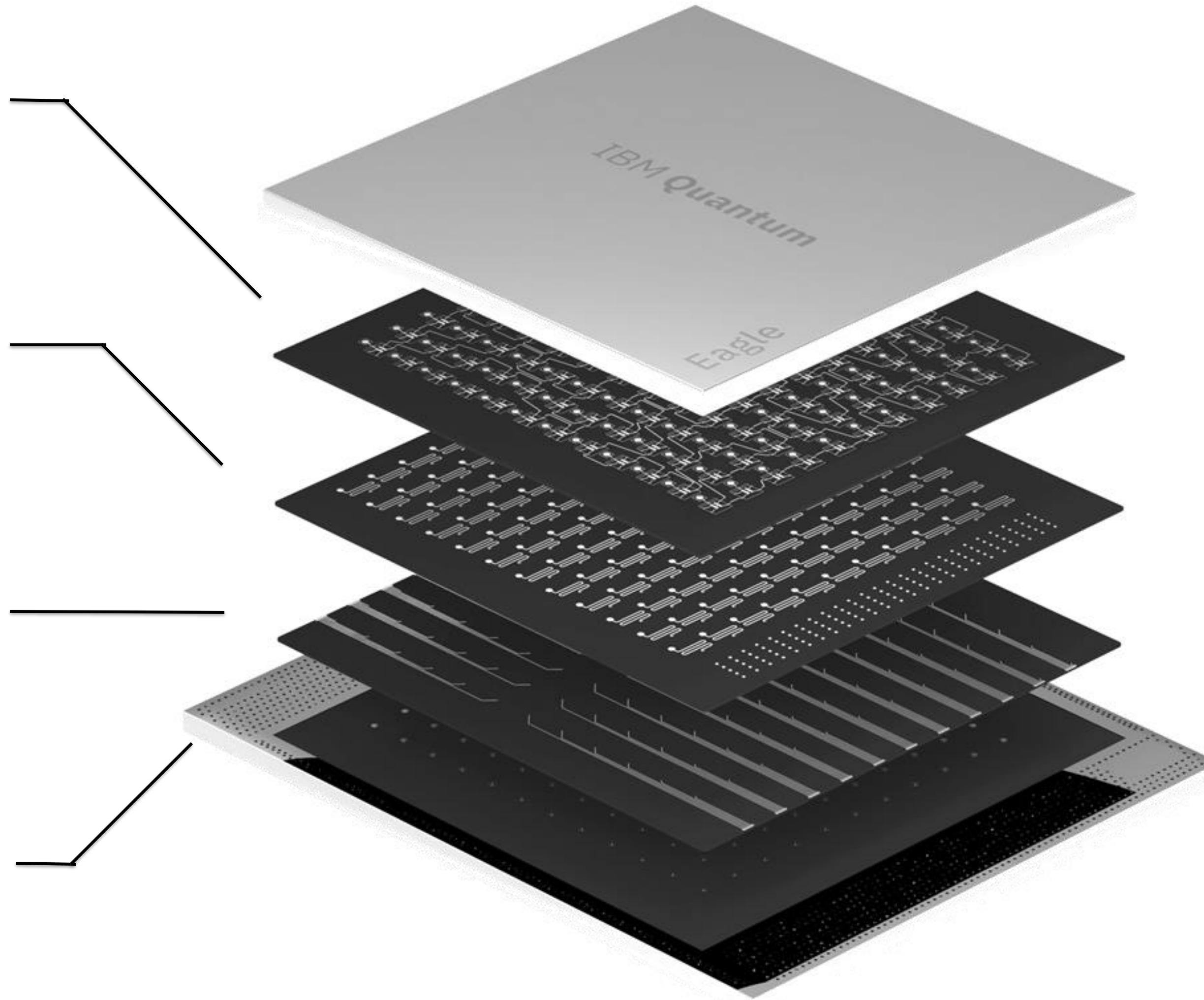
Readout resonators wired through connections.

Wiring plane

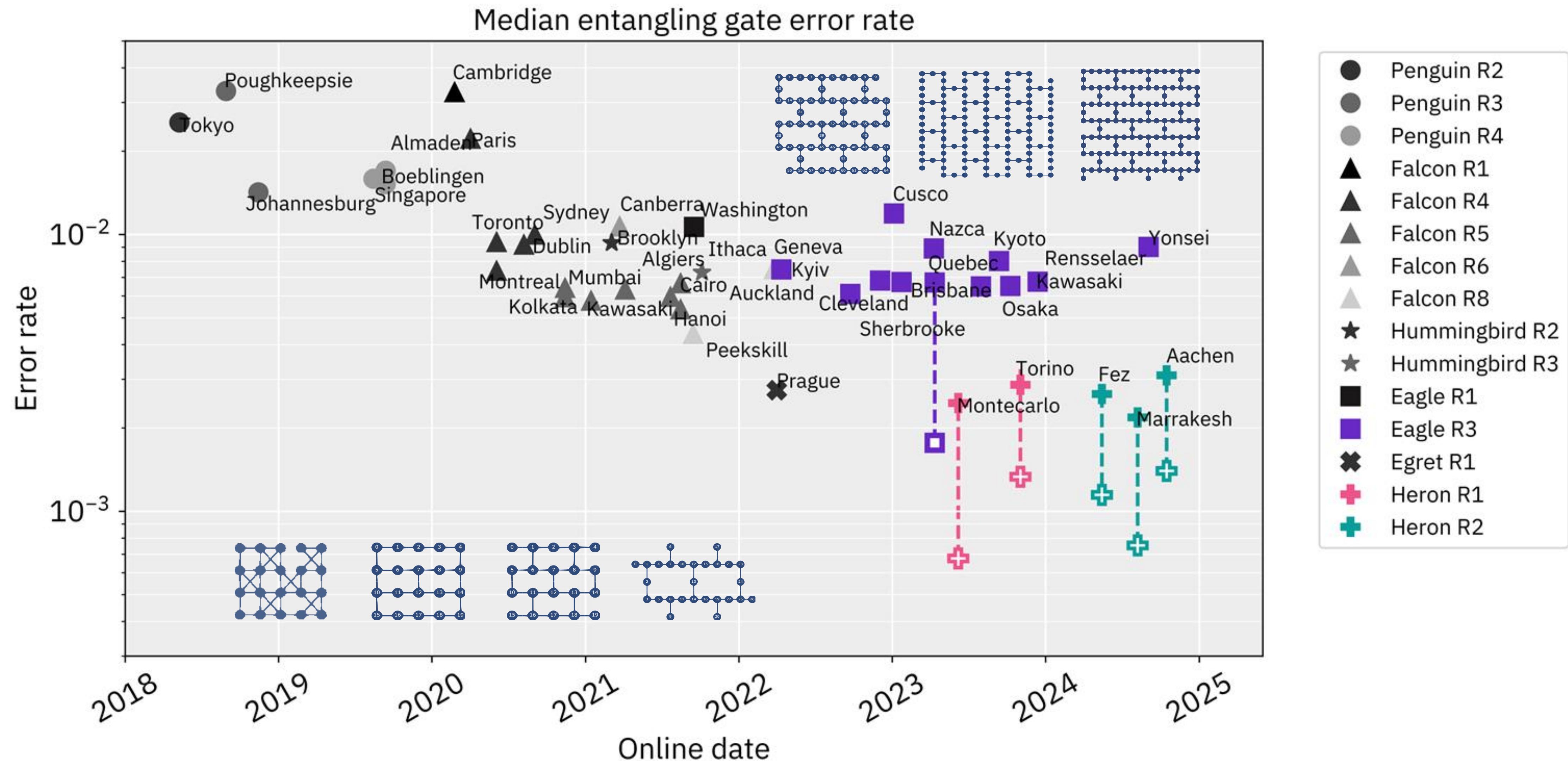
Through substrate vias (TSV) providing connections through planes.

Interposer chip

Leverages CMOS packaging techniques.



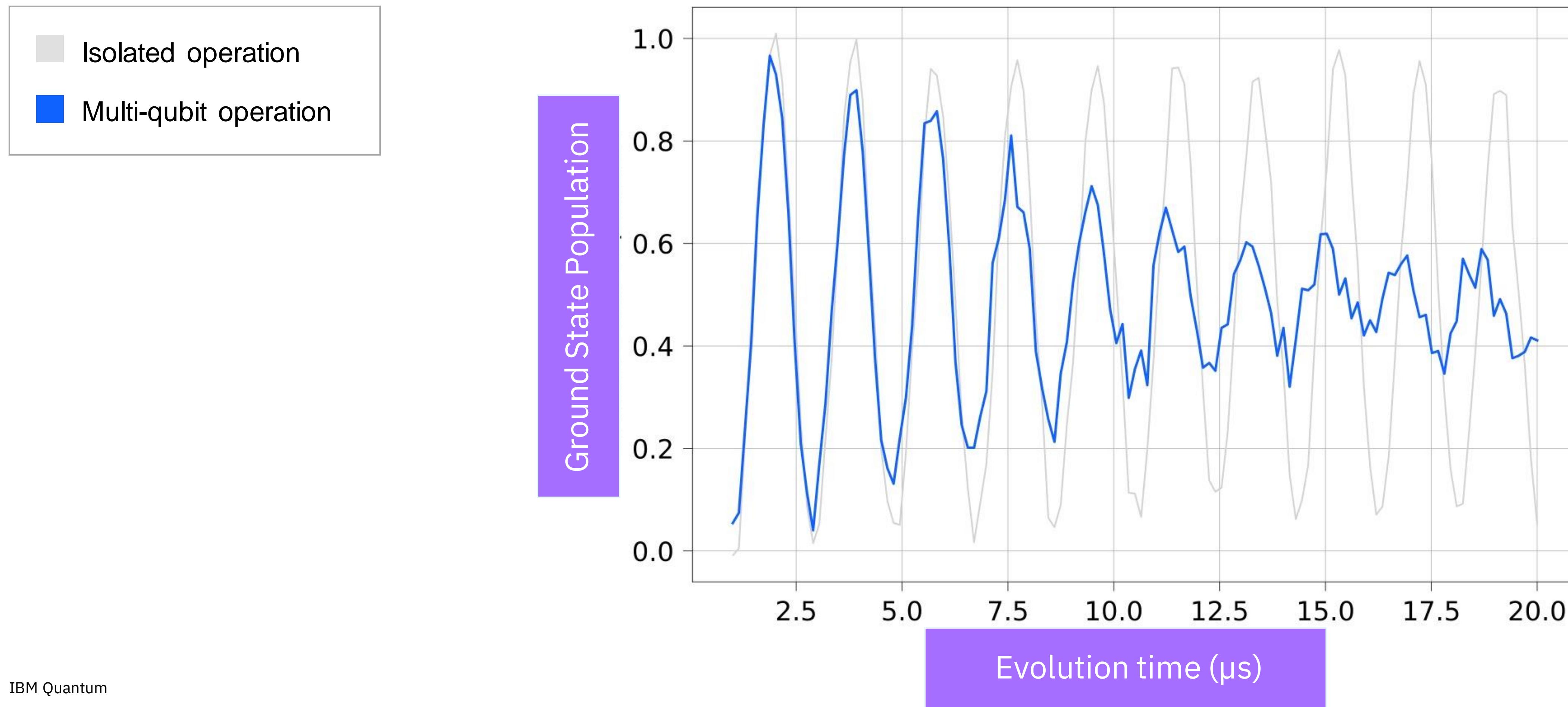
Road to Improved 2Q Gate Errors



Tunable Coupler Architecture

Multi-qubit T_2^* measurement

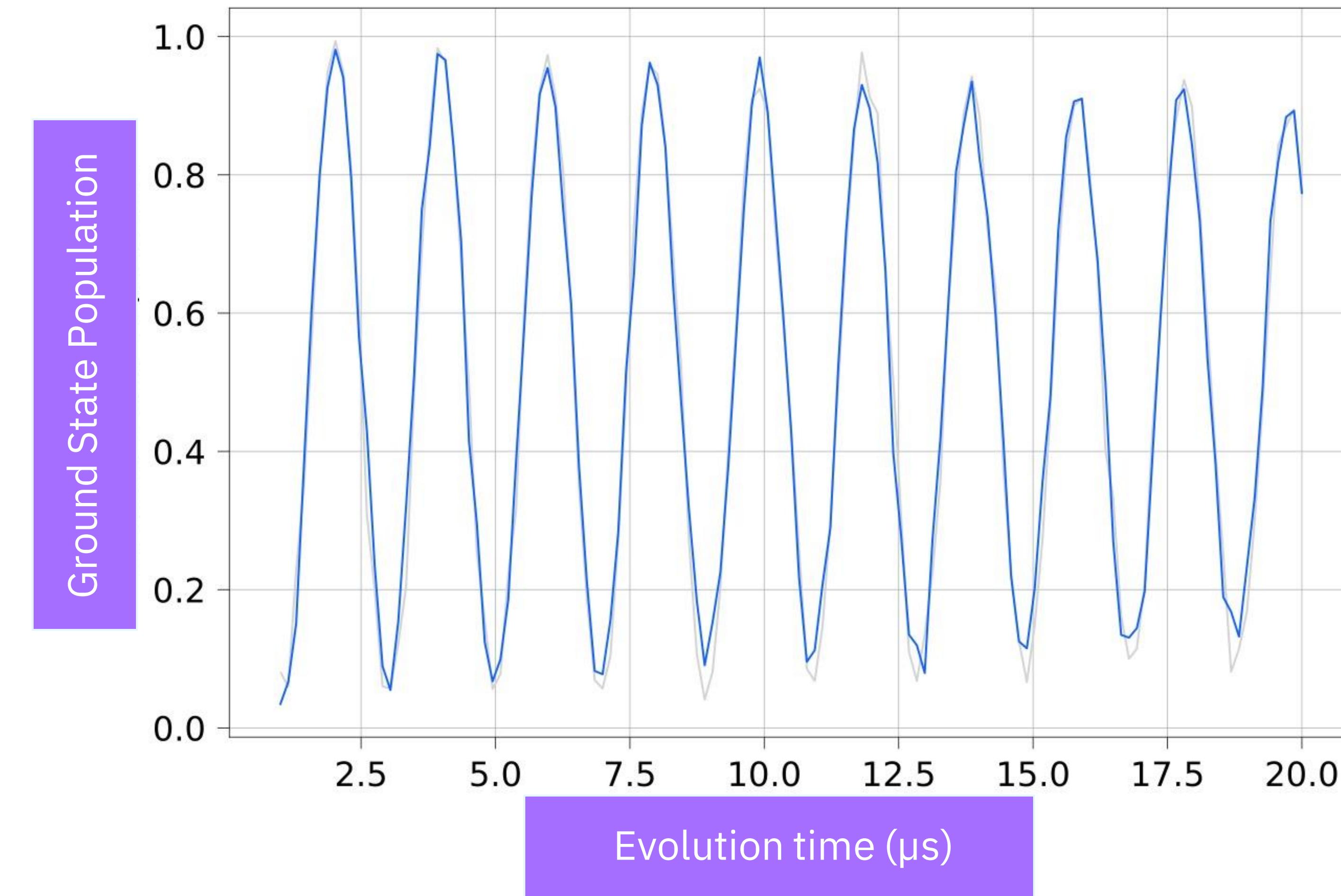
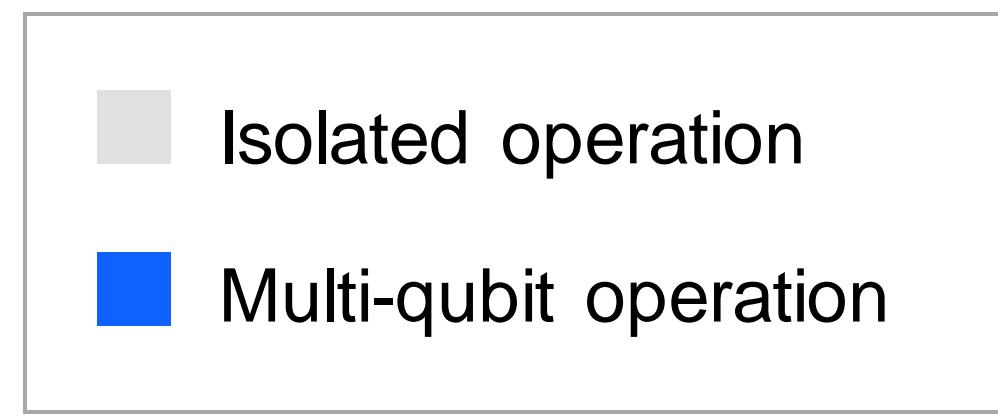
Eagle: ZZ ~ 60 kHz



Tunable Coupler Architecture

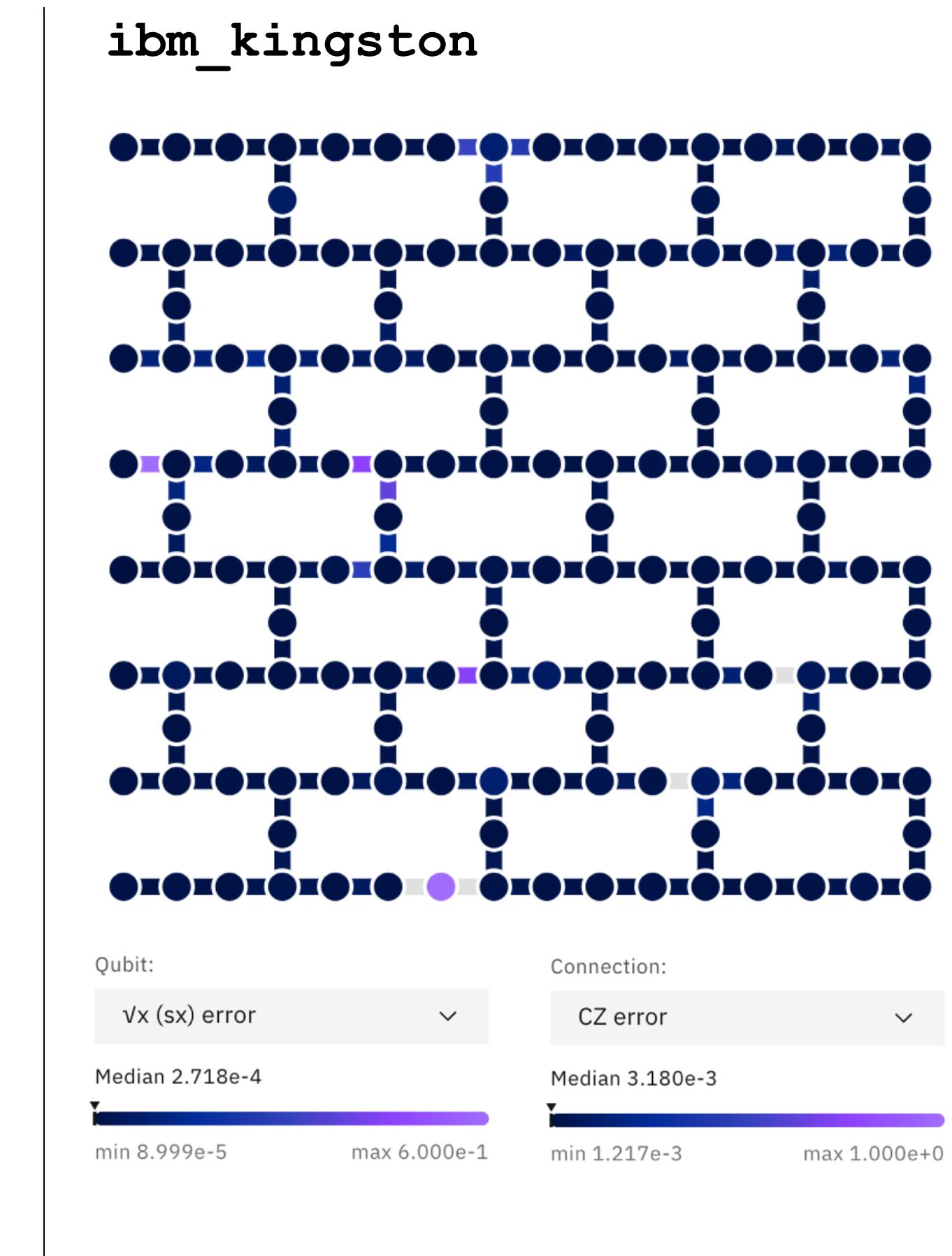
Multi-qubit T_2^* measurement

Heron: ZZ < 10 kHz



Heron Fact Sheet

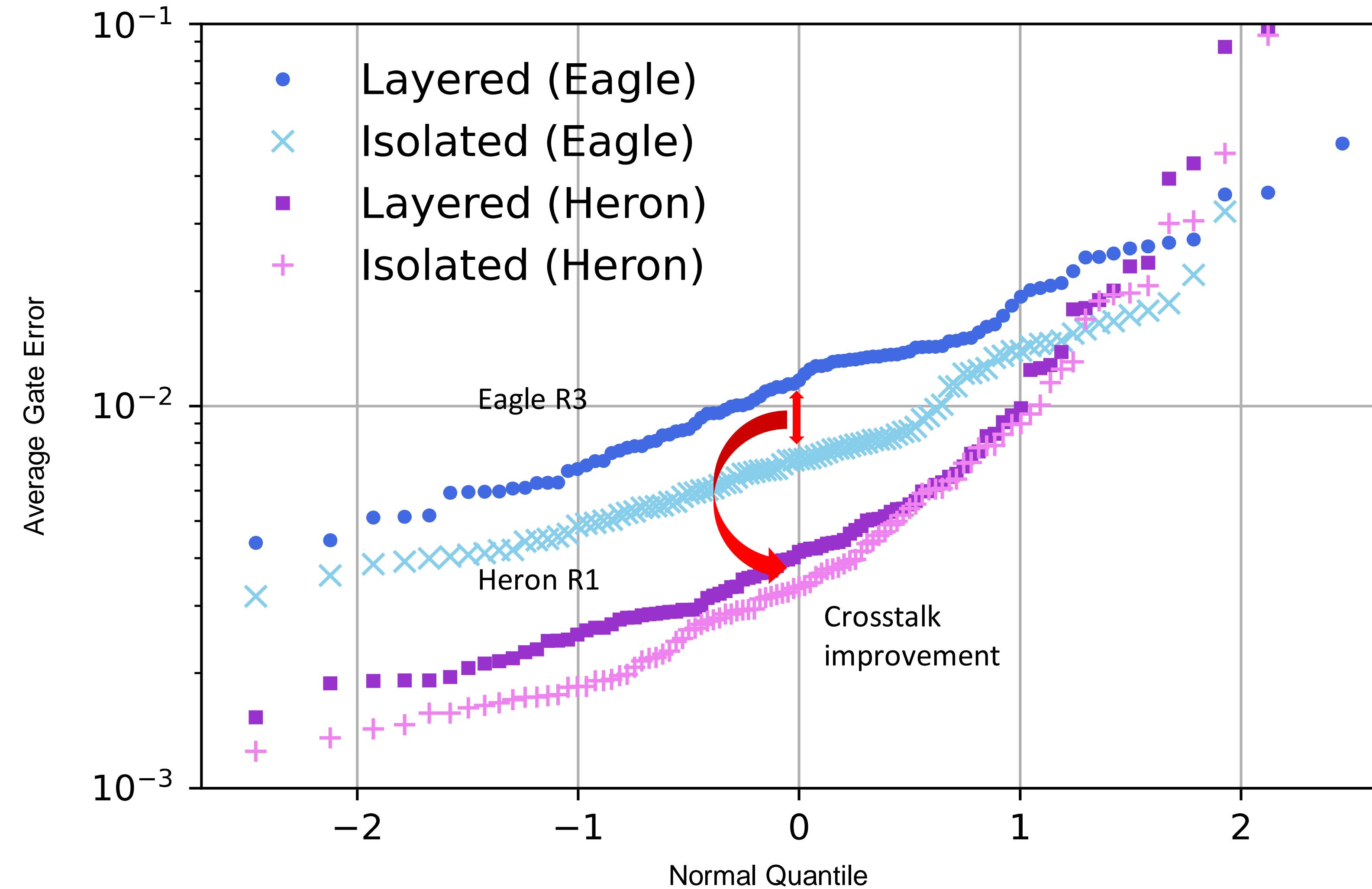
- 156 qubit processor
- Fixed frequency transmon qubits
- Tunable coupler architecture
- Heavy hex lattice
- Multi-layer wiring



	ibm_sherbrooke <i>Eagle</i>	ibm_kingston (Heron R2)
Gate Error (best system)	0.6-0.7%	0.3% - Best ~ 0.1%
Crosstalk	High (qubit-qubit collisions)	Significantly reduced
Gate time	500-600ns	90-100ns

Reduction in Median Gate Error & Improved Crosstalk

Comparison of best Eagle processor with first Heron processor



2016–2019 ✓

2020 ✓

2021 ✓

2022 ✓

2023 ✓

2024 ✓

2025

2026

2027

2028

2029

2033+

Development Roadmap ↓

Ran quantum circuits on IBM Quantum Platform	Released multi-dimensional roadmap publicly with initial focus on scaling	Enhanced quantum execution speed by 100x with Qiskit Runtime	Brought dynamic circuits to unlock more computations	Enhanced quantum execution speed by 5x with Quantum Serverless and execution modes	Demonstrated accurate execution of a quantum circuit at a scale beyond exact classical simulation (5K gates on 156 qubits)	Deliver quantum + HPC tools that will leverage Nighthawk, a new higher-connectivity quantum processor able to execute more complex circuits	Enable the first examples of quantum advantage using a quantum computer with HPC	Improve quantum circuit quality to allow 10K gates	Improve quantum circuit quality to allow 15K gates	Deliver a fault-tolerant quantum computer with the ability to run 100M gates on 200 logical qubits	Beyond 2033, quantum computers will run circuits comprising a billion gates on up to 2000 logical qubits, unlocking the full power of quantum computing
Code assistant ✓											
Functions ✓											
Use case benchmarking toolkit											
Computation libraries											
Advanced classical transpilation tools ✓											
Advanced classical mitigation tools ⚡											
Utility mapping tools											
Circuit libraries											
Resource Management											
Qiskit Serverless ✓											
Plugins for HPC ✓											
C API ⚡											
Profiling tools											
Workflow accelerators											
Execution modes ✓											

Accurately and efficiently executing on quantum computers

IBM Quantum Experience	Qiskit Runtime	OpenQASM 3 ✓	Dynamic Circuits ✓	Error mitigation 28	200K CLOPS ✓	Utility-scale dynamic circuits ⚡	Fault-tolerant ISA
Early	Falcon	OpenQASM 3 ✓	Dynamic Circuits ✓	Error mitigation 28	200K CLOPS ✓	Utility-scale dynamic circuits ⚡	Fault-tolerant ISA
Canary 5 qubits	Albatross 16 qubits	Penguin 20 qubits	Prototype 53 qubits	Benchmarking 27 qubits	Eagle 127 qubits	Heron (5K) 5K gates 133 qubits	Nighthawk (5K) 5K gates 120 qubits

Innovation Roadmap ↓

Software innovation	IBM Quantum Experience ✓	Qiskit ✓	Application modules ✓	Qiskit Runtime ✓	Quantum Serverless ✓	AI-enhanced quantum ✓	HPC-Quantum integration ✓	Advantage candidates ⚡	Error correction decoder	Workflow accelerator	Fault-tolerant ISA
Hardware innovation	Early Canary 5 qubits	Falcon Albatross 16 qubits	Hummingbird Demonstrate scaling with I/O routing with bump bonds	Eagle Demonstrate scaling with multiplexing readout	Osprey Demonstrate scaling with high density signal delivery	Condor Single-system scaling and fridge capacity	Flamingo Demonstrate scaling with I-couplers	Loon ⚡	Kookaburra Demonstrate c-couplers and next-generation packaging for FTQC	Cockatoo Demonstrate entanglement of modules consisting of a logical processing unit and quantum memory	Starling Demonstrate multiple modules and magic state distillation

✓ Completed
⚡ On target

2024

2025

2026

2027

2028

2029

2033+

Development Roadmap

Heron (5K) Error mitigation 5K gates 133 qubits	Nighthawk (5K) Error mitigation 5K gates 120 qubits	Nighthawk (7.5K) Error mitigation 7.5K gates 120 qubits Up to $120 \times 3 = 360$ qubits	Nighthawk (10K) Error mitigation 10K gates 120 qubits Up to $120 \times 9 = 1080$ qubits	Nighthawk (15K) Error mitigation 15K gates 120 qubits Up to $120 \times 9 = 1080$ qubits	Starling (100M) Fault-tolerant 100M gates 200 logical qubits	Blue Jay (1B) Fault-tolerant 1B gates 2000 logical qubits
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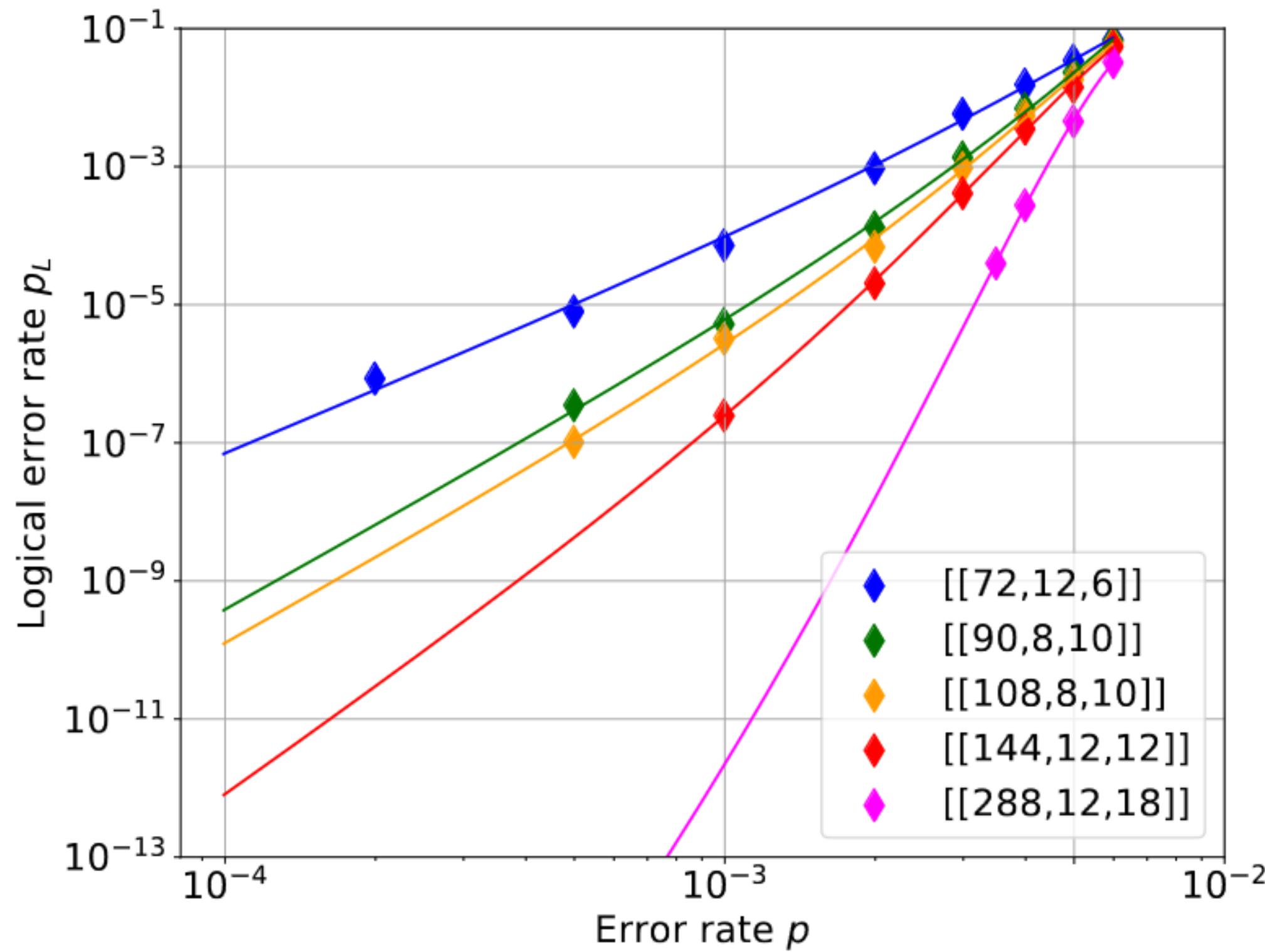
Innovation Roadmap

Flamingo Demonstrate scaling with l-couplers	Loon Demonstrate c-couplers and next-generation packaging for FTQC	Kookaburra Demonstrate a complete module consisting of a logical processing unit and quantum memory	Cockatoo Demonstrate entanglement of modules using a universal adapter	Starling Demonstrate multiple modules and magic state distillation
Crossbill Demonstrate m-couplers				

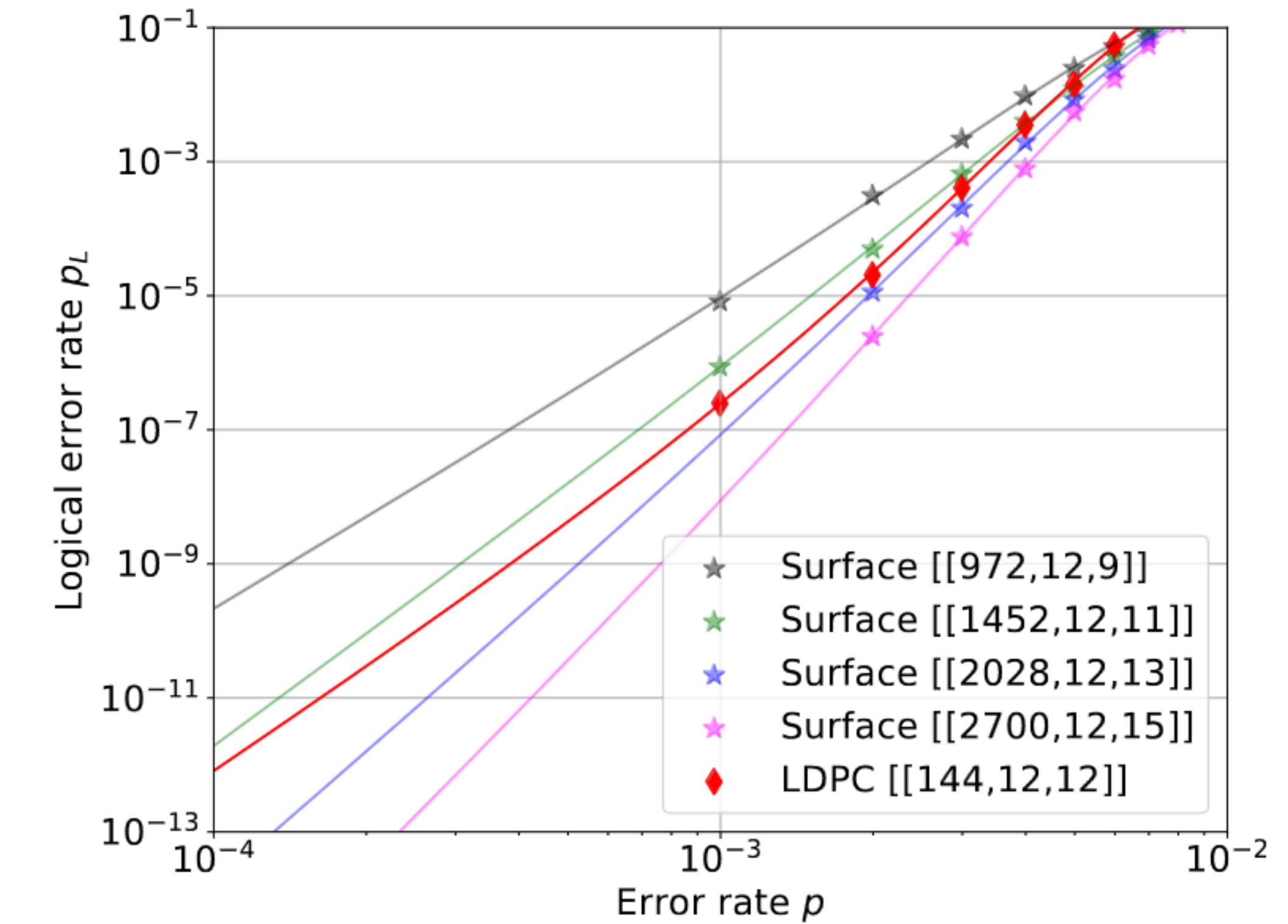
Hardware Innovation Towards Error-Corrected Quantum Computers

A New Family of Codes

Each code block encodes many qubits
Different codes with different error rates are available

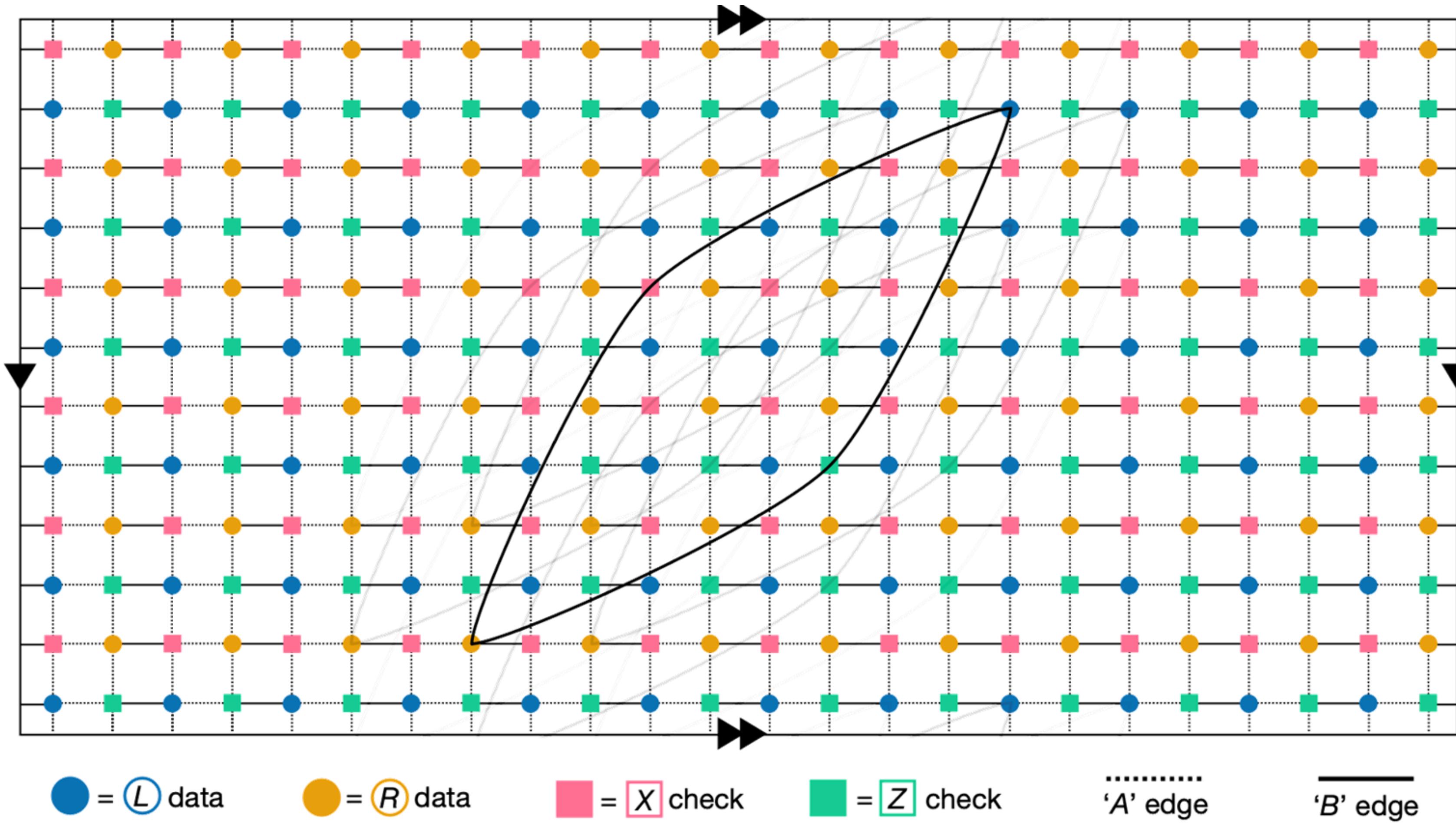


For “Gross code”, same error rates as surface code but with 10x fewer qubits



from Bravyi et al., Nature 627, 778-782 (2024)

Bivariate Bicycle Code on a 2D Grid



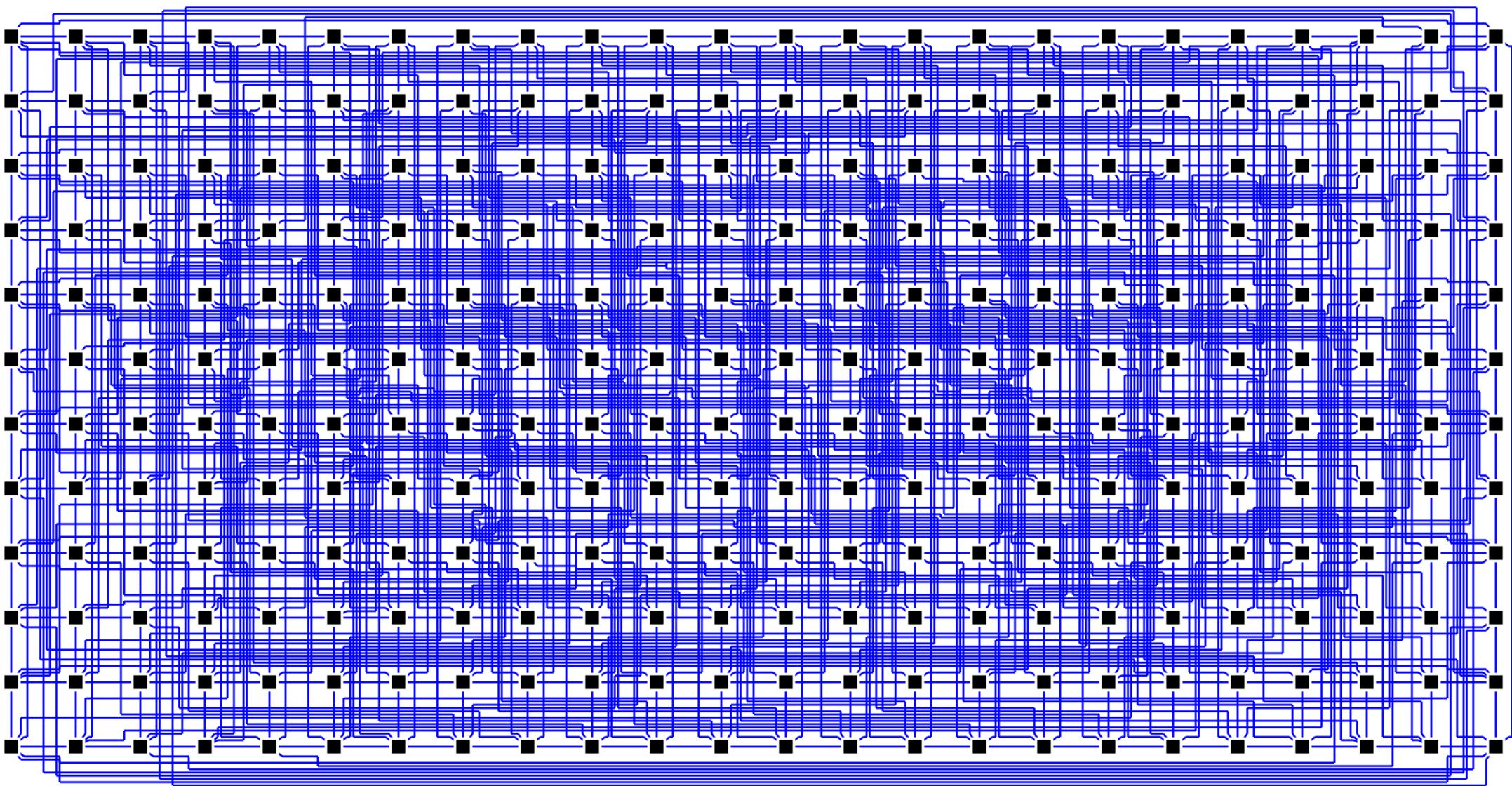
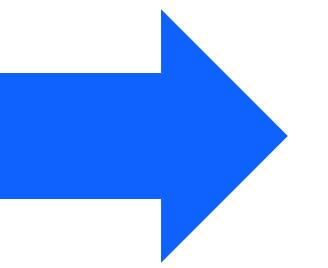
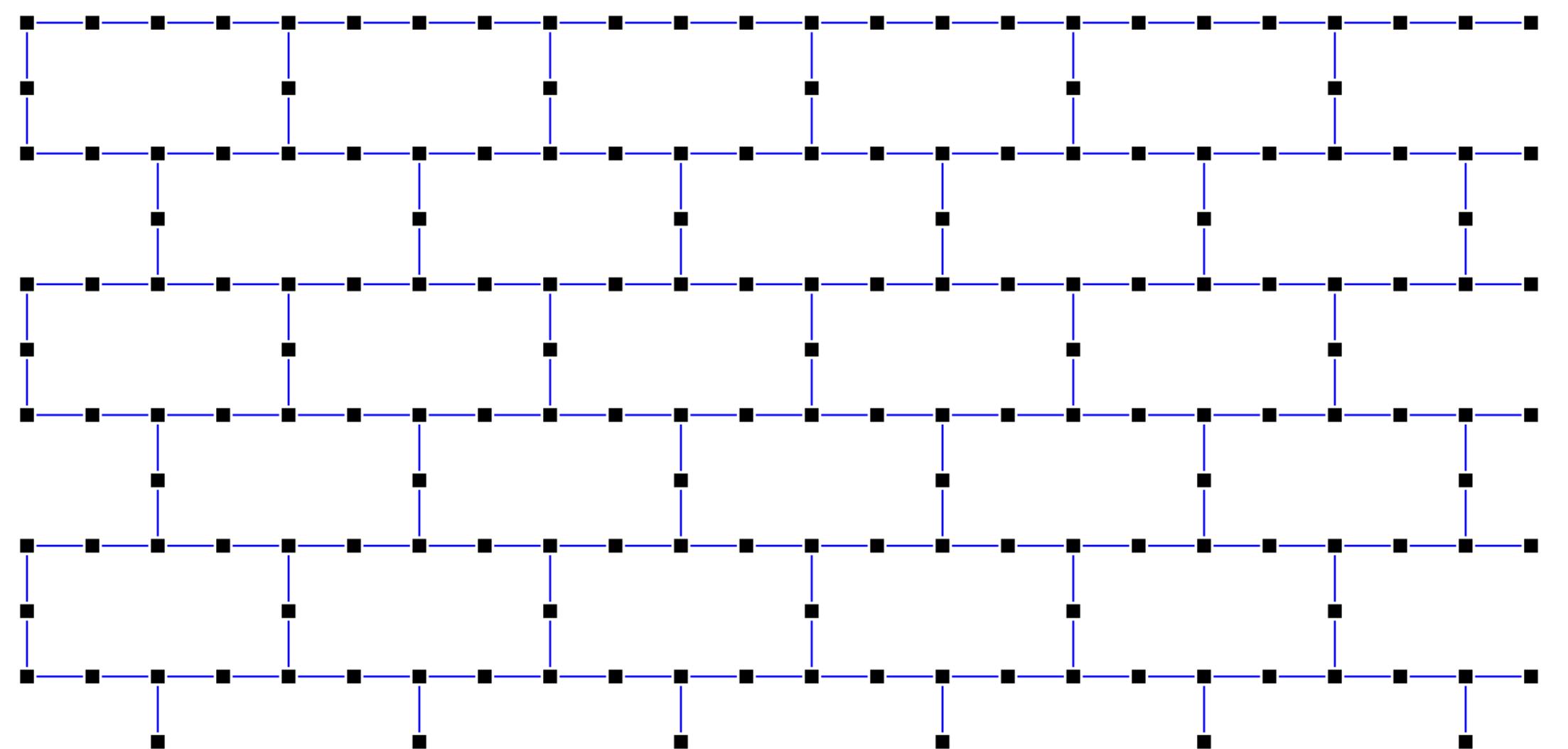
Gates required between non-neighbor physical qubits

Implements distance 12 code for 12 logical qubits

Logical memory
288 qubits + 864 couplers
6 degree connectivity

Logical processing unit
401 qubits + 1203 couplers
3-8 degree connectivity
(based on arXiv:2407.18393)

qLDPC – All About the Couplers



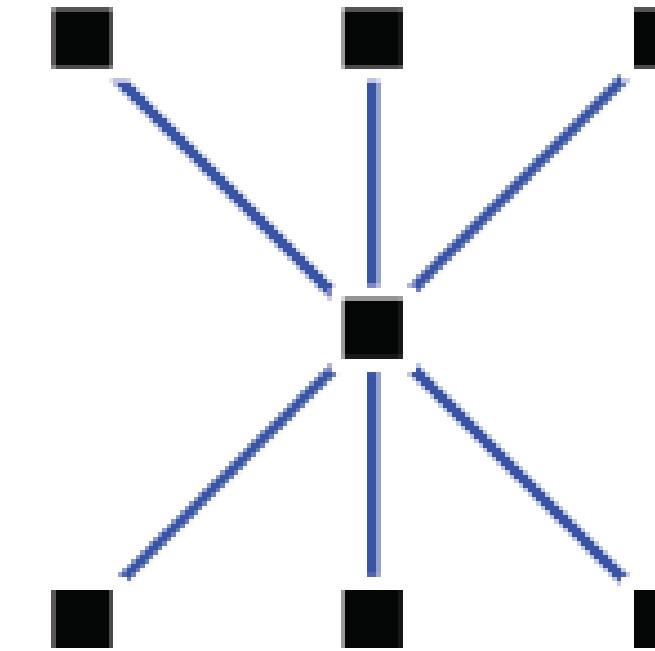
- Higher connectivity of LDPC codes requires significantly more couplers.

Ingredients for qLDPC Devices

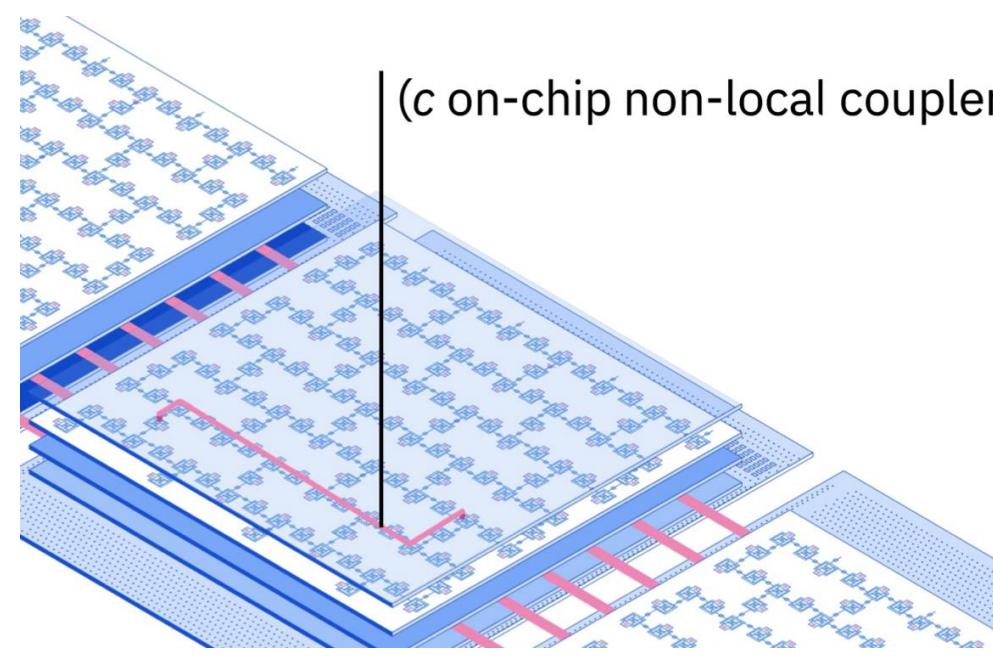
Efforts underway for bringing qLDPC devices to life:

Allowing 1 qubit to controllably interact with 6 neighbors with minimal crosstalk

→ Enables higher degree connectivity (smaller swap overhead)

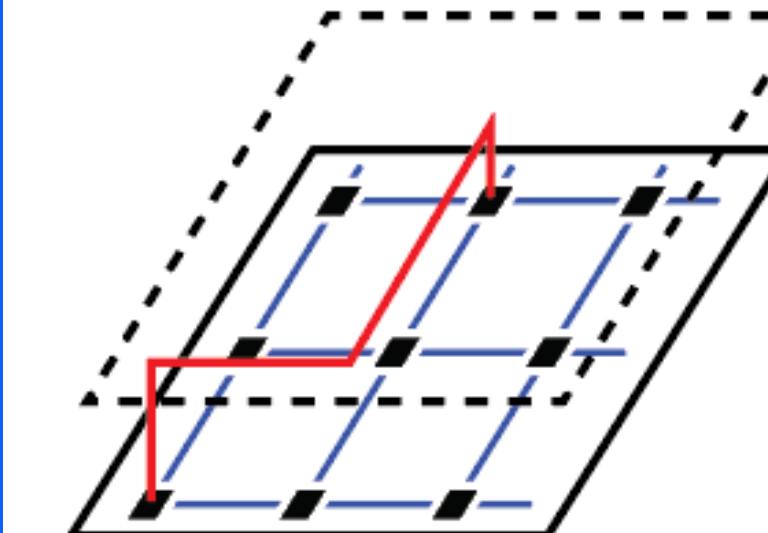


Increasing Length of the couplers



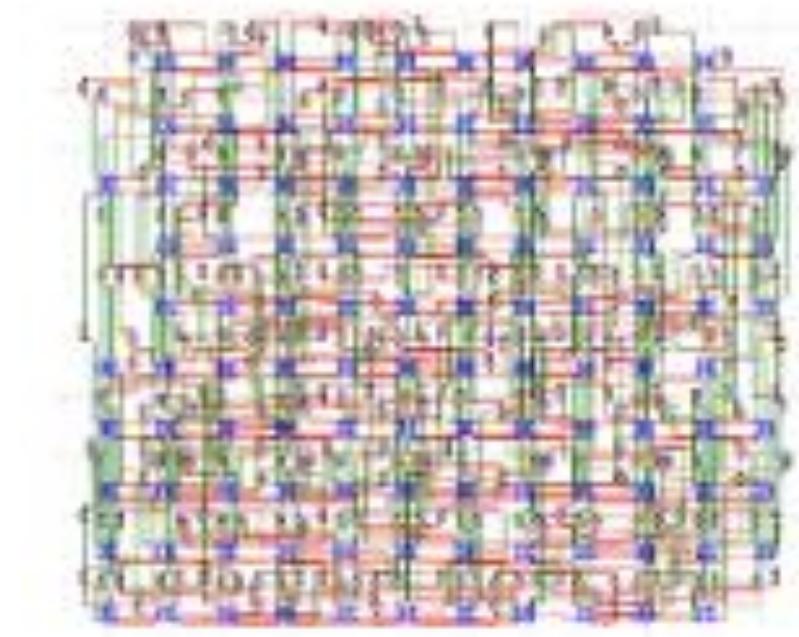
c-coupler layers to allow crossing of couplers.

→ Enables beyond 2D connectivity



Design automation work to allow rapid designs of more complex error corrected devices.

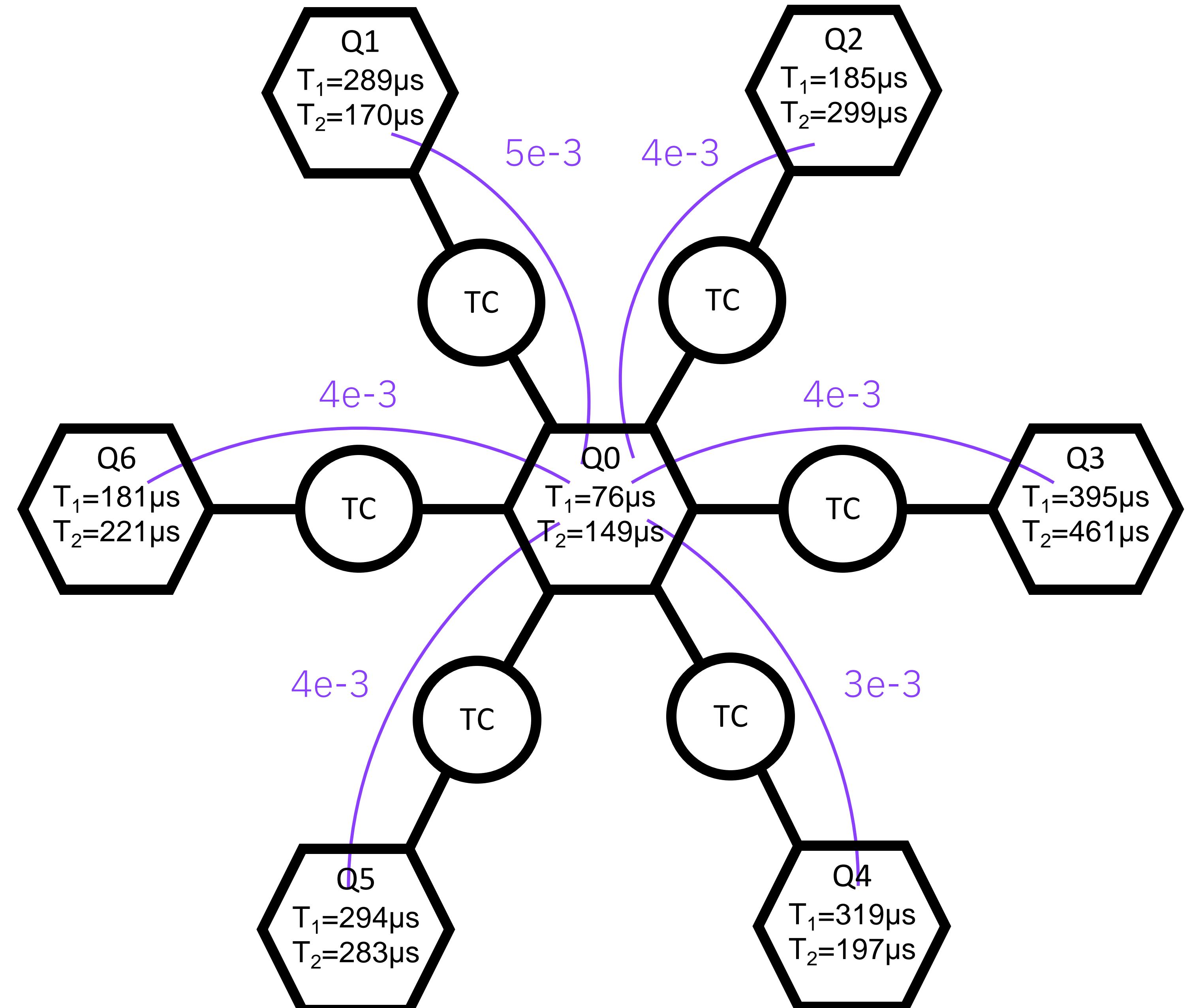
→ Enables faster design time.



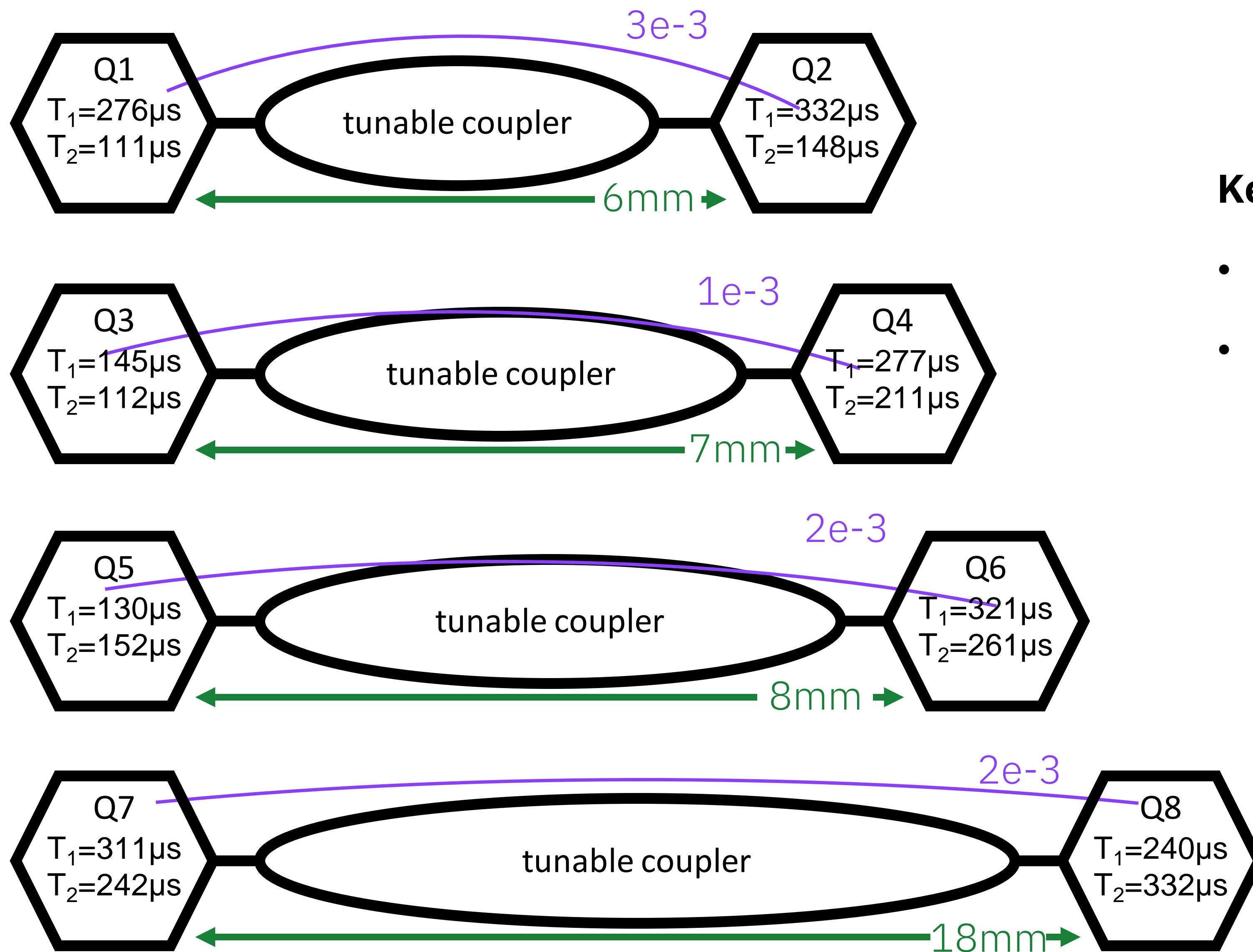
Increasing Connectivity

Key challenges:

- Crosstalk
- Increased role of tunable coupler in qubit performance



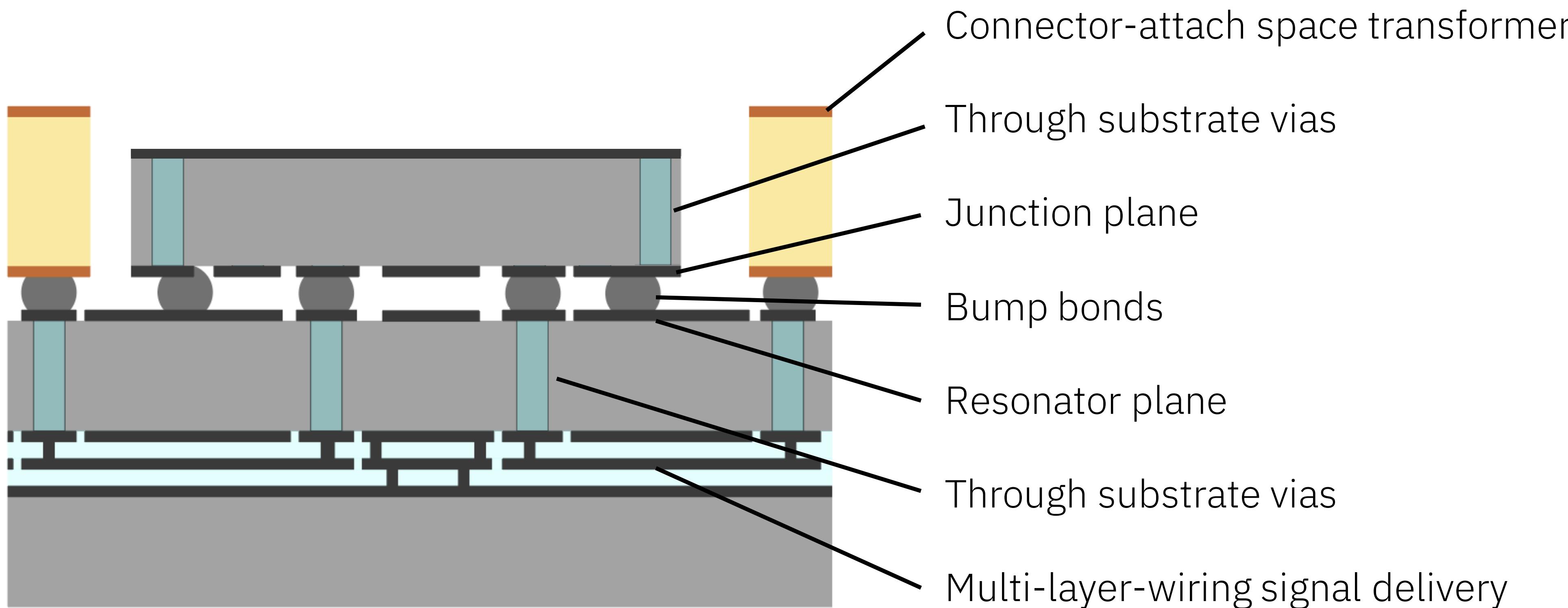
Extending the Range of On-Chip Gates



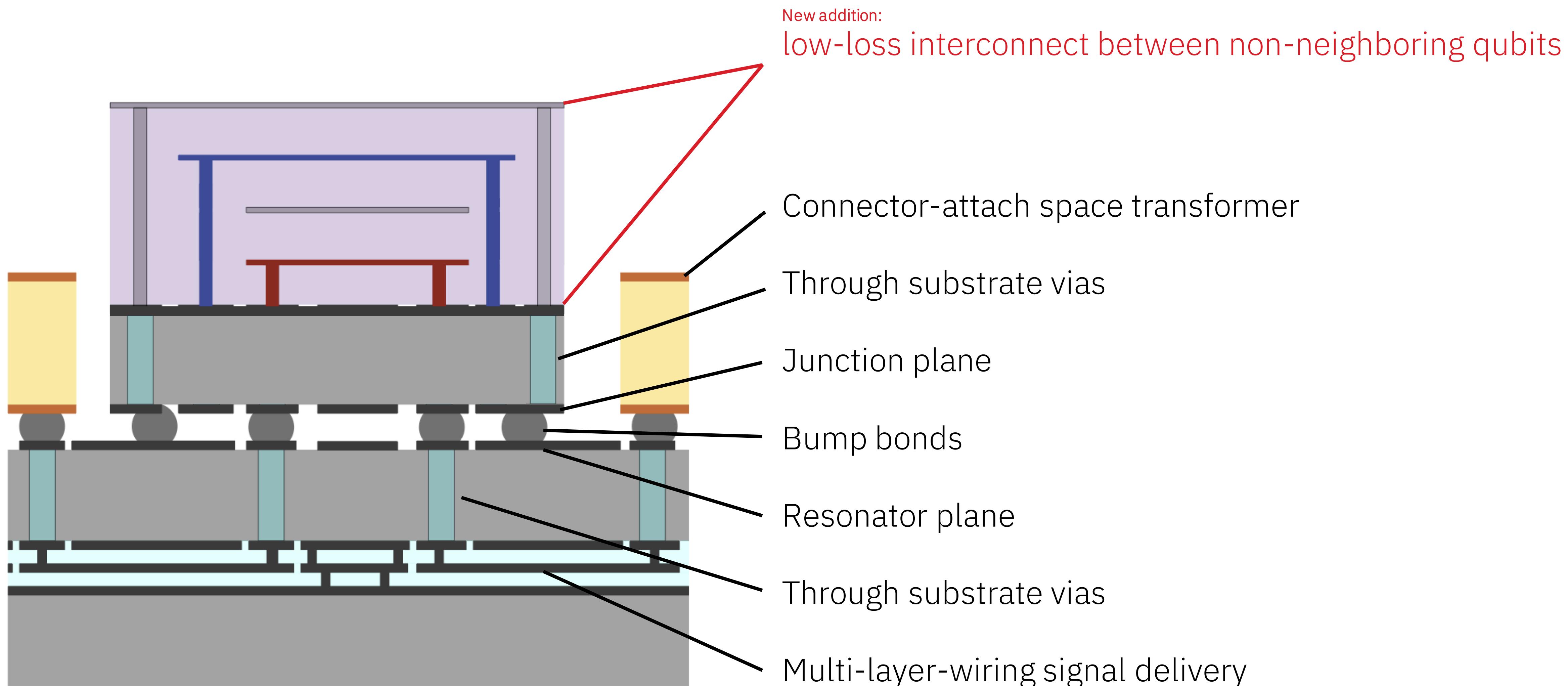
Key challenges:

- Coupling strength
- Increased complexity of design over a variety of lengths

Extending Our Packaging Technology

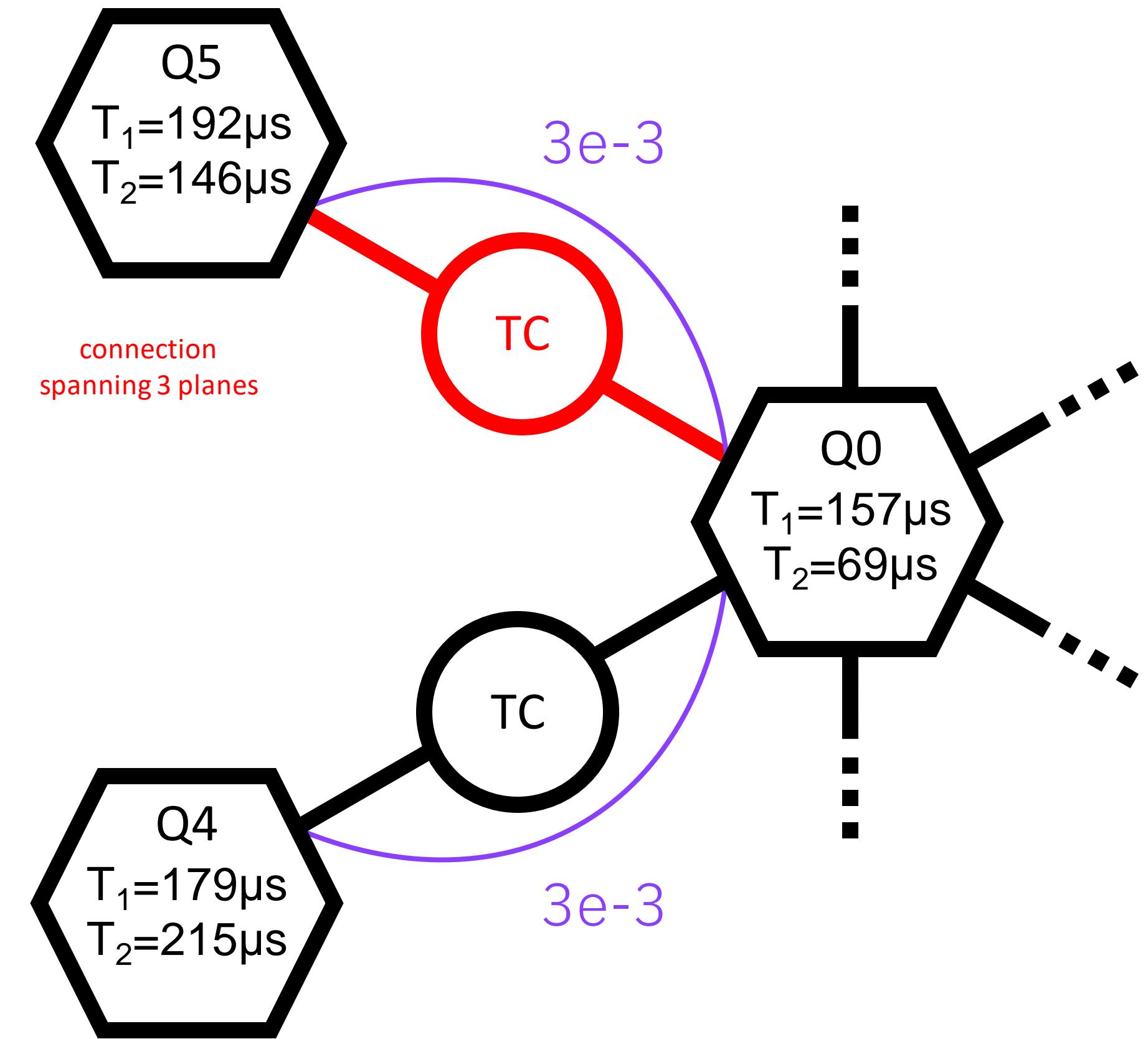
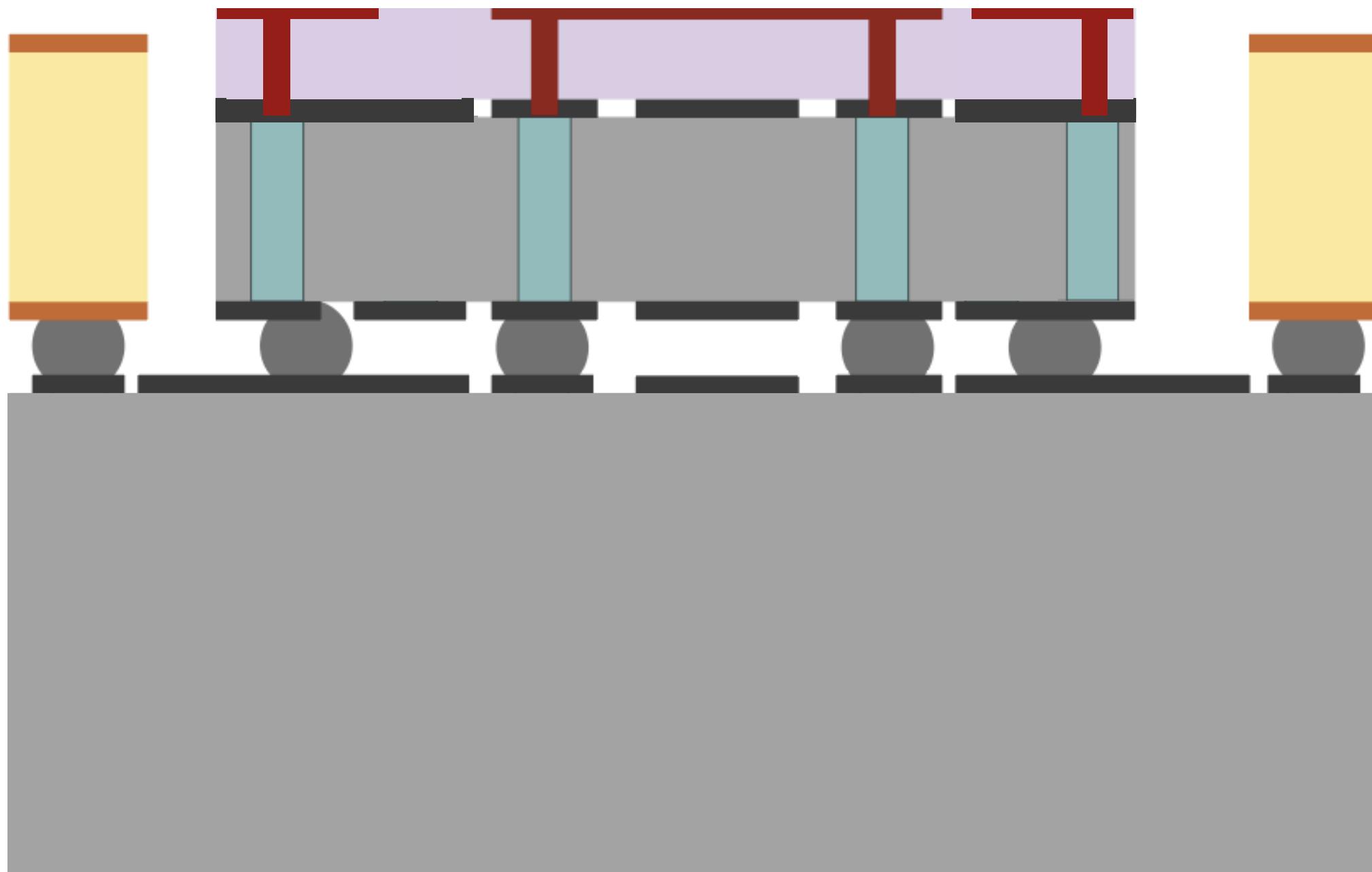


Extending Our Packaging Technology

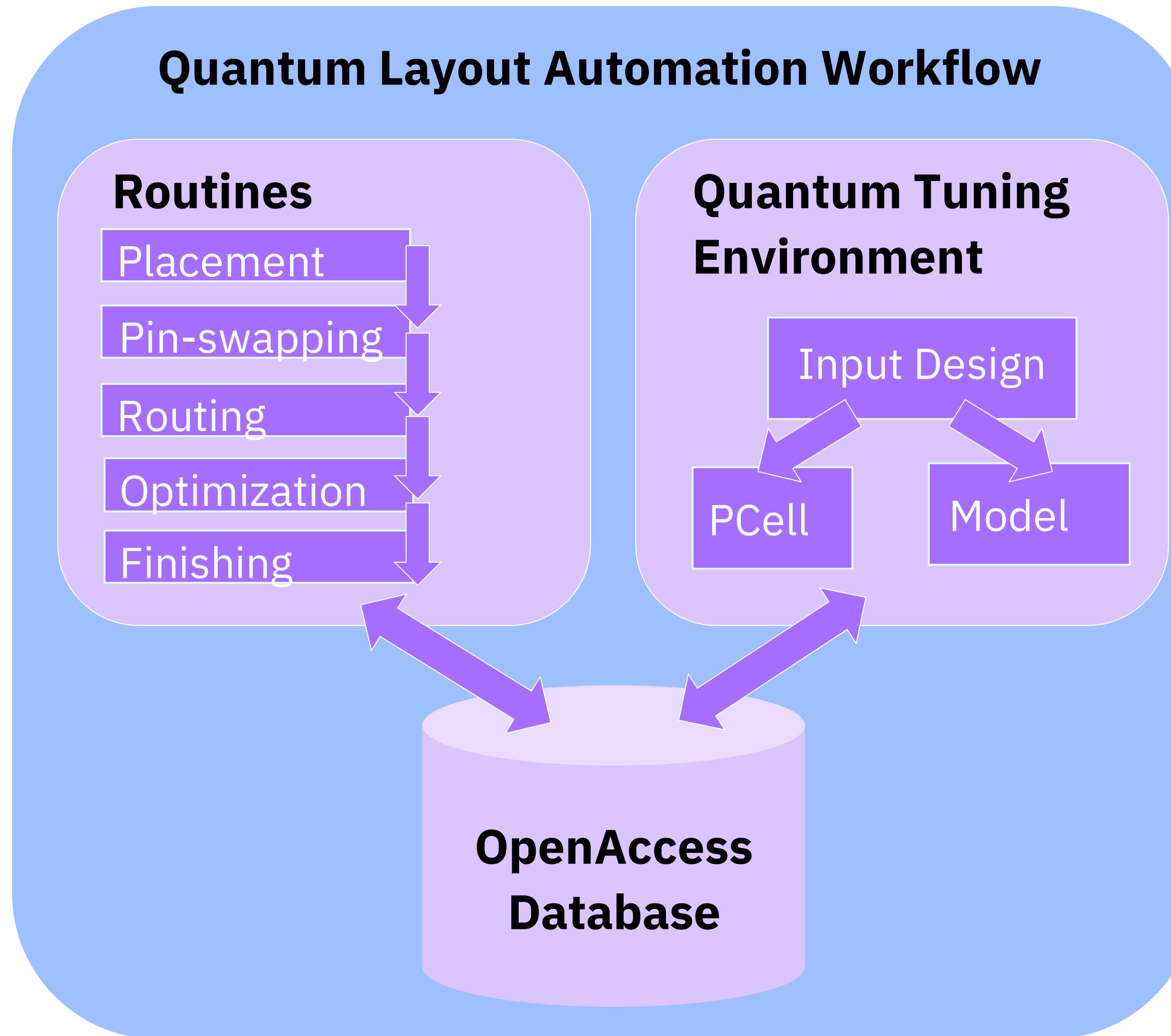


Test Device Proof of Concept

single additional layer of low-loss interconnect



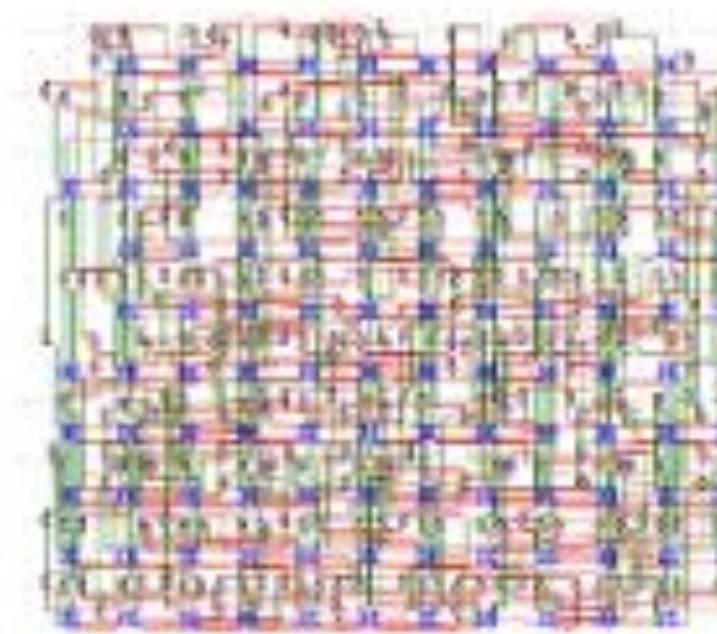
Electronic Design Automation



Workflow uses standard interchange formats:

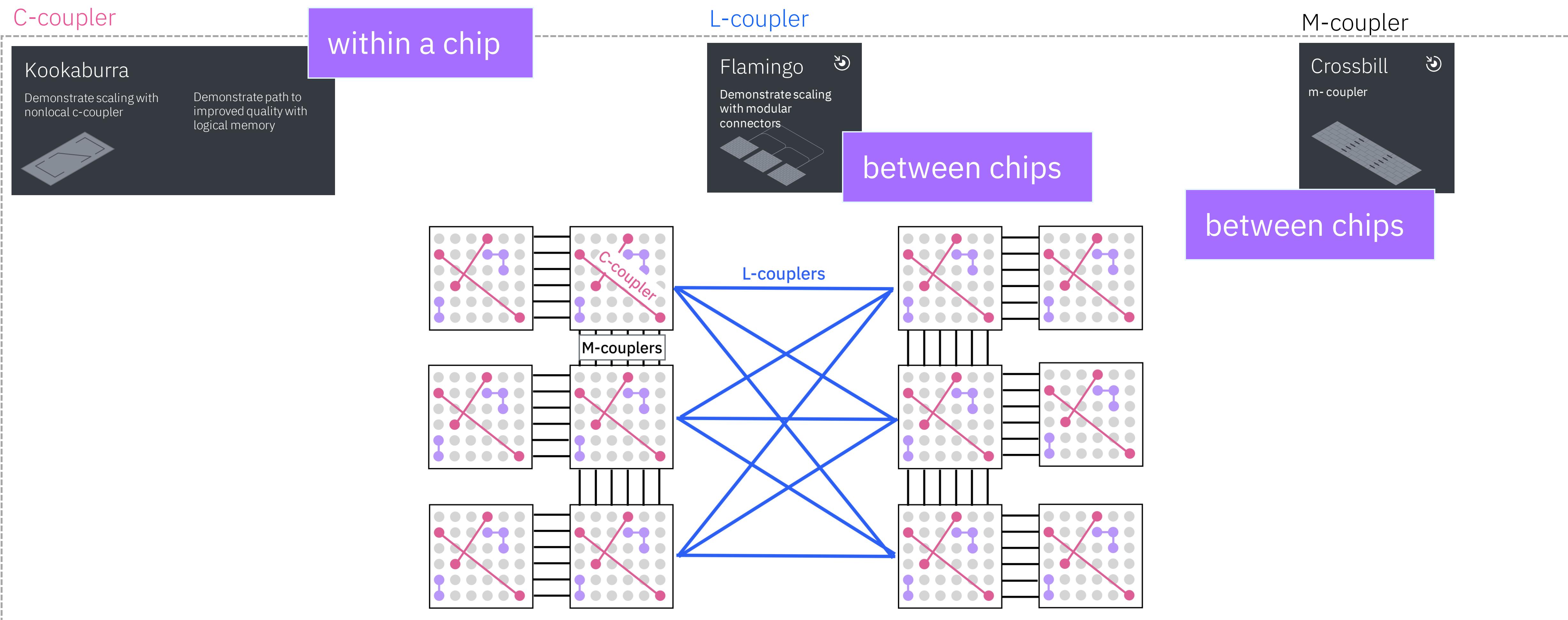
- enables the use of existing CMOS design tooling.

Example output:

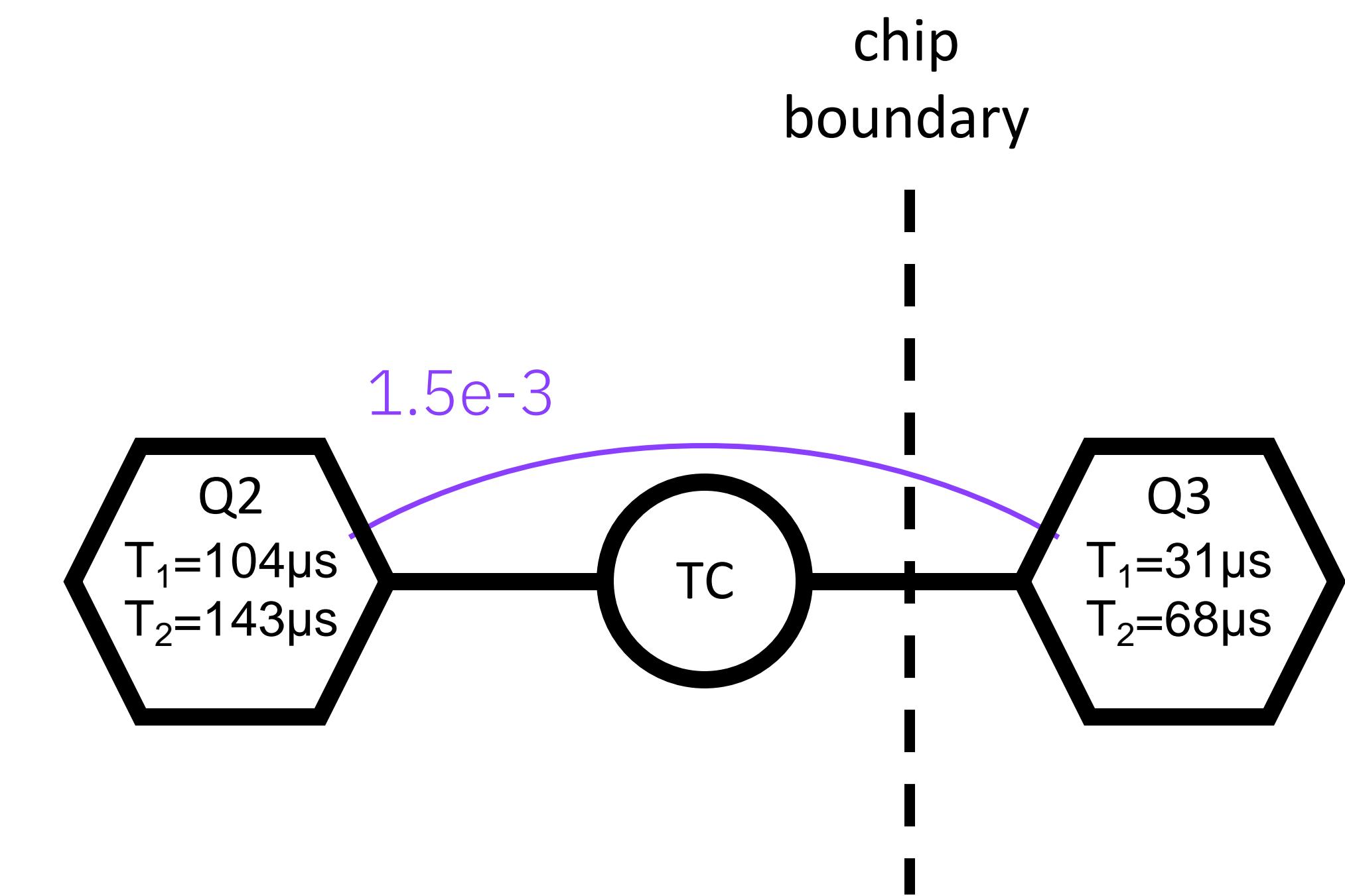
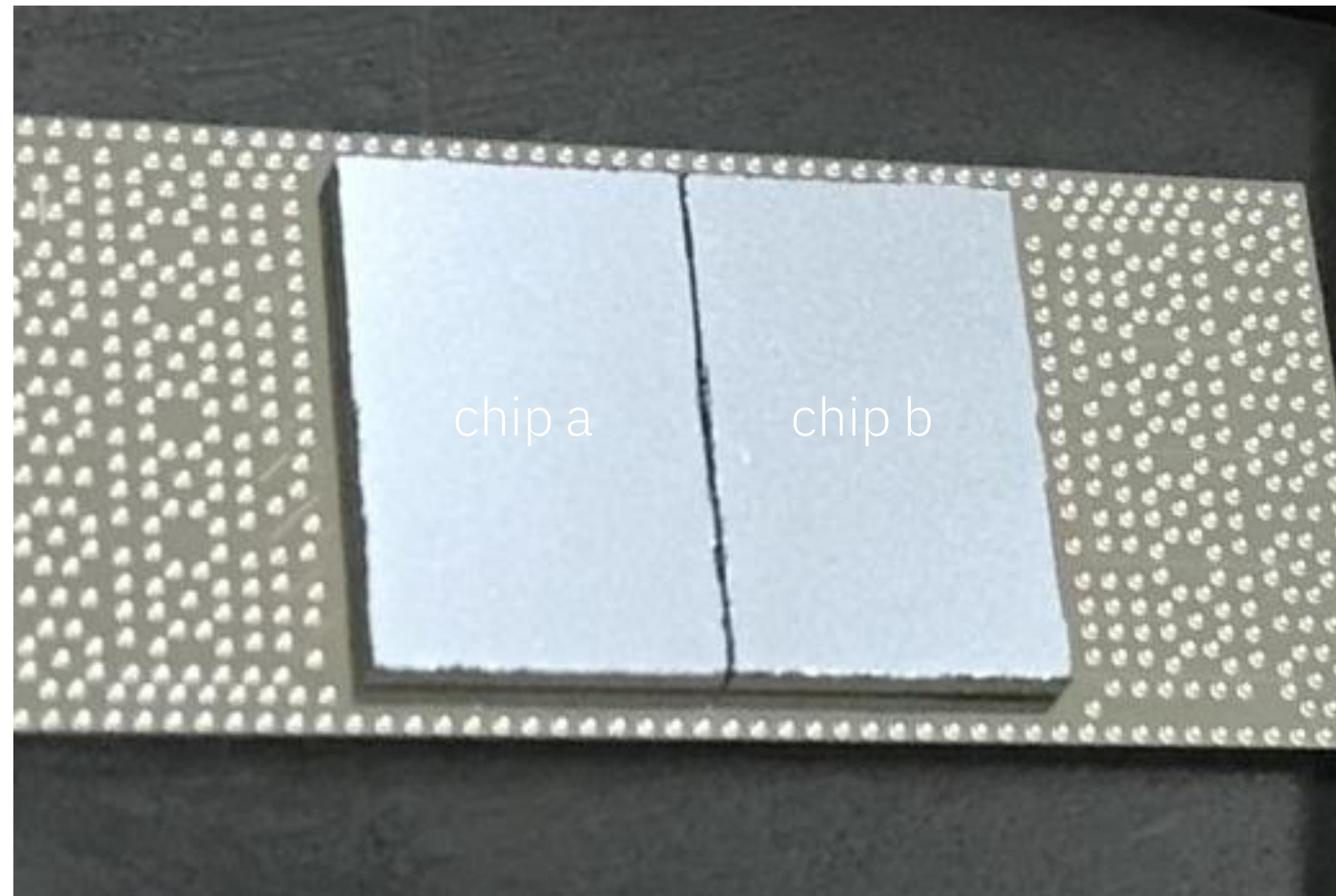


Building a Bigger Computer

Multi-Chip Processors

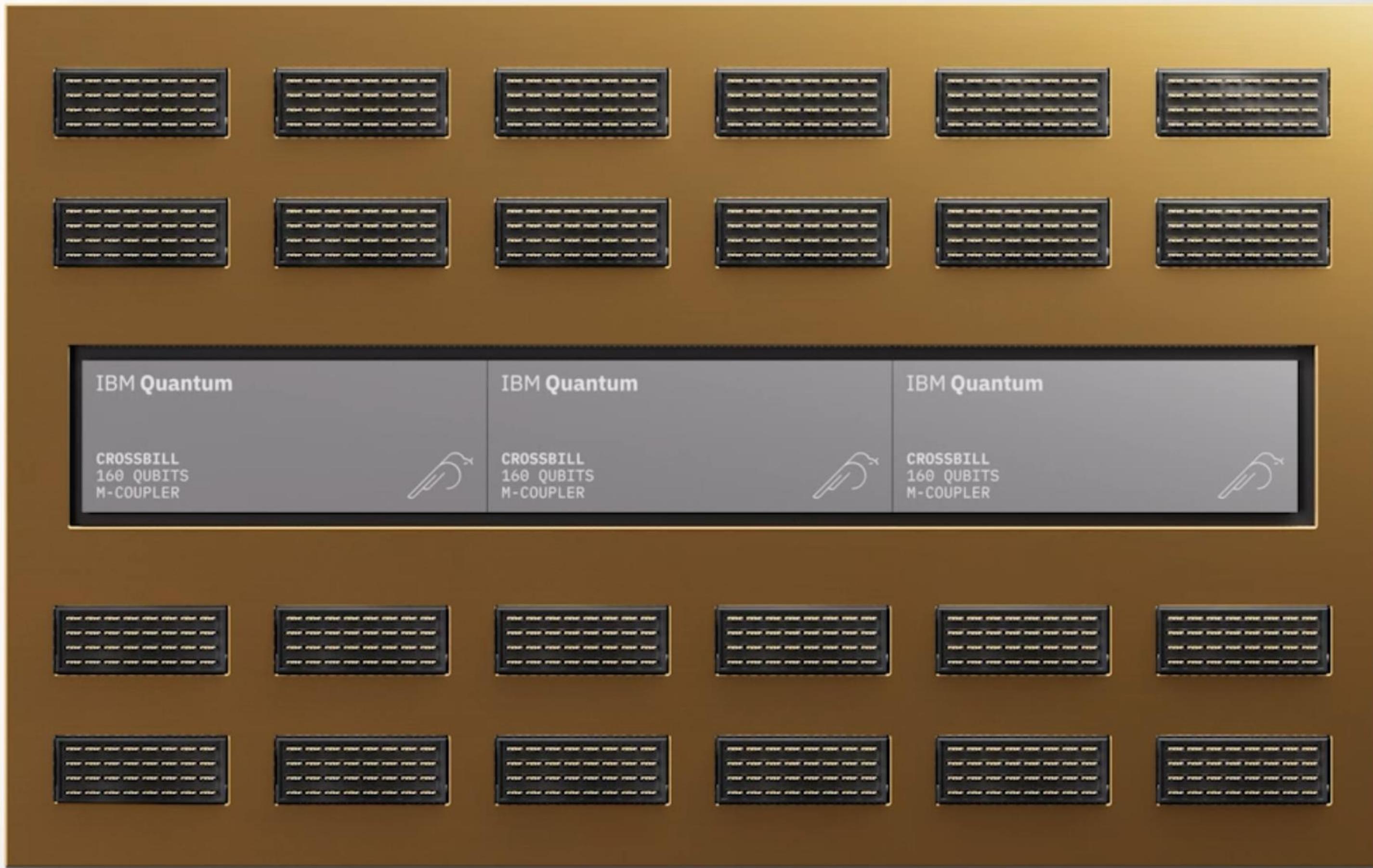


Test Device Validation of Chip-to-Chip Gate

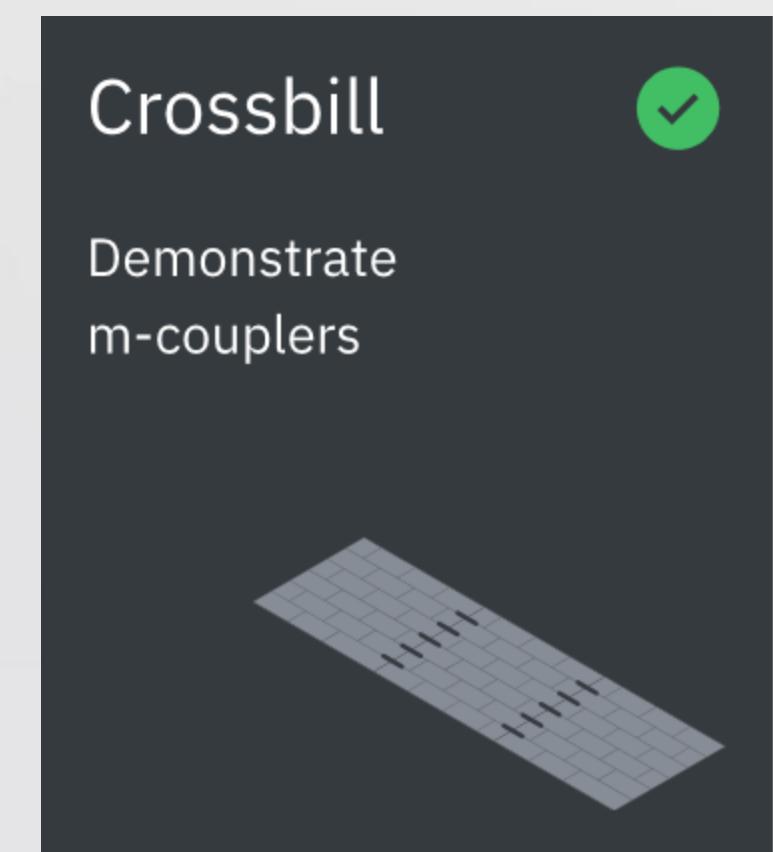


Crossbill: m-coupler Demonstration System

3 × 160 (480) qubits
548 total couplers



* artist's rendition of actual package

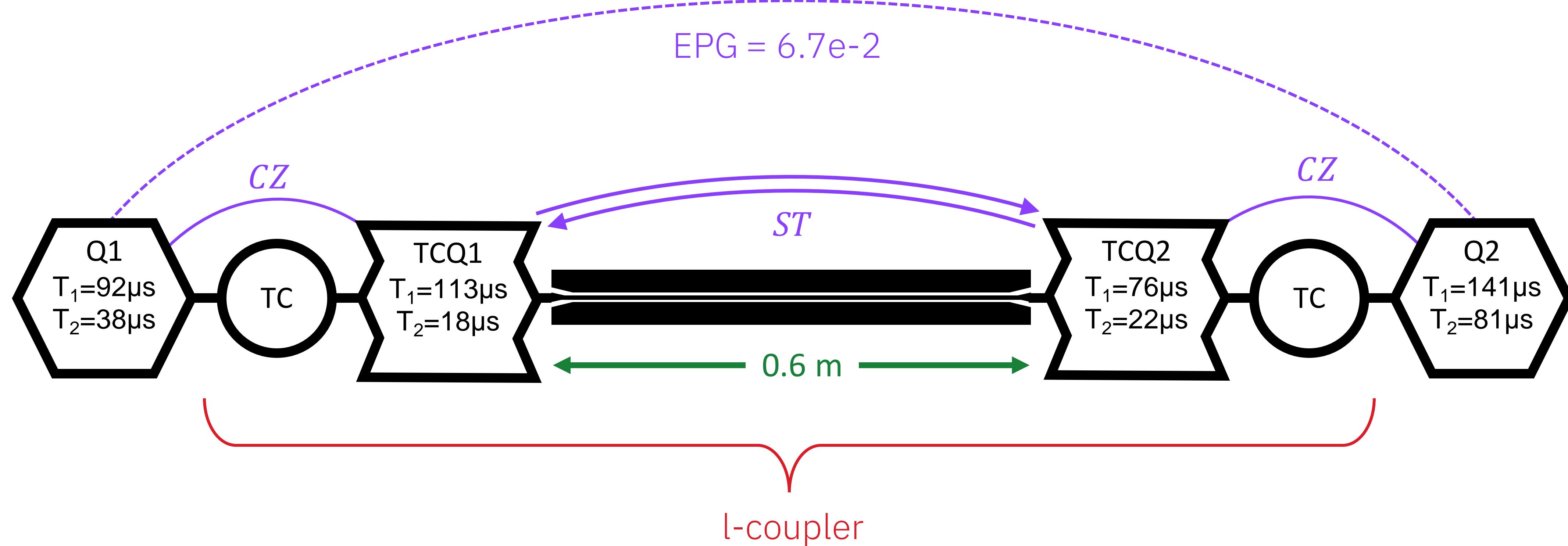


high-density connectors

large scale silicon packaging

I-coupler Gate Demonstration

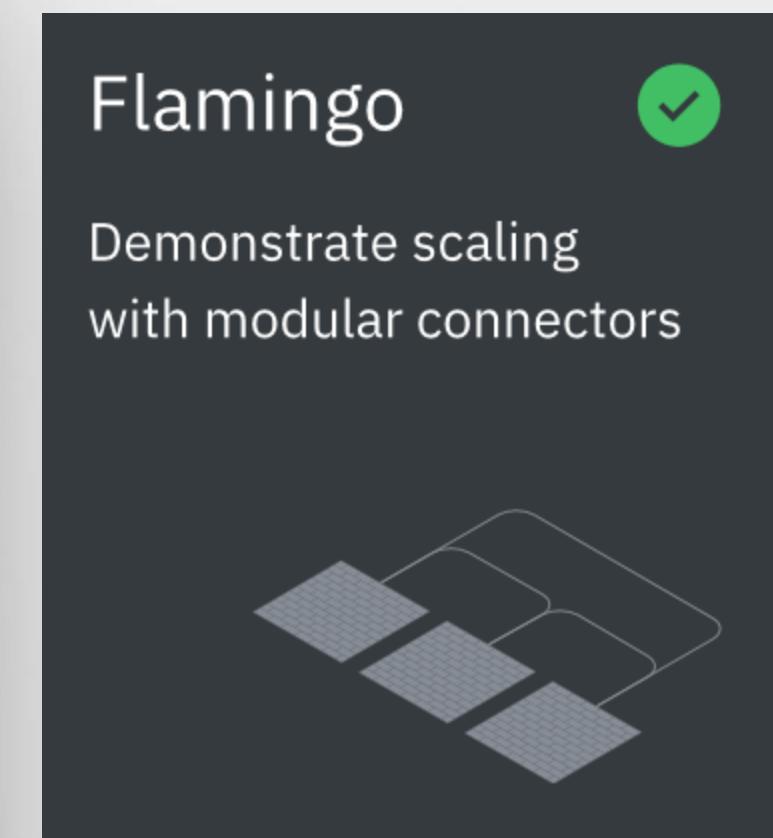
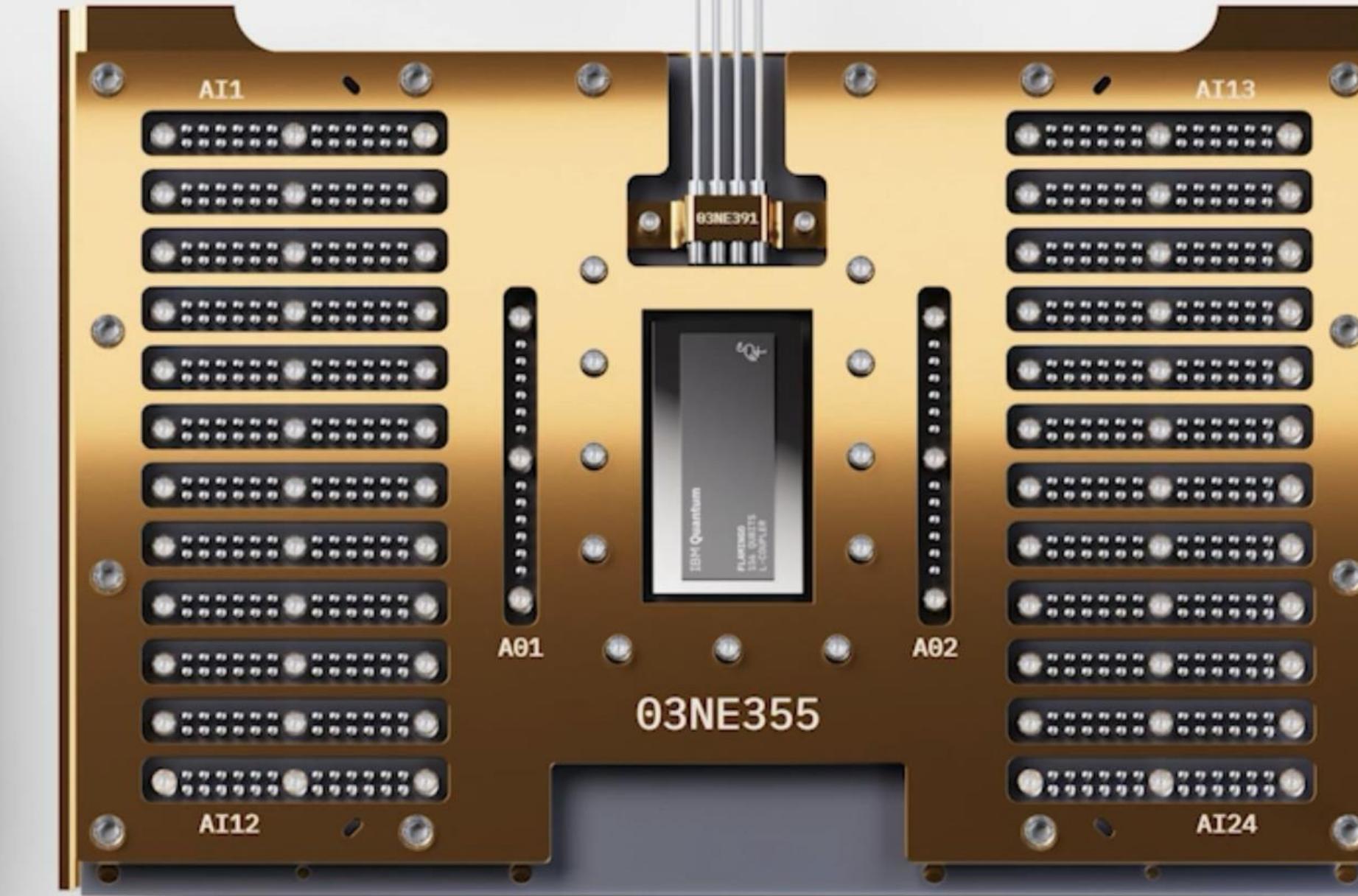
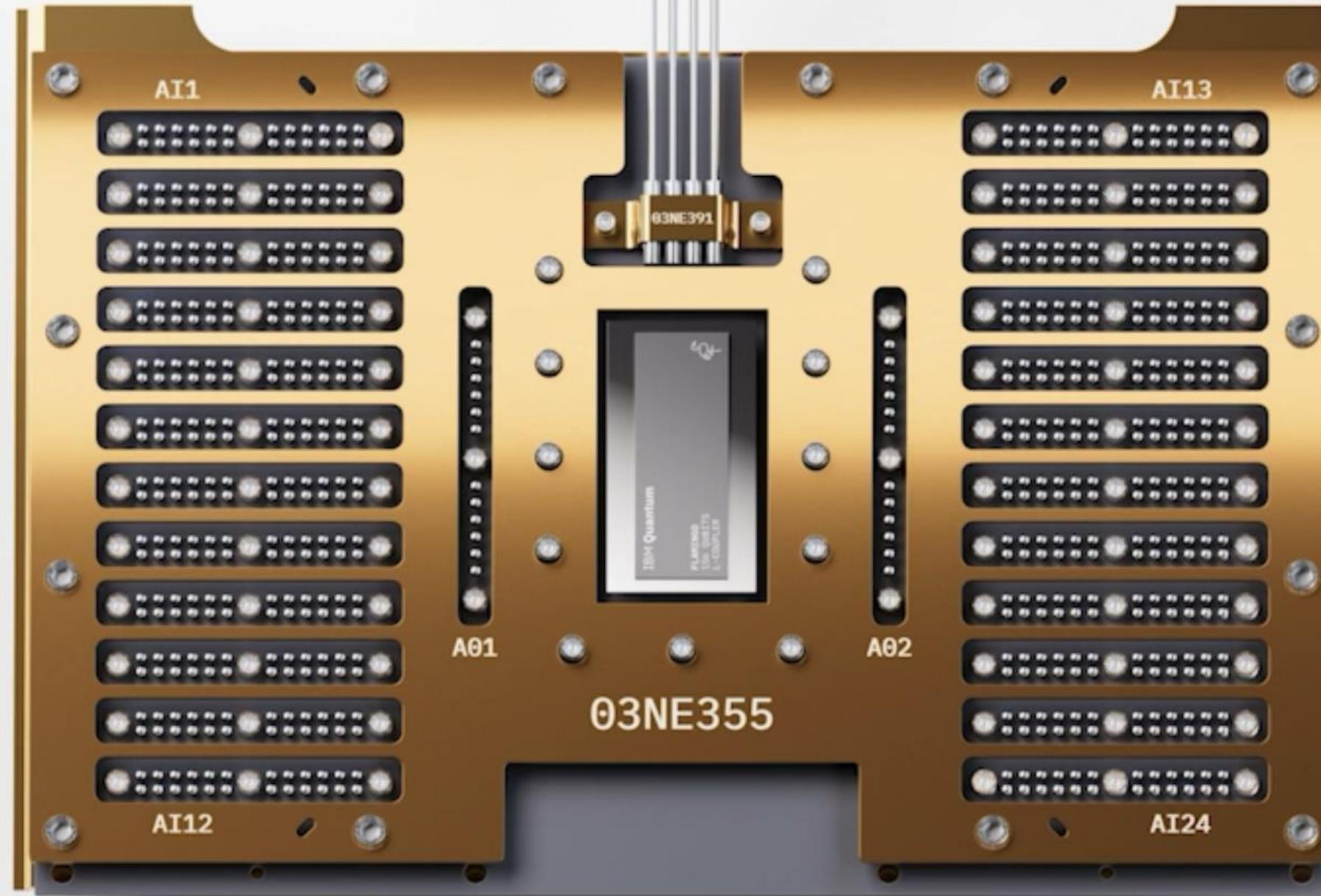
What is the operation that we can achieve over a long interconnect?



TCQ = tunable coupling qubit

Flamingo: I-coupler Demonstration System

2 × 156 qubits
4x I-coupler connections,
0.7 to 1 meter long



* artist's rendition of actual package

Summary

- Looking back: 10 years of engineering progress in
 - control electronics,
 - wiring,
 - packaging and
 - quantum chip performance.
- Looking forward: engineering towards error-corrected superconducting quantum computer with
 - long range on chip couplers,
 - new design tools and
 - multi-chip technology.

Thank you!

IBM Quantum

