Design and Development Task in Power Electronic and Devices (EE348)

Project End Semester-Report on

Cascaded H-Bridge Multilevel Inverter with SPWM Technique

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BACHELOR OF TECHONOLOGY

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ELECTRICAL AND ELECTRONICS ENGINNERING

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DECLARATION

We hereby declare that the report entitled **"Cascaded H-Bridge Multilevel Inverter with SPWM Technique"** is a Bonafide record of the project work carried out by us in fulfilment of the requirements of the course **EE348 - Design and Development Task in Power Electronic and Drives** in the Department of Electrical and Electronics Engineering, National Institute of Technology Karnataka, Surathkal. The work presented in this report is original and has not been submitted to any other University or Institution for the award of any degree, diploma, or certification.

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CERTIFICATE

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ABSTRACT

The increasing adoption of electric vehicles and renewable energy systems has intensified the demand for high-performance power converters with low harmonic distortion. Conventional two-level inverters generate output with significant harmonic content and require bulky filters to meet power-quality standards. To overcome these drawbacks, this project presents the design and simulation of a **Sinusoidal Pulse Width Modulation (SPWM)** based inverter system in **MATLAB/Simulink**, including both a **single H-bridge inverter** and a **Cascaded H-Bridge (CHB) five-level inverter**.

SPWM pulses were produced by comparing a **50 Hz sinusoidal reference** with a **triangular carrier** signal, and applied to **MOSFET switches** in the inverter modules. Performance was evaluated under R and RL load conditions by measuring **RMS voltage**, **RMS current**, and **Total Harmonic Distortion (THD)** using Simulink measurement tools. The system was later scaled to a **five-level inverter** by cascading two H-bridge units, and the same assessments were conducted. Additionally, an **LC filter** was introduced at the output, and the impact of **different inductance values** on power quality was analyzed.

The experimental findings clearly show that the five-level inverter provides significantly lower THD and better waveform quality than the two-level inverter. The inclusion of an LC filter further suppresses high-frequency harmonics, resulting in a much closer-to-sinusoidal waveform. Overall, the results validate the effectiveness of the **CHB multi-level inverter with SPWM control** for applications requiring improved power quality, especially in **renewable energy conversion** and **electric drive systems**.

Keywords: SPWM, Cascaded H-Bridge (CHB), Mutli Level Inverter, MATLAB/Simulink, THD, LC Filter, Power Quality

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INTRODUCTION

1.1 Background

The expansion of power electronic converters in systems such as electric vehicle drives and renewable energy generation has made power quality enhancement a major requirement. Traditional two-level inverters generate waveforms containing a high amount of harmonic distortion, which negatively impacts system efficiency, reliability, and electromagnetic compatibility.

To overcome these drawbacks, multilevel inverter technologies have been developed. Among them, the Cascaded H-Bridge (CHB) architecture is especially attractive due to its simple modular design, ability to produce multiple voltage levels, and improved sinusoidal output characteristics

1.2 Problem Statement

Square-like waveforms from a standard two-level inverter led to high harmonic content, requiring large passive filters to meet power quality standards, which increases cost and system size. Thus, a topology capable of reducing harmonics while maintaining a compact structure is essential for modern power electronic applications.

1.3 Objectives

This project aims to:

- Develop SPWM using Simulink for switching control
- Implement a MOSFET-driven H-Bridge inverter
- Analyze THD and RMS values under R load.
- Extend the system to a five-level CHB inverter and evaluate performance improvement
- Study the influence of an LC filter by varying inductance values

1.4 Scope of Work

This study is limited to simulation-based evaluation using MATLAB/Simulink. All results, including THD and RMS values, are obtained through built-in measurement blocks without hardware implementation

SYSTEM MODELLING IN MATLAB/SIMULINK

2.1 SPWM Signal Development

SPWM signals are produced by comparing a 50 Hz sinusoidal reference with a triangular carrier generated from a Repeating Sequence block. The comparator output determines the ON/OFF switching instants of each MOSFET.

2.2 Control Circuit Design (SPWM Implementation)

The SPWM control circuit for the 5-level cascaded H-bridge inverter is implemented using a sinusoidal reference and two level-shifted carrier signals. The complete procedure is as follows.

2.2.1. Sinusoidal Reference Signal (V_{ref})

- Add a *Sinusoidal Voltage Source* (or Sine Wave) block.
- Set:
  - Amplitude $A_m = 2$
  - Frequency $f = 50$ Hz
  - Phase = 0°
- Use this signal as the common reference for both cascaded cells.

2.2.2. Level-Shifted Carrier Signals (CA, CB)

- Add two *Repeating Sequence Stair* (or equivalent triangular) blocks.
- For both carriers, set:
  - Time values: [0 1]
- Set output values as:
  - Carrier CA (lower carrier, range 0–1): [1 2]
  - Carrier CB (upper carrier, range 1–2): [1 2]
- Adjust:
  - Sample time and time scaling so that the effective carrier frequency is $f_c \approx 2500$ Hz (or desired switching frequency).

2.2.3. Comparator Stage (SPWM Generation)

- For a 5-level CHB with two series cells, generate four comparison signals.
- Use four *Relational Operator* blocks configured as:
  - Operator: u1 > u2 (reference compared with carrier).
- Inputs:
  - $u1$: sinusoidal reference V_{ref}
  - $u2$: carrier CA or CB, depending on which cell is being modulated.

2.2.4. Gate Signal Generation – Positive Half Cycle

- Define primary gate pulses for the upper switches of each cell:
  - S_{11}: output of comparator $V_{ref} > C_B$, Drives the positive switch of Cell 1.
  - S_{12}: output of comparator $V_{ref} > C_A$, Drives the positive switch of Cell 2.
- These two pulses determine which cell contributes to the stepped output at any instant.

2.2.5. Gate Signal Distribution (H-Bridge Logic)

- Use Logical Operator and NOT blocks to derive complementary and leg-safe signals.
- Typical relations for each H-bridge leg:
  - $S_{13} = \neg S_{11}$ (complement of S_{11})
  - $S_{14} = \neg S_{12}$ (complement of S_{12})
- Ensure interlock:
  - Switches in the same leg (e.g., S_{11} and S_{13}, or S_{12} and S_{14}) must never be high at the same time.
- Where available, use a dedicated PWM Generator / H-Bridge block to:
  - Enforce complementary gating,

- Insert dead-time,
- Simplify interlock and protection logic.

2.2.6. Control Signal Assignment to Cascaded Cells

- For **Cell 1** H-bridge:
  - S_{11}, S_{13}: upper and lower switches of leg-1.
  - S_{12}, S_{14}: upper and lower switches of leg-2.
- For **Cell 2** H-bridge:
  - Duplicate the same structure and naming, e.g.:
    - S_{21}, S_{23} (leg-1),
    - S_{22}, S_{24} (leg-2), generated from the corresponding CA/CB comparisons and NOT operations.
- Route the final eight gate signals:
  - Cell 1: $S_{11}, S_{12}, S_{13}, S_{14}$
  - Cell 2: $S_{21}, S_{22}, S_{23}, S_{24}$
    directly to the gate inputs of the two H-bridge power stages.

2.3 MOSFET-Based H-Bridge Inverter

Four MOSFET switches arranged in an H-Bridge configuration are driven by the SPWM pulses. Complementary gating ensures that output polarity alternates, forming an AC waveform from a DC input.

2.4 DC Power Supply

A DC source is used to provide input power to the inverter. In the five-level inverter, two DC sources with the same voltage are used. This helps the inverter create five voltage levels at the output:

+2Vdc, +Vdc, 0, –Vdc, –2Vdc

The DC source block in Simulink is connected correctly so the inverter works properly.

2.5 R Load Modelling

The system is tested with different load configurations:

- Pure resistive (R) load

This helps examine both power and harmonic behaviours under realistic operating conditions.

2.6 Measurement of RMS and THD in Simulink

Simulink measurement blocks are used:

- RMS Voltage and Current measurement blocks
- THD Analysis block with 50 Hz as fundamental frequency

LC FILTER DESIGN & PERFORMANCE ANALYSIS

3.1 LC Output Filter

The LC filter improves the inverter output by reducing unwanted harmonic components.

- The inductor (L) blocks fast-changing switching signals
- The capacitor (C) reduces voltage ripples
- Together, they make the output voltage much smoother

Because of this, the filter improves power quality, reduces noise in the load, and protects connected equipment from harmonic effects.

3.2 LC Filter in Simulink

The LC filter is placed between the inverter and the load.

- L is connected in series with the output line
- C is connected across the load

The filter is built using standard Simulink components, and the parameters are easily adjustable for testing performance.

3.3 Changing Inductor Values

To study the filter behaviour, different values of the inductor are tested while keeping the capacitor fixed.
Observations:

- When L increases, the waveform becomes more smooth
- THD decreases as more harmonics are filtered out
- Current waveform becomes more sinusoidal, especially for RL load
- Too much inductance can cause:
    - Voltage drops
    - Slow response to load changes

THREE-LEVEL INVERTER USING SPWM

4.1 Simulink Model Description

- The 3-level H-bridge inverter uses two H-bridge cells connected in series.
- Each H-bridge has its own DC supply, typically split from a main DC bus.
- The inverter synthesizes output voltages by selecting switching states of the H-bridge transistors.

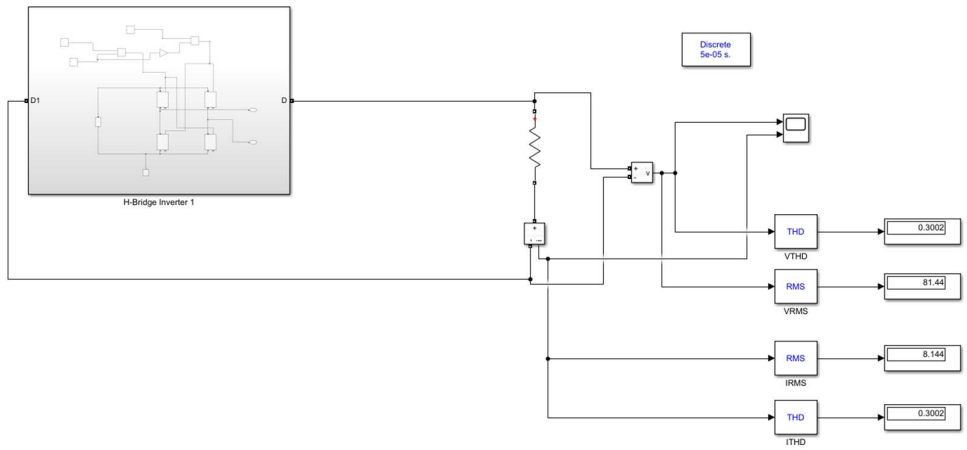

Fig.4.1.1 Circuit diagram for Rload without Filter (R_{load} = 10 Ω)

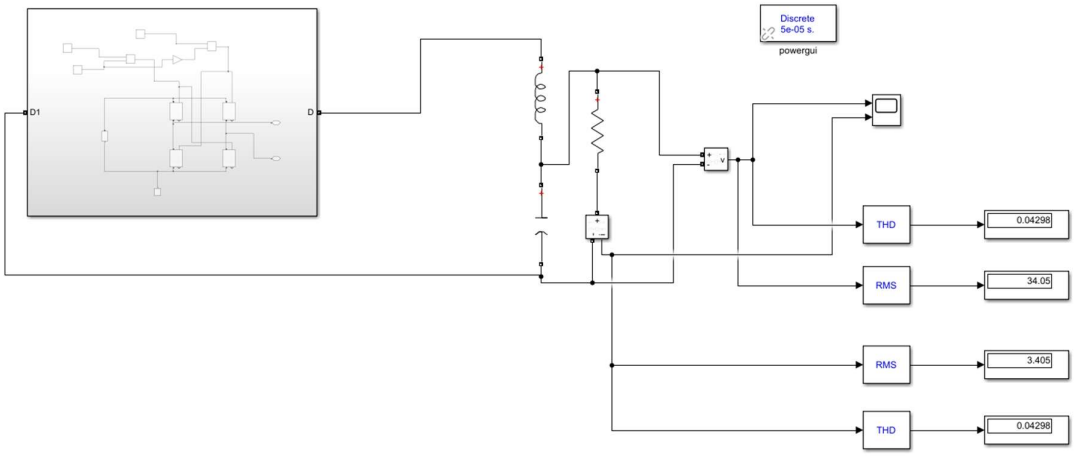

Fig.4.1.2 Circuit diagram for Rload with Filter (R_{load} = 10 Ω)

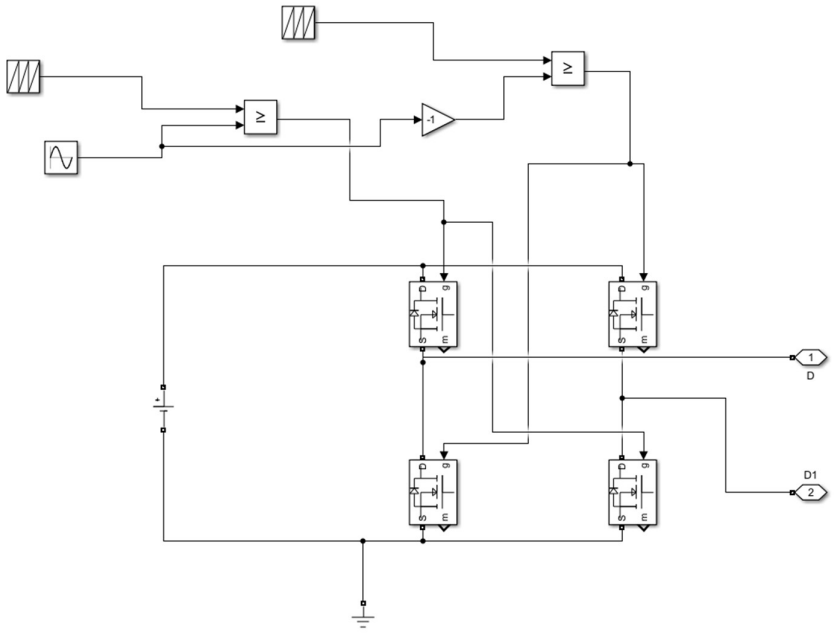

Fig.4.1.3 Circuit diagram for H-bridge Inverter

4.2 Three-Level Output Voltage Generation

- The output voltage can have three levels:
    - +Vdc (positive DC voltage)
    - 0 (zero voltage)
    - -Vdc (negative DC voltage)
- These voltage levels approximate the sinusoidal waveform with more steps than a 2-level inverter, reducing harmonic distortion.
- The inverter switches operate in complementary pairs to generate output voltage levels:

Switch Configuration	**Output Voltage Level**
Bridge 1 **ON** positive leg, Bridge 2 **ON** positive leg	+Vdc
One or both bridges in neutral or zero state	0
Bridge 1 **ON** negative leg, Bridge 2 **ON** negative leg	-Vdc

4.3 Simulation for R Load

Without Filter:

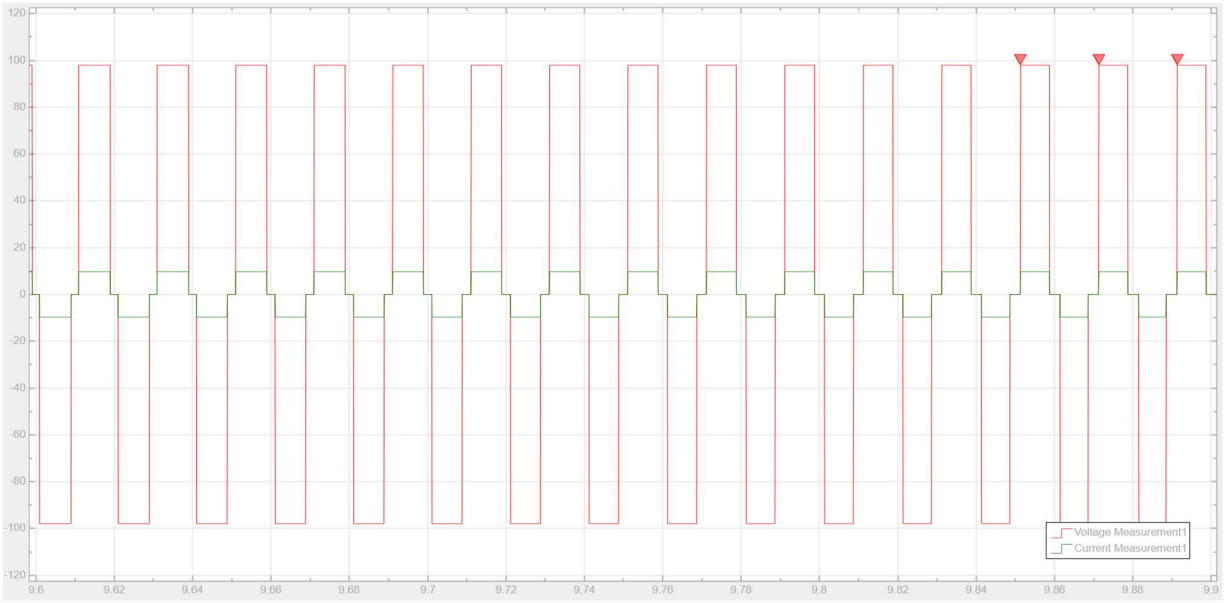

Fig.4.3.1 Output Voltage and curent waveforms when R_{load} = 10 Ω

With Filter:

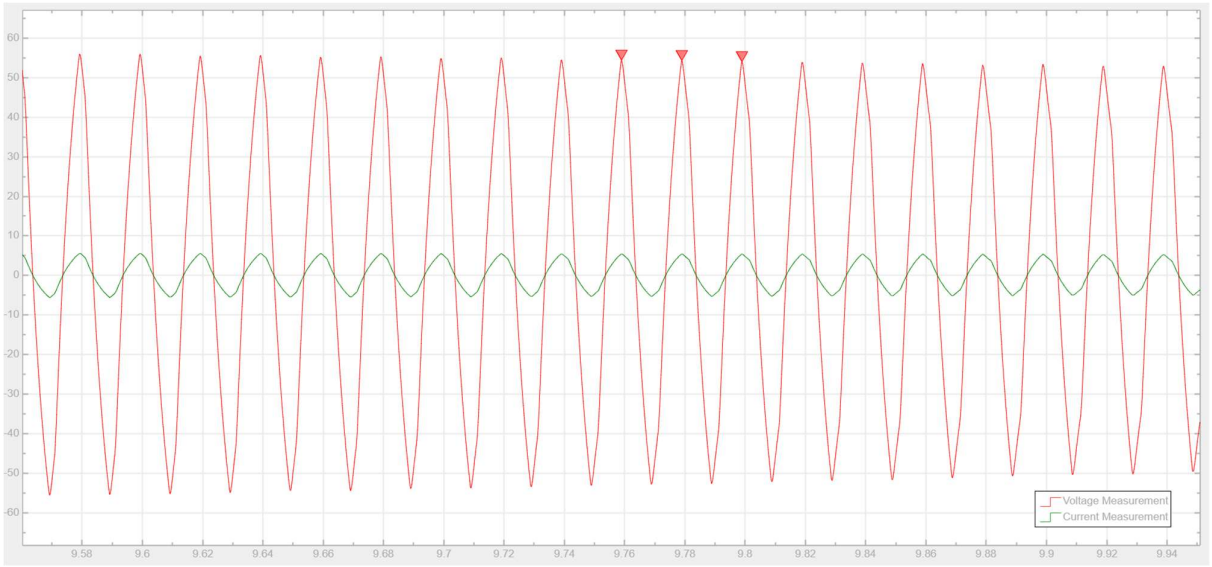

Fig.4.3.2 Output Voltage and Curent waveforms when R_{load} = 10 Ω

4.4 RMS and THD Analysis for 3-Level Inverter

R LOAD WITHOUT FILTER	
V_{rms}	81.44 V
I_{rms}	8.144 A
THD_V	0.3002
THD_I	0.3002
R_{load}	10 Ω

Table.4.4.1 Parameters of 3-Level Inverter without Filter

R LOAD WITH FILTER	
V_{rms}	34.05 V
I_{rms}	3.405 A
THD_V	0.04298
THD_I	0.04298
R_{load}	10 Ω

Table.4.4.2 Parameters of 3-Level Inverter with Filter

- **Filter Parameters:**
    1. **Inductance :** 70 mH
    2. **Capacitance :** 33 μF
- **DC Voltage :** 100 V

CASCADED H-BRIDGE FIVE-LEVEL INVERTER

5.1 Cascading of Two H-Bridges

The 5-level cascaded H-bridge inverter consists of:

- **Two H-bridge cells** per phase (total 4 switches per bridge = 8 switches for single-phase implementation)
- **Two independent DC sources:** V_{dc1} and V_{dc2} (equal magnitude for symmetric operation)
- **Output filter:** LC network with load resistance R
- **Modulation:** Sinusoidal Pulse Width Modulation (SPWM) with two carrier waves

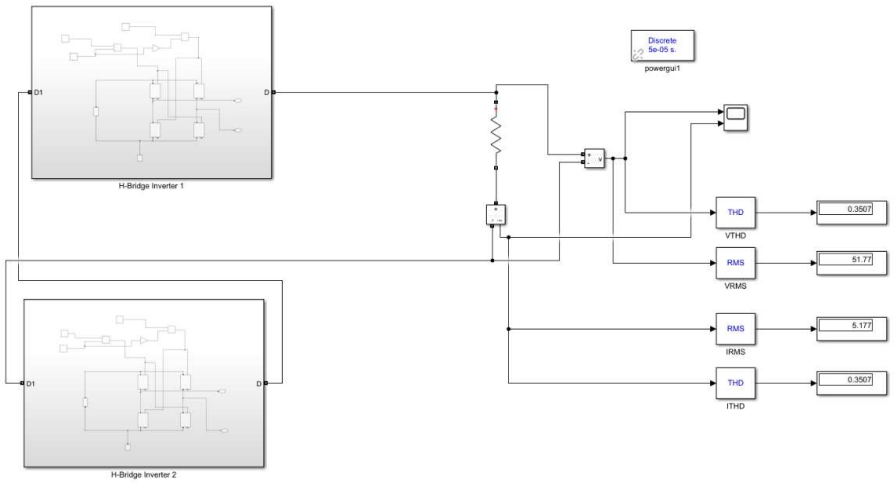

Fig.5.1.1 Circuit diagram for Rload without Filter (R_{load} = 10 Ω)

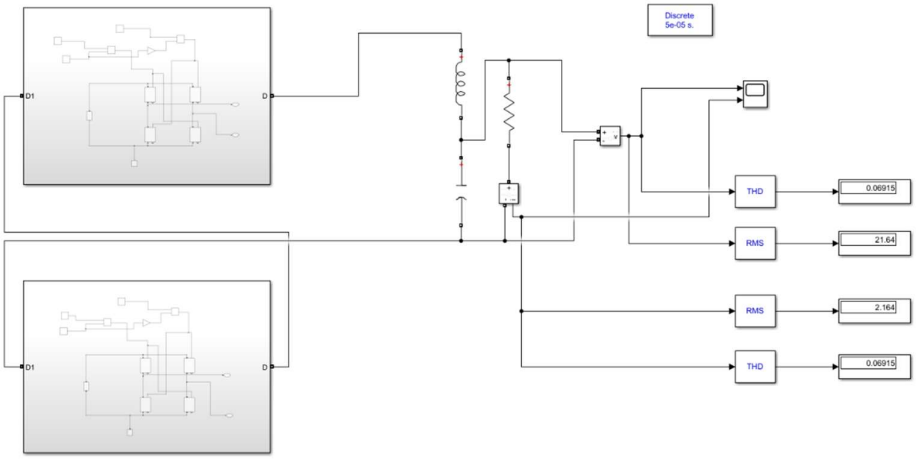

Fig.5.1.2 Circuit diagram for Rload with Filter (R_{load} = 10 Ω)

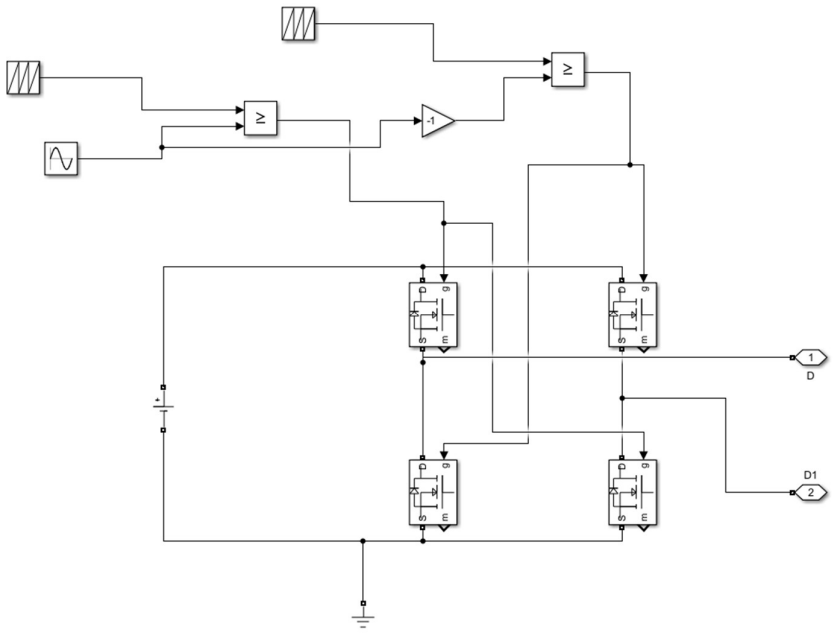

Fig.5.1.3 Circuit diagram for H-bridge Inverter

5.2 Five-Level Output Voltage Generation

Each H-bridge can generate three voltage levels: $-V_{dc}, 0, +V_{dc}$

For cascaded configuration with two bridges, the output voltage levels are:

Level	H-Bridge 1	H-Bridge 2	Output Voltage
1	+Vdc	+Vdc	+2Vdc
2	+Vdc	0	+Vdc
3	0	0 or ±Vdc	0
4	-Vdc	0	-Vdc
5	-Vdc	-Vdc	-2Vdc

5.3 Simulation for R Load

Without Filter:

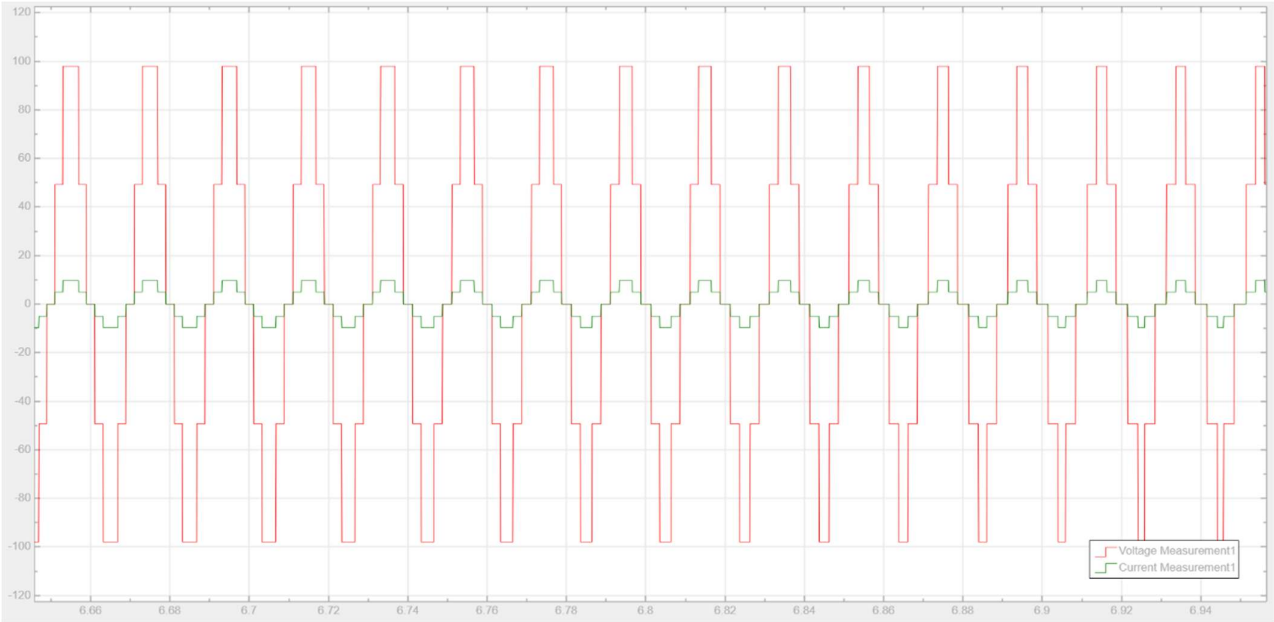

Fig.5.3.1 Output Voltage and curent waveforms when R_{load} = 10 Ω

With Filter:

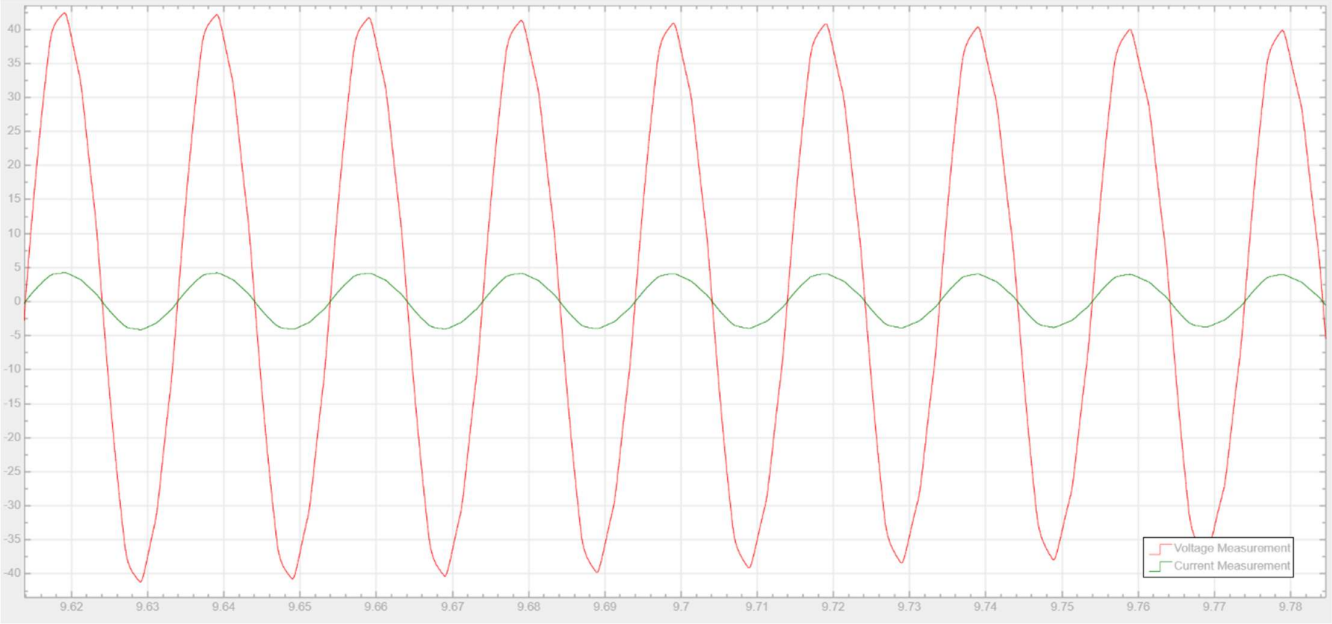

Fig.5.3.2 Output Voltage and curent waveforms when R_{load} = 10 Ω

5.4 RMS and THD Analysis for 5-Level Inverter

R LOAD WITHOUT FILTER	
V_{rms}	51.77 V
I_{rms}	5.177 A
THD_V	0.3507
THD_I	0.3507
R_{load}	10 Ω

Table.5.4.1 Parameters of 5-Level Inverter without Filter

R LOAD WITH FILTER	
V_{rms}	21.64 V
I_{rms}	2.164 A
THD_V	0.06915
THD_I	0.06915
R_{load}	10 Ω

Table.5.4.2 Parameters of 5-Level Inverter with Filter

- **Filter Parameters:**
    1. **Inductance :** 70 mH
    2. **Capacitance :** 33 μF
- **DC Voltage :** 100 V

RESULTS AND DISCUSSION

6.1 Performance Comparison: Three-Level vs Five-Level Inverter

- For R = 10 Ω without filter, the three-level inverter gives higher V_{rms} (81.44 V) and I_{rms} (8.144 A) than the five-level inverter (51.77 V, 5.177 A).
- With the LC filters connected, the three-level inverter still maintains a higher V_{rms} (34.05 V) than the five-level inverter (21.64 V).
- Under the chosen DC voltages and modulation indices, the three-level topology therefore utilises the DC link more effectively and delivers more real power to the load.

6.2 Effect of Cascading on THD

- For operation without filter, **the three-level inverter** has **THDv = THDi = 0.3002 (≈ 30.02%),** while **the five-level inverter** has **THDv = THDi = 0.3507 (≈ 35.07%).**
- The extra voltage levels in the five-level inverter do not automatically reduce THD; in this setup the unfiltered five-level output is slightly more distorted than the three-level output.
- Cascading improves waveform resolution, but proper selection of DC voltage and modulation strategy is still required to obtain a meaningful THD reduction.

6.3 Impact of LC Filter on Harmonic Reduction

- For both 3-level and 5-level inverters, the LC filter drastically reduces THD from **roughly 30–35%** to **below 10%**, confirming that passive filtering is essential for meeting power-quality requirements with multilevel H-bridge inverters.
- The 3-level inverter with filter achieves the lowest THD **(≈ 4.3%),** while the 5-level inverter with filter settles around **≈ 6.9%**.
- In both cases, the filter causes a substantial reduction in RMS output voltage, indicating that the filter design trades fundamental-voltage utilization for improved harmonic performance.

6.4 Observations and Inferences

- Both three-level and five-level inverters produce high **THD (≈ 30–35%)** in the unfiltered case and are not suitable for power-quality-sensitive loads without filtering.
- After filtering, the three-level inverter achieves lower **THD (≈ 4.3%)** and higher Vrms than the filtered five-level inverter **(≈ 6.9% THD)**, giving a better balance between voltage magnitude and distortion.
- The measured data show that practical performance depends more on DC link selection, SPWM settings and LC design than on the nominal number of levels alone.

CONCLUSION & REFERENCES

7.1 Conclusion

- The project successfully implemented and analysed three-level and five-level cascaded H-bridge inverters feeding a 10 Ω resistive load.
- LC output filtering was found to be essential, reducing THD from about **30–35%** to **below 10%** and making the inverter outputs suitable for many AC applications.
- For the tested DC voltages and filter parameters, the three-level inverter provided higher RMS output voltage and lower final THD than the five-level inverter, and thus offered the better overall performance in this study.

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