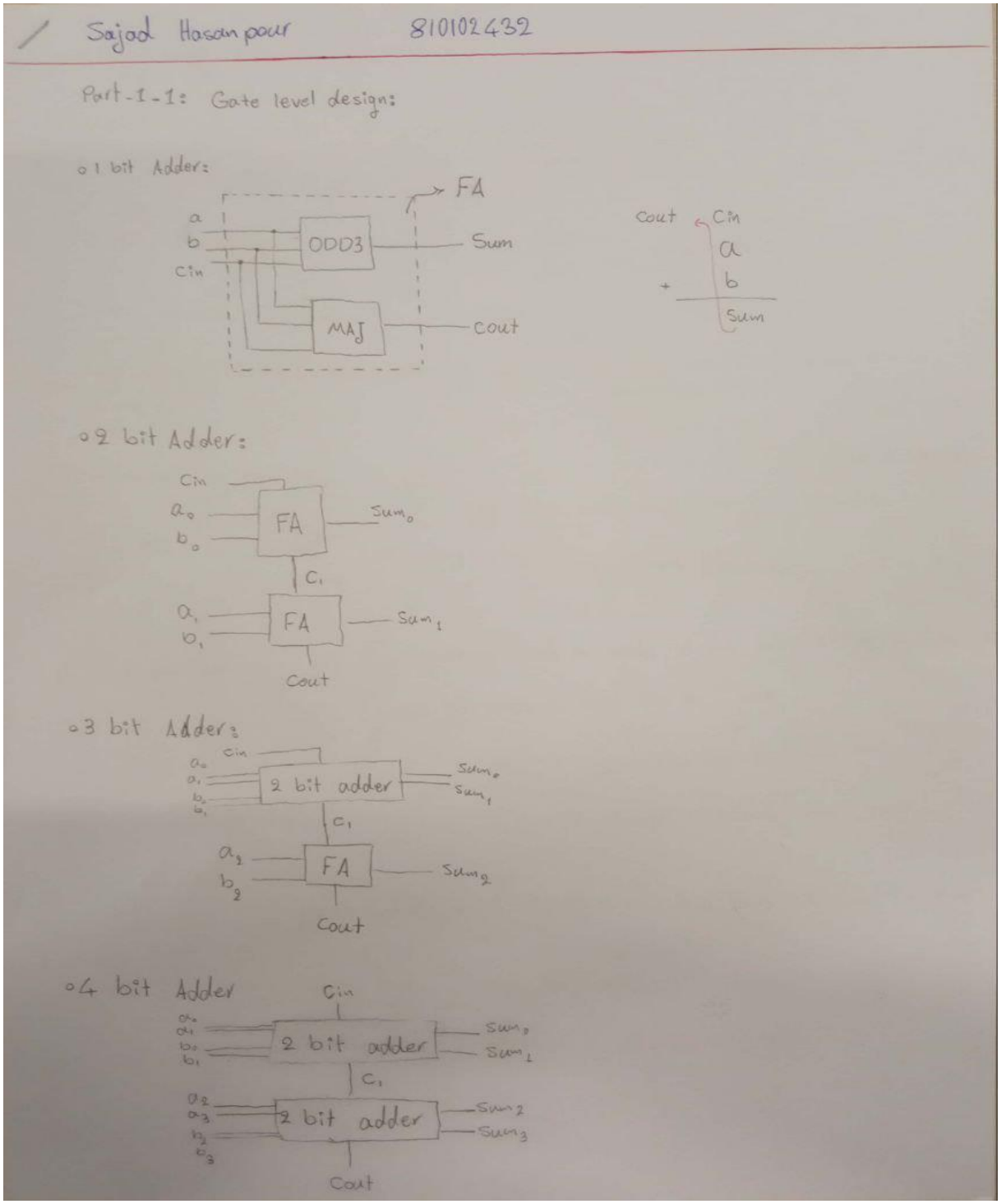
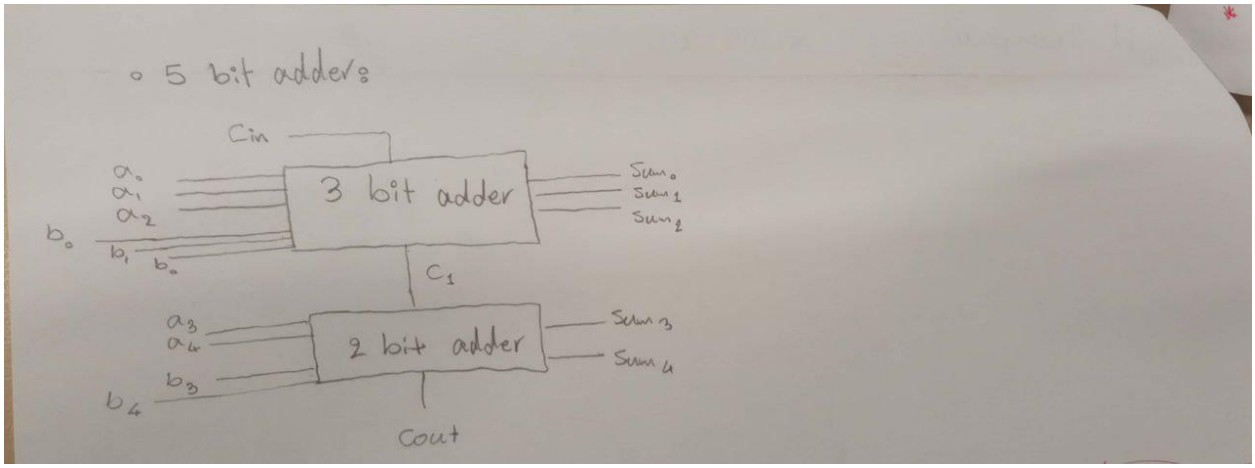
Part1:

1. **Gate Level Design**:





2. **System Verilog Modules**:

```
module MAJ(input  a,b,c,output w);
    assign #(35,36) w=((b&c) | (a&c) | (a&b));
endmodule

module ODD3(input a,b,c,output w);
    assign #(28,27) w= a^b^c;
endmodule
```

```
module fulladder(input a,b,cin,output sum,cout);
    Odd3 odd(a,b,cin,sum);
    Maj3 maj(a,b,cin,cout);
endmodule
```

```
module two_bit_adder(input [1:0]a,b,input cin,output [1:0]sum,output cout);
    wire c1;
    fulladder F1(a[0],b[0],cin,sum[0],c1);
    fulladder F2(a[1],b[1],c1,sum[1],cout);
endmodule
```

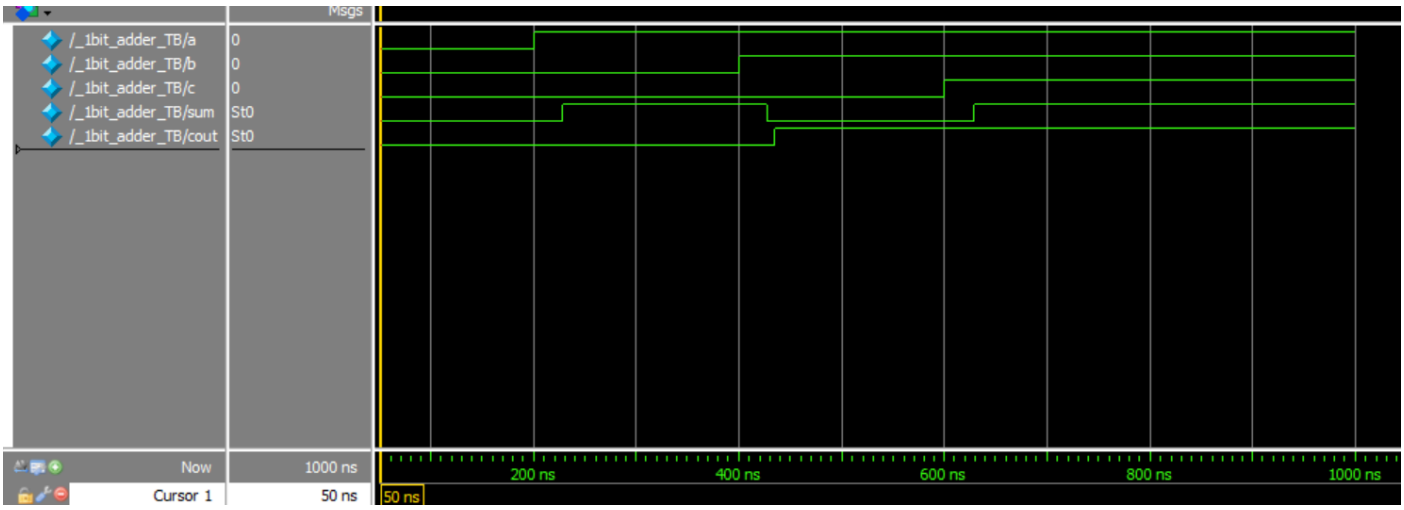
```
module three_bit_adder(input [2:0]a,b,input cin, output [2:0]sum,output cout);
    wire c1;
    two_bit_adder T1(a[1:0],b[1:0],cin,sum[1:0],c1);
    fulladder F1(a[2],b[2],c1,sum[2],cout);
endmodule
```

```
module four_bit_adder(input [3:0]a,b,input cin, output [3:0]sum,output cout);
    wire c1;
    two_bit_adder T1(a[1:0],b[1:0],cin,sum[1:0],c1);
    two_bit_adder T2(a[3:2],b[3:2],c1,sum[3:2],cout);
endmodule
```

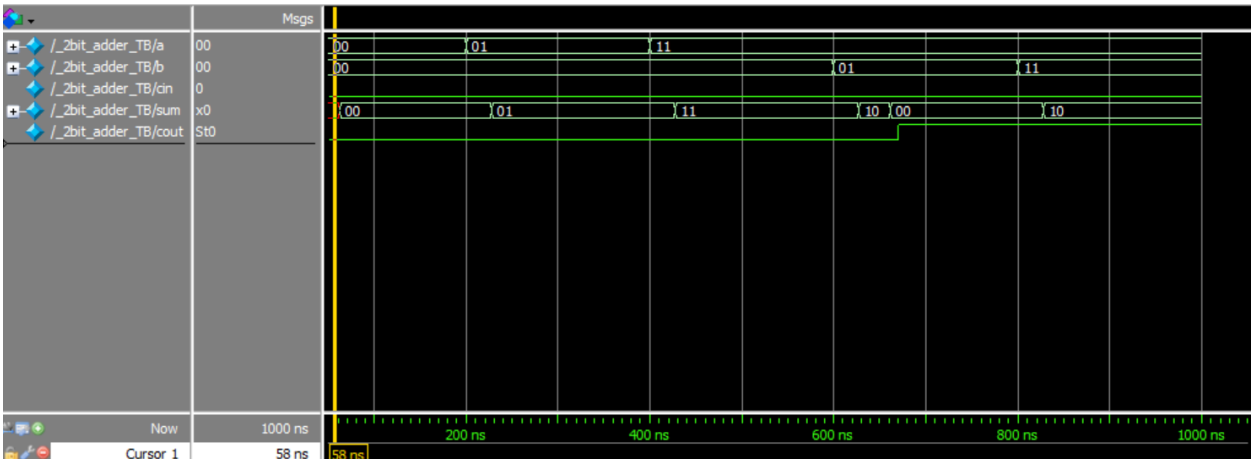
```
module five_bit_adder(input [4:0]a,b,input cin, output [4:0]sum,output cout);
    wire c1;
    three_bit_adder T1(a[2:0],b[2:0],cin,sum[2:0],c1);
    two_bit_adder T2(a[4:3],b[4:3],c1,sum[4:3],cout);
endmodule
```

3. Simulation and Waveforms:

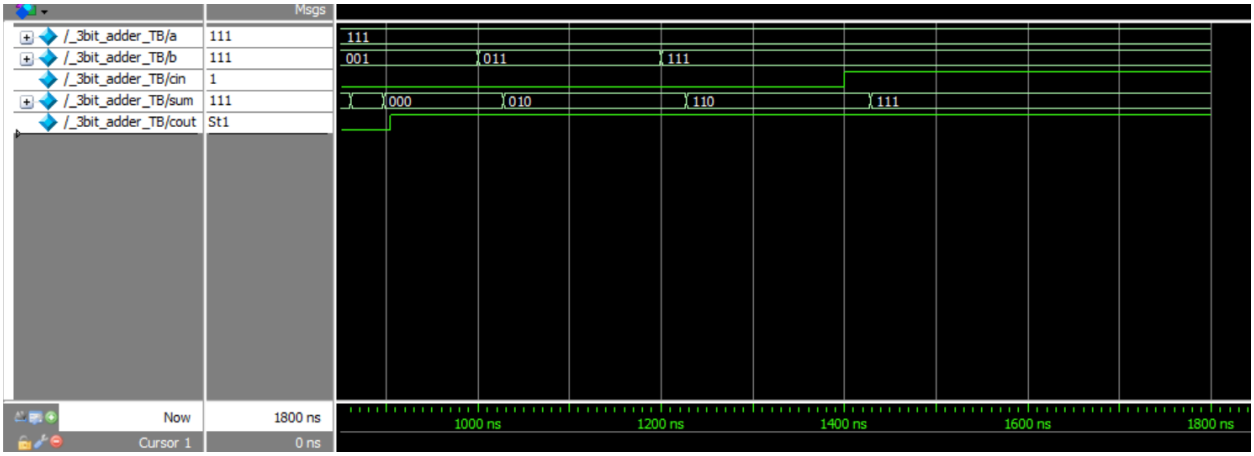
1-Full adder:



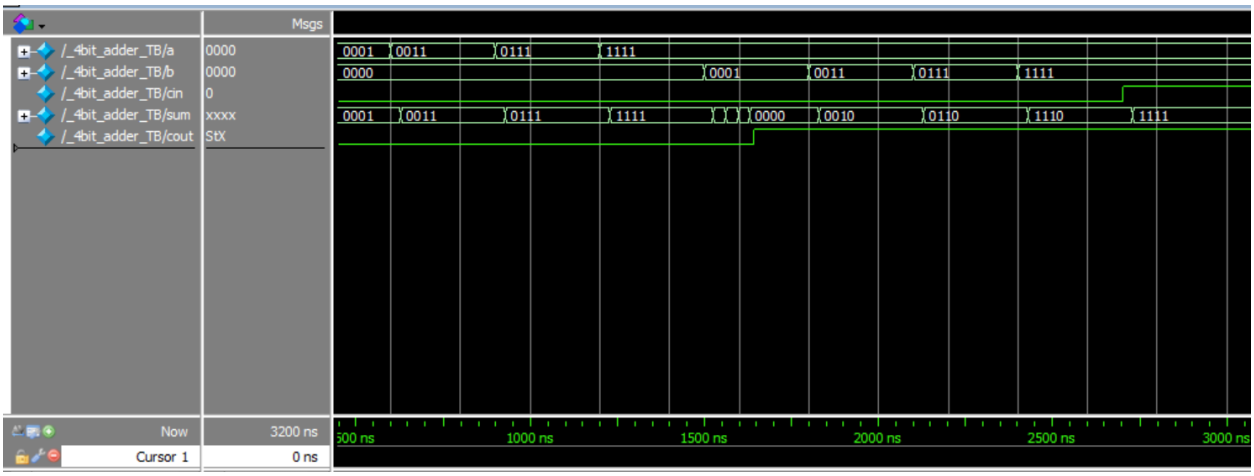
2-Two bit adder:



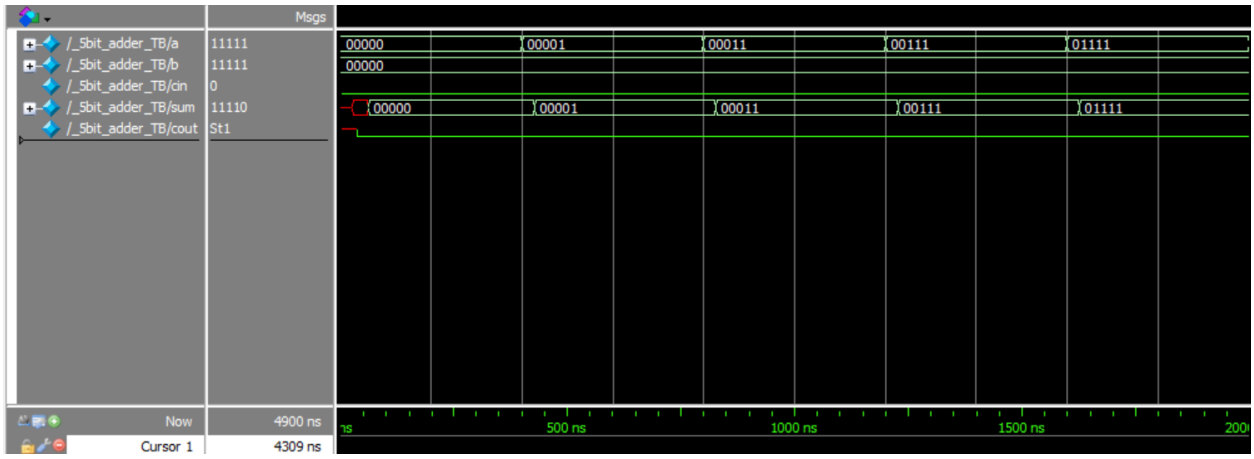
3- Three bit adder:

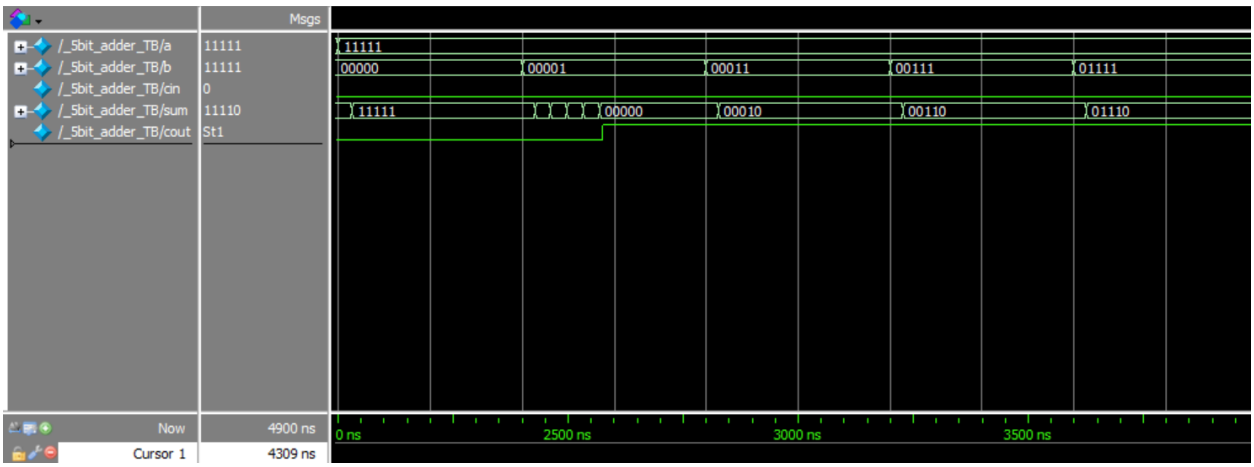


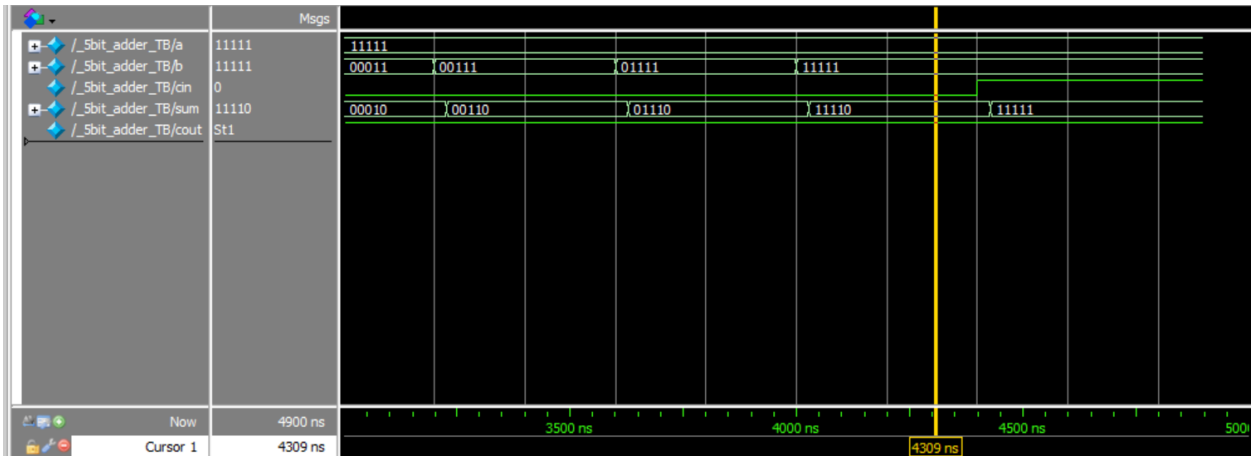
4- Four bit adder:



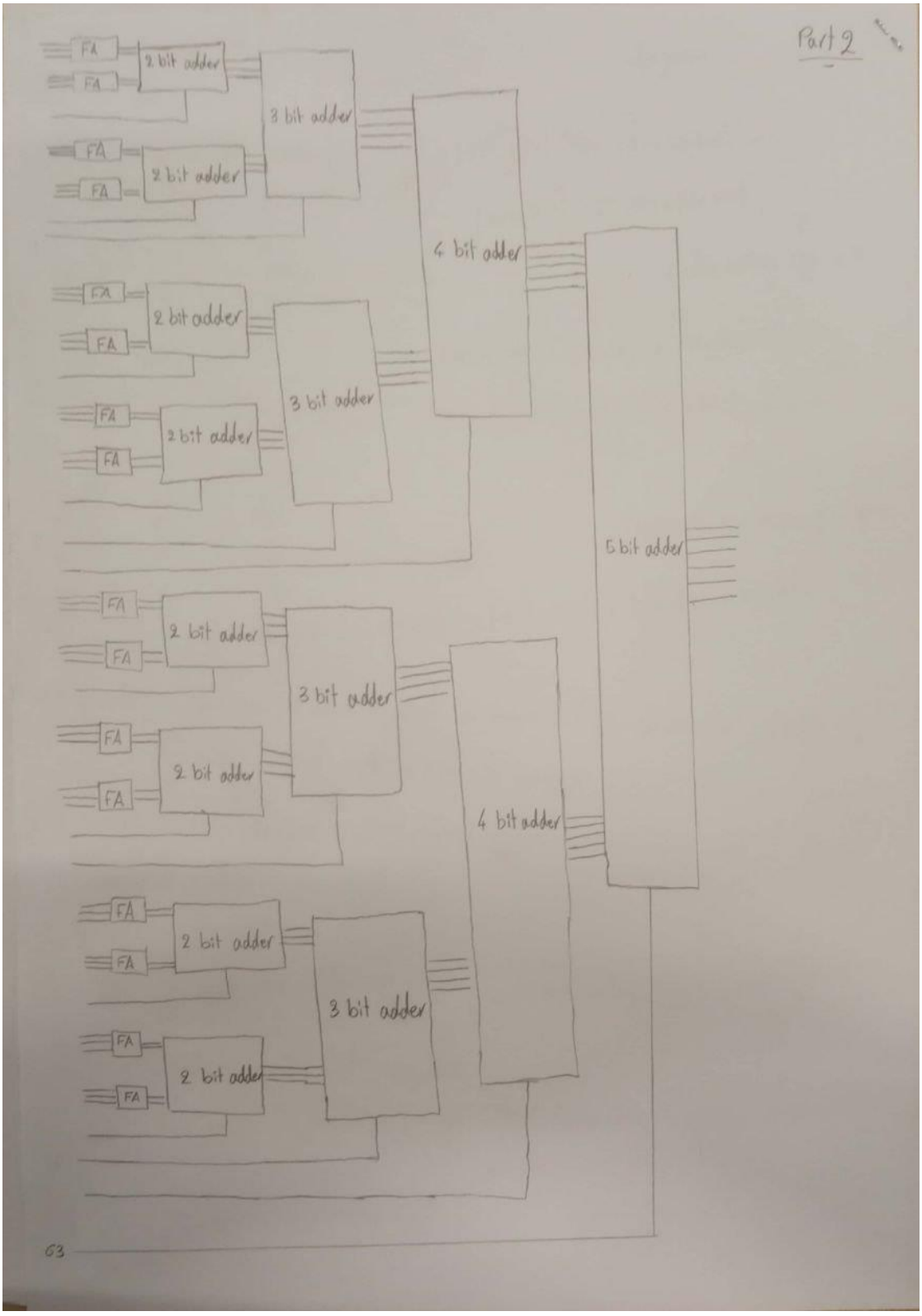
5- Five bit adder:



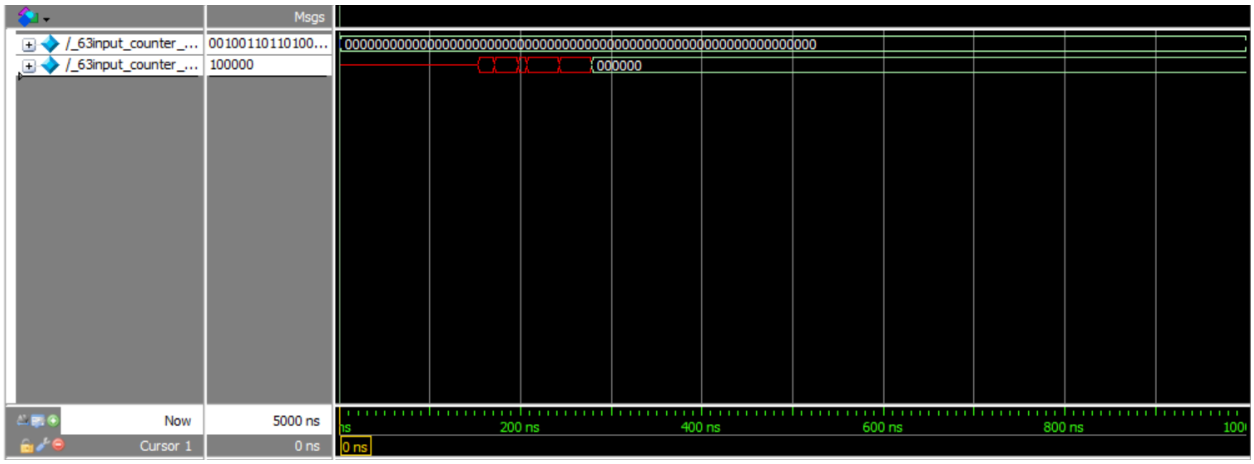


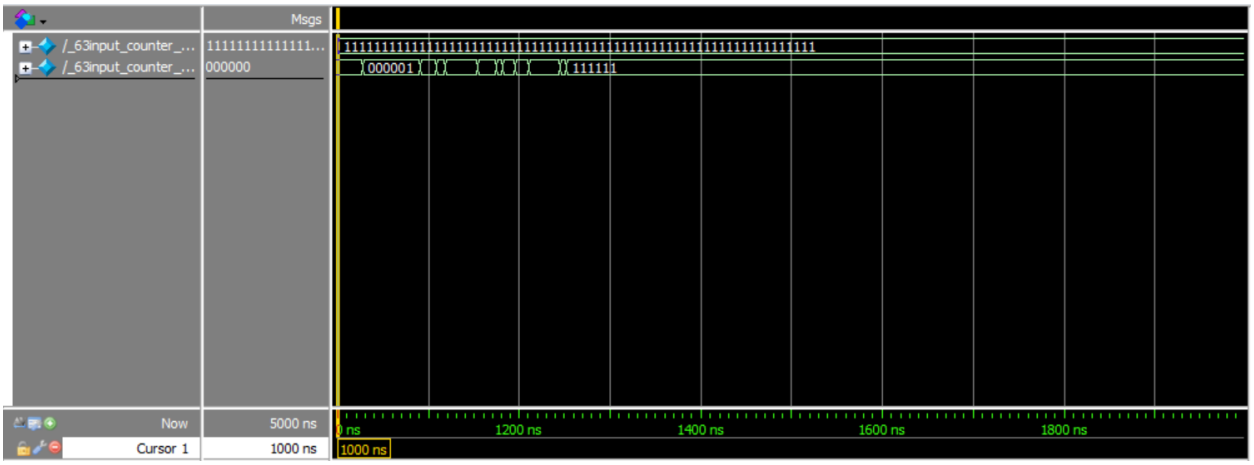


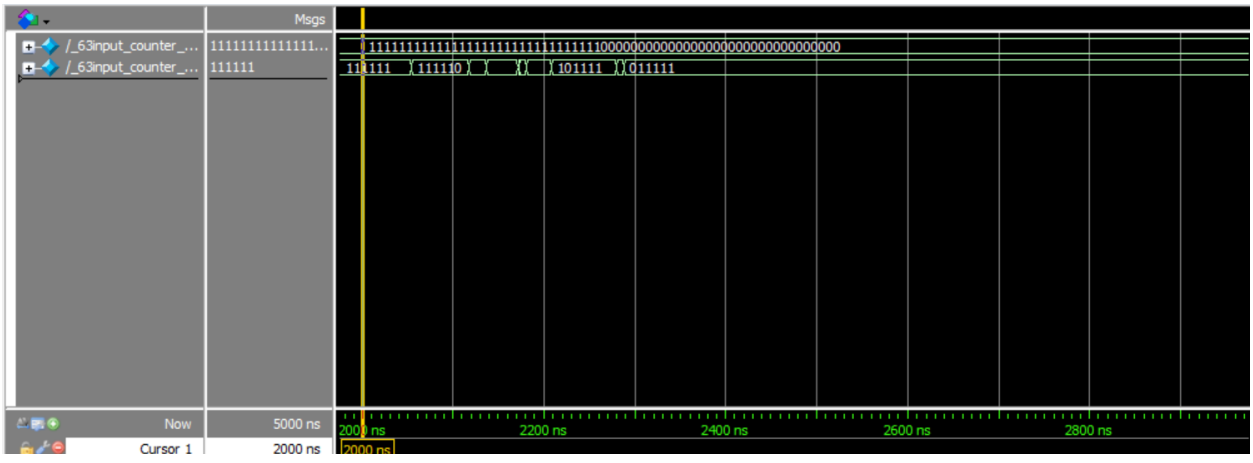
Part2:

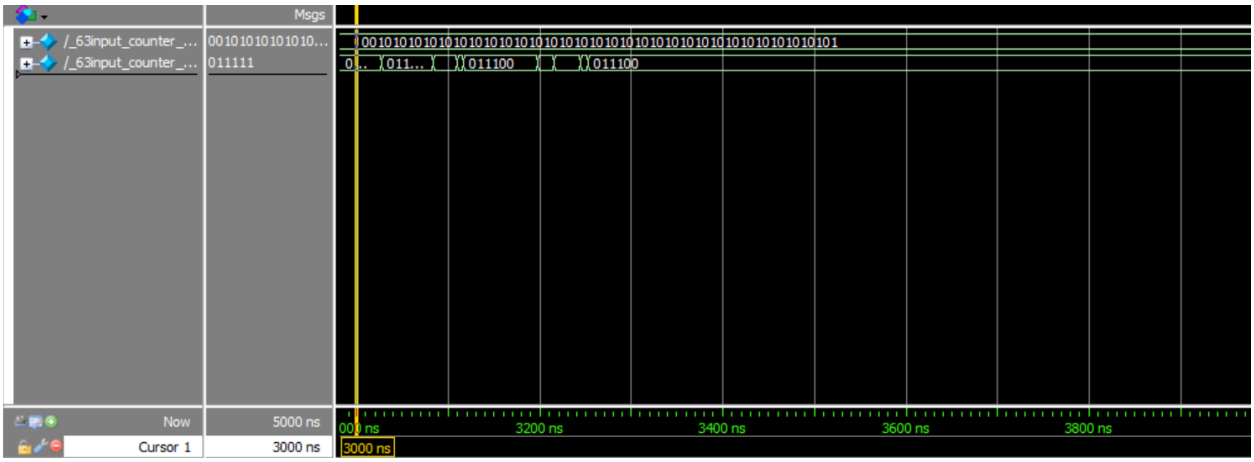


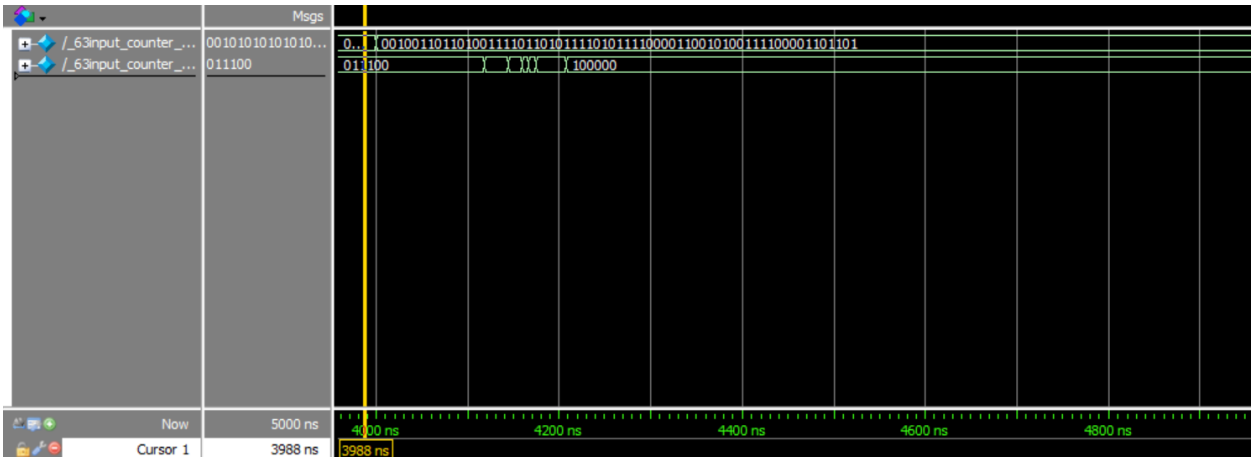
Part2-waveforms:



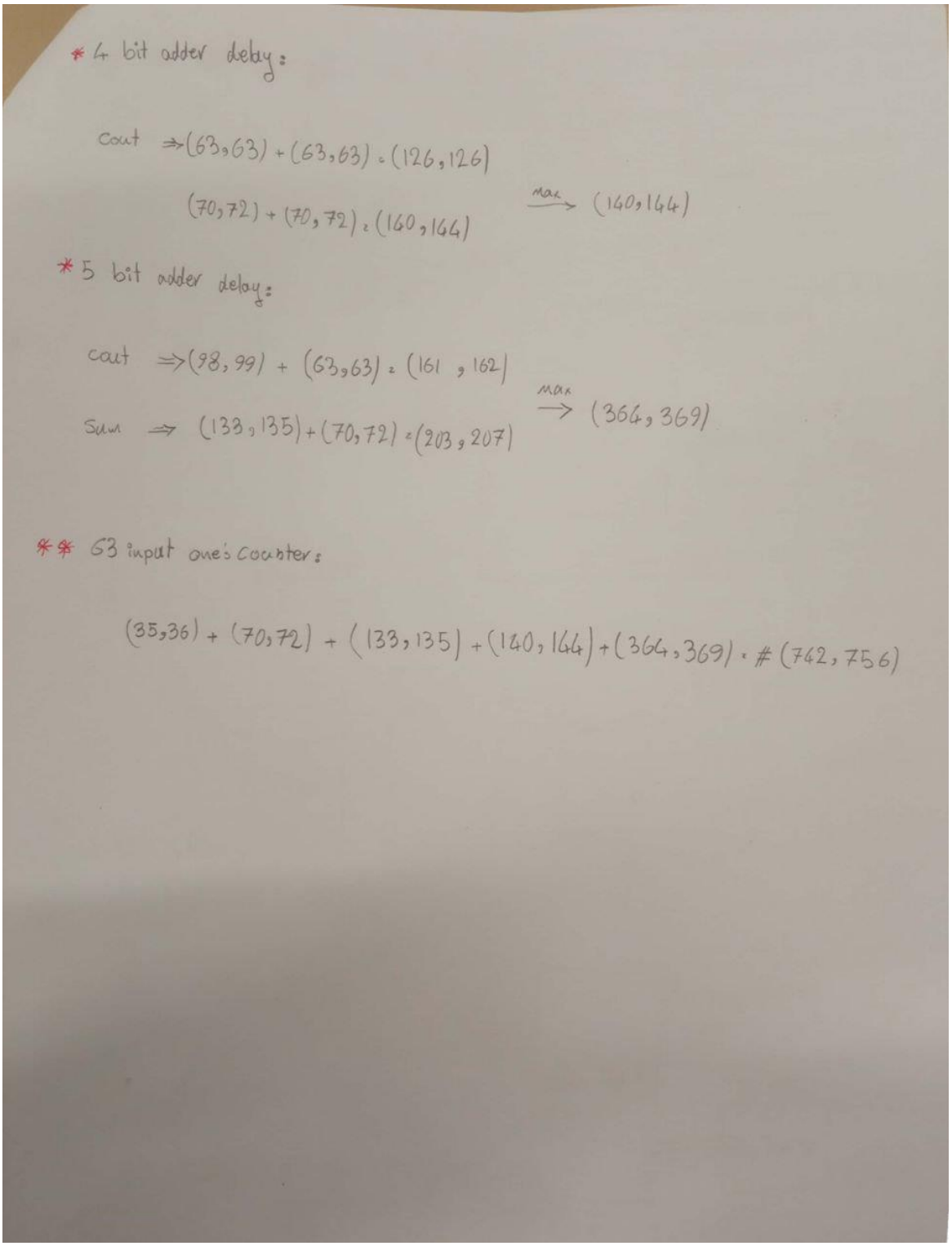


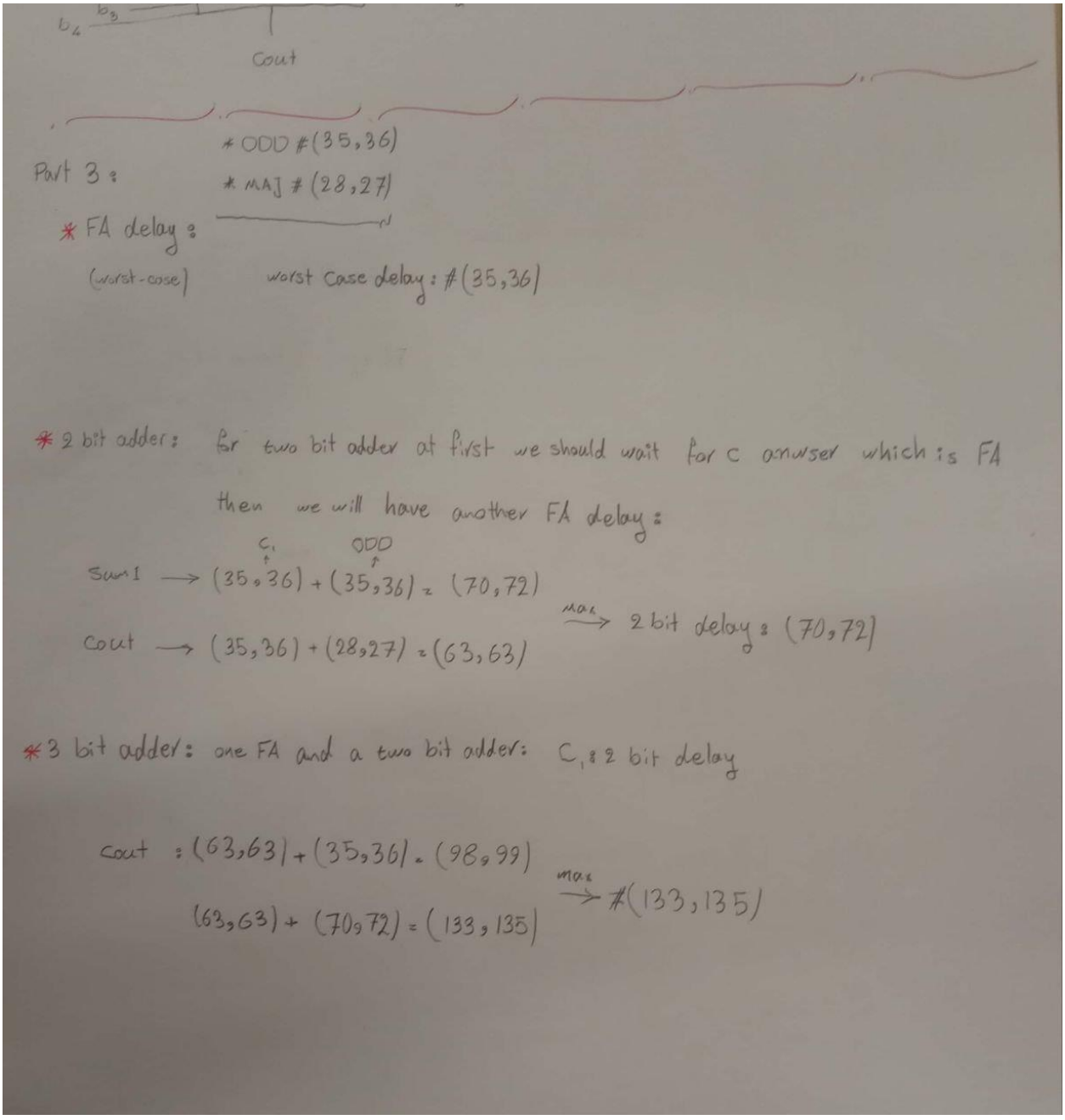



Msgs
/_63input_counter_...
/_63input_counter_...
Now
5000 ns
Cursor 1
3000 ns
3200 ns
3400 ns
3600 ns
3800 ns


Msgs
/_63input_counter_...
/_63input_counter_...
Now
5000 ns
Cursor 1
3988 ns
4000 ns
4200 ns
4400 ns
4600 ns
4800 ns

Part3:


* 4 bit adder delay:
cout ⇒(63,63) + (63,63) = (126,126)
(70,72) + (70,72) = (160,164)
max → (140,144)
* 5 bit adder delay:
cout ⇒(98,99) + (63,63) = (161, 162)
Sum ⇒ (133,135) + (70,72) = (203,207)
max → (364,369)
** 63 input one's counter:
(35,36) + (70,72) + (133,135) + (140,144) + (364,369) = # (742,756)



* ODD $\#(35,36)$
* MAJ $\#(28,27)$

Part 3 :

* FA delay :

(worst-case) worst case delay : $\#(35,36)$

* 2 bit adder : for two bit adder at first we should wait for c answer which is FA then we will have another FA delay :

C_1 ODD

Sum1 $\longrightarrow$ $(35,36) + (35,36) = (70,72)$

Cout $\longrightarrow$ $(35,36) + (28,27) = (63,63)$

$\xrightarrow{max}$ 2 bit delay : $(70,72)$

* 3 bit adder : one FA and a two bit adder : C_1 : 2 bit delay

Cout : $(63,63) + (35,36) = (98,99)$

$(63,63) + (70,72) = (133,135)$

$\xrightarrow{max}$ $\#(133,135)$