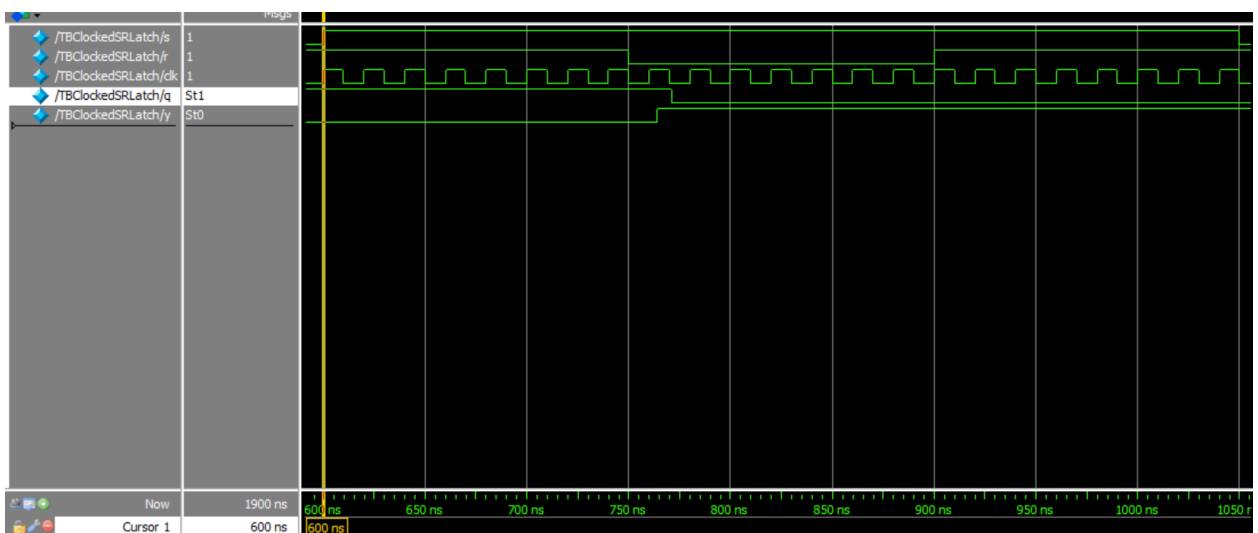
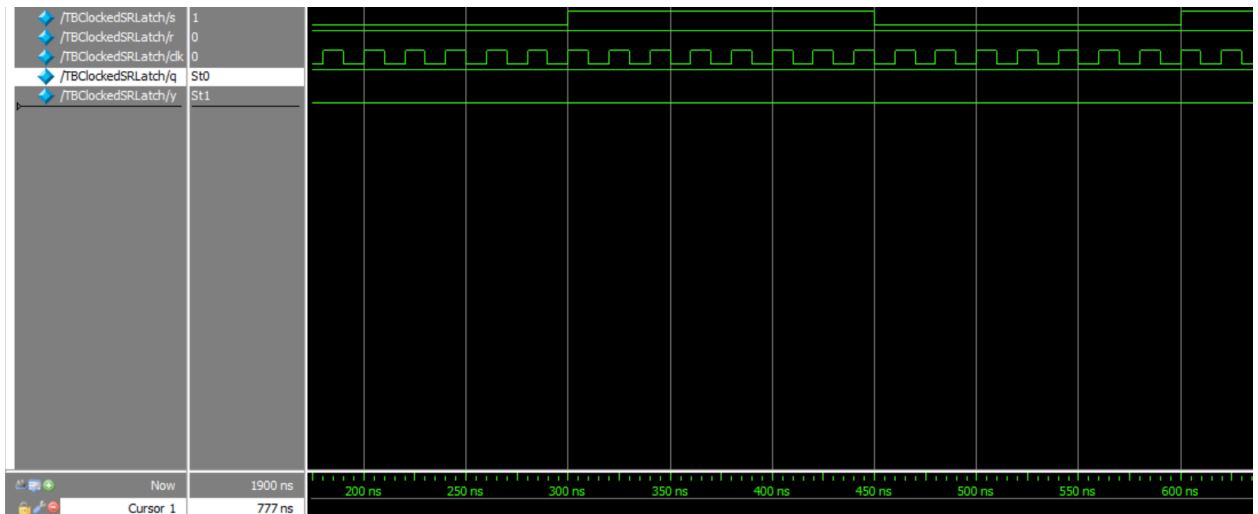


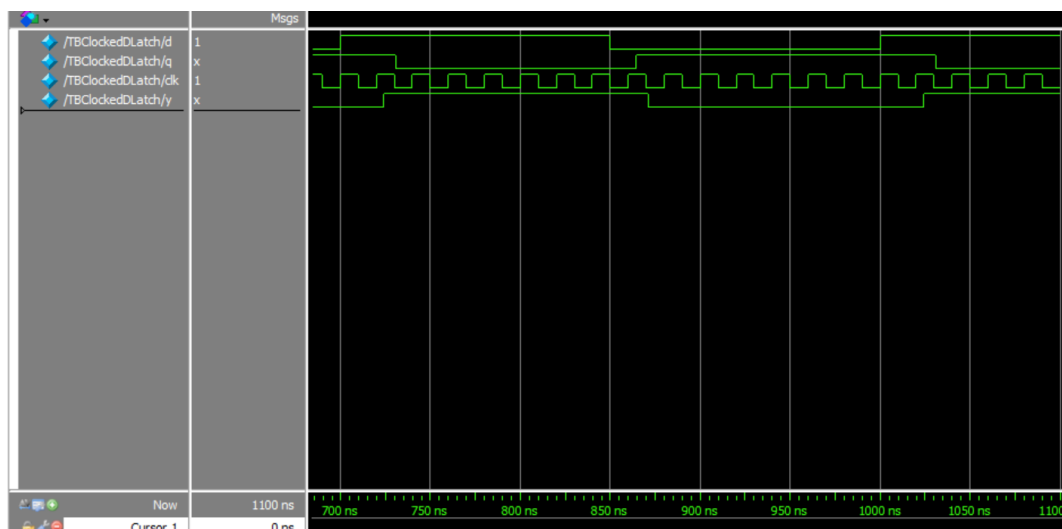
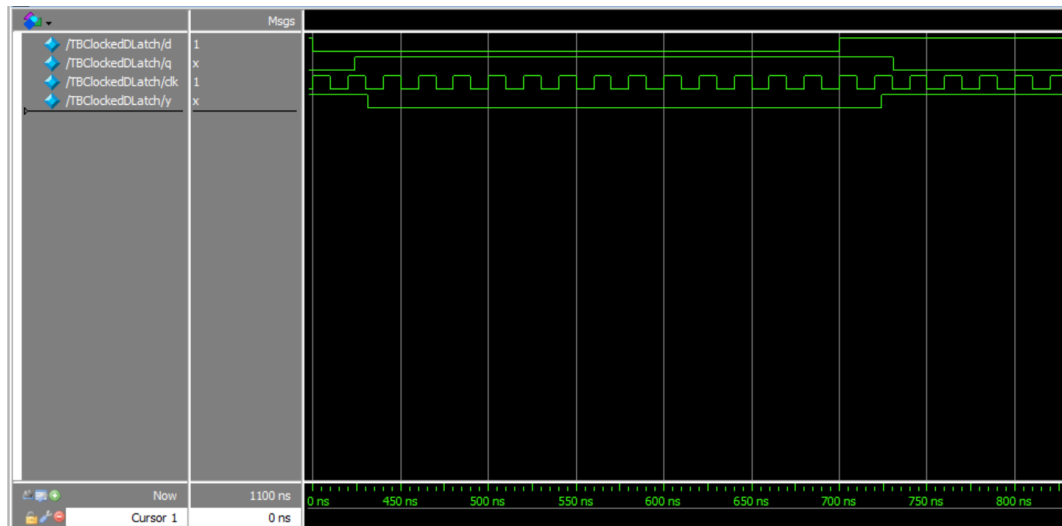
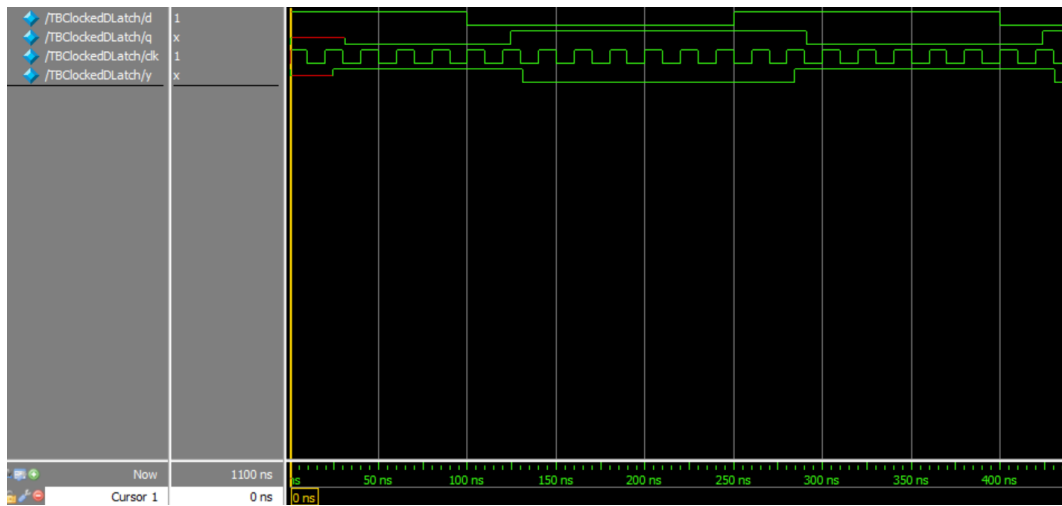
Q2:

Wave form:

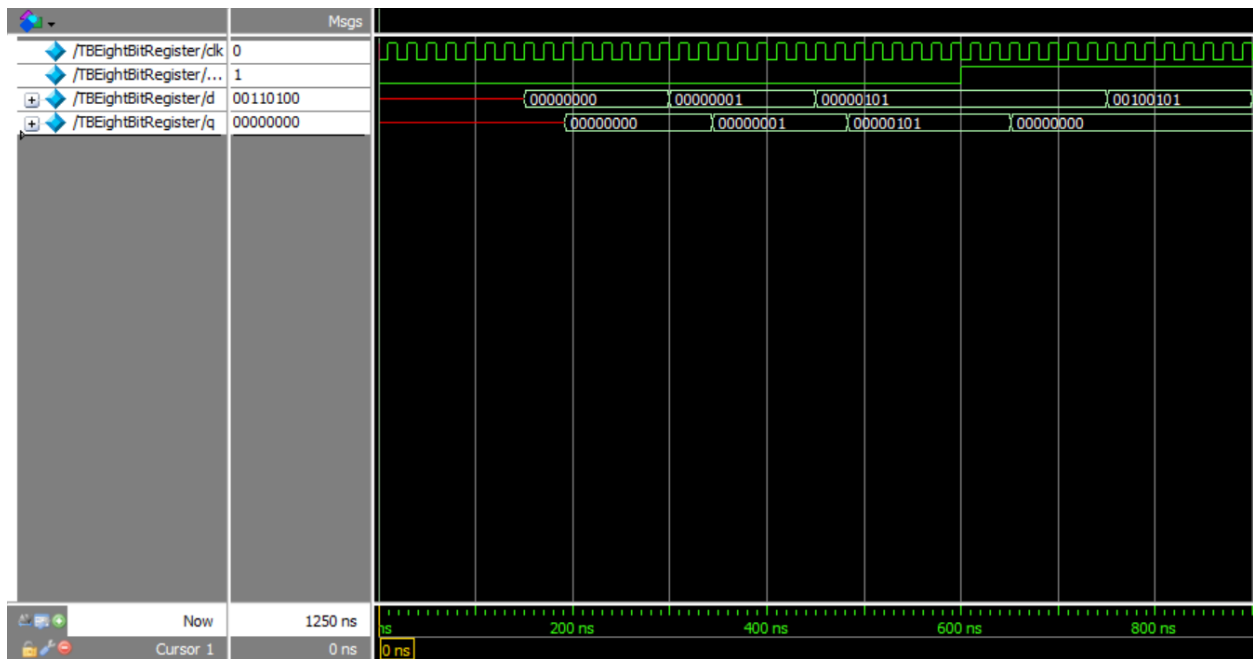


Q4:

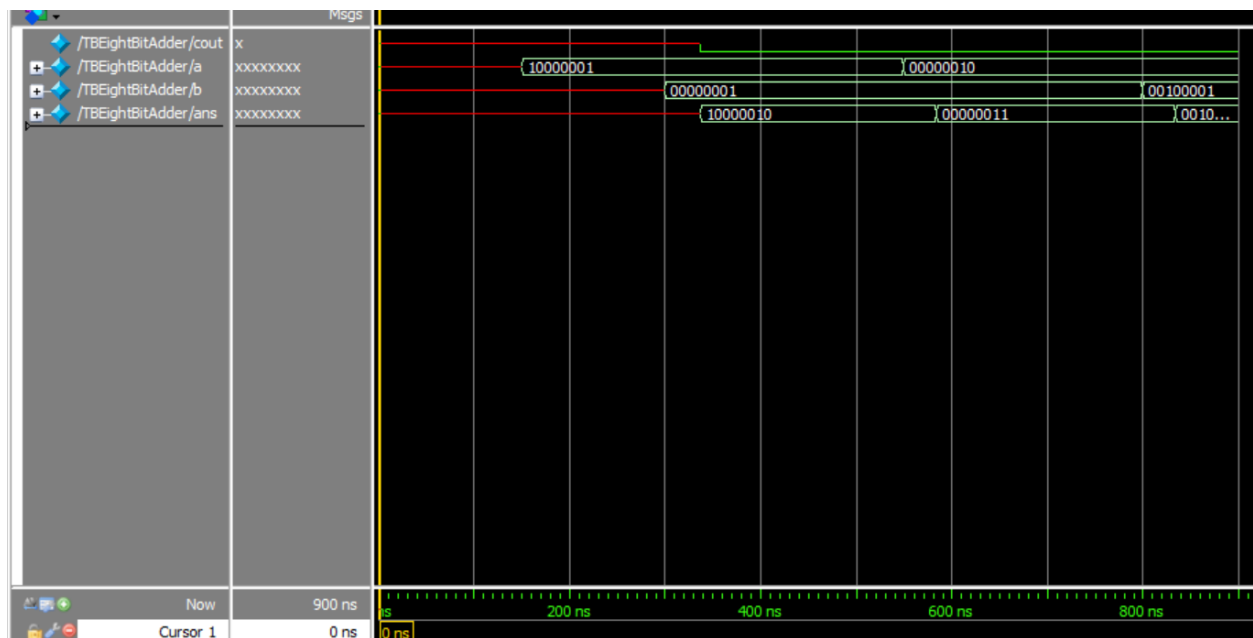
Wave form:



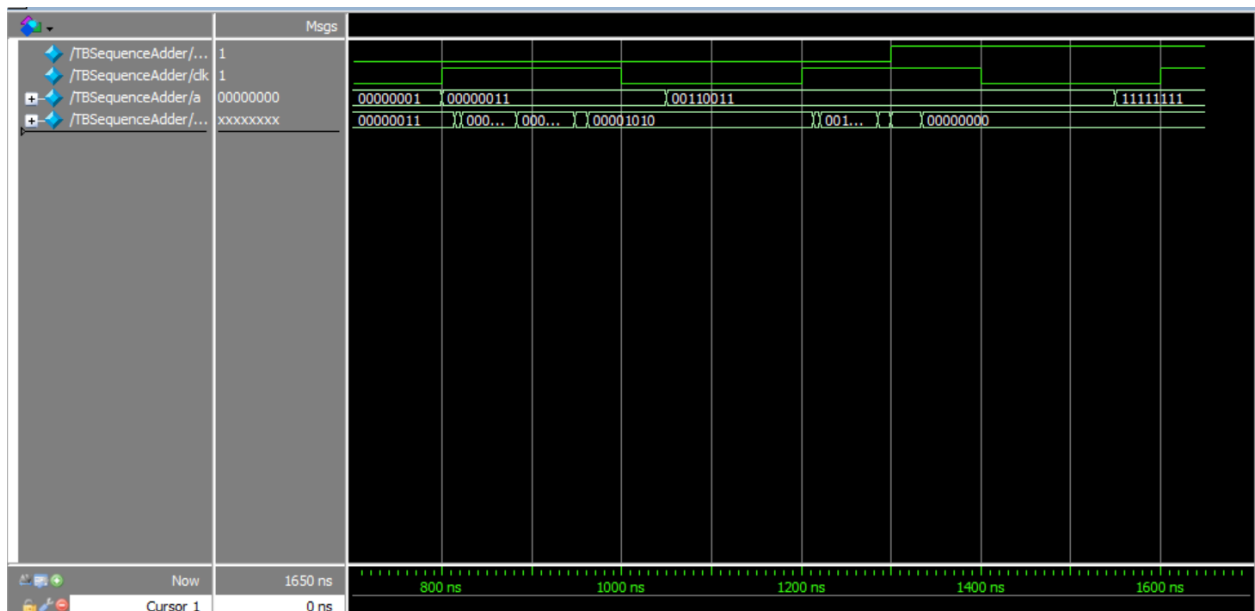
Q5:



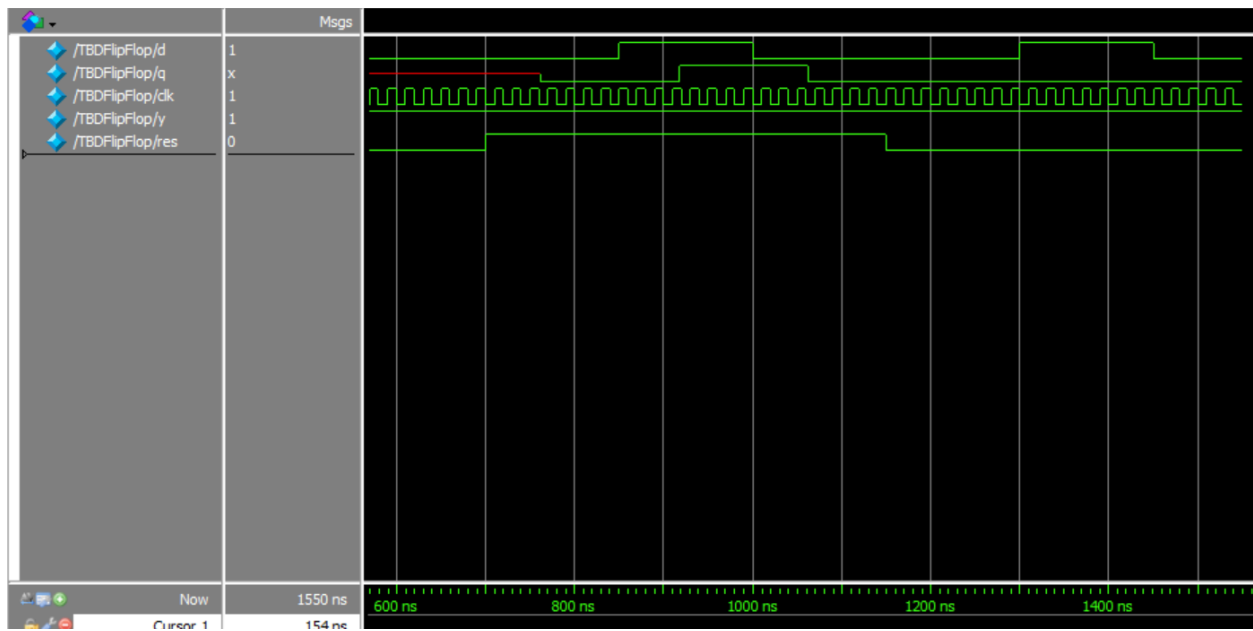
Q6:



The screenshot displays a logic analyzer interface. On the left, a message trace shows four messages from the component `/TBSequenceAdder/...`. The first two messages have a value of `1`, the third has `00000000`, and the fourth has `xxxxxxx`. The right side of the image shows a timing diagram for a signal. The signal is high (represented by a green bar) for the first two messages and low (represented by a black bar) for the last two. The signal is labeled with values like `00000000`, `00000001`, and `00000011`. The timing diagram includes a scale bar at the bottom indicating time intervals of 200 ns, 400 ns, 600 ns, 800 ns, and 1000 ns. The cursor is positioned at 0 ns.



Q8:



Q9:

