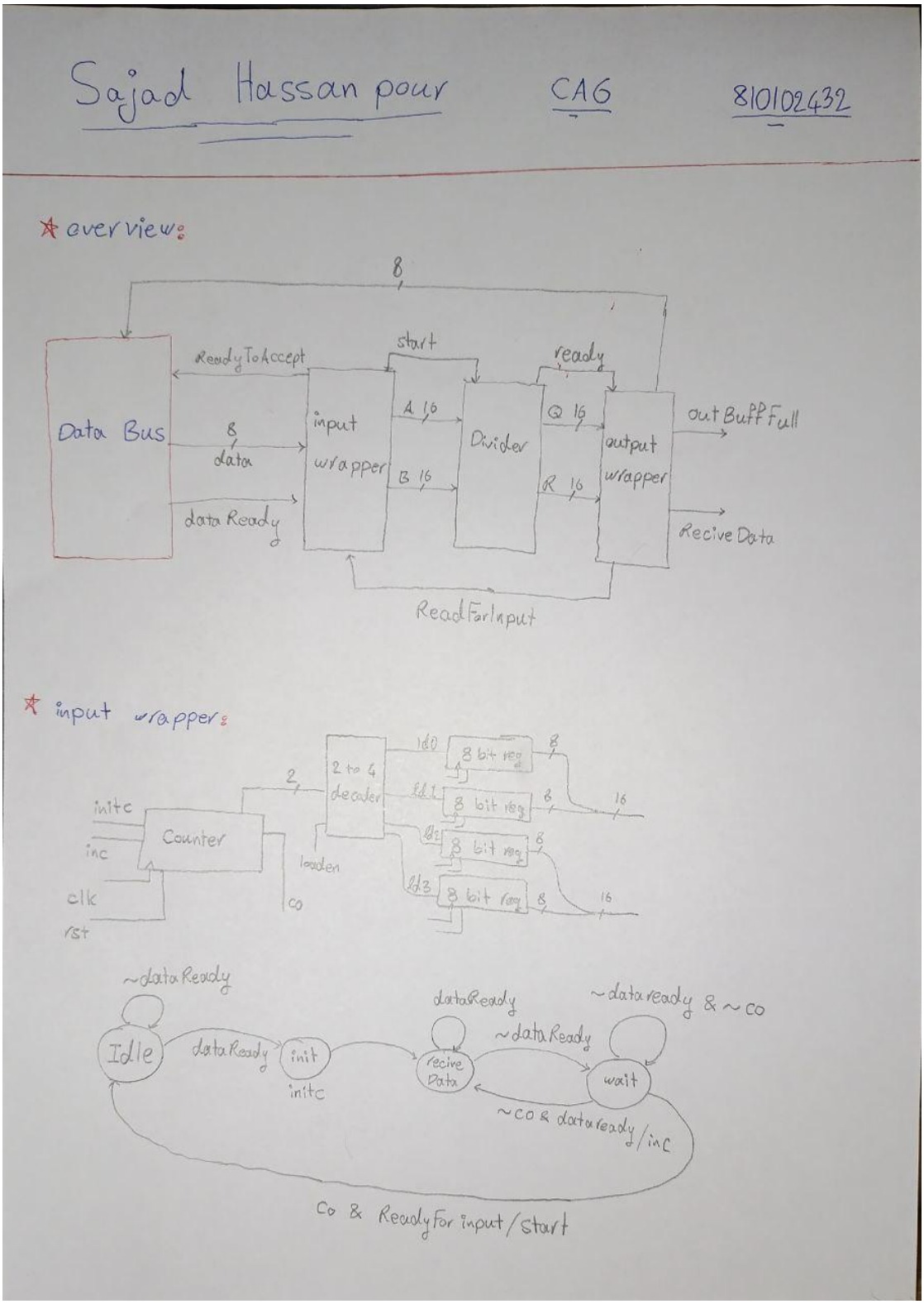
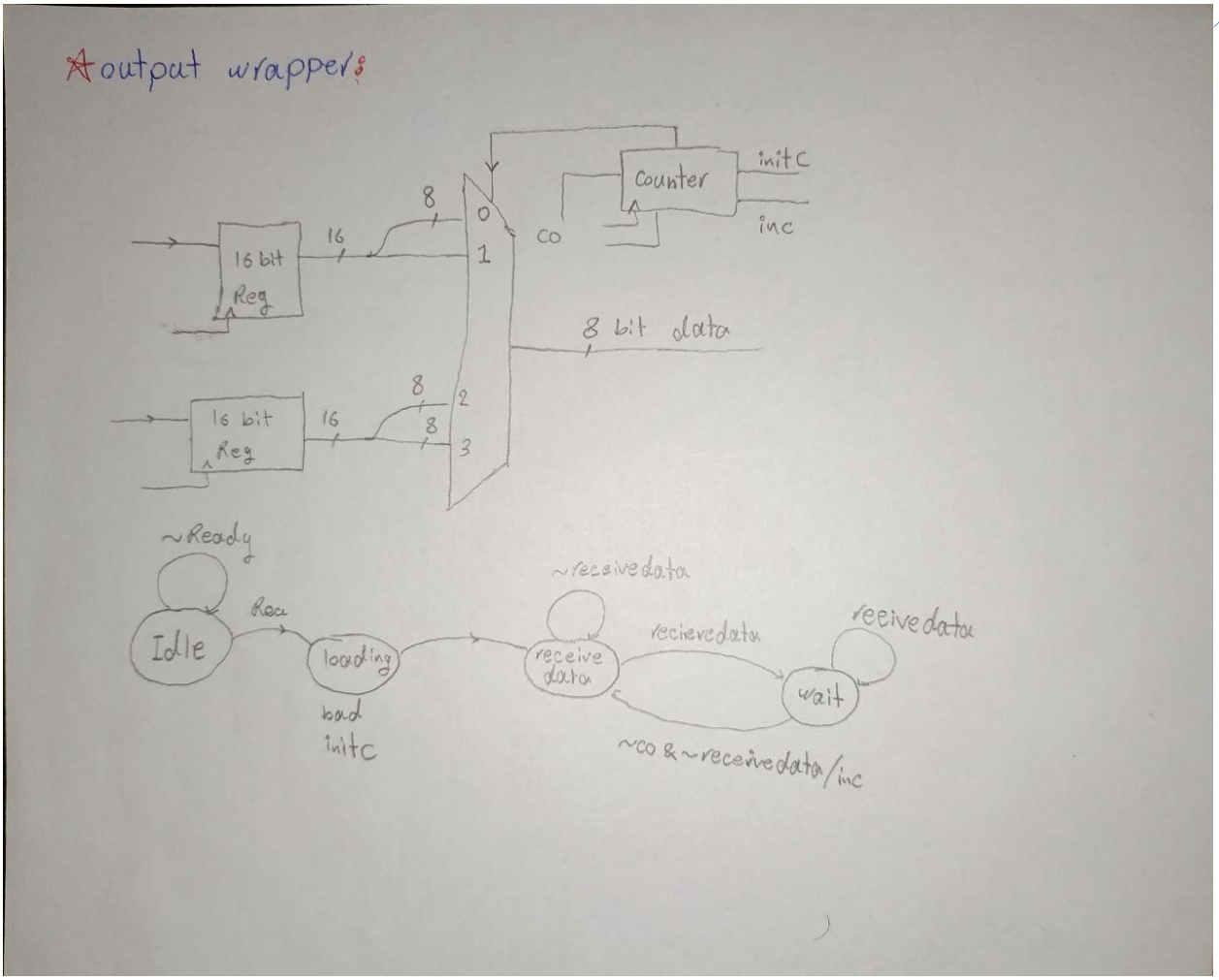
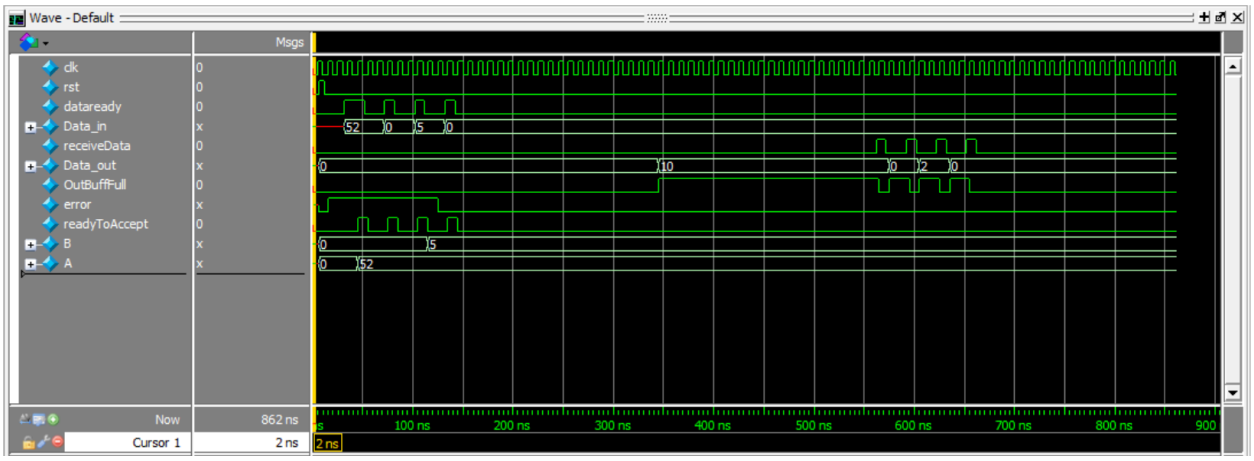
Data paths & Controller:

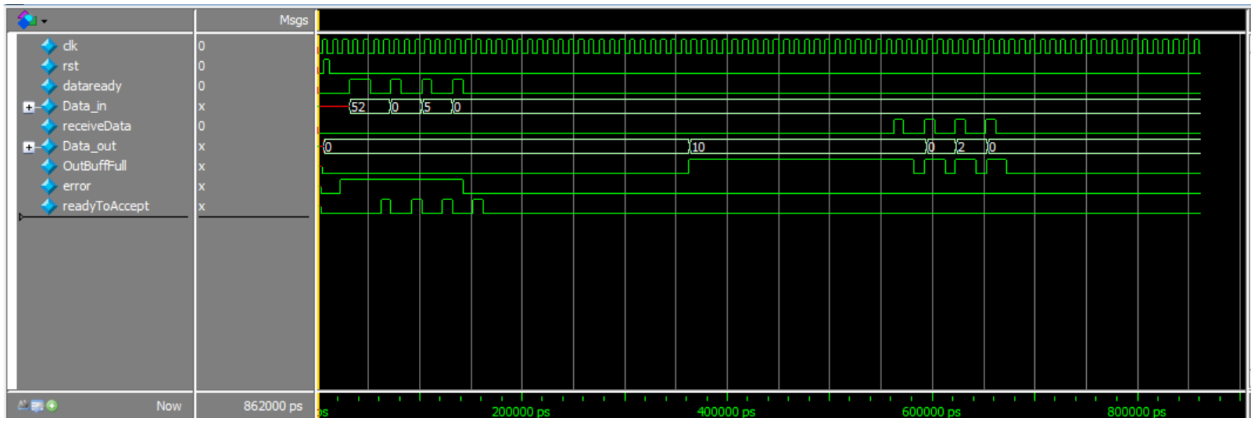


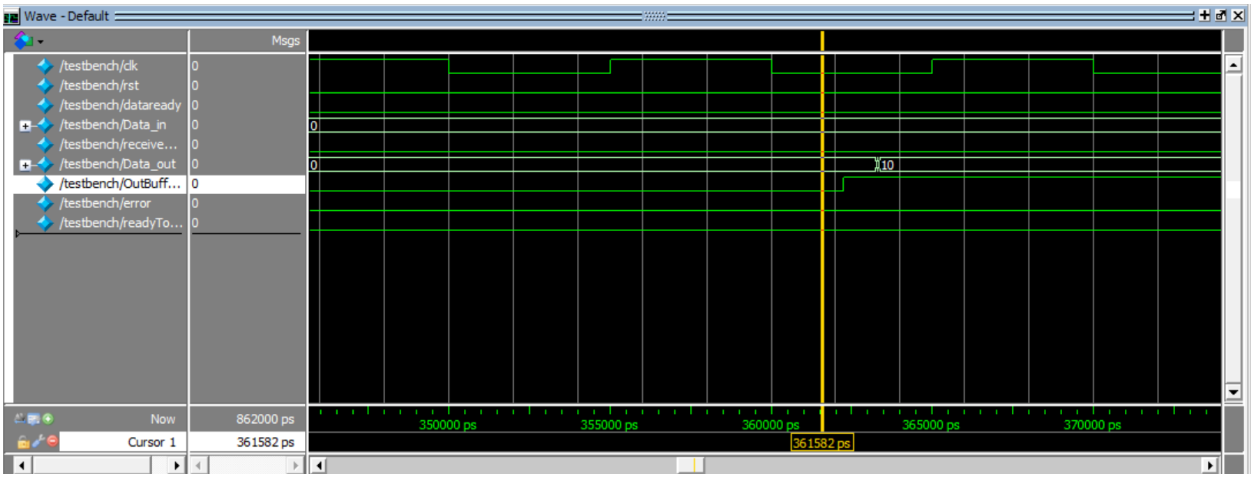

output wrapper
16 bit Reg
16
8
0
1
CO
Counter
initC
inc
8 bit data
16 bit Reg
16
8
8
2
3
~Ready
Idle
Rea
loading
load initC
~receivedata
receive data
recievedata
wait
receivedata
~co & ~receivedata/inc

Simulation:(pre synthesize)



Simulation:(post synthesize)

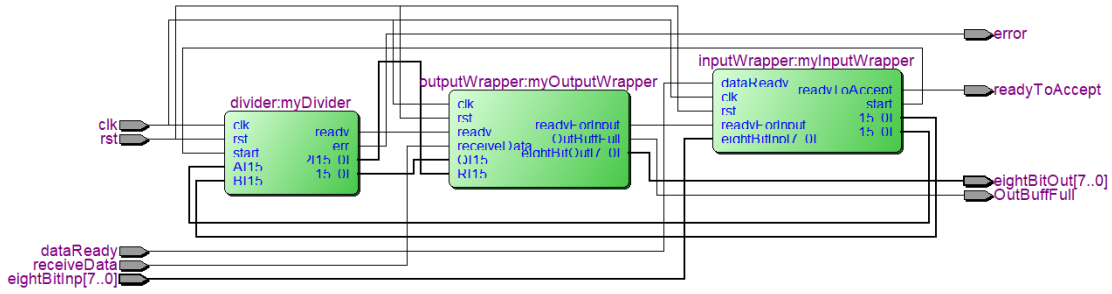




Flow Summary:

Flow Summary	
Flow Status	Successful - Fri Jan 31 13:36:22 2025
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	eightBusInterface
Top-level Entity Name	eightBusInterface
Family	Cyclone II
Device	EP2C5AF256A7
Timing Models	Final
Total logic elements	169 / 4,608 (4 %)
Total combinational functions	153 / 4,608 (3 %)
Dedicated logic registers	132 / 4,608 (3 %)
Total registers	132
Total pins	23 / 158 (15 %)
Total virtual pins	0
Total memory bits	0 / 119,808 (0 %)
Embedded Multiplier 9-bit elements	0 / 26 (0 %)
Total PLLs	0 / 2 (0 %)

RTL viewer:



Chip planner: