Data paths & Controller:

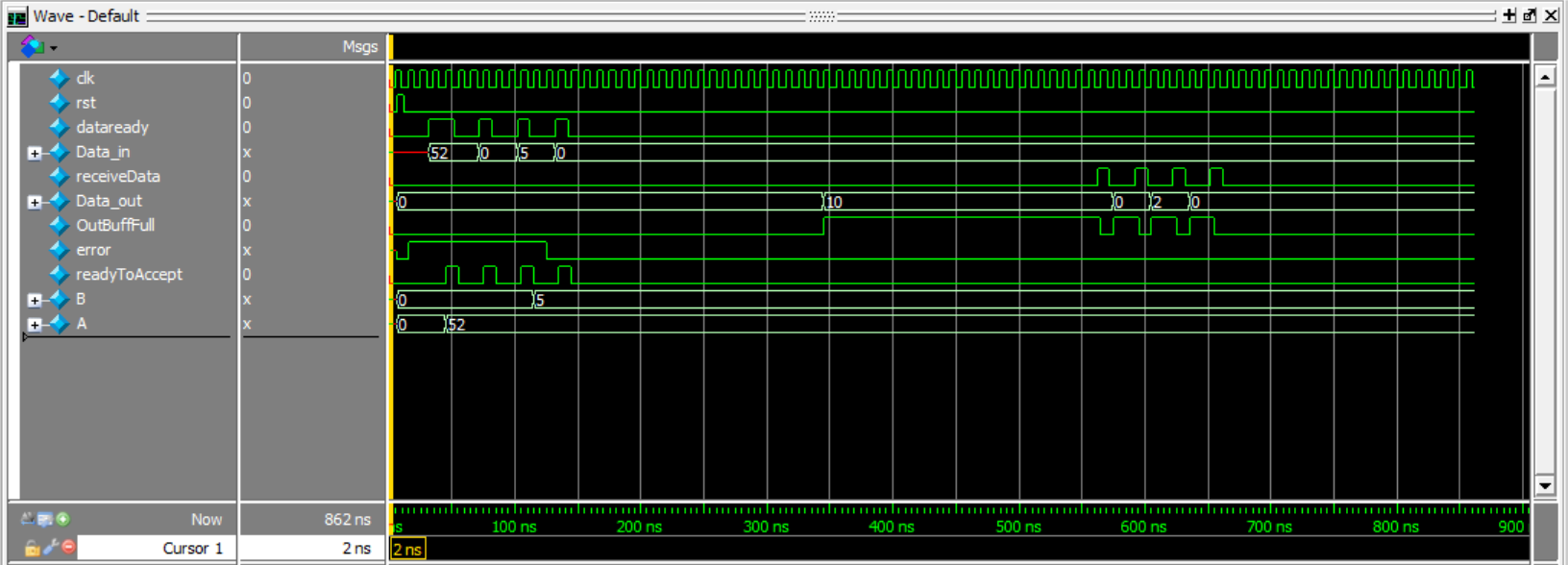
A white board with writing on it

Description automatically generated

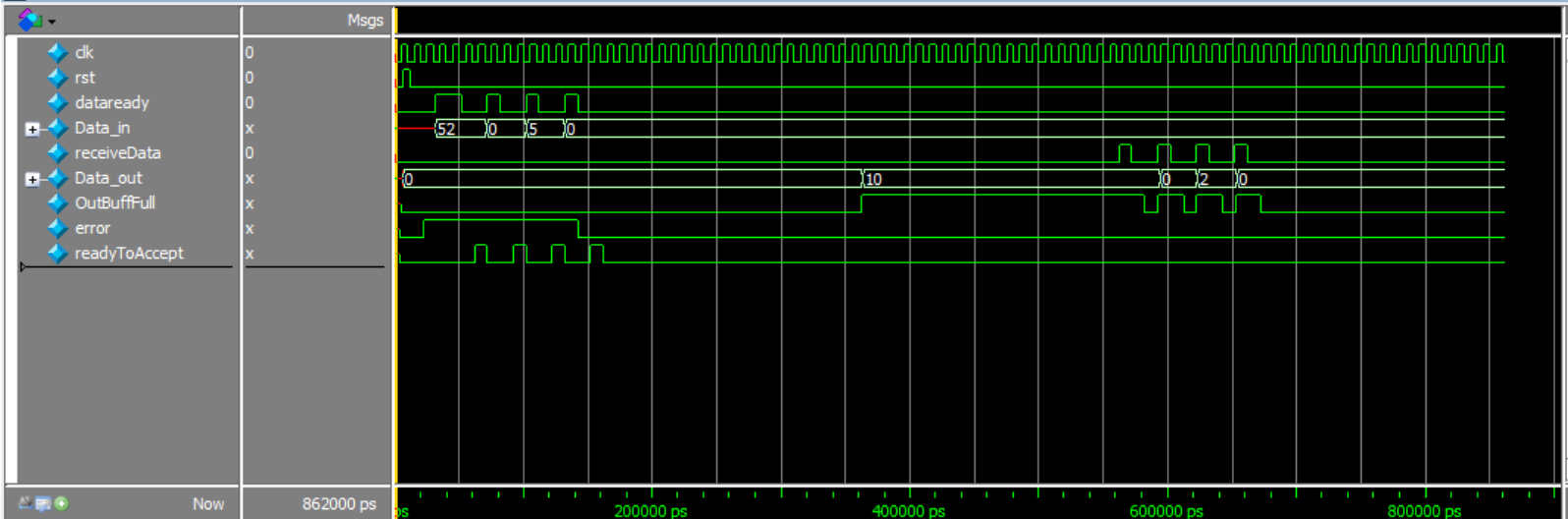
A diagram of a computer system

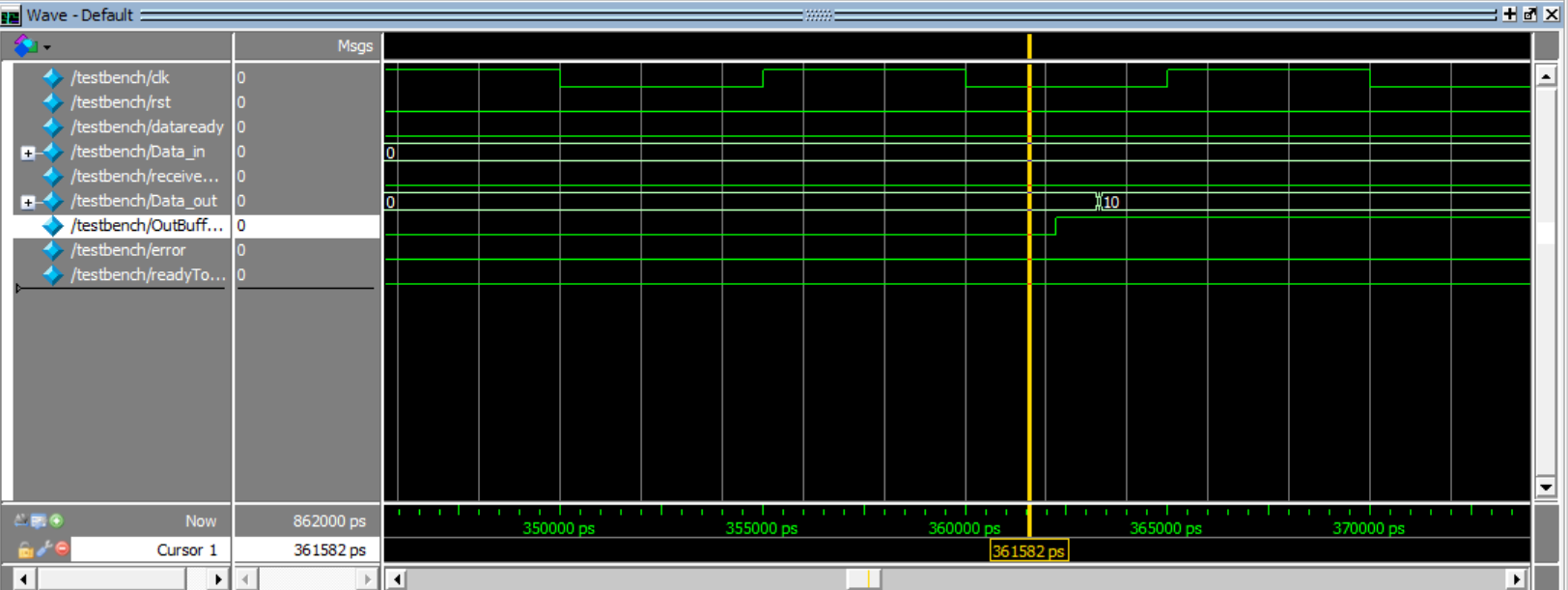
Description automatically generated with medium confidence

Simulation:( pre synthesize)

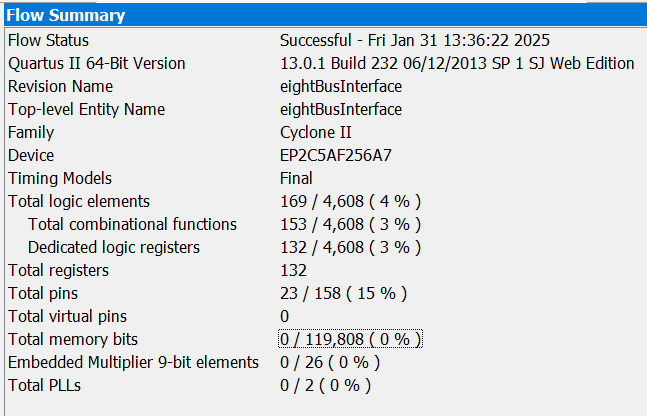


Simulation:( post synthesize)

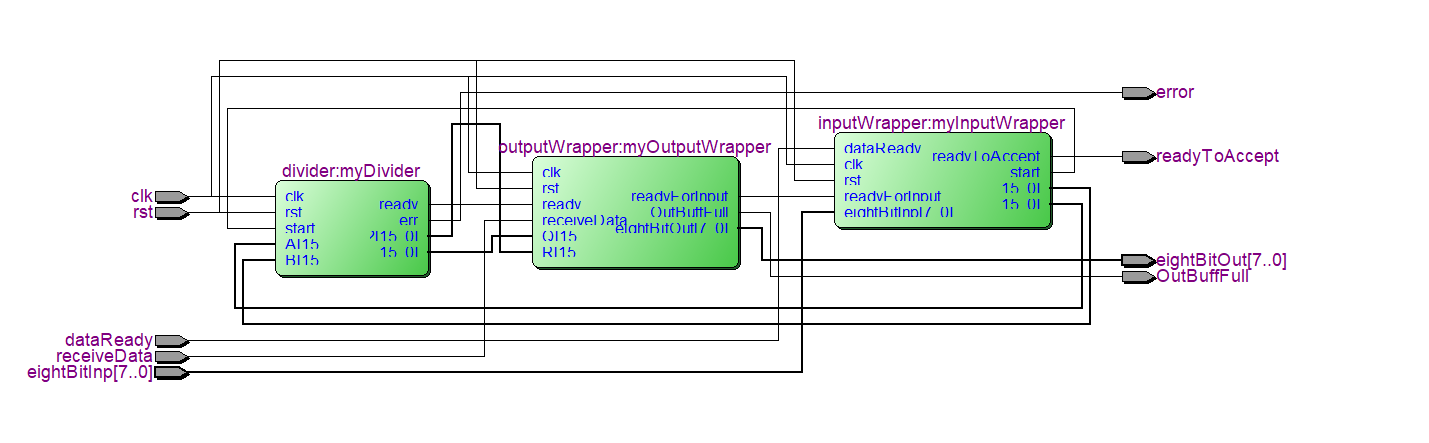




Flow Summary:



RTL viewer:



Chip planner:

