KATHMANDU UNIVERSITY

Department of Computer Science and Engineering

Dhulikhel, Kavre

Lab Sheet 2

Adder (Half and Ful) Implementation using Proteus Design Suite

Embedded System

[Course Code: COMP 306]

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CE(3rd Year/ 2nd Semester)

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Half Adder:

A half adder is a type of adder, an electronic circuit that performs the addition of numbers. The half adder is able to add two single binary digits and provide the output plus a carrying value. It has two inputs, and two outputs S (sum) and C (carry). The Simulation of Half Adder in Proteus is given Below:

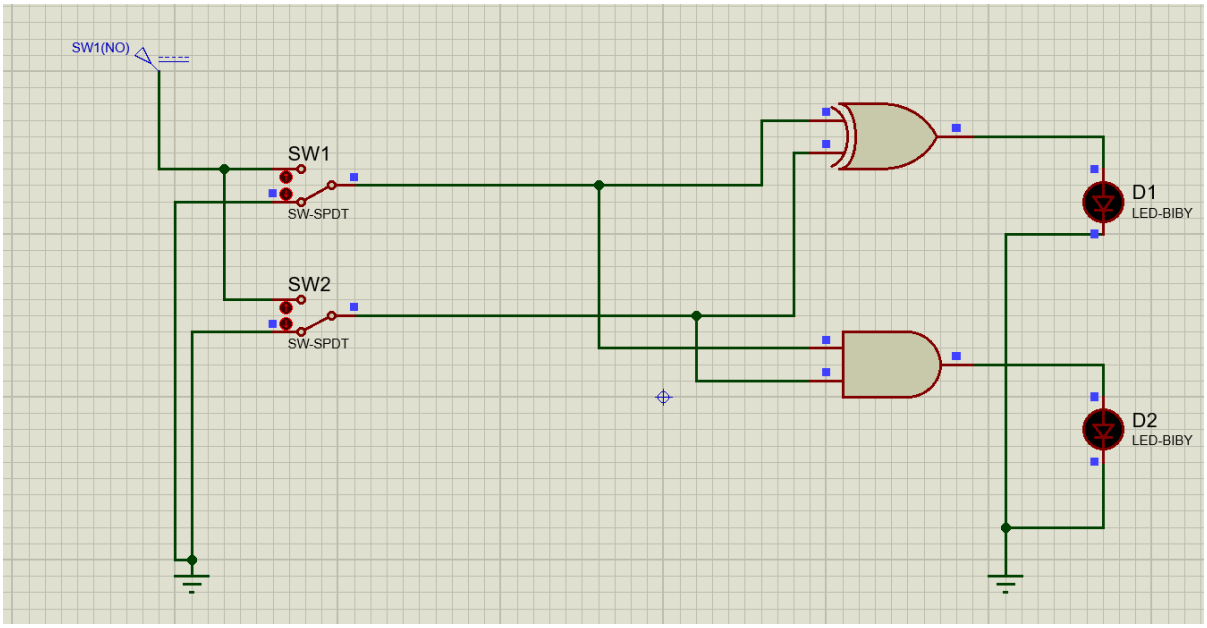

Figure 1.A

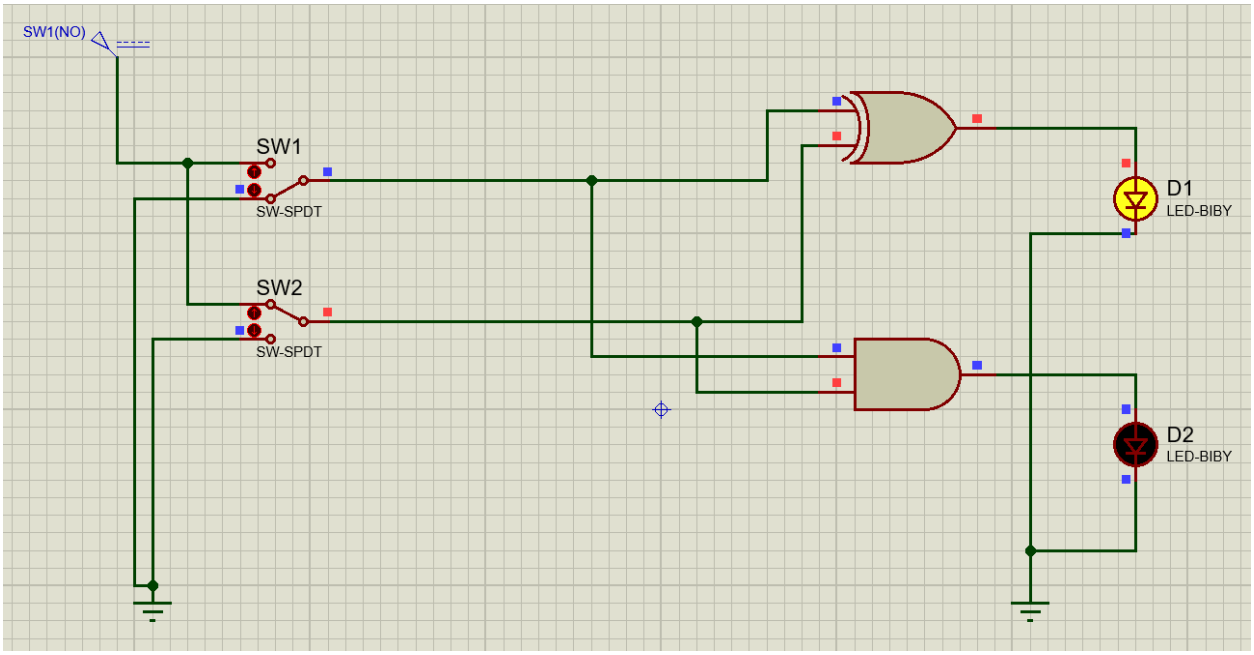

Figure 1.B

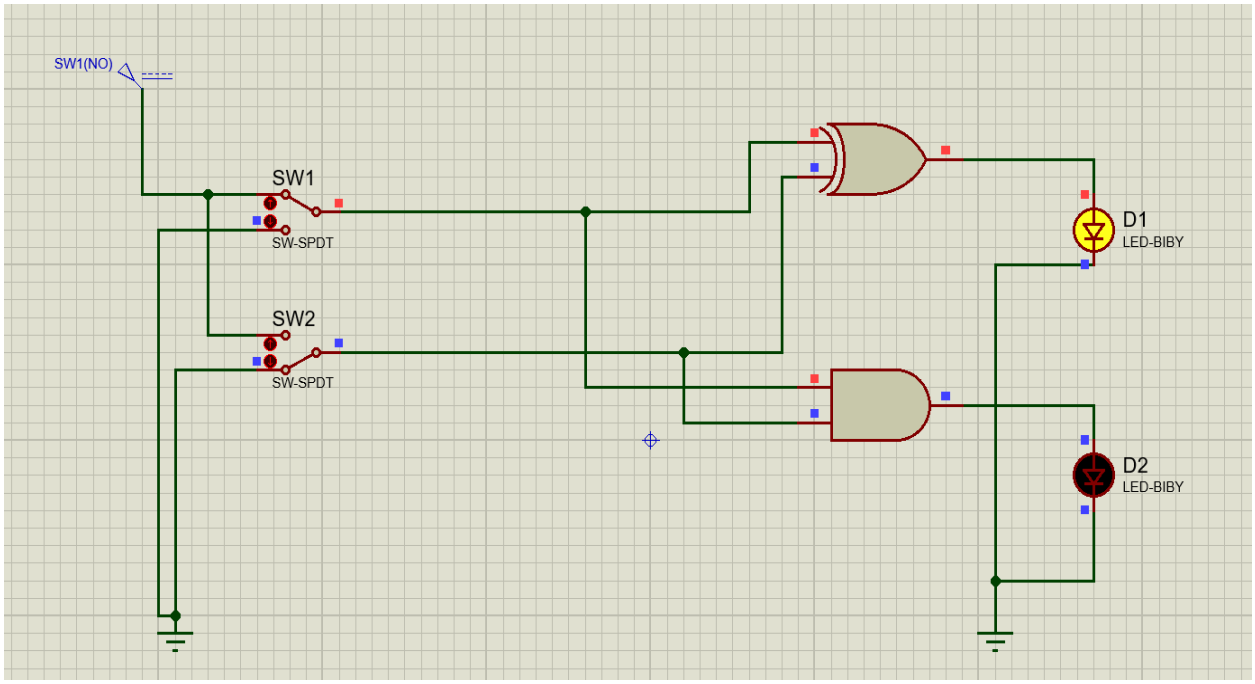

Figure 1.C

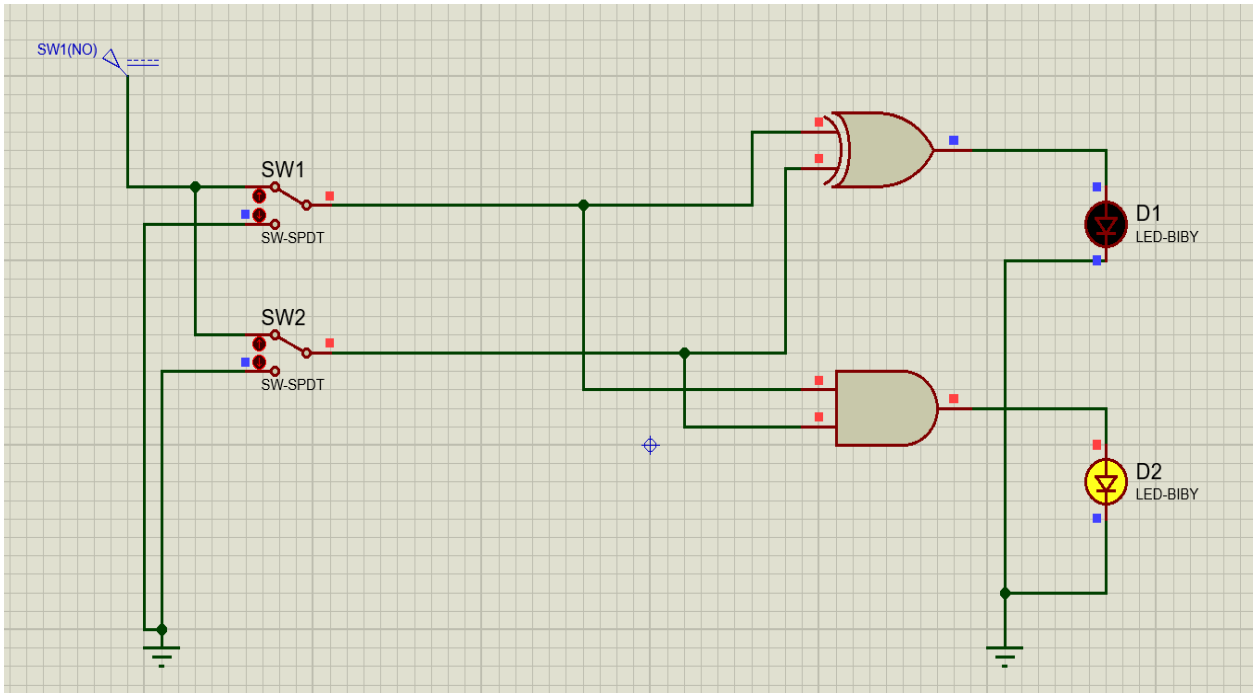

Figure 1.D

Truth Table

The truth table for AND gate taking the above simulations are reference is given below:

Figure	Input 1	Input 2	SUM	CARRY
1.A	0	0	0	0
1.B	0	1	1	0
1.C	1	0	1	0
1.D	1	1	0	1

Full Adder

A full adder adds binary numbers and accounts for values carried in as well as out. A one-bit full-adder adds three one-bit numbers, often written as A, B, and Cin; A and B are the operands, and Cin is a bit carried in from the previous less-significant stage. The Simulation of a full adder is shown below:

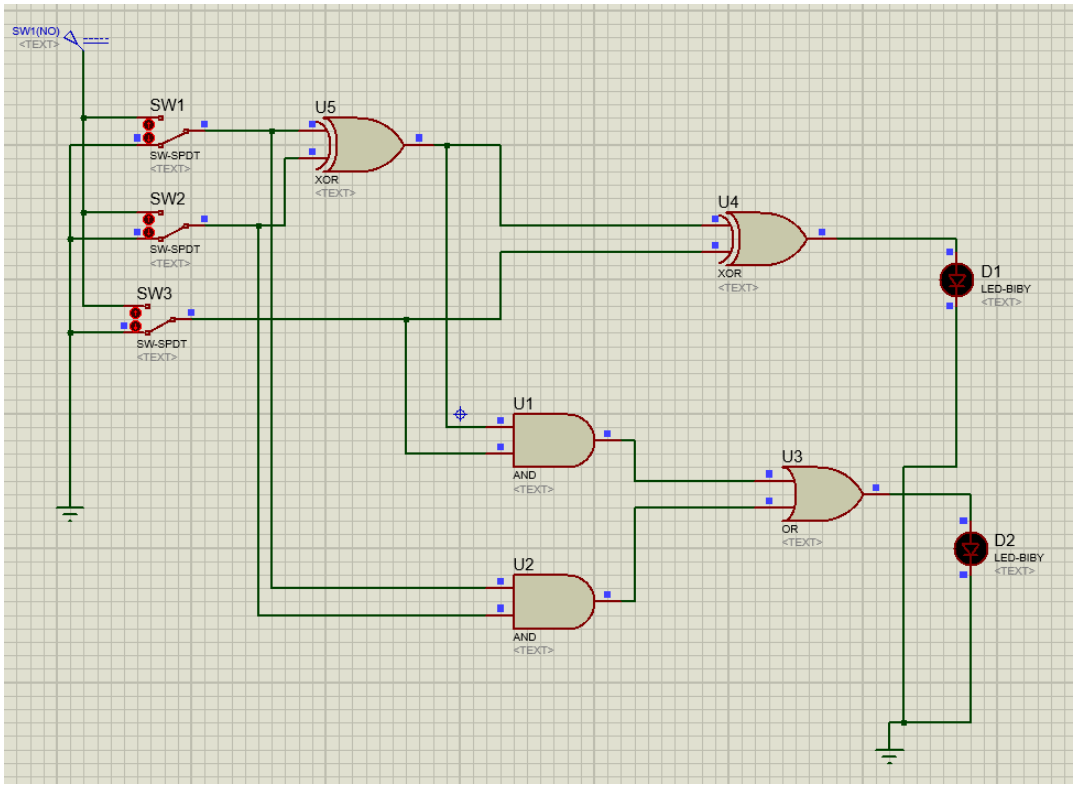

Figure 2.A

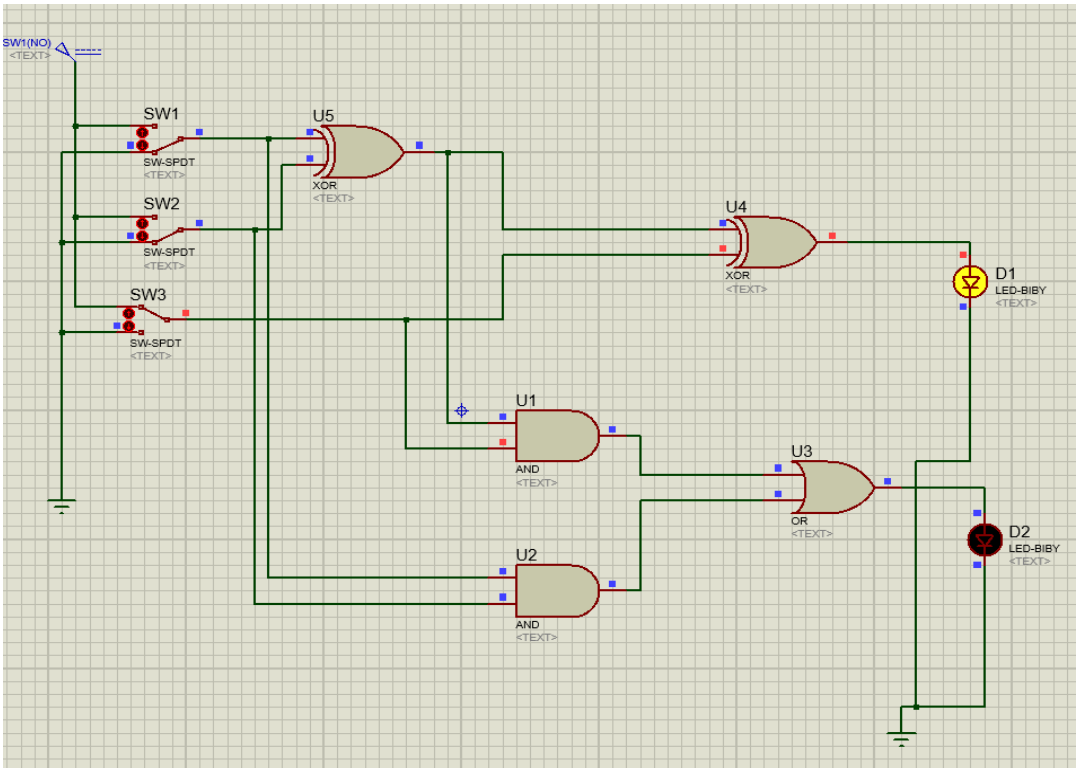

Figure 2.B

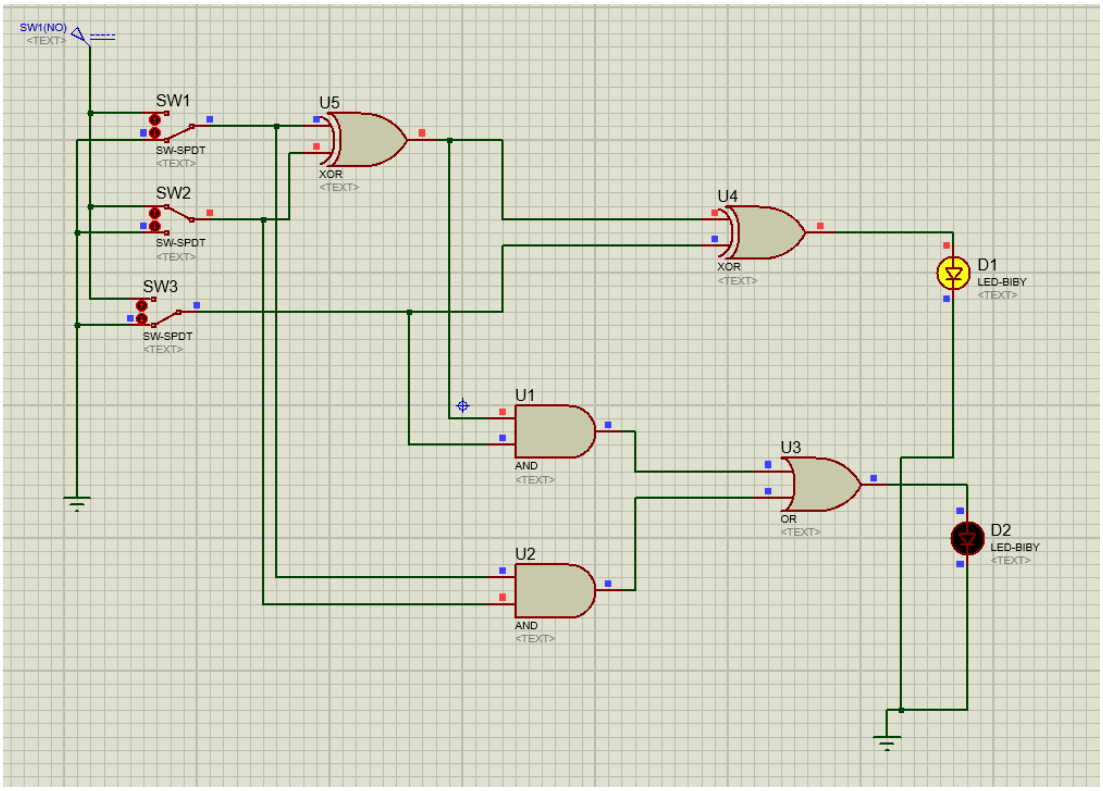

Figure 2.C

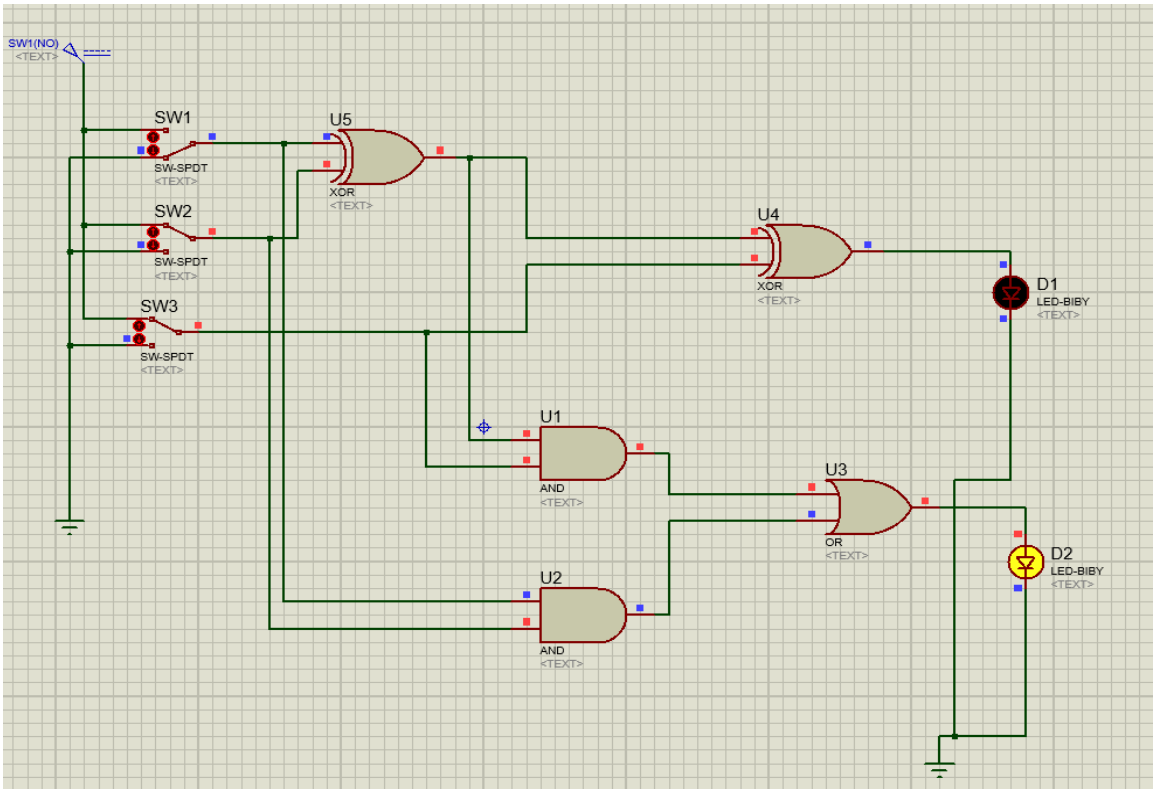

Figure 2.D

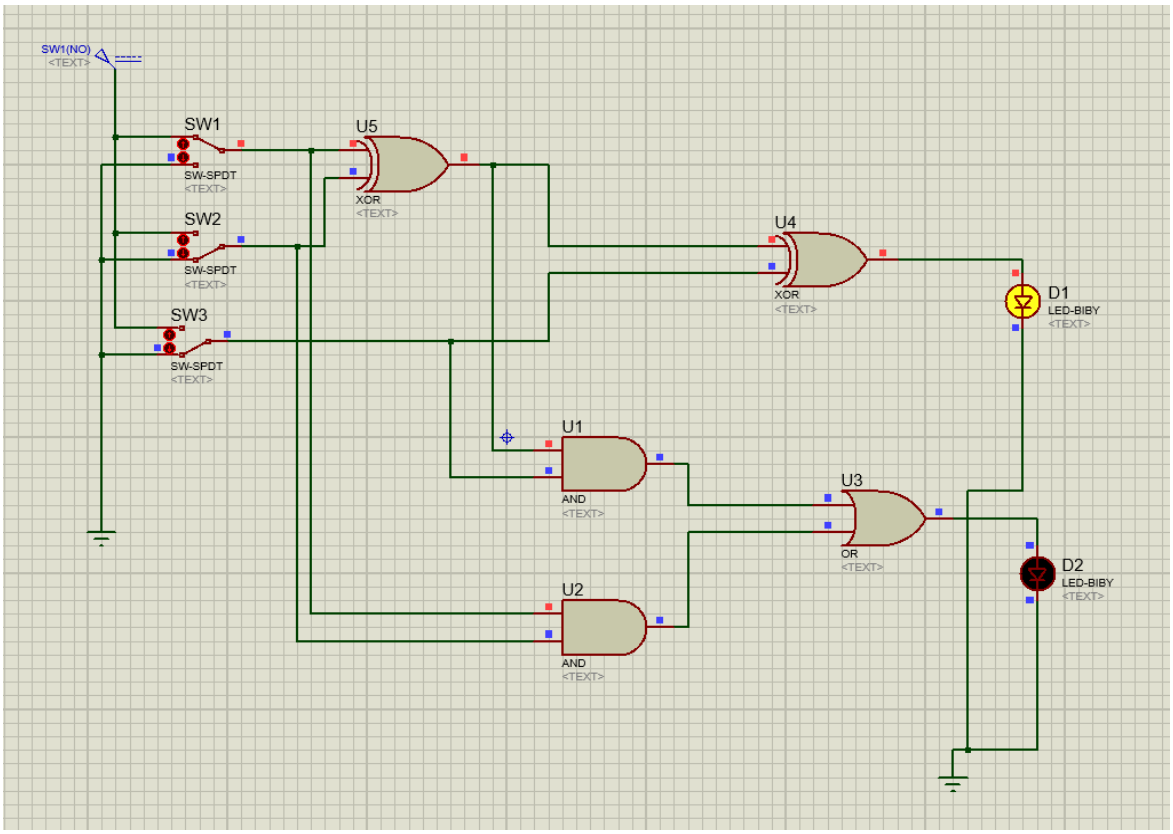

Figure 2.E

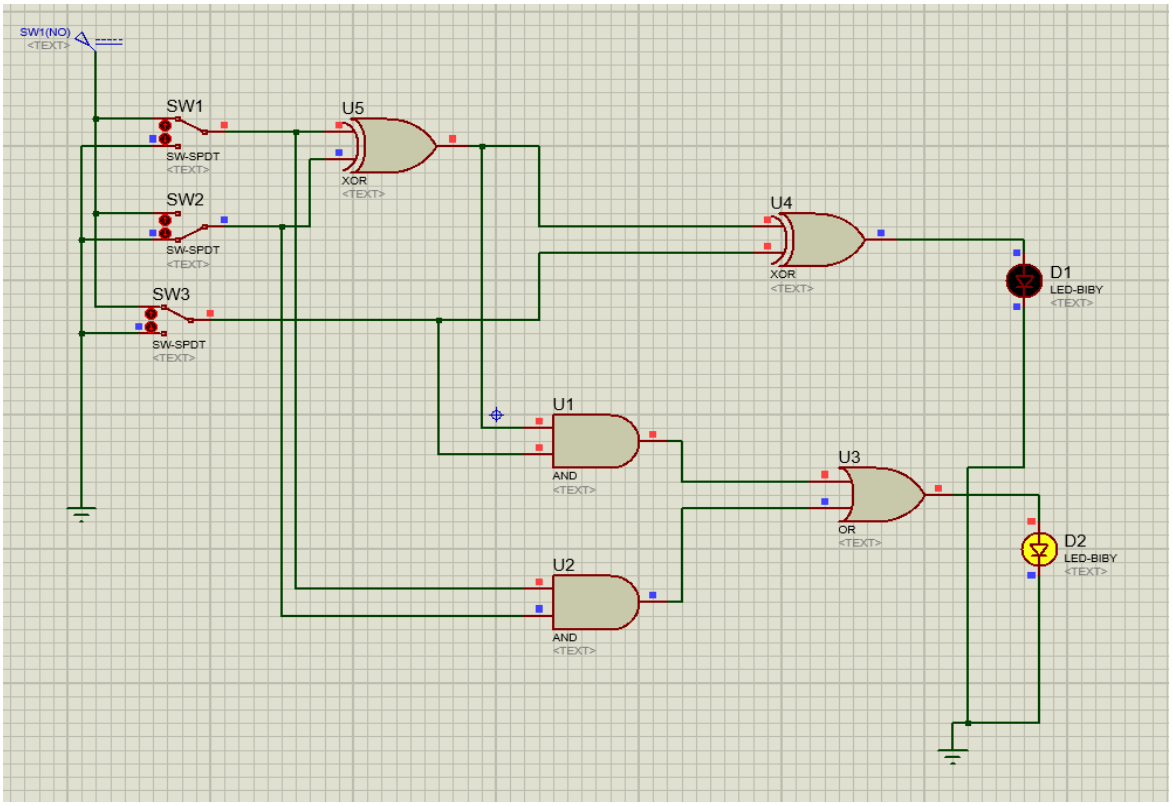

Figure 2.F

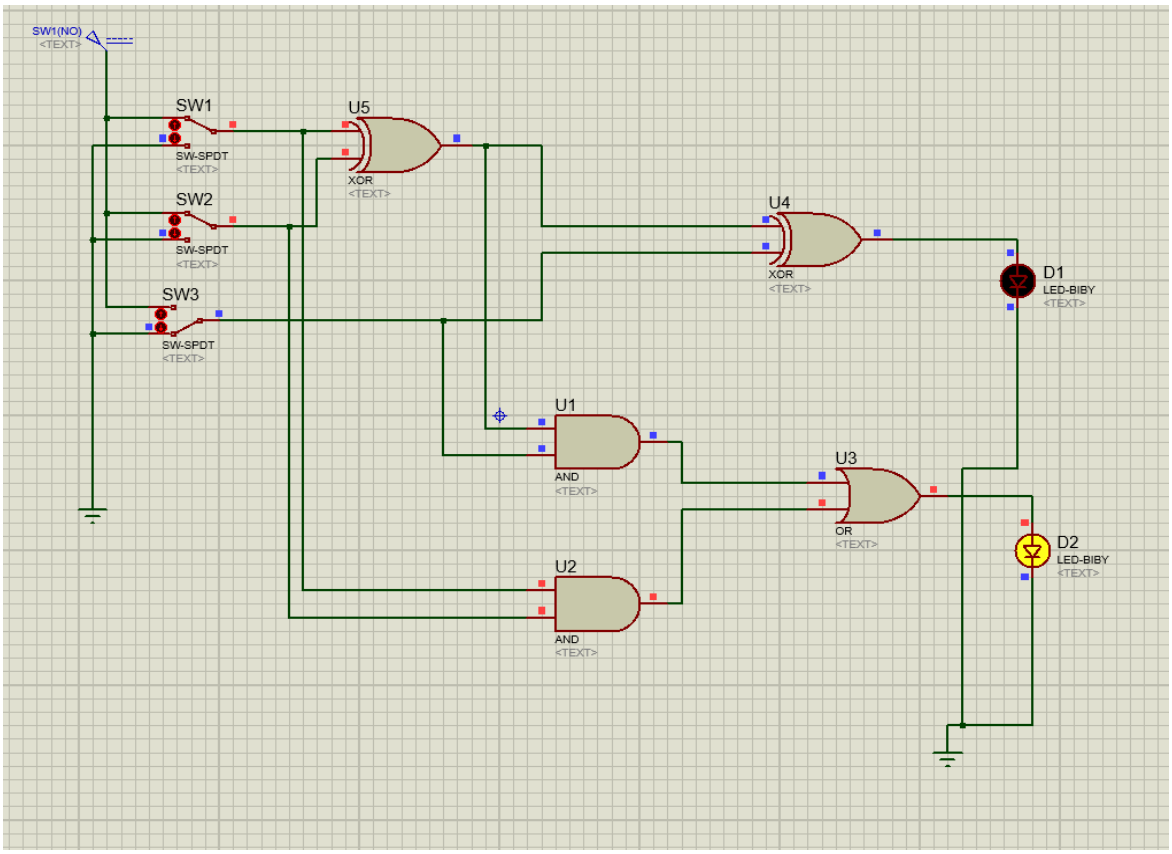

Figure 2.G

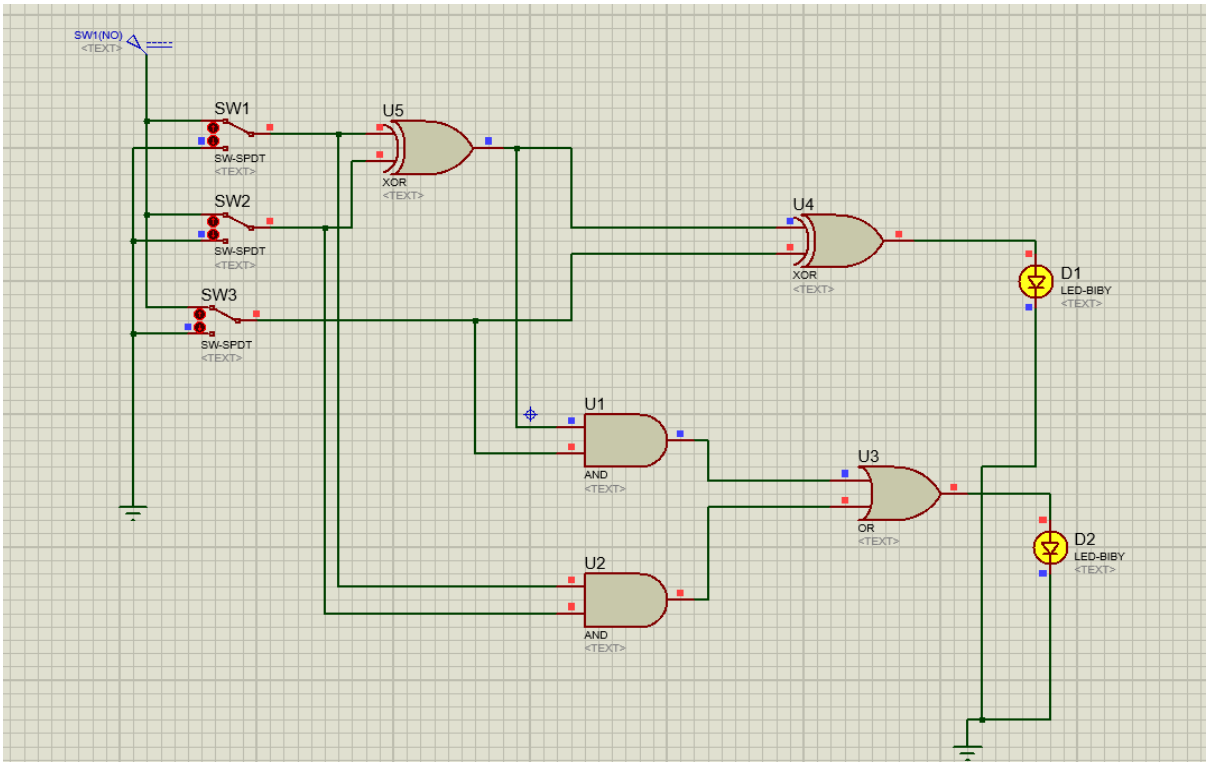

Figure 2.H

Truth Table

The truth table for Full Adder taking the above simulations are reference is given below:

Figure	Input A	Input B	Input C_{in}	Sum	Carry
2.A	0	0	0	0	0
2.B	0	0	1	1	0
2.C	0	1	0	1	0
2.D	0	1	1	0	1
2.E	1	0	0	1	0
2.F	1	0	1	0	1
2.G	1	1	0	0	1
2.H	1	1	1	1	1