**KATHMANDU UNIVERSITY**

**Department of Computer Science and Engineering**

**Dhulikhel, Kavre**

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Lab Sheet 1

**Logic Gates Implementation using**

**Proteus Design Suite**

**Embedded System**

**[Course Code: COMP 306]**

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# Introduction to Proteus

The Proteus Design Suite is a proprietary software tool suite used primarily for electronic design automation. The software is used mainly by electronic design engineers and technicians to create schematics and electronic prints for manufacturing printed circuit boards.

Lab 1 is based upon the simulation of Logic Gates using Proteus Design (i.e using Proteus 8 Professional). The screenshots of the simulation for various logical gates are as follows:

## AND Gate:

The Simulation of And Gate in Proteus is given Below:

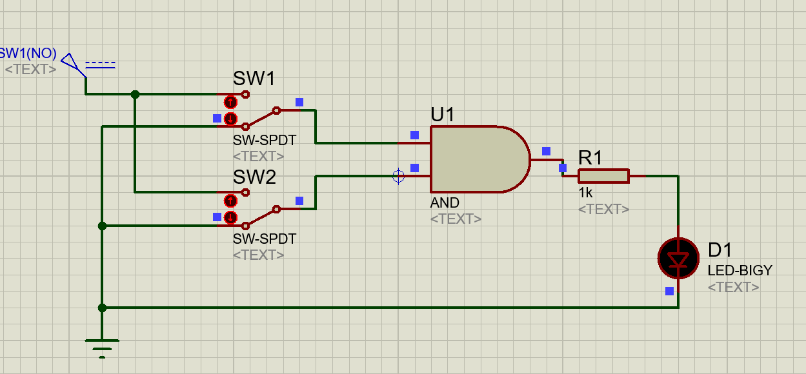


Figure .A

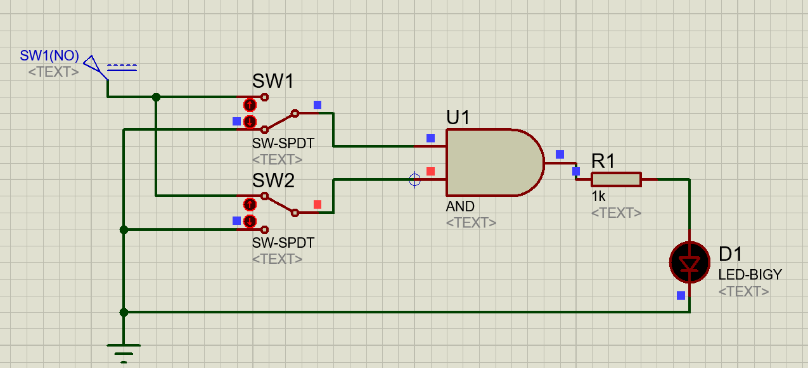


Figure 2.B

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Figure 3.C

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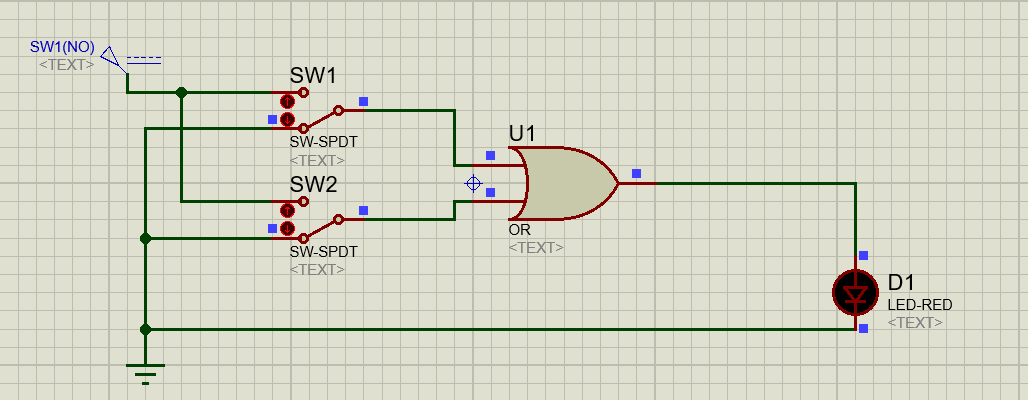
Figure .D

## Truth Table

The truth table for AND gate taking the above simulations are reference is given below:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Figure | Input 1 | Input 2 | Output (AND) | Glowing of LED |
| 1.A | 0 | 0 | 0 | NO |
| 1.B | 0 | 1 | 0 | NO |
| 1.C | 1 | 0 | 0 | NO |
| 1.D | 1 | 1 | 1 | YES |

## OR Gate:

The Simulation of And Gate in Proteus is given Below:

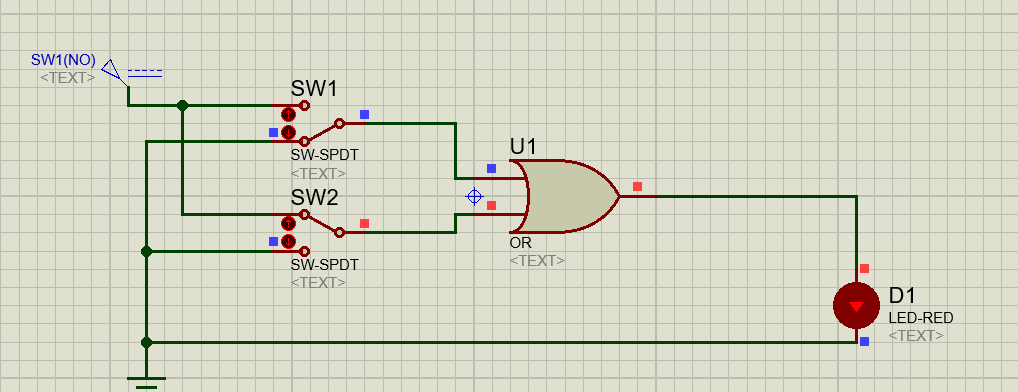
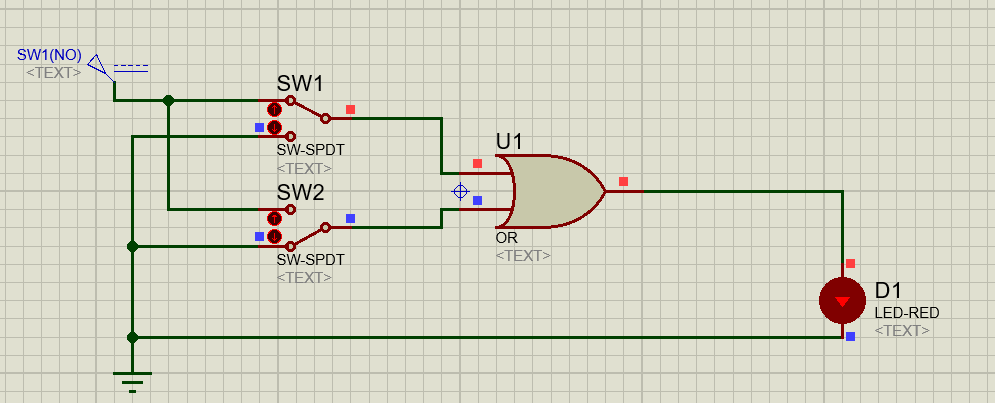


Figure 2.C

Figure 2.B

Figure 2.A

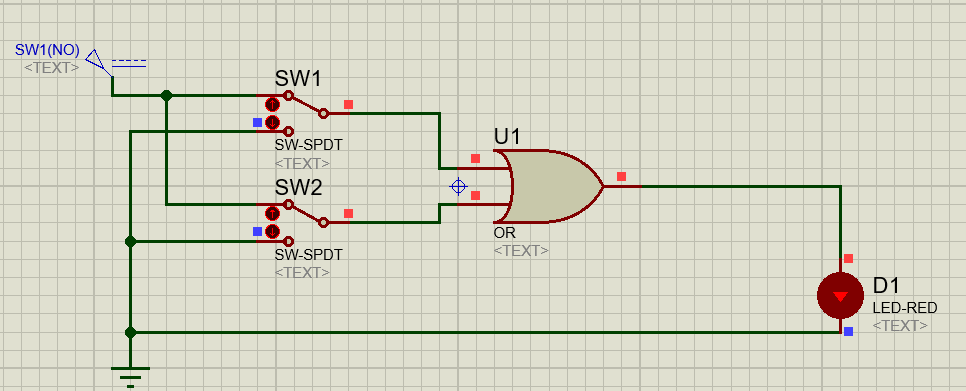


Figure 2.D

## Truth Table

The truth table for AND gate taking the above simulations are reference is given below:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Figure | Input 1 | Input 2 | Output (OR) | Glowing of LED |
| 2.A | 0 | 0 | 0 | NO |
| 2.B | 0 | 1 | 1 | YES |
| 2.C | 1 | 0 | 1 | YES |
| 2.D | 1 | 1 | 1 | YES |

## NOT Gate:

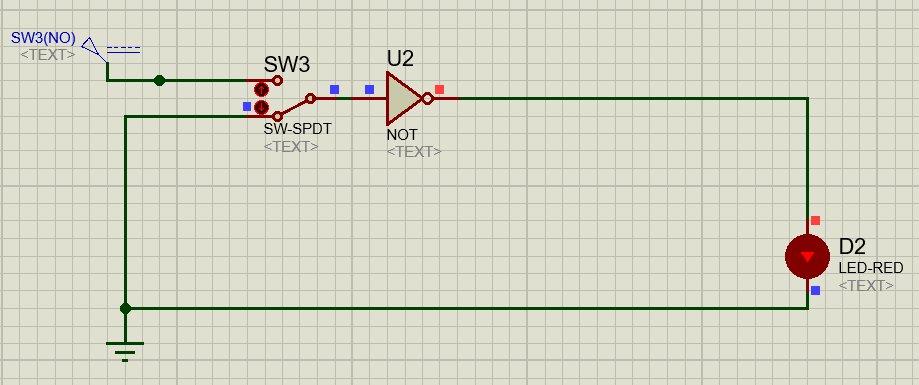
The Simulation of And Gate in Proteus is given Below:

Figure 3.A

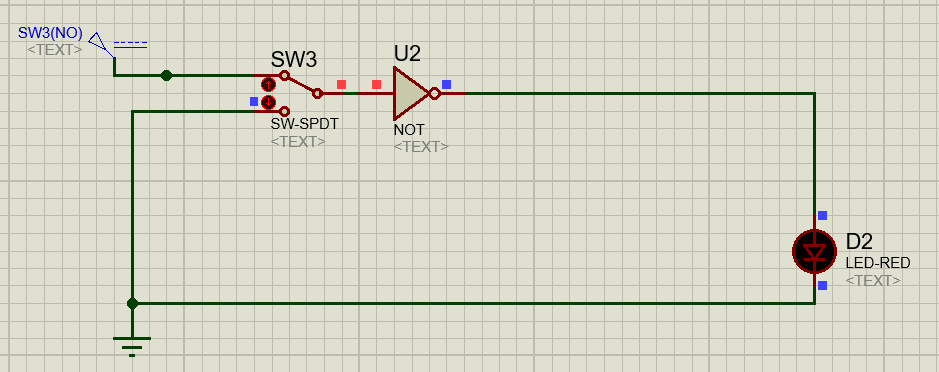


Figure 3.B

## Truth Table

The truth table for AND gate taking the above simulations are reference is given below:

|  |  |  |  |
| --- | --- | --- | --- |
| Figure | Input | Output (OR) | Glowing of LED |
| 3.A | 0 | 1 | YES |
| 3.B | 1 | 0 | NO |

## NAND Gate:

The Simulation of the NAND Gate in Proteus is given Below:

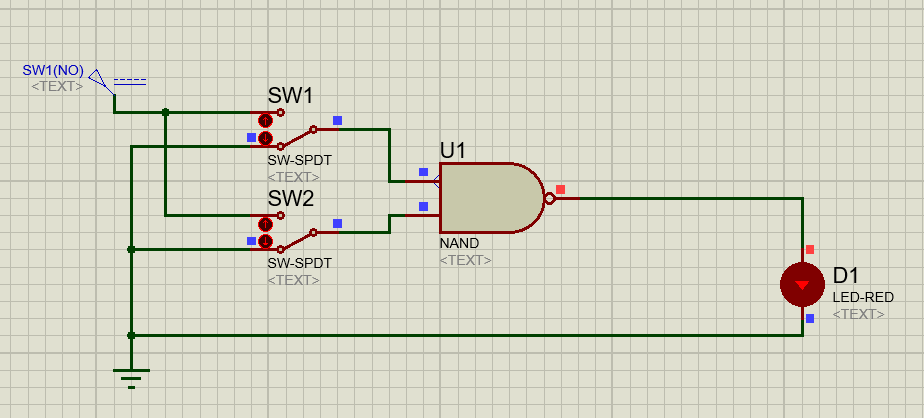


Figure 4.A

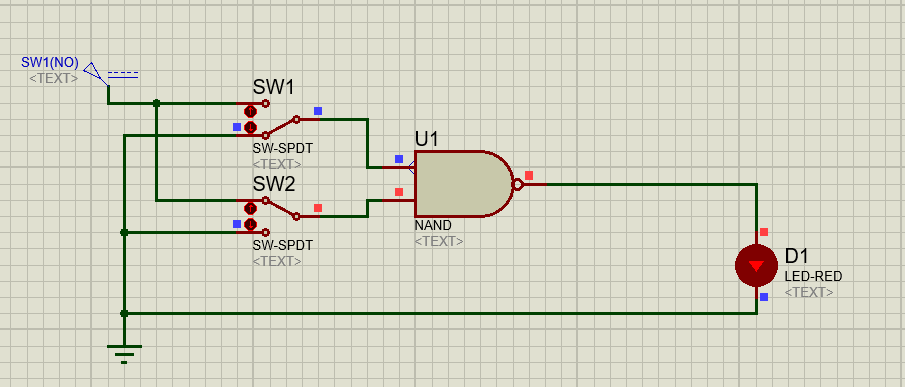


Figure 4.B

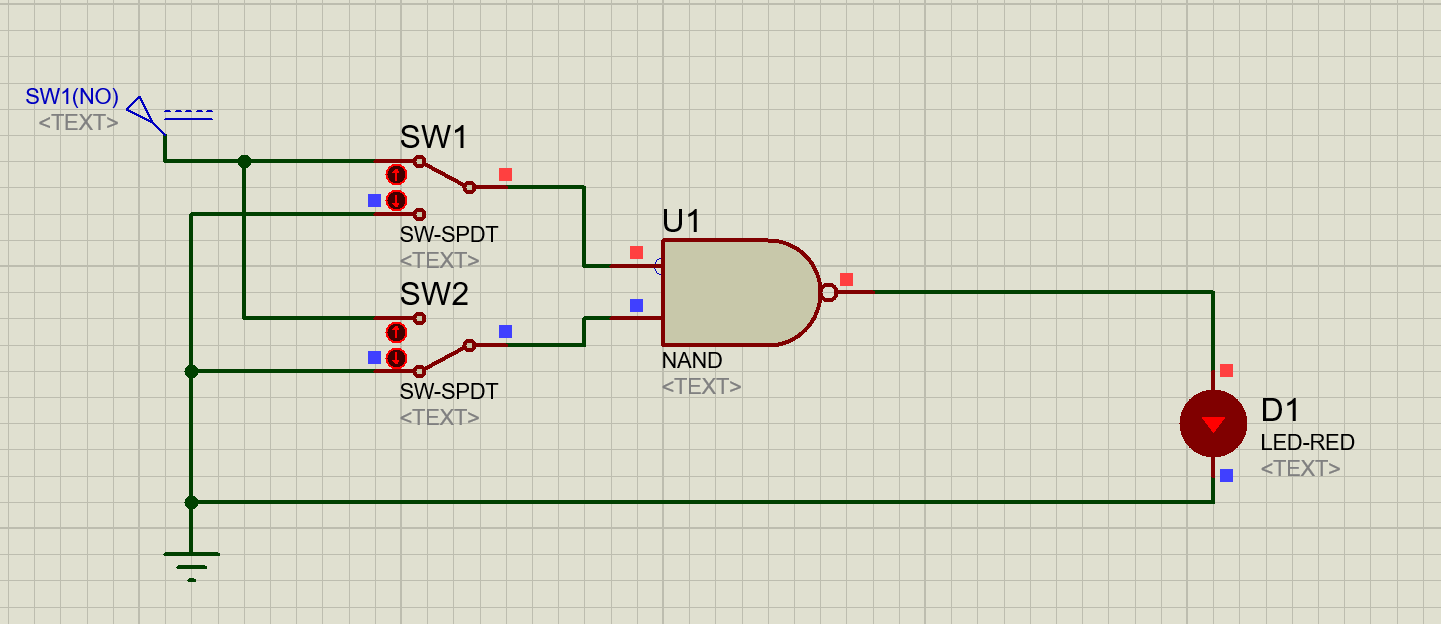


Figure 4.C

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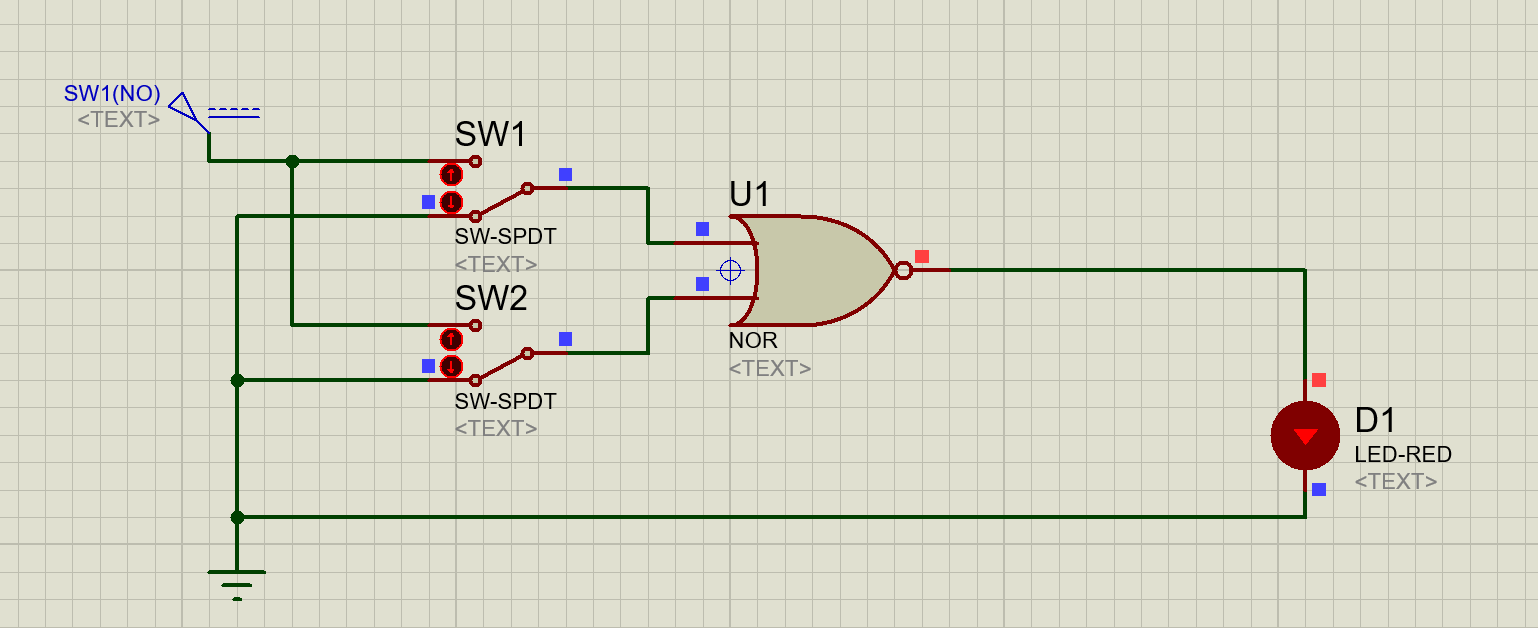
Figure 4.D

## Truth Table

The truth table for NAND gate taking the above simulations are reference is given below:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Figure | Input 1 | Input 2 | Output (NAND) | Glowing of LED |
| 4.A | 0 | 0 | 1 | YES |
| 4.B | 0 | 1 | 1 | YES |
| 4.C | 1 | 0 | 1 | YES |
| 4.D | 1 | 1 | 0 | NO |

## NOR Gate:

The Simulation of the NOR Gate in Proteus is given Below:

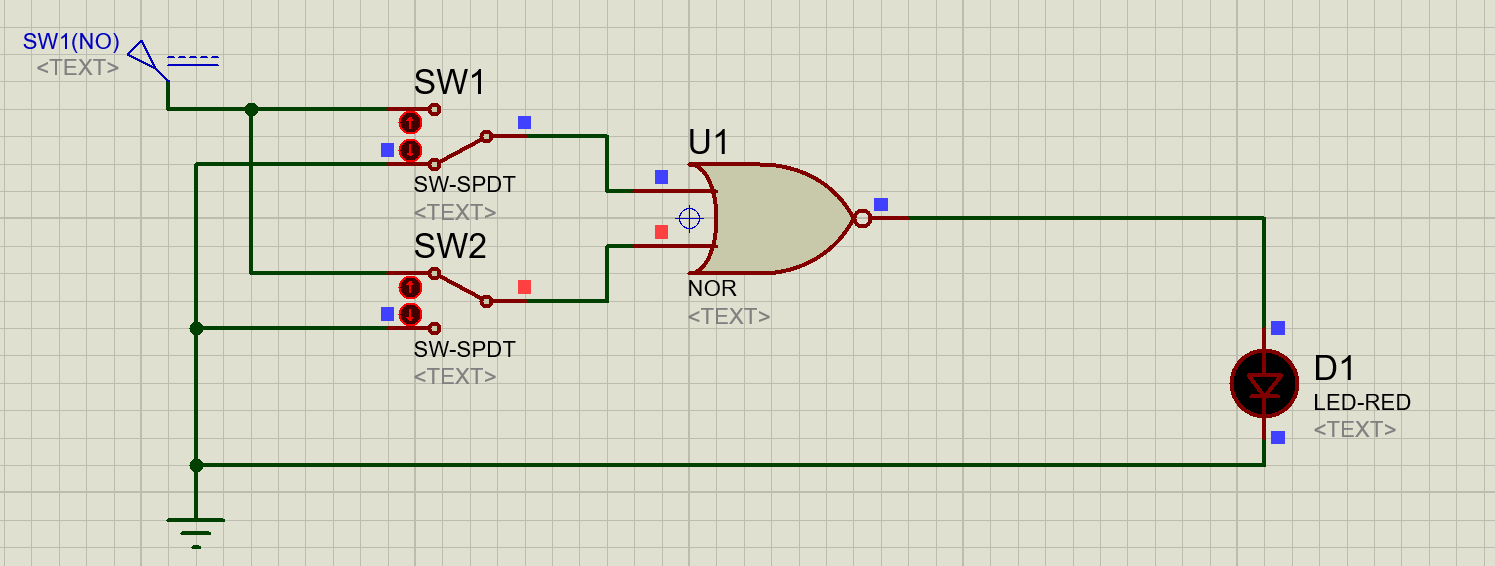


Figure 5.A

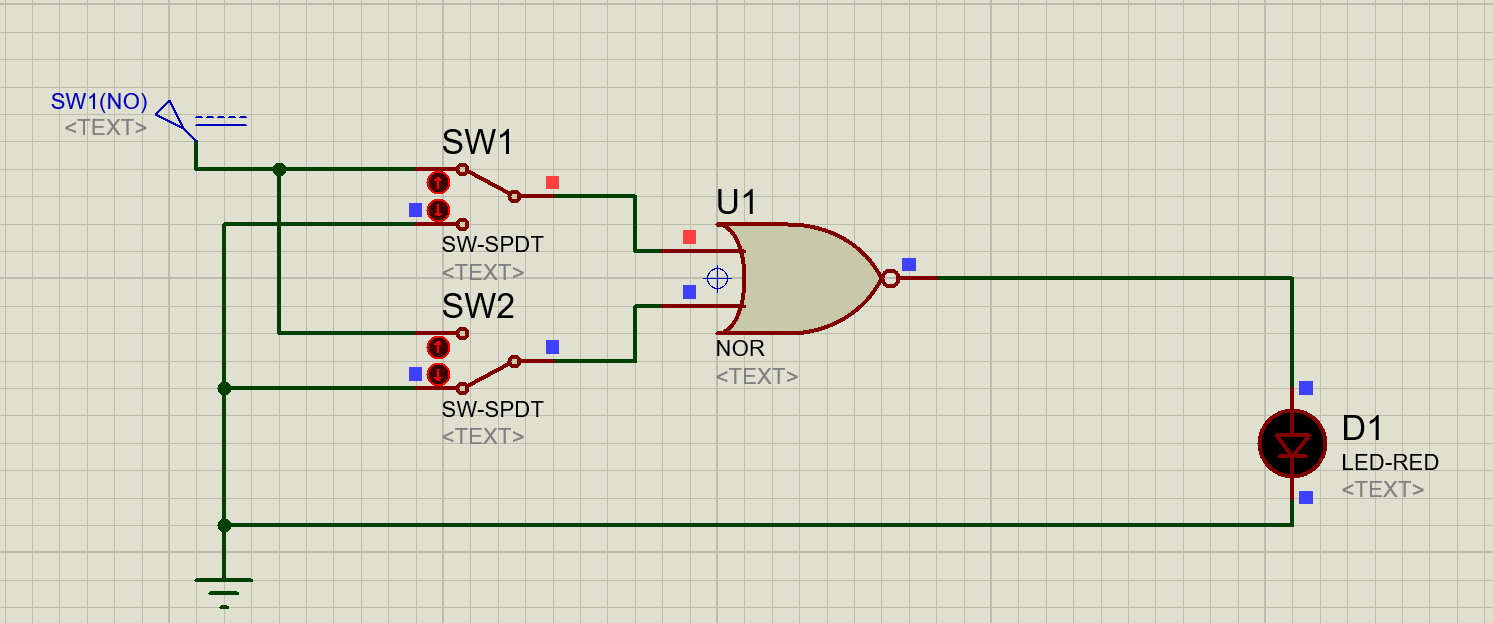


Figure 5.B

Figure 5.C

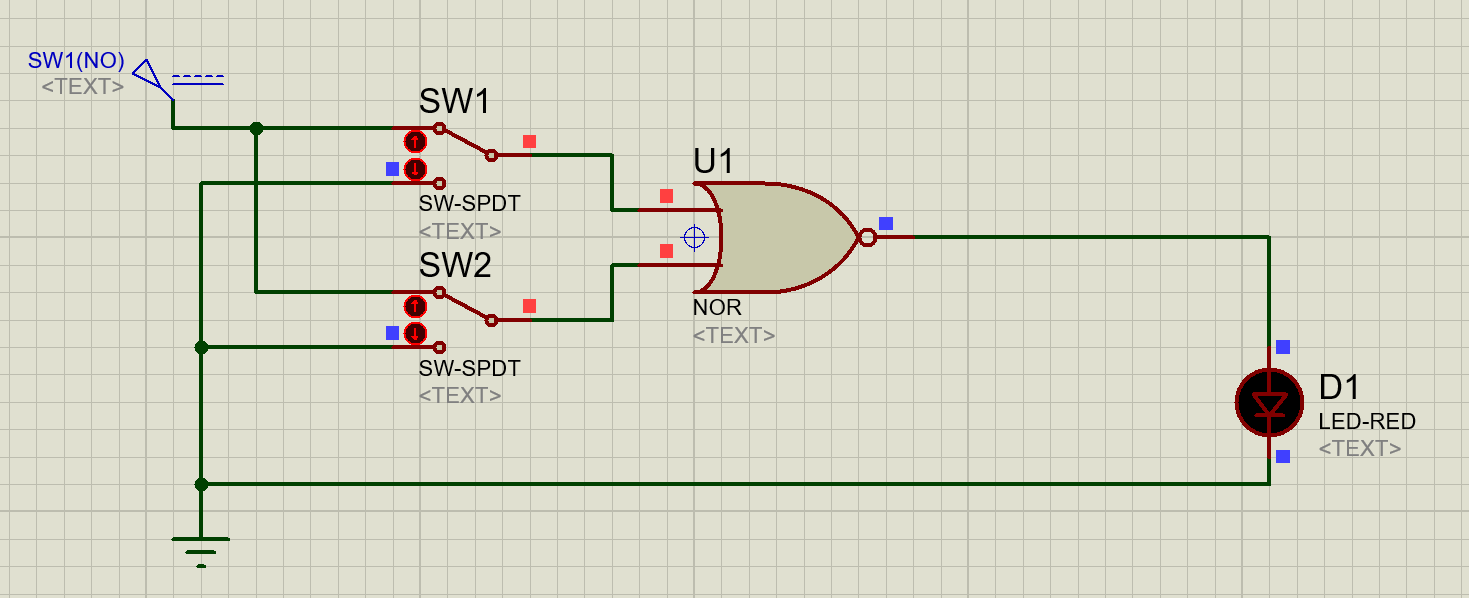


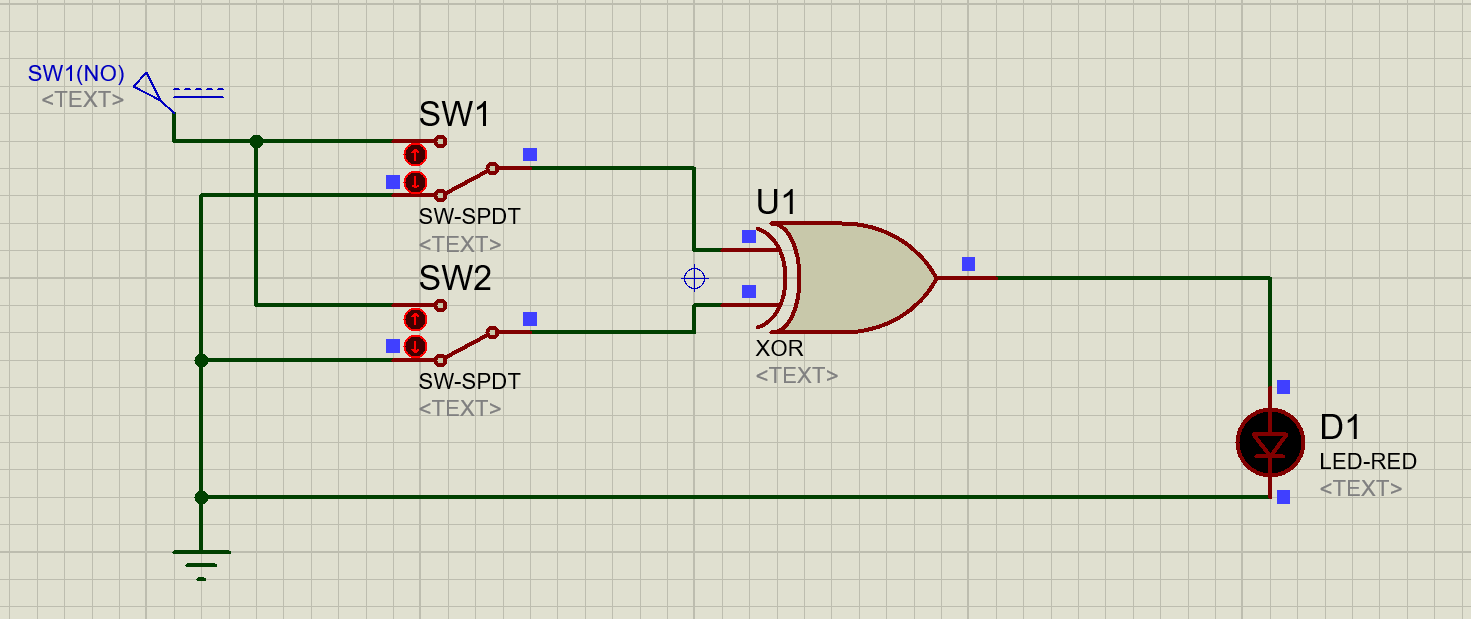
Figure 5.D

## Truth Table

The truth table for NAND gate taking the above simulations are reference is given below:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Figure | Input 1 | Input 2 | Output (NOR) | Glowing of LED |
| 5.A | 0 | 0 | 1 | YES |
| 5.B | 0 | 1 | 0 | NO |
| 5.C | 1 | 0 | 0 | NO |
| 5.D | 1 | 1 | 0 | NO |

## XOR Gate:

The Simulation of the NAND Gate in Proteus is given Below:

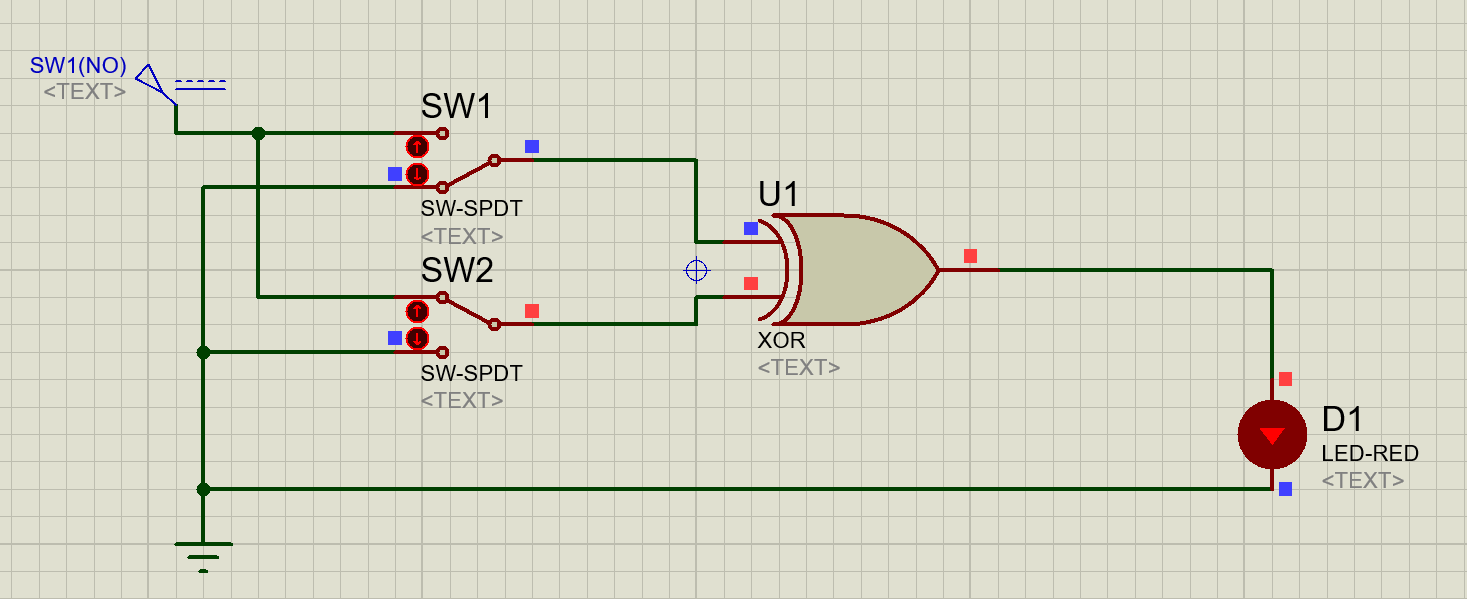


Figure 6.A

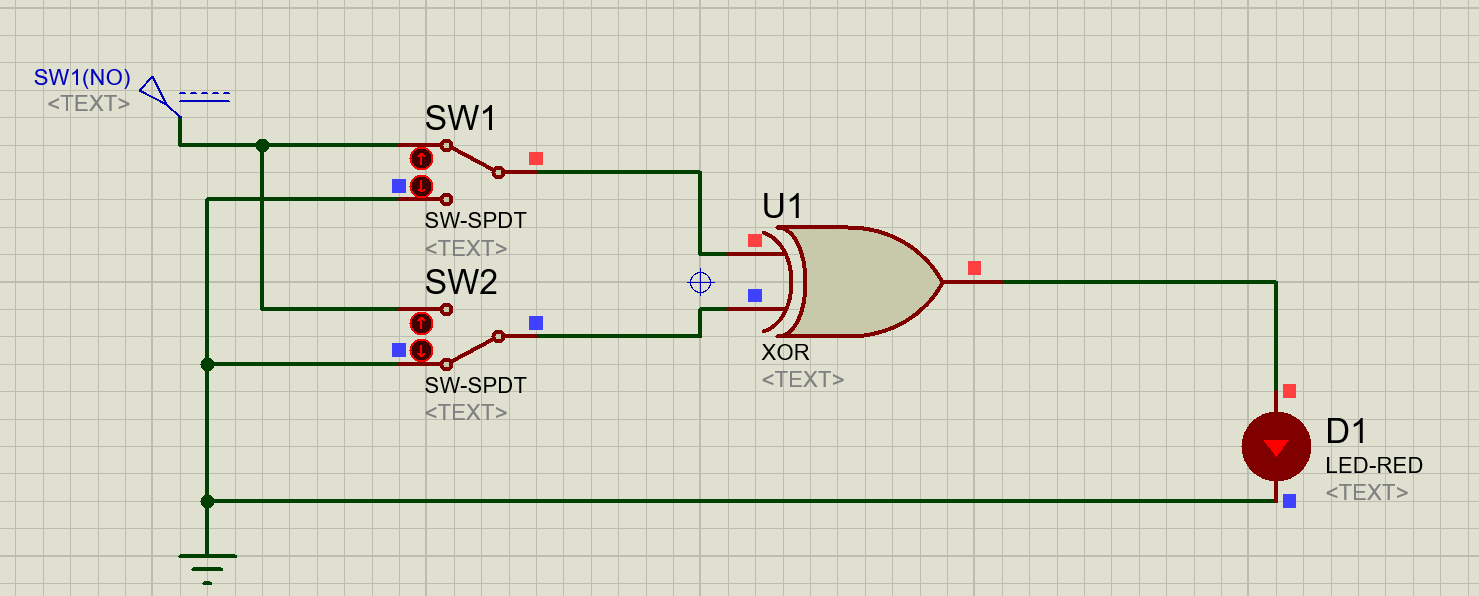


Figure 6.B

Figure 6.C

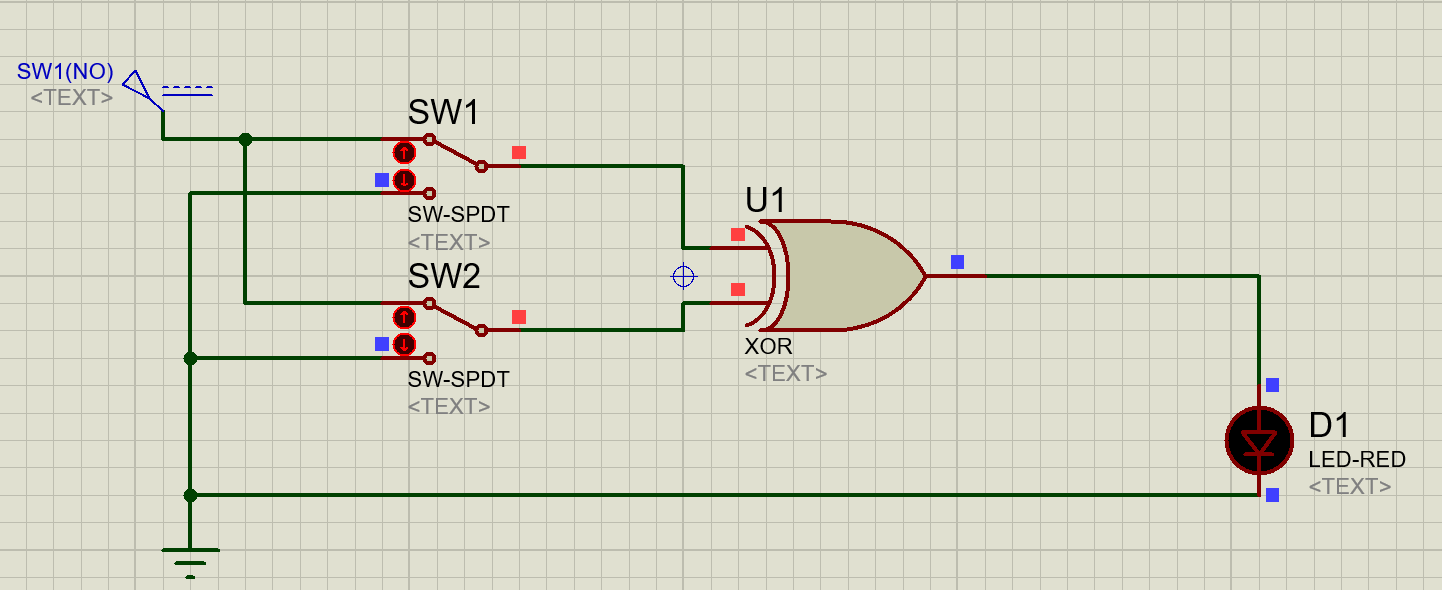


Figure 6.D

## Truth Table

The truth table for XOR gate taking the above simulations are reference is given below:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Figure | Input 1 | Input 2 | Output (XOR) | Glowing of LED |
| 6.A | 0 | 0 | 0 | NO |
| 6.B | 0 | 1 | 1 | YES |
| 6.C | 1 | 0 | 1 | YES |
| 6.D | 1 | 1 | 0 | NO |