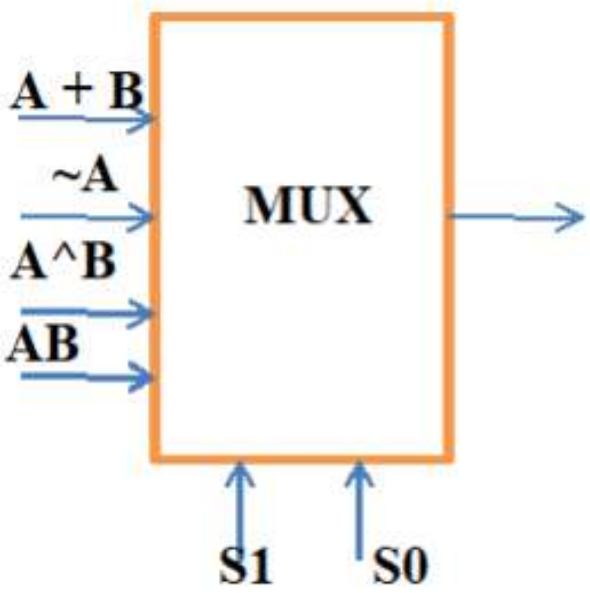
ALU DESIGN

Question:

Design a simple ALU for the following functions using Mux. Create the symbols and simulate the ALU, also find out the Propagation delay for each function.



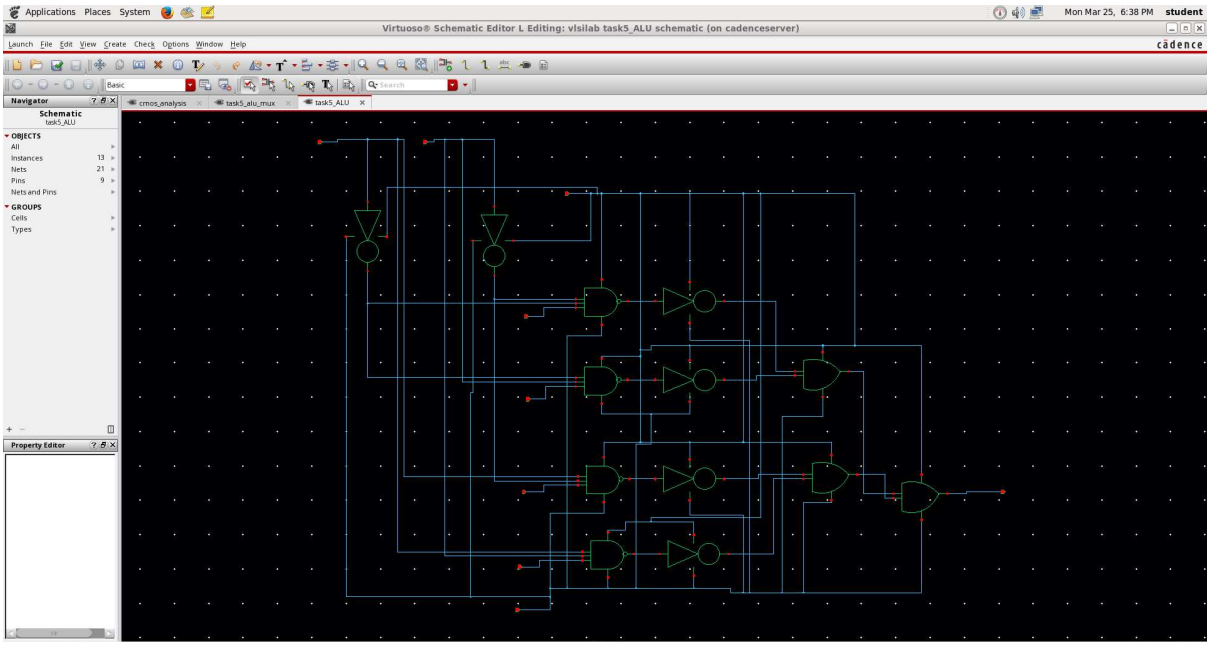
S1	S0	Function
0	0	A+B
0	1	~A
1	0	A^B
1	1	AB

Here we need to create a 4 x 1 multiplexer. This takes four inputs and based on the values of selection lines gives one output.
Consider the inputs to be I_0, I_1, I_2 and I_3, the select lines be S_0 and S_1, then the output will be:

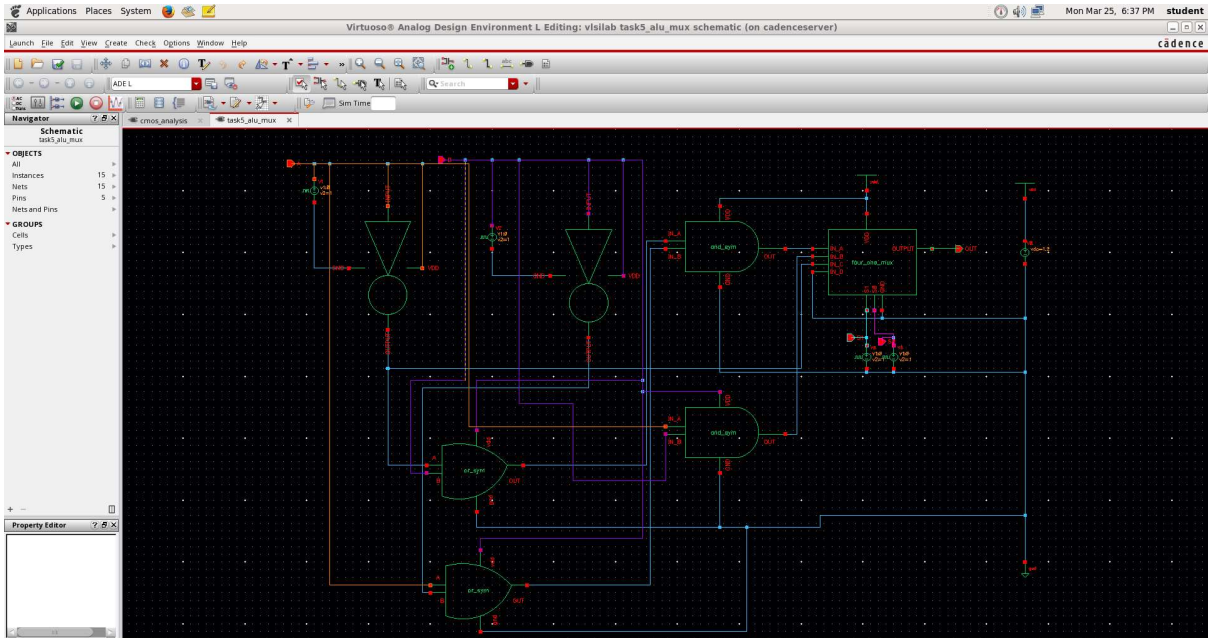
$$Y = S_1'S_0'I_0 + S_1'S_0I_1 + S_1S_0'I_2 + S_1S_0I_3$$

We implement this in Cadence using four 3-input AND gates and 2 2-input OR gate in CMOS logic with sizing ratio of 3:1.

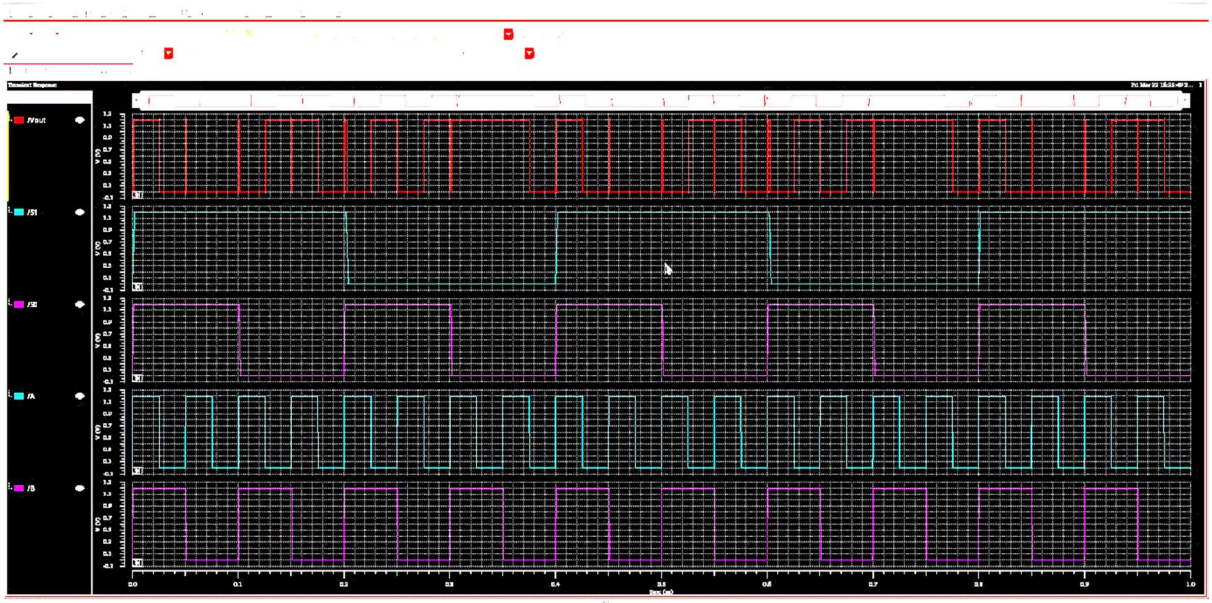
Now the **MUX** schematic will be:



Now the complete circuit to Implement the **ALU** is:



On running this circuit, we observe the following output:



The output truth table is:

S1	S0	Function
0	0	**A+B**
0	1	**~A**
1	0	**A^B**
1	1	**AB**

This is the required output.