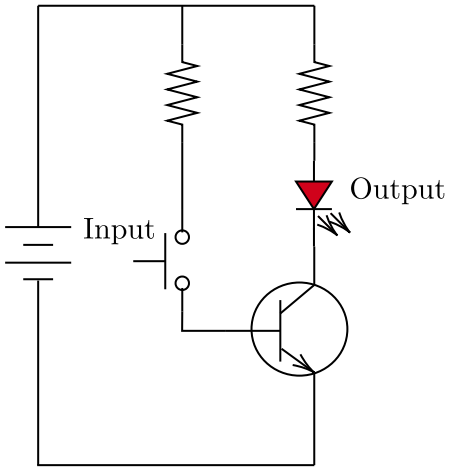
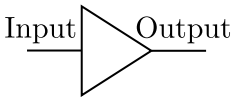
GATES USING TRANSISTORS

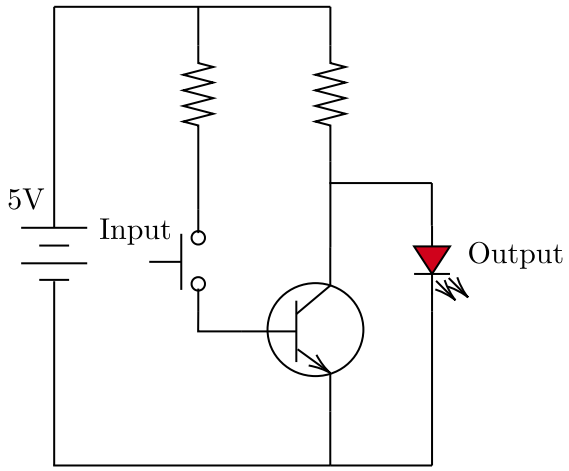
Buffer



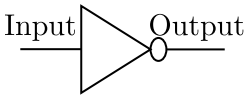
Input	Output
High	High
Low	Low



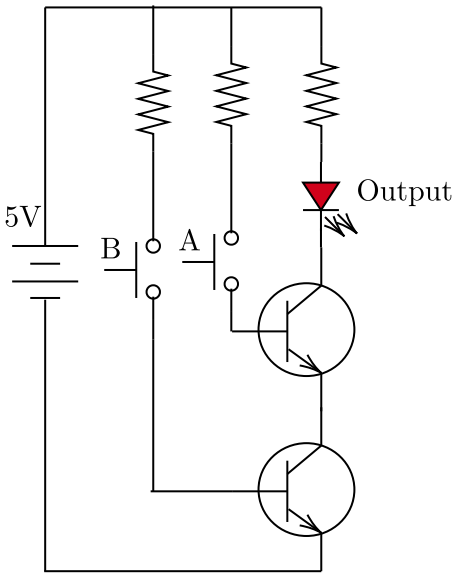
Inverter



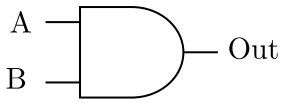
Input	Output
High	Low
Low	High



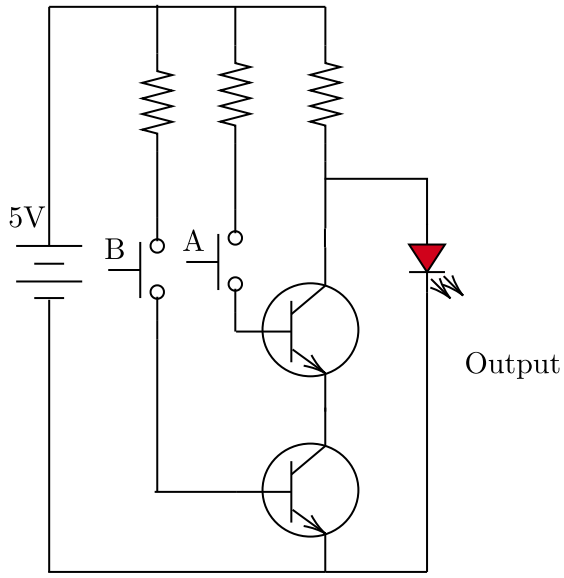
AND Gate



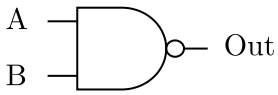
A	B	Out
Low	Low	Low
High	Low	Low
Low	High	Low
High	High	High



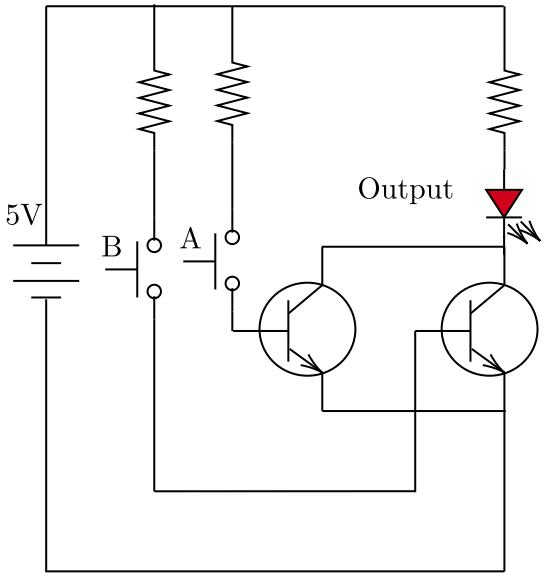
NAND Gate



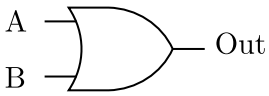
A	B	Out
Low	Low	High
High	Low	High
Low	High	High
High	High	Low



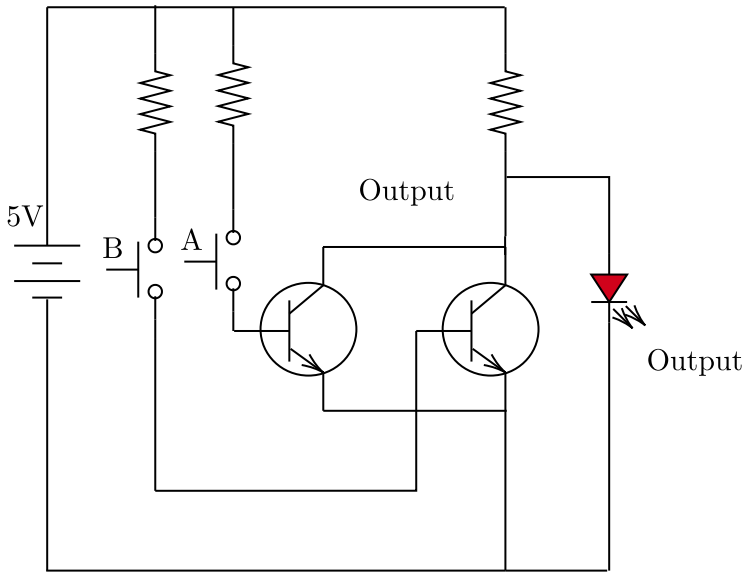
OR Gate



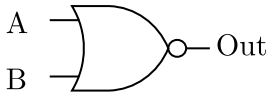
A	B	Out
Low	Low	Low
High	Low	High
Low	High	High
High	High	High



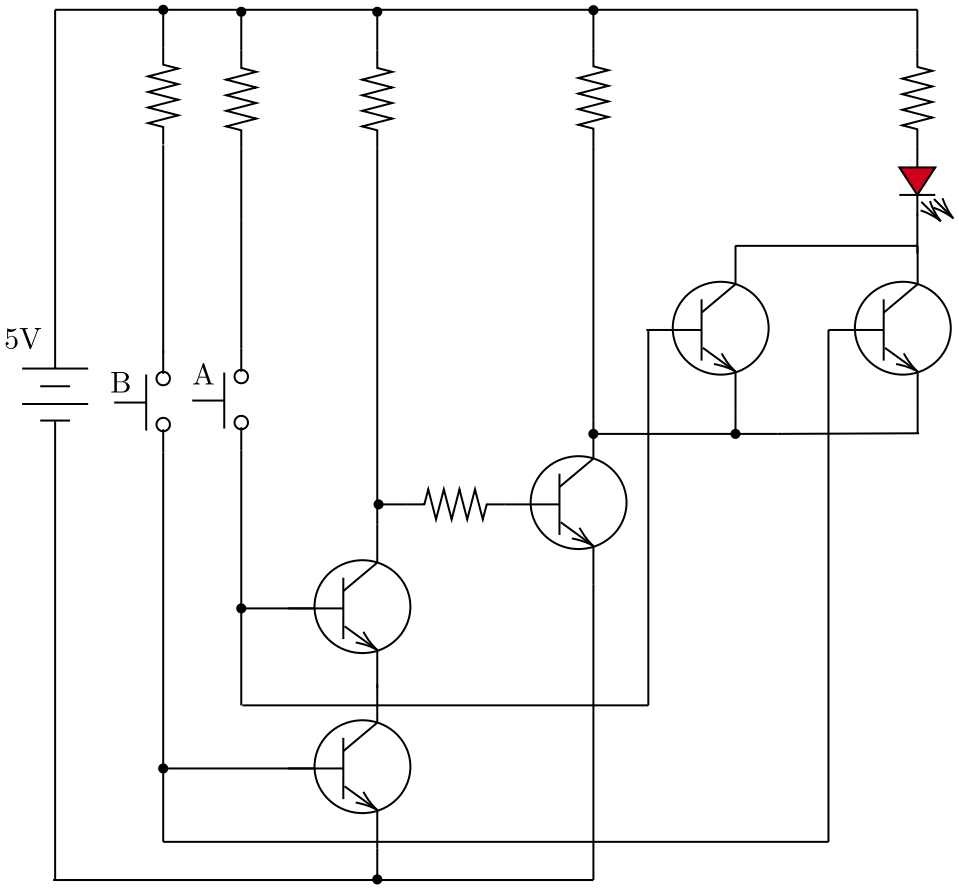
NOR Gate



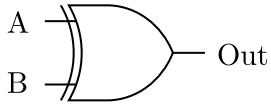
A	B	Out
Low	Low	High
High	Low	Low
Low	High	Low
High	High	Low



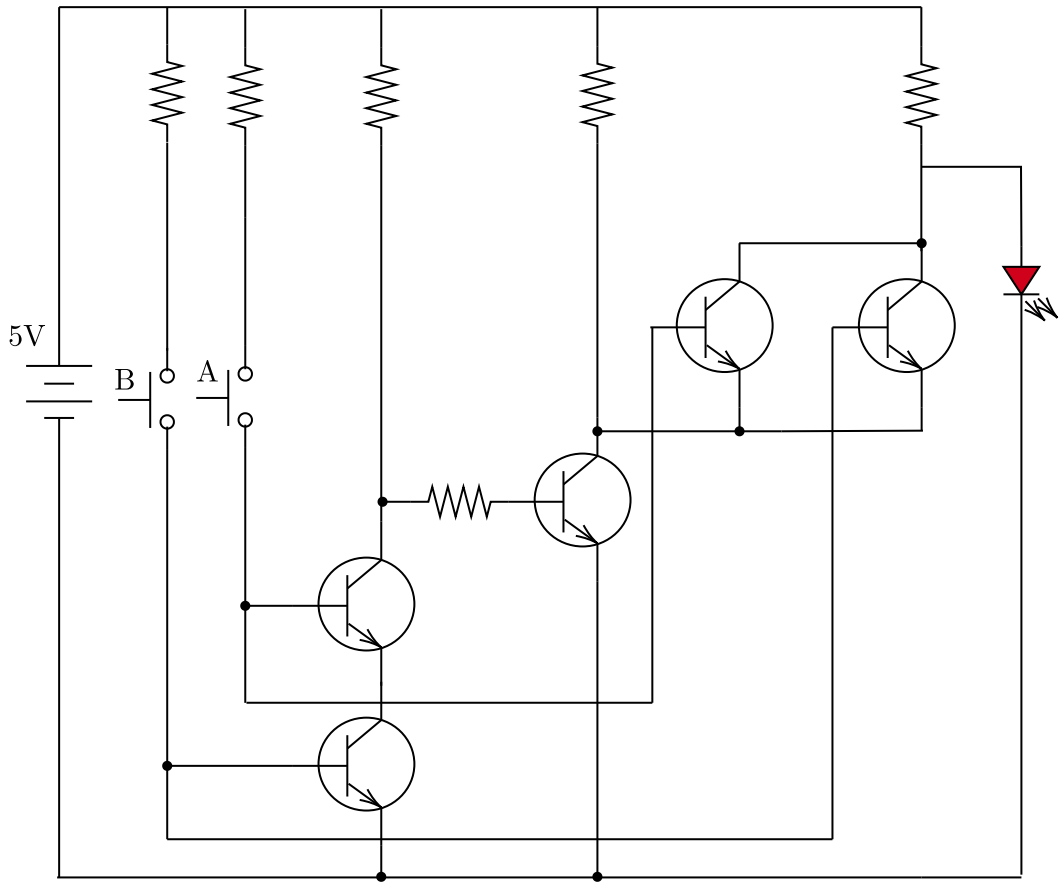
XOR Gate



A	B	Out
Low	Low	Low
High	Low	High
Low	High	High
High	High	Low



XNOR Gate



A	B	Out
Low	Low	High
High	Low	Low
Low	High	Low
High	High	High