Exp. No. (5)

Multiplexer and Demultiplexer

Object

To demonstrate a basic Multiplexer / Demultiplexer system, and become familiar with different types of multiplexer and demultiplexer.

Theory

1. *Multiplexer*

It is not necessary to use only discrete gates (AND, OR, NAND, NOR, EXOR, EXNOR) in the design of the combinational logic circuit, with the availability of the medium scale integrated (MSI) and large scale integrated (LSI), it is possible to design a very complicated circuits with a simple procedure, for example it is waste of time in most cases to try to minimize combinational logic circuit which has eight input using tabular method, while it will simpler if we used multiplexers.

A multiplexer is a network that has many inputs and one output, and the value of the output will be the value of one of inputs which will be decided by some select lines. The simplest type of multiplexer is the two line to one line data multiplexer. Let A be one of the inputs and B is the other input and Y is the output as in Fig. (1), and S is the select line, then

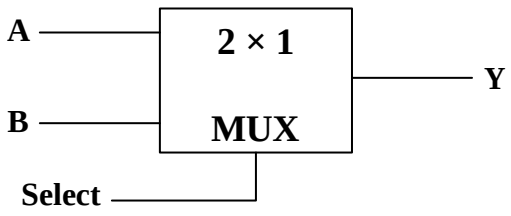


Fig. (1)
Two to One Line Multiplexer

Y = A if Select = 0.

Y = B if Select = 1.

The logic circuit diagram of the Two to One line Multiplexer is shown in Fig. (2).

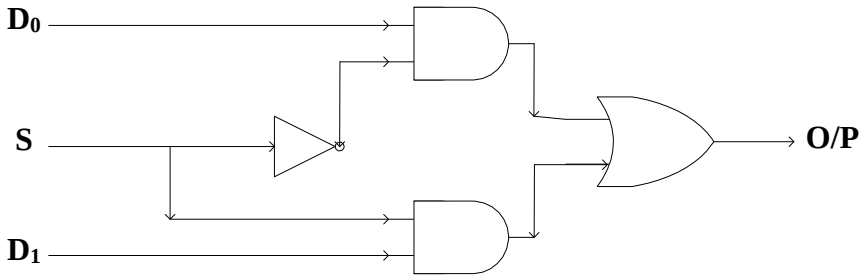


Fig. (2)
Logic Circuit of Two to One Line Multiplexer.

There are many 2 to 1 data selectors as a MSI, for example (7498, 74157, 74158) which contains four (quadruple) two-to-one data selectors in one chip.

There are other types of multiplexers 4-to-1 line, 8-to-1 line, and 16-to-1 line multiplexer, and the number of select lines of these multiplexer are 2, 3, and 4 lines respectively. Fig.(3) shows the four to one line multiplexer and its function block diagram.

To use the multiplexer in the design of combinational logic circuit, usually the truth table of K-map of function is used in which the table or the map is divided into 2, 4, 8, or 16 equal parts according to the type of multiplexer used. Some of the inputs of the combinational circuit is connected directly to the select lines while data lines of the multiplexer will be a function to the other inputs according to the sun map or sub tables.

Example:

Design the following expression using multiplexer.

$$F(A,B,C) = \overline{A}C + \overline{B}C + AB\overline{C}$$

Solution:

Number of variables = 3, it is better to use 4-to-1 line multiplexer, i.e.:

Number of selection lines = Number of variable -1.

The truth table of the function is shown below:

A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

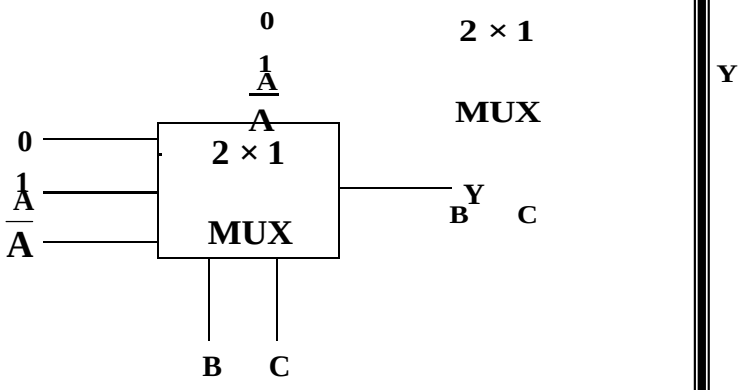


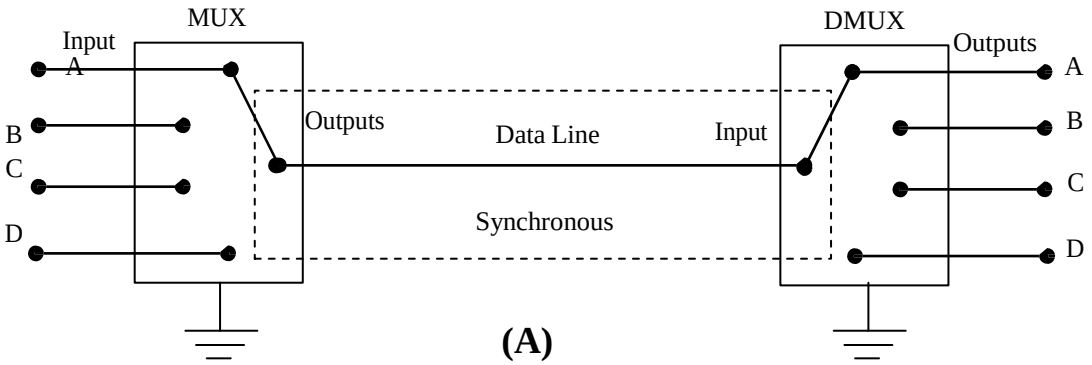
Fig. (4)

Fig. (4)

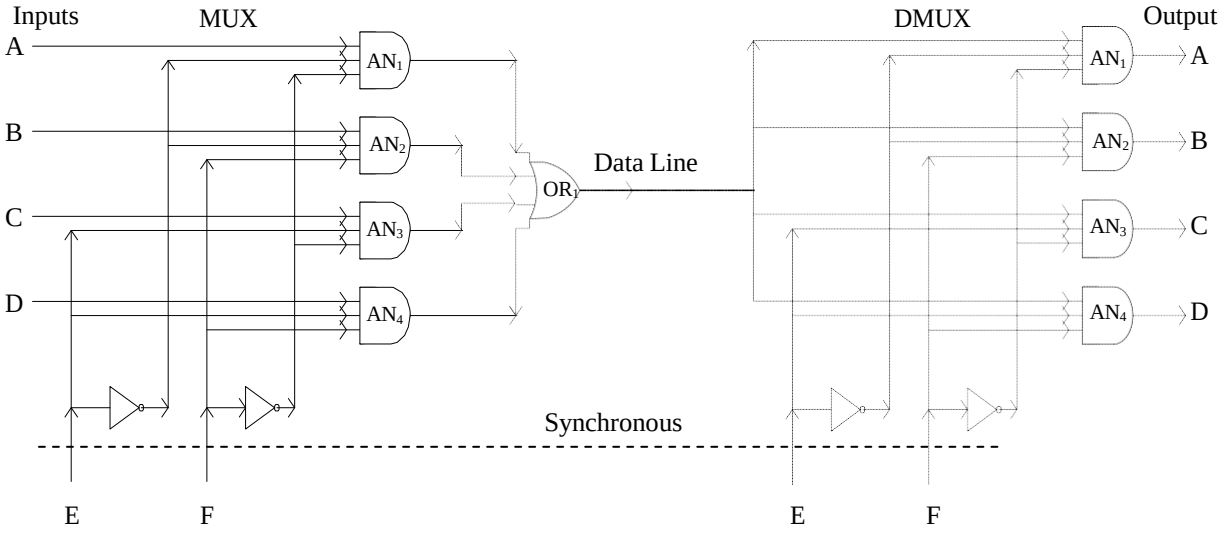
2. Demultiplexer

A demultiplexer basically reverses the multiplexing function. It is take data from one line and distribute them to given number of output lines. Fig. (3) shown a one to four line demultiplexer circuit. The input data line goes to all of the AND gates. The two select lines enable only one gate at a time and the data appearing on the input line will pas through the selected gate to the associated output line.

The simplest type of demultiplexer is the one to two lines DMUX. as shown in Fig. (5).



(A)



(B)

Fig. (3)
MUX/DMUX System: (A). Switch Analog. (B). Logic Gate Circuit .

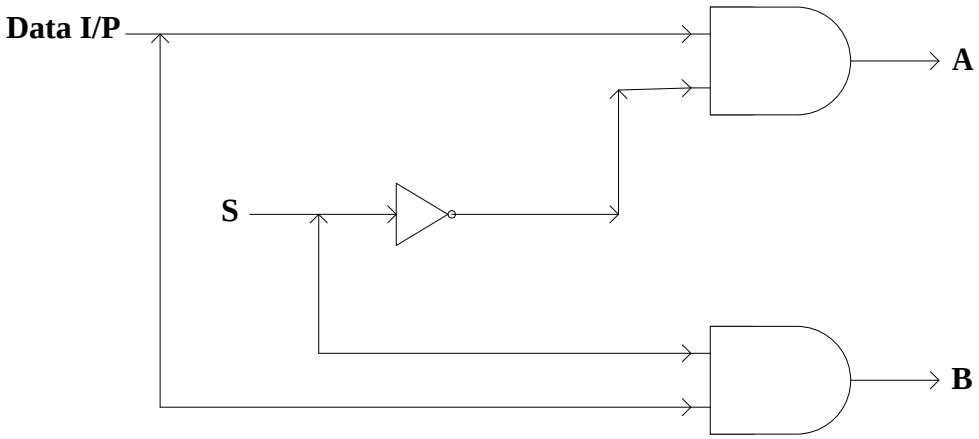


Fig. (5)
One to Two Lines Demultiplexer

Procedure

1. Connect the circuit as shown in Fig. (2).
2. Apply a signal to (A) input from clock (High Speed) of the logic INTIKIT unit. Draw the wave form.
3. Apply signal to (B) input from the pulse generator of amplitude = 5 Volt (p-p) frequency = 50 KHz. Draw the wave form.
4. Set the selector control input (S = 0), draw the output waveform from the multiplexer.
5. Set S = 1, draw the output waveform of the multiplexer.
6. Connect the output of MUX to the DMUX circuit of Fig. (5) and find the output of demultiplexer when S = 0 and when S = 1.

Discussion

1. Construct 8 × 1 MUX by using 2 × 1 MUX.
2. Construct 16 × 1 MUX by using 4 × 1 MUX and 2 × 4 Decoder.
3. Give some applications for the Multiplexer.
4. How many chips of 2×1 MUX you will need if you want to design 16×1 MUX.
5. Design the following expression using multiplexer:

   $$\mathbf{F(A,B,C) = \overline{A}\,\overline{B} + A\,C}$$

   Put the selection circuit S_1, S_0 = A C, A B, B C.