**Folder and Files details**

1. Constraint files :- This folder contain the timing constraint file used for synthesis and implementation
2. Report and Presentation:- This folder contains the report (RISC\_CPU\_Report.pdf) and Presentation(RISC\_CPU\_PPT.pdf)
3. Source Files:- This folder contains all the VHDL source files of the project
   1. RISC\_Main.vhd :- This is the top module where processor and Memory are instantiated
   2. RISC\_CPU.vhd :- Processor module file
   3. data\_path.vhd :- data path elements are instantiated and combined
   4. Controller\_and\_decoder.vhd :- controller module
   5. ALU\_MUX.vhd :- Mux unit controlling input of ALU
   6. ALU\_unit.vhd :- ALU unit design file
   7. Decoding.vhd :- Instruction decoder
   8. Interrupt\_Synchr.vhd :- Interrupt pulse detection circuit
   9. Program\_Counter.vhd :- Program counter file
   10. reg\_write\_mux.vhd :- Register write mux that control the date to be written to register file
   11. Register\_File.vhd :- Register file design
   12. Folder IP :- This contains the files associated with the data memory and instruction memory generated using distributed ram block of Xilinx
4. TestBench :- This folder contains the test bench used for testing the RISC processor.
   1. RISC\_TB.vhd :- Testbench file. Use RISC\_Main.vhd as the test module
   2. Instr.txt :- Text file having instruction saved. These instructions are written to instruction memory from test bench