***CIRCUIT DESIGN AND SIMULATION MARATHON BY IIT BOMBAY FOSSEE TEAM WITH VSD***

3-bit-FLASH-ADC-using-eSim

Abstract

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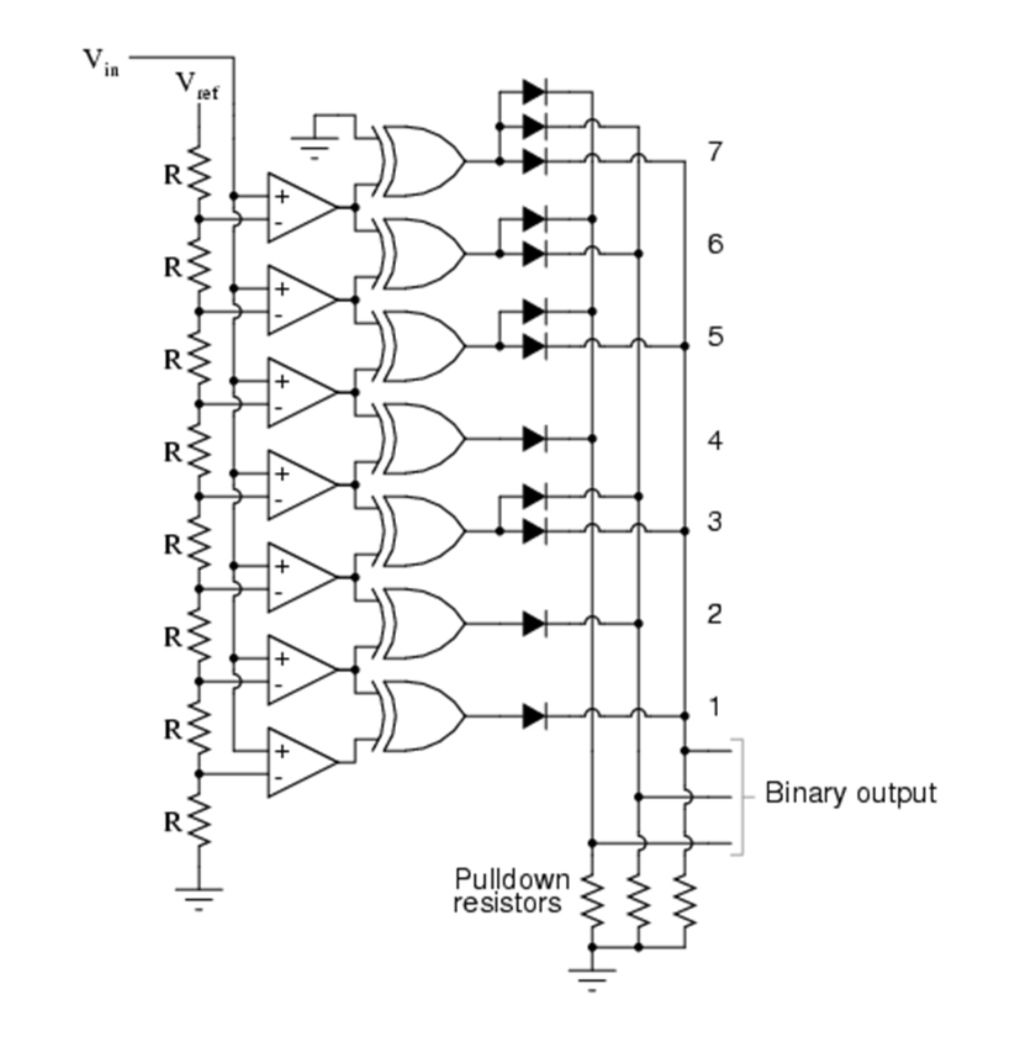
Output Waveform

Author

**Abstract**

Flash ADC is also known as the parallel A/D converter. It is formed of a series of comparators, each one comparing the input signal to an unique reference voltage. The comparator outputs connect to the inputs of a priority encoder circuit built with gates and diode which then produces a binary output. Flash converters are extremely fast compared to many other types of ADCs. This paper explains the simulation of flash adc using esim

**Reference Circuit Diagram**



**Circuit Details**

This three-bit flash ADC requires seven comparators. A four-bit version would require 15 comparators. With each additional output bit, the number of required comparators doubles. It has seven op-amps and seven Exclusive-OR gates. Vref is a stable reference voltage provided by a precision voltage regulator as part of the converter circuit and Vin is given as 5V. The Vref used here is PWL wave and its connected to non – inverting terminal of the op-amp.

**Methodology**

Verilog code for Ex-OR Gate is created and simulated using MakerChip. The Code is dumped in Ngveri and model is created. Schematics is drawn on eSim. Generating Netlist for the mixed signal circuit. Kicad to Ngspice conversion is done by adding simulation parameters for the circuit. Simulation is done.

**Software Used**

eSim:

It is an Open Source EDA developed by FOSSEE, IIT Bombay. It is used for electronic circuit simulation. It is made by the combination of two software namely NgSpice and KiCAD. For more details refer: <https://esim.fossee.in/home>

NgSpice:

It is an Open Source Software for Spice Simulations. For more details refer: <http://ngspice.sourceforge.net/docs.html>

**Makerchip**:

It is an Online Web Browser IDE for Verilog/System-verilog/TL-Verilog Simulation. Refer <https://www.makerchip.com/>

Verilator:

It is a tool which converts Verilog code to C++ objects. Refer: <https://www.veripool.org/verilator/>

**Verilog Code**

module flashadc\_pratyusha(a,b,c);

input a,b;

output c;

Xor x(c,a,b);

endmodule

MakerChip

Code:

\TLV\_version 1d: tl-x.org \SV /\* verilator lint\_off UNUSED\*/ /\* verilator lint\_off DECLFILENAME\*/ /\* verilator lint\_off BLKSEQ\*/ /\* verilator lint\_off WIDTH\*/ /\* verilator lint\_off SELRANGE\*/ /\* verilator lint\_off PINCONNECTEMPTY\*/ /\* verilator lint\_off DEFPARAM\*/ /\* verilator lint\_off IMPLICIT\*/ /\* verilator lint\_off COMBDLY\*/ /\* verilator lint\_off SYNCASYNCNET\*/ /\* verilator lint\_off UNOPTFLAT / / verilator lint\_off UNSIGNED\*/ /\* verilator lint\_off CASEINCOMPLETE\*/ /\* verilator lint\_off UNDRIVEN\*/ /\* verilator lint\_off VARHIDDEN\*/ /\* verilator lint\_off CASEX\*/ /\* verilator lint\_off CASEOVERLAP\*/ /\* verilator lint\_off PINMISSING\*/ /\* verilator lint\_off BLKANDNBLK\*/ /\* verilator lint\_off MULTIDRIVEN\*/ /\* verilator lint\_off WIDTHCONCAT\*/ /\* verilator lint\_off ASSIGNDLY\*/ /\* verilator lint\_off MODDUP\*/ /\* verilator lint\_off STMTDLY\*/ /\* verilator lint\_off LITENDIAN\*/ /\* verilator lint\_off INITIALDLY\*/

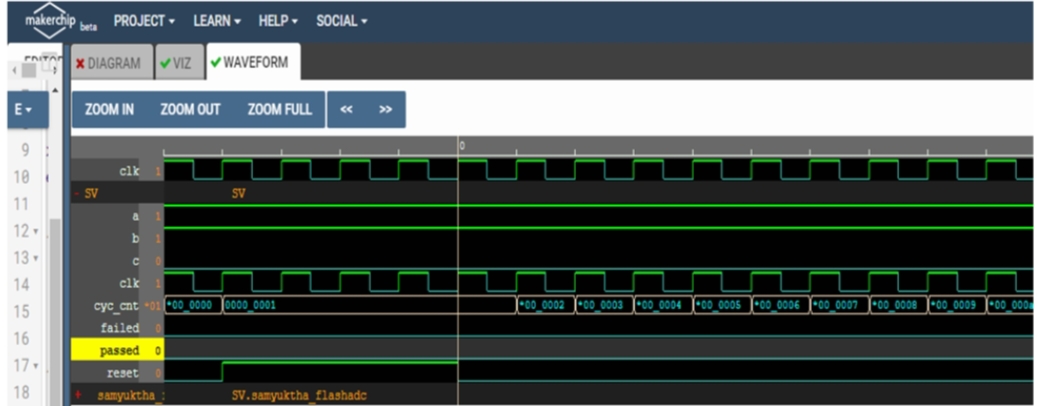
//Your Verilog/System Verilog Code Starts Here: module pratyusha\_flashadc(c,a,b); input a,b; output c; xor (c,a,b); endmodule

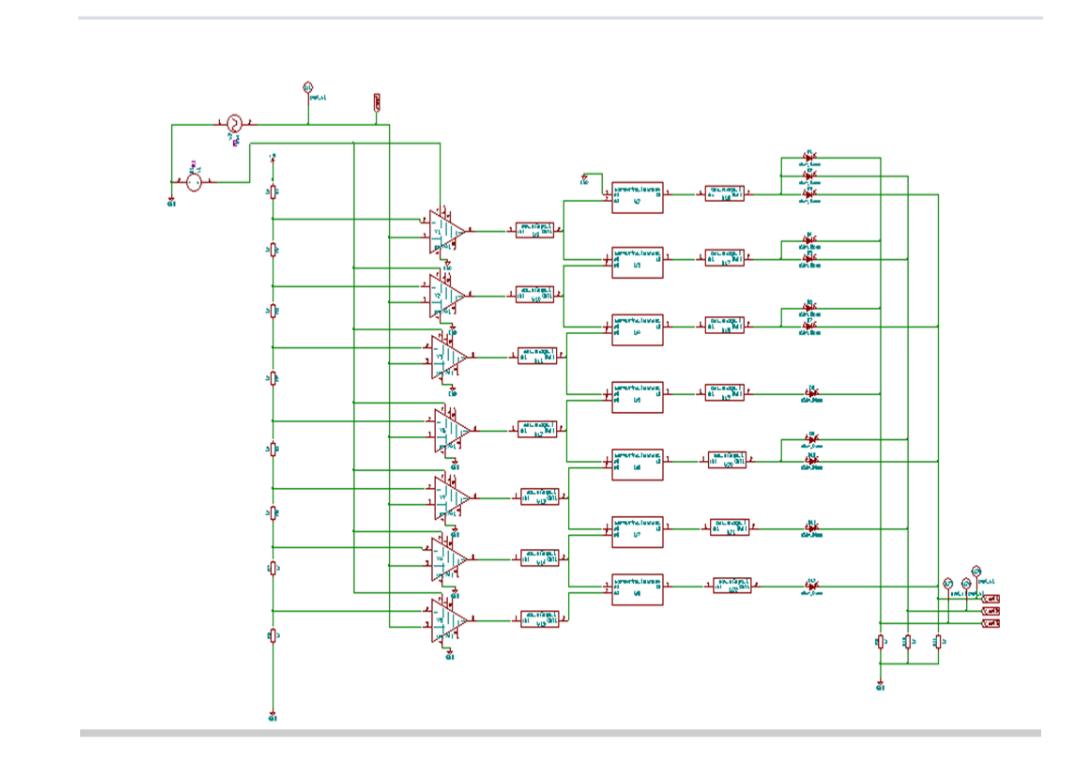
//Top Module Code Starts here: module top(input logic clk, input logic reset, input logic [31:0] cyc\_cnt, output logic passed, output logic failed); logic a;//input logic b;//input logic c;//output //The $random() can be replaced if user wants to assign values assign a = $random(); assign b = $random(); pratyusha\_flashadc pratyusha\_flashadc(.a(a), .b(b), .c(c));

\TLV //Add \TLV here if desired

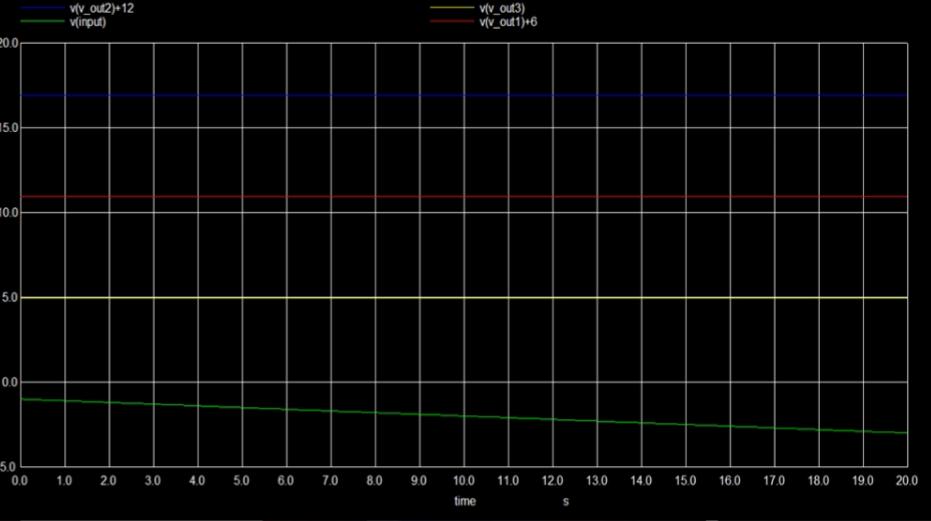
\SV endmodule

**Waveform**



**Schemat**ic

**Output Waveforms**



**Author**

Sajja Pratyusha

Pre-Final Year B.tech ECE

Rajiv Gandhi University of Knowledge Technologies

Mail : [sajjapratyusha@gmail.com](mailto:sajjapratyusha@gmail.com)

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