OpenROAD Flow Scripts on a Ibex Pipeline

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Abstract— In this paper, using OpenROAD Flow Scripts (ORFS) on a specific design project. we see the two-stage pipeline design of the Ibex CPU powering RISC-V 32-bit ISA Extensions. This OpenROAD Flow design aims for automated, no-human-in-the-loop digital circuit design with 24-hour turnaround time.

Keywords— Ibex, RISC-V, pipeline, OpenROAD,

I. INTRODUCTION

Ibex has 2-stage pipeline. One is Instruction Fetch and another one is Instruction Decode and Execute. Ibex can configure to have a third pipeline stage i.e., Writeback. The OpenROAD Flow project aims to automate digital circuit design with no human intervention and achieve a 24hour turnaround time. In this paper, we see several configurations, Ibex RISC-V core.

II. DESIGN FLOW OVERVIEW

IF, ID these 2-stage pipeline of the Ibex CPU powering. The components can be configured at design time to support the RISC-V 32bit ISA extensions. We were able to achieve the reducing time delay of less than 24 hours, which is impressive considering the complexity of the design.

Ibex offers several configuration parameters to meet the needs of various application scenarios. The options include different choices for the architecture of the multiplier unit, as well s a range of performance and security features.

III. Improvement with Ibex

Ibex was initially developed as part of the PULP platform under the name of “Zero-riscy” and has contributed to lowRISC. Which lowRISC is focusing for performance evolution and design verification. Ibex with basic system targets simulation. It is intended to provide an easy way to get bare metal binaries running on Ibex in simulation.

Ibex is production-quality open source 32-bit RISC-V CPU core written in system Verilog. The CPU core is heavily parametrizable.

Ibex supports the Integer Multiplication, Division, compressed, Bit Manipulation extensions. Reduces execution time improves fastest runtime.

IV. CONCLUSIONS

In conclusion, Scripts on a Ibex specific design project has been largely positive. The use of Ibex greatly simplifies the design process and allows for rapid exploration of design alternatives. However, Ibex compatibility and versioning, as well as careful analysis of design results, is necessary to avoid unexpected issues. Majorly it reduces the time delay and improves execution.

So by using the RISC-V cores from the OpenROAD flow-scripts of Ibex. The fastest Runtime from RTL-GDSII with good performance and area. Time delay will be reduced for execution. And no-human-in-the-loop digital.

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