

Place **R2** or **R34** resistors as close as possible to the input pin of TLV3801

IN+

R2 1/49R9

GND

IN-

R34 1/49R9

GND

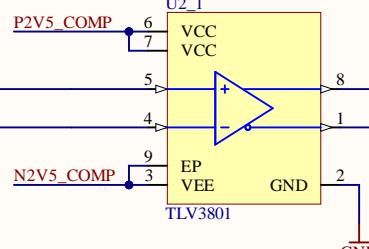
TLV3801

Input voltage range: VEE+1.5 ... VCC+0.1 [V]
(-1 ... 2.6 [V])

Input offset voltage: typ. $\sim +0.5$ mV, max. $\sim +5$ mV

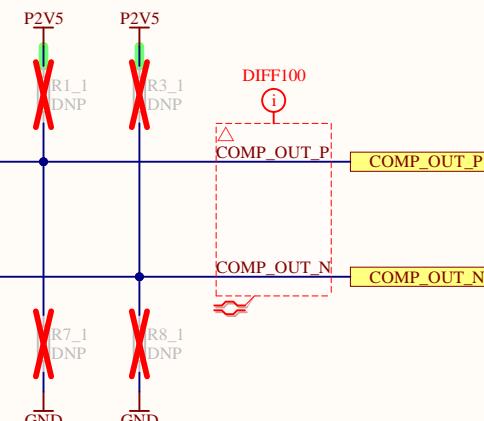
Input hysteresis: 2 mV

Common-mode voltage range: VEE+1.5 ... VCC [V]



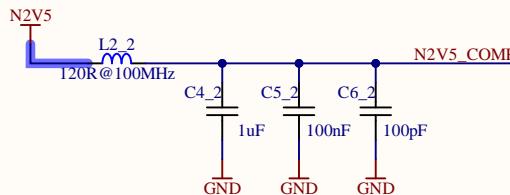
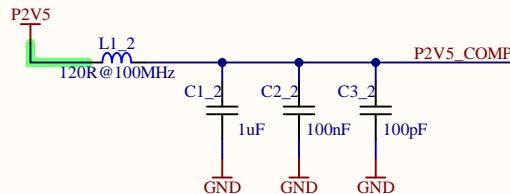
EP connection of **U2** verified with TI support.

Alternative configurations for LVDS termination.



Project:	Time_Sampling_Oscilloscope.PrjPcb	Engineer: Szymon Jedliński	Revision: 1.0	WEITIISE ul. Nowowiejska 15/19 00-665 Warszawa
Title:	*	Drawn by:Szymon Jedliński	Sheet: 2	
File:	Comparator.SchDoc	Checked by:*	Total Sheet: 11	
Variant:	Basic Assembly	Approved by:*	Date: 15.08.2023	





Place **R2** or **R34** resistors as close as possible to the input pin of TLV3801



ComparatorA: **R34** DNP
ComparatorB: **R2** DNP

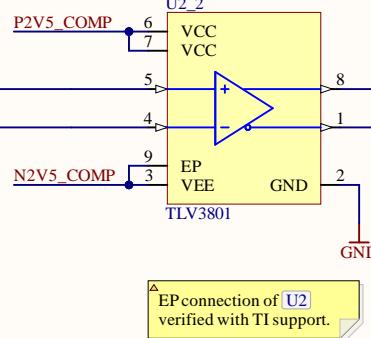
TLV3801

Input voltage range: VEE+1.5 ... VCC+0.1 [V]
(-1 ... 2.6 [V])

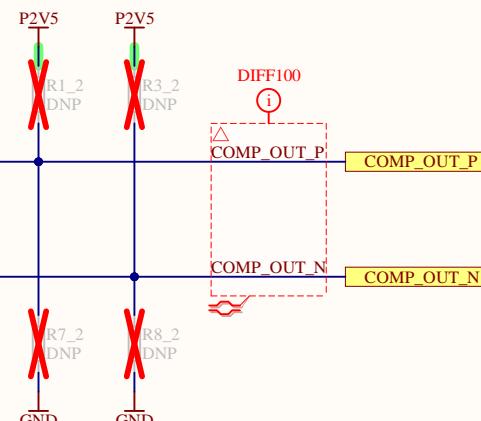
Input offset voltage: typ. $\sim +0.5$ mV, max. $\sim +5$ mV

Input hysteresis: 2 mV

Common-mode voltage range: VEE+1.5 ... VCC [V]

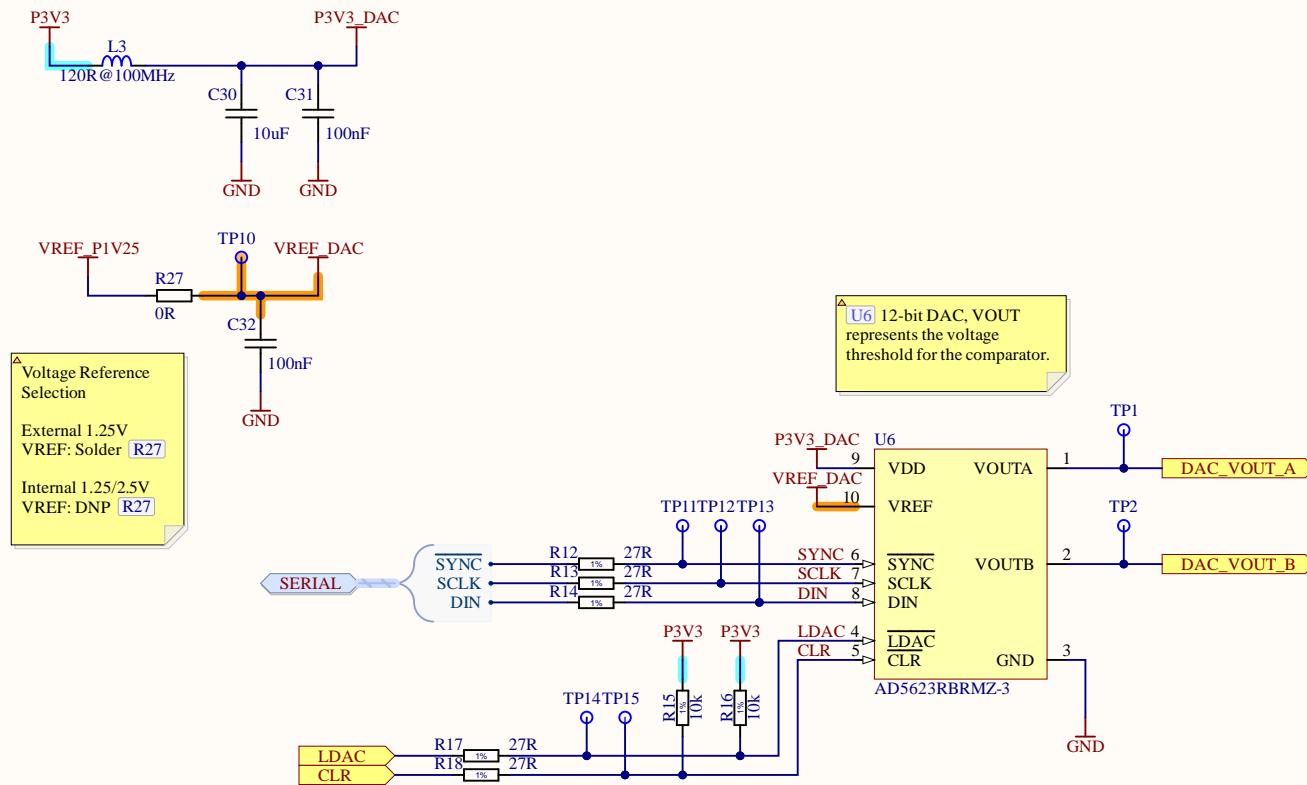


Alternative configurations for LVDS termination.

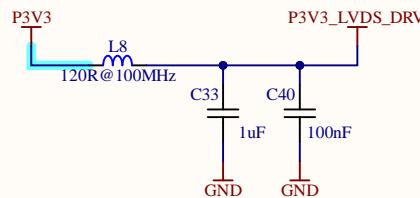
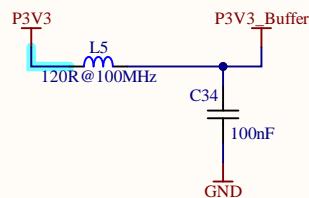


Project:	Time_Sampling_Oscilloscope.PrjPcb	Engineer: Szymon Jedliński	Revision: 1.0	WEITIISE ul. Nowowiejska 15/19 00-665 Warszawa
Title:	*	Drawn by:Szymon Jedliński	Sheet: 2	
File:	Comparator.SchDoc	Checked by:*	Total Sheet: 11	
Variant:	Basic Assembly	Approved by:*	Date: 15.08.2023	



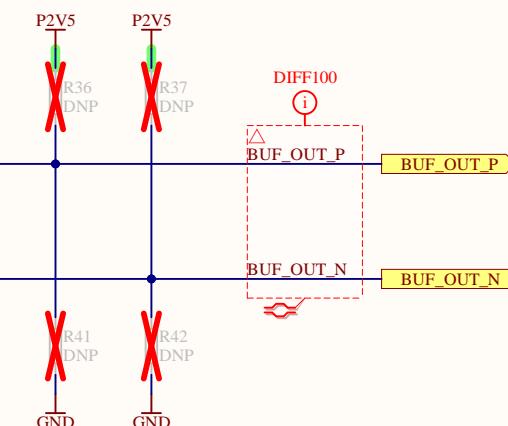
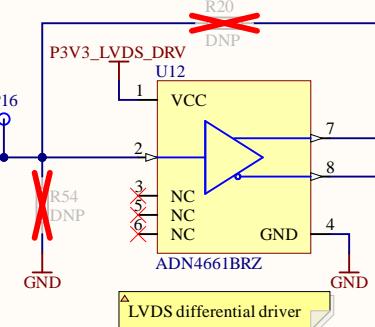
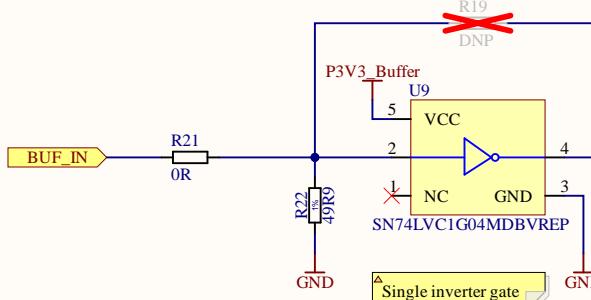


A



△ Alternative configurations for LVDS termination.

B



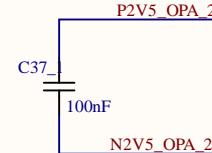
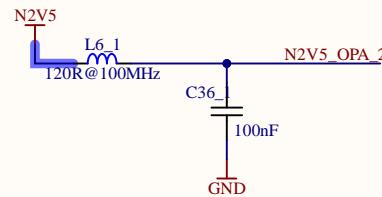
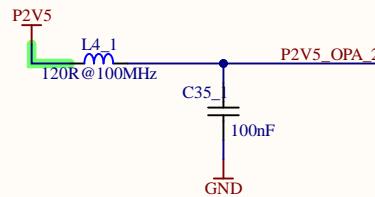
C

D

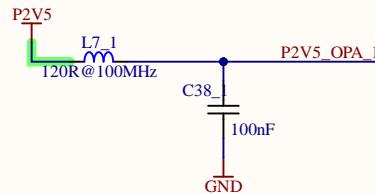
Project:	Time_Sampling_Oscilloscope.PrjPcb	Engineer: Szymon Jedliński	Revision: 1.0	WEITIISE ul. Nowowiejska 15/19 00-665 Warszawa
Title:	*	Drawn by: Szymon Jedliński	Sheet: 4	
File:	External_Trigger_Buffer.SchDoc	Checked by:*	Total Sheet: 11	
Variant:	Basic Assembly	Approved by:*	Date: 14.08.2023	



A

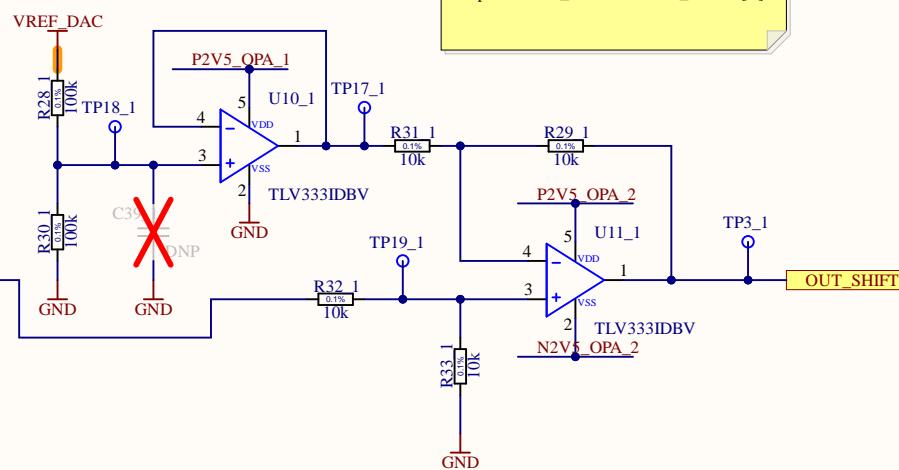


B



Voltage divider + voltage follower
Out = VREF_DAC/2

Non-inverting op amp with inverting positive reference
Input: 0..VREF_DAC [V]
Output: -VREF_DAC/2...VREF_DAC/2 [V]



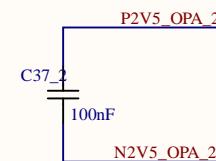
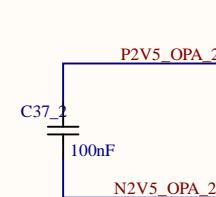
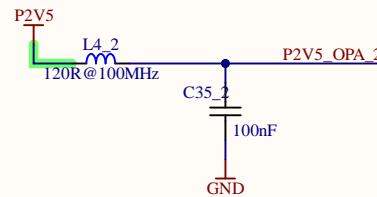
C

D

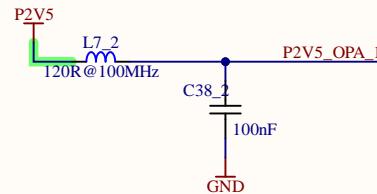
Project:	Time_Sampling_Oscilloscope.PrjPcb	Engineer: Szymon Jedliński	Revision: 1.0	WEITI ISE ul. Nowowiejska 15/19 00-665 Warszawa
Title:	*	Drawn by: Szymon Jedliński	Sheet: 5	
File:	Bipolar_Offset_Shifter.SchDoc	Checked by:*	Total Sheet: 11	
Variant:	Basic Assembly	Approved by:*	Date: 15.08.2023	



A

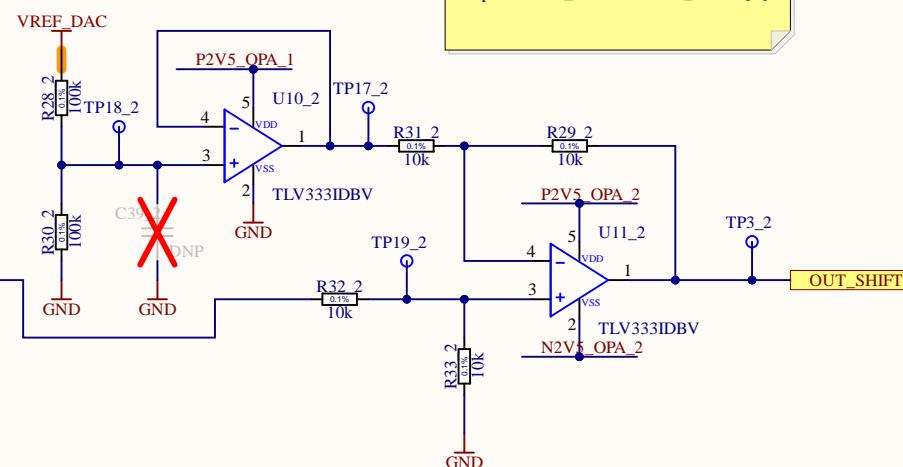


B



Voltage divider + voltage follower
Out = VREF_DAC/2

Non-inverting op amp with inverting positive reference
Input: 0..VREF_DAC [V]
Output: -VREF_DAC/2...VREF_DAC/2 [V]



C

D

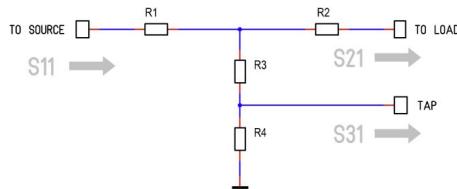
Project:	Time_Sampling_Oscilloscope.PrjPcb	Engineer: Szymon Jedliński	Revision: 1.0	WEITIISE ul. Nowowiejska 15/19 00-665 Warszawa
Title:	*	Drawn by: Szymon Jedliński	Sheet: 5	
File:	Bipolar_Offset_Shifter.SchDoc	Checked by:*	Total Sheet: 11	
Variant:	Basic Assembly	Approved by:*	Date: 15.08.2023	



A
Resistive Unequal Power Divider
S21 0.5 [dB]
S31 31 [dB]
<https://www.changpuak.ch/electronics/ResistivePowerSignalITap.php>

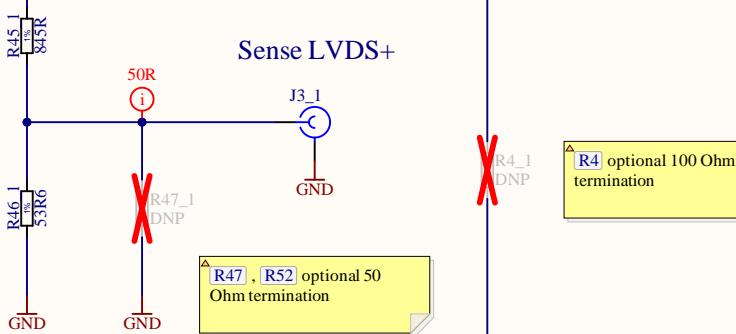
Resistive Power Signal Tap Designer

aka RF Sampler, Resistive Unequal Power Divider



C

Mainline Loss, S21 [dB]	0.50	+ 0.1	- 0.1
Coupling, S31 [dB]	30.81		
System Impedance [Ω]	50.00		
R1, R2 [Ω]	1.439		
R3 [Ω]	842.368		
R4 [Ω]	53.056		



D

Project:	Time_Sampling_Oscilloscope.PrjPcb	Engineer: Szymon Jedliński	Revision: 1.0	WEITIISE ul. Nowowiejska 15/19 00-665 Warszawa
Title:	*	Drawn by: Szymon Jedliński	Sheet: 6	
File:	Resistive_Unequal_Power_Divider.SchDoc	Checked by:*	Total Sheet: 11	
Variant:	Basic Assembly	Approved by:*	Date: 15.08.2023	

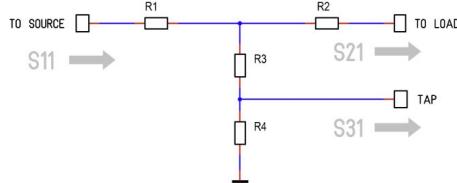


A

Resistive Unequal Power Divider
S21 0.5 [dB]
S31 31 [dB]
<https://www.changpuak.ch/electronics/ResistivePowerSignalITap.php>

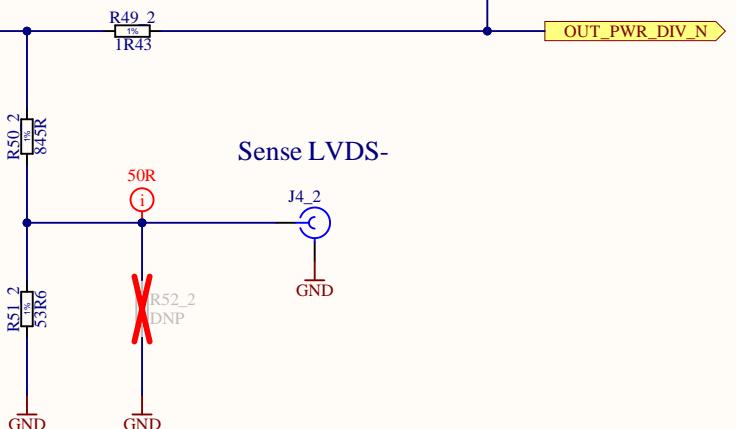
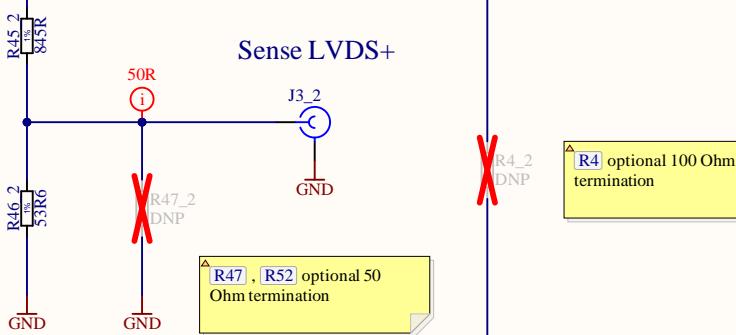
Resistive Power Signal Tap Designer

aka RF Sampler, Resistive Unequal Power Divider



C

Mainline Loss, S21 [dB]	0.50	+ 0.1	- 0.1
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System Impedance [Ω]	50.00		
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R3 [Ω]	842.368		
R4 [Ω]	53.056		



D

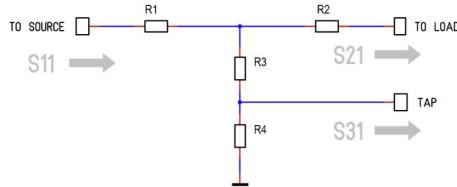
Project:	Time_Sampling_Oscilloscope.PrjPcb	Engineer: Szymon Jedliński	Revision: 1.0	WEITIISE ul. Nowowiejska 15/19 00-665 Warszawa
Title:	*	Drawn by: Szymon Jedliński	Sheet: 6	
File:	Resistive_Unequal_Power_Divider.SchDoc	Checked by:*	Total Sheet: 11	
Variant:	Basic Assembly	Approved by:*	Date: 15.08.2023	



A
Resistive Unequal Power Divider
S21 0.5 [dB]
S31 31 [dB]
<https://www.changpuak.ch/electronics/ResistivePowerSignalITap.php>

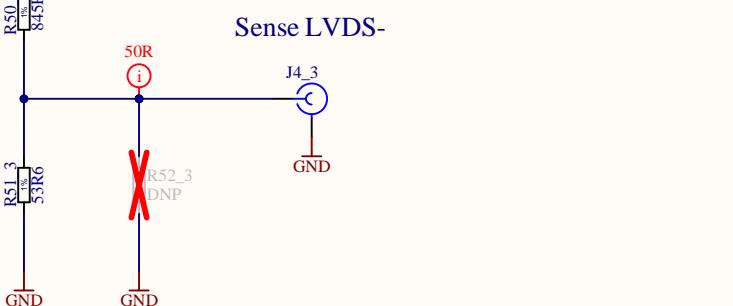
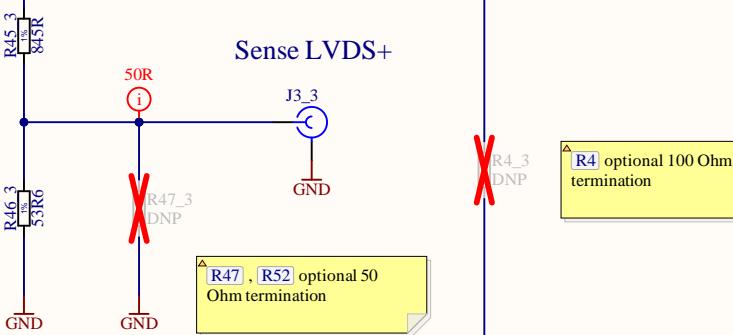
Resistive Power Signal Tap Designer

aka RF Sampler, Resistive Unequal Power Divider



C

Mainline Loss, S21 [dB]	0.50	+ 0.1	- 0.1
Coupling, S31 [dB]	30.81		
System Impedance [Ω]	50.00		
R1, R2 [Ω]	1.439		
R3 [Ω]	842.368		
R4 [Ω]	53.056		



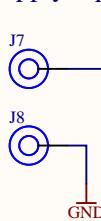
Project:	Time_Sampling_Oscilloscope.PrjPcb	Engineer: Szymon Jedliński	Revision: 1.0	WEITE ISE ul. Nowowiejska 15/19 00-665 Warszawa
Title:	*	Drawn by: Szymon Jedliński	Sheet: 6	
File:	Resistive_Unequal_Power_Divider.SchDoc	Checked by:*	Total Sheet: 11	
Variant:	Basic Assembly	Approved by:*	Date: 15.08.2023	



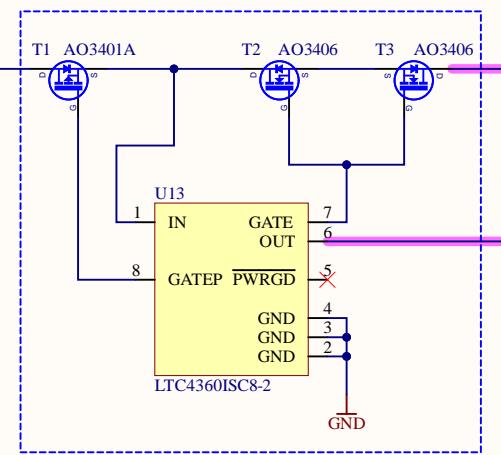
A

A

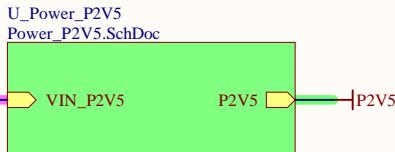
Power supply input



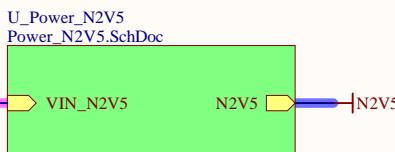
Negative voltage protection, overvoltage, reverse current protection



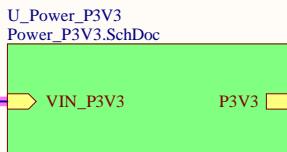
2.5V LDO



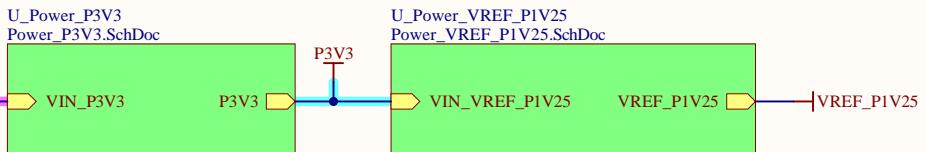
-2.5V LDO



3.3V LDO



1.25V Voltage reference



Project:	Time_Sampling_Oscilloscope.PrjPcb	Engineer: Szymon Jedliński	Revision: 1.0	WEITE ISE ul. Nowowiejska 15/19 00-665 Warszawa
Title:	*	Drawn by: Szymon Jedliński	Sheet: 7	
File:	Power_Supply.SchDoc	Checked by: *	Total Sheet: 11	
Variant:	Basic Assembly	Approved by: *	Date: 13.08.2023	



A

A

B

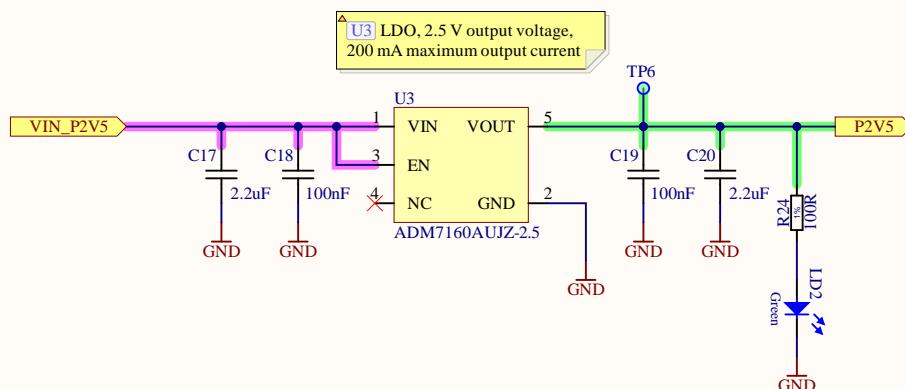
B

C

C

D

D



Project:	Time_Sampling_Oscilloscope.PrjPcb	Engineer:	Szymon Jedliński	Revision:	1.0	WEITIISE ul. Nowowiejska 15/19 00-665 Warszawa
Title:	*	Drawn by:	Szymon Jedliński	Sheet:	8	
File:	Power_P2V5.SchDoc	Checked by:	*	Total Sheet:	11	
Variant:	Basic Assembly	Approved by:	*	Date:	13.08.2023	



A

A

B

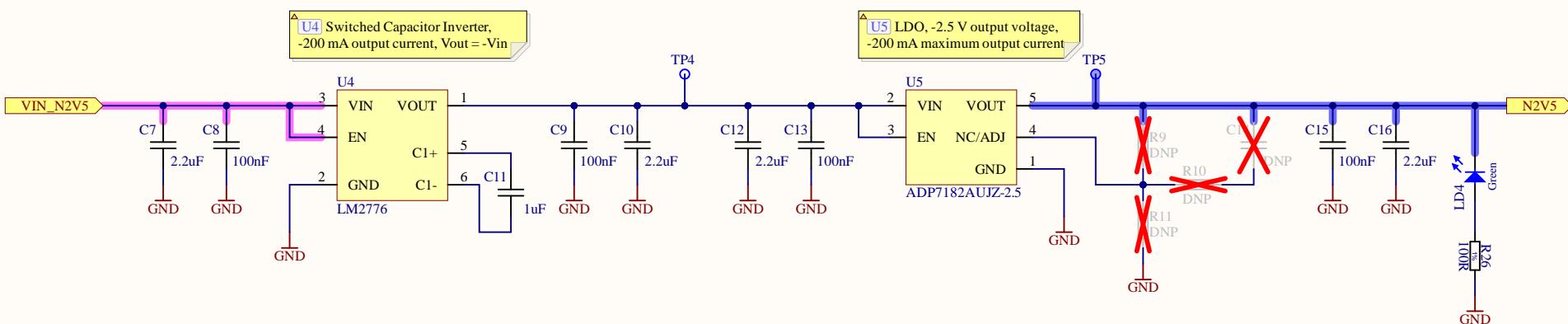
B

C

C

D

D



Project:	Time_Sampling_Oscilloscope.PrjPcb	Engineer: Szymon Jedliński	Revision: 1.0	WEITE ISE ul. Nowowiejska 15/19 00-665 Warszawa
Title:	*	Drawn by: Szymon Jedliński	Sheet: 9	
File:	Power_N2V5.SchDoc	Checked by:*	Total Sheet: 11	
Variant:	Basic Assembly	Approved by:*	Date: 13.08.2023	

A

B

C

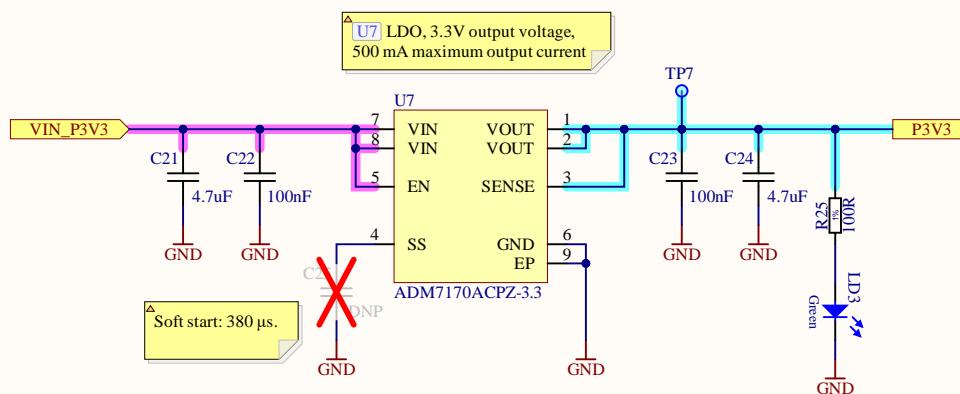
D

A

B

C

D



Project:	Time_Sampling_Oscilloscope.PrjPcb	Engineer: Szymon Jedliński	Revision: 1.0	WEITI ISE ul. Nowowiejska 15/19 00-665 Warszawa
Title:	*	Drawn by: Szymon Jedliński	Sheet: 10	
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Variant:	Basic Assembly	Approved by:*	Date: 13.08.2023	

A

A

B

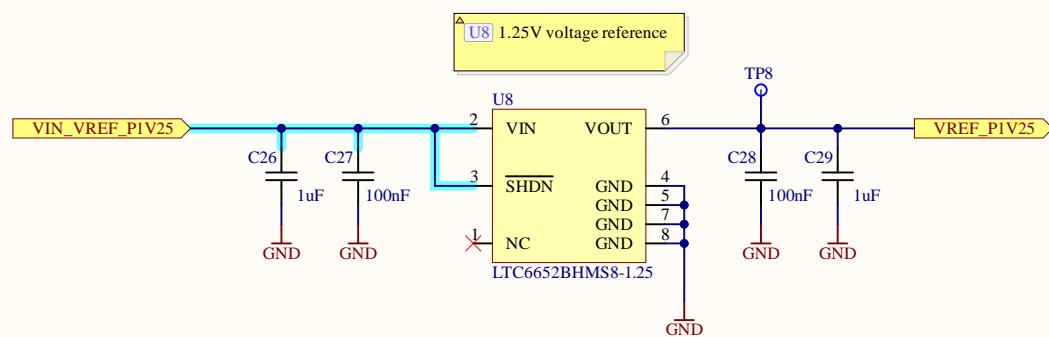
B

C

C

D

D



Project:	Time_Sampling_Oscilloscope.PrjPcb	Engineer: Szymon Jedliński	Revision: 1.0	WEITI ISE ul. Nowowiejska 15/19 00-665 Warszawa
Title:	*	Drawn by: Szymon Jedliński	Sheet: 11	
File:	Power_VREF_P1V25.SchDoc	Checked by:*	Total Sheet: 11	
Variant:	Basic Assembly	Approved by:*	Date: 06.08.2023	

