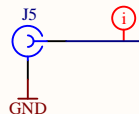


A

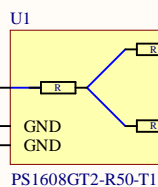
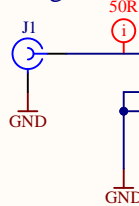
Sense IN+



A higher input voltage range requires selecting DAC's internal 2.5V voltage reference. Be careful about the power dissipated in a splitter and the 50 Ohm terminating resistors.

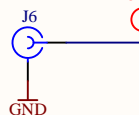
Input impedance: 50 Ohm  
Recommended input voltage range: +/- 2V  
Maximum input voltage range: +/- 2.5V

Input Signal

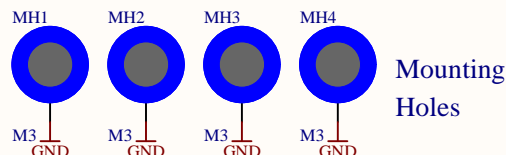
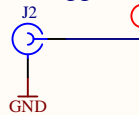


6dB resistive splitter  
Amplitude range (recommended input voltage range): +/- 0.5V

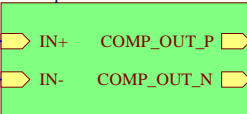
Sense IN-



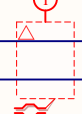
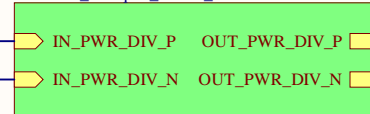
External Trigger



## Measuring section

U\_ComparatorA  
Comparator.SchDoc

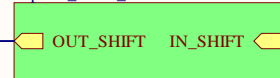
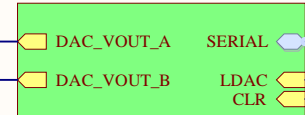
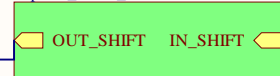
DIFF100

U\_Resistive\_Unequal\_Power\_DividerA  
Resistive\_Unequal\_Power\_Divider.SchDoc

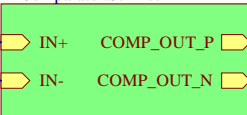
DIFF100



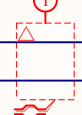
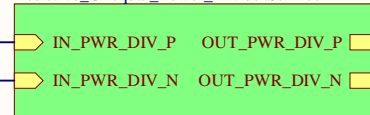
## Voltage Threshold

U\_Bipolar\_offset\_shifterA  
Bipolar\_offset\_shifter.SchDocU\_DAC  
DAC.SchDocU\_Bipolar\_offset\_shifterB  
Bipolar\_offset\_shifter.SchDoc

## Triggering Section

U\_ComparatorB  
Comparator.SchDoc

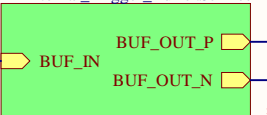
DIFF100

U\_Resistive\_Unequal\_Power\_DividerB  
Resistive\_Unequal\_Power\_Divider.SchDoc

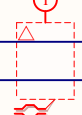
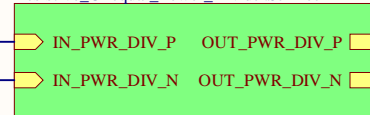
DIFF100



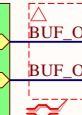
## External Trigger Buffer

U\_External\_Trigger\_Buffer  
External\_Trigger\_Buffer.SchDoc

DIFF100

U\_Resistive\_Unequal\_Power\_DividerB  
Resistive\_Unequal\_Power\_Divider.SchDoc

DIFF100



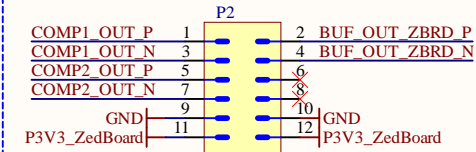
## Zedboard Connectors

## Zedboard Connectors

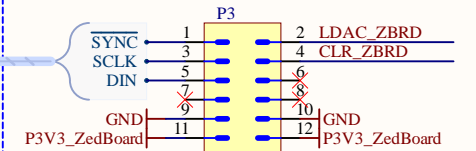
Datasheet:  
[https://digilent.com/reference/\\_media/reference/programmable-logic/zedboard/zedboard\\_ug.pdf](https://digilent.com/reference/_media/reference/programmable-logic/zedboard/zedboard_ug.pdf)

Schematics:  
[https://digilent.com/reference/\\_media/reference/programmable-logic/zedboard/zedboard\\_sch.pdf](https://digilent.com/reference/_media/reference/programmable-logic/zedboard/zedboard_sch.pdf)

## JD1 Zedboard Conn

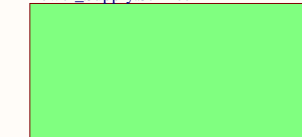


## JE1 Zedboard Conn



Change to proper gold pin connectors.

## Power Supply

U\_Power\_Supply  
Power\_Supply.SchDoc

Project:	Time_Sampling_Oscilloscope.PrjPcb	Engineer:	Szymon Jedliński	Revision:	1.0
Title:	*	Drawn by:	Szymon Jedliński	Sheet:	1
File:	Main.SchDoc	Checked by:	*	Total Sheet:	11
Variant:	Basic Assembly	Approved by:	*	Date:	05.08.2023

WEITI ISE  
ul. Nowowiejska 15/19  
00-665 Warszawa



A

B

C

D

A

B

C

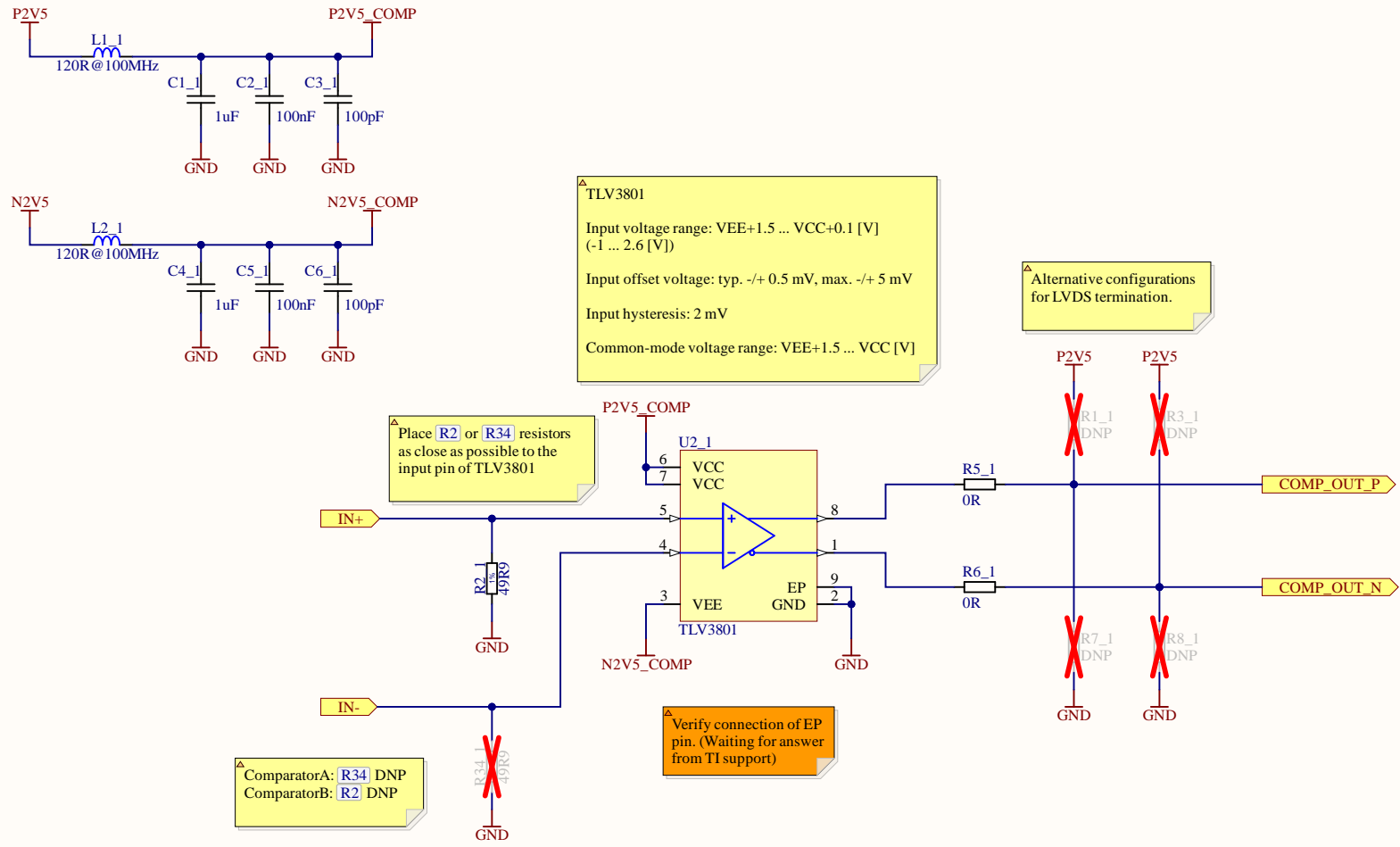
D

A

B

C

D



Project:	Time_Sampling_Oscilloscope.PrjPcb	Engineer:	Szymon Jedliński	Revision:	1.0
Title	*	Drawn by:	Szymon Jedliński	Sheet:	2
File:	Comparator.SchDoc	Checked by:*		Total Sheet:	11
Variant:	Basic Assembly	Approved by:*		Date:	05.08.2023

WEITI ISE  
ul. Nowowiejska 15/19  
00-665 Warszawa



A

B

C

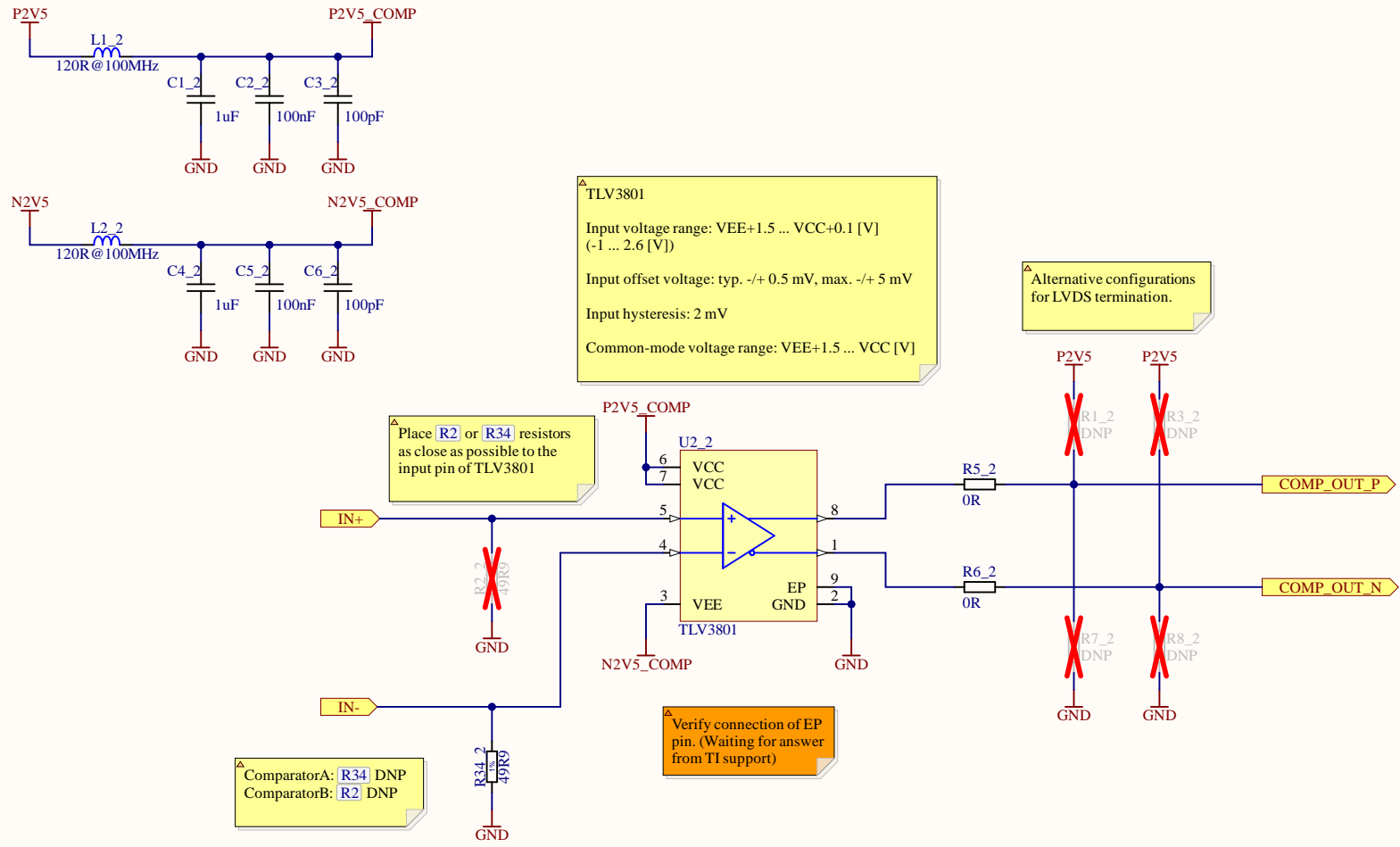
D

A

B

C

D

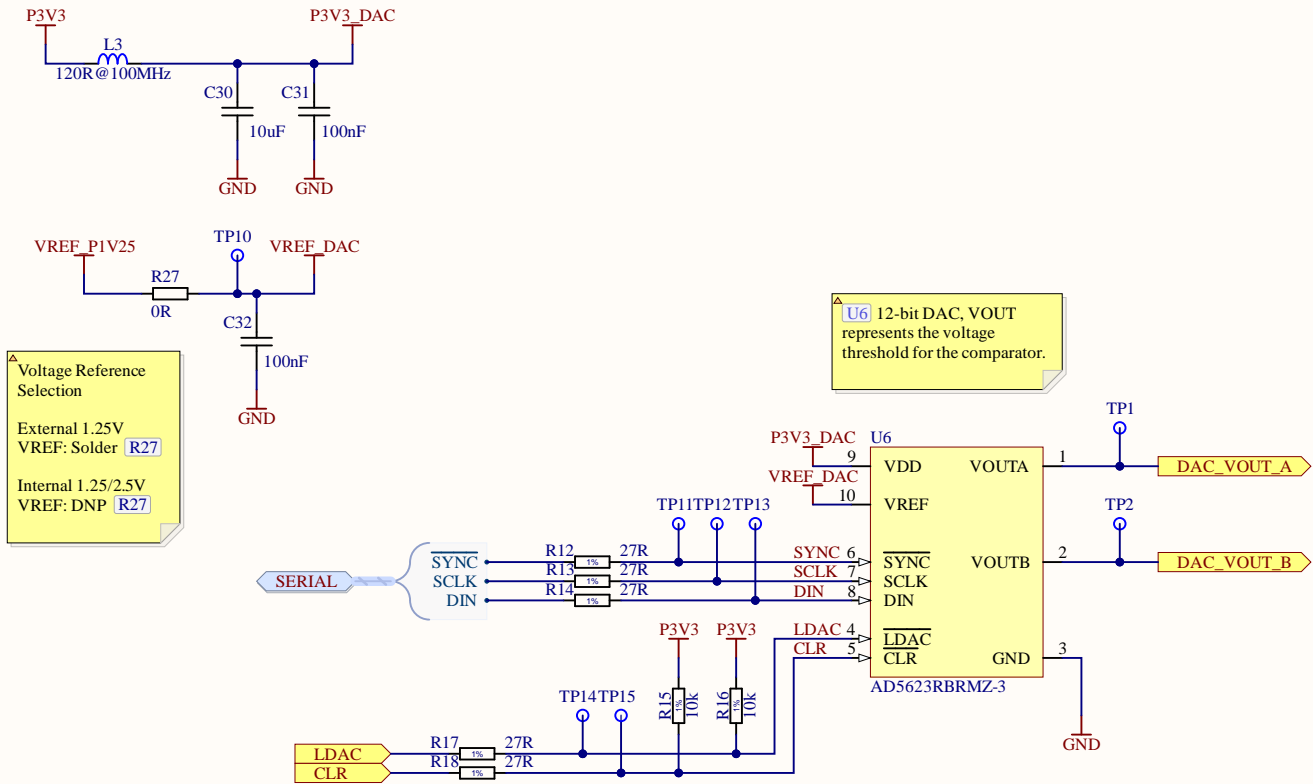


Project:	Time_Sampling_Oscilloscope.PrjPcb	Engineer:	Szymon Jedliński	Revision:	1.0
Title	*	Drawn by:	Szymon Jedliński	Sheet:	2
File:	Comparator.SchDoc	Checked by:*		Total Sheet:	11
Variant:	Basic Assembly	Approved by:*		Date:	05.08.2023

WEITI ISE

ul. Nowowiejska 15/19

00-665 Warszawa



Project:	Time_Sampling_Oscilloscope.PrjPcb	Engineer:	Szymon Jedliński	Revision:	1.0	<i>WEITI ISE</i> <i>ul. Nowowiejska 15/19</i> <i>00-665 Warszawa</i>	
Title	*	Drawn by:	Szymon Jedliński	Sheet:	3		
File:	DAC.SchDoc	Checked by:	*	Total Sheet:	11		
Variant:	Basic Assembly	Approved by:	*	Date:	05.08.2023		

A

A

B

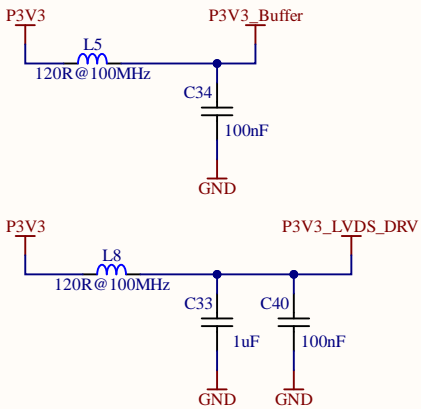
B

C

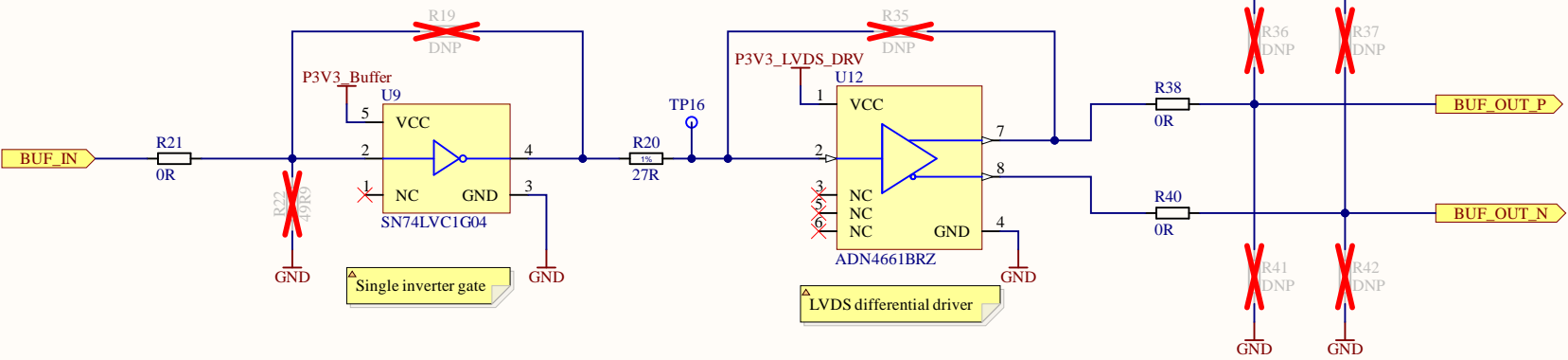
C

D

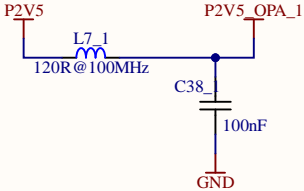
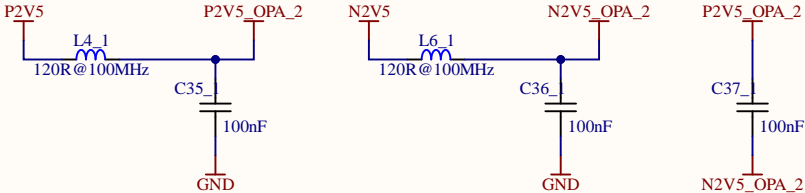
D



Alternative configurations for LVDS termination.

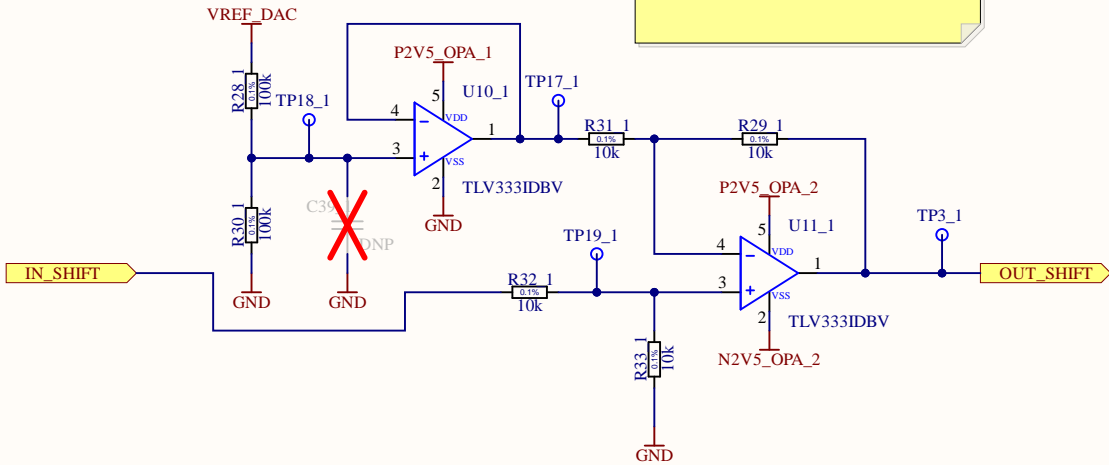


Project:	Time_Sampling_Oscilloscope.PrjPcb	Engineer:	Szymon Jedliński	Revision:	1.0	<div>WEITI ISE</div> <div>ul. Nowowiejska 15/19</div> <div>00-665 Warszawa</div> <div></div>
Title:	*	Drawn by:	Szymon Jedliński	Sheet:	4	
File:	External_Trigger_Buffer.SchDoc	Checked by:	*	Total Sheet:	11	
Variant:	Basic Assembly	Approved by:	*	Date:	05.08.2023	



△ Voltage divider + voltage follower  
Out = VREF\_DAC/2

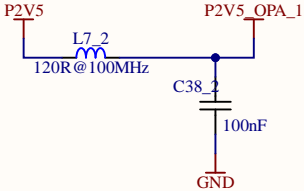
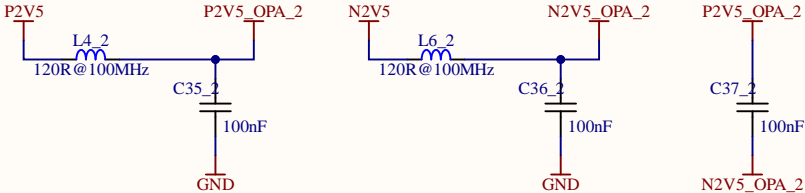
△ Non-inverting op amp with inverting positive reference  
Input: 0...VREF\_DAC [V]  
Output: -VREF\_DAC/2...VREF\_DAC/2 [V]



Project:	Time_Sampling_Oscilloscope.PrjPcb	Engineer:	Szymon Jedliński	Revision:	1.0
Title	*	Drawn by:	Szymon Jedliński	Sheet:	5
File:	Bipolar_Offset_Shifter.SchDoc	Checked by:*		Total Sheet:	11
Variant:	Basic Assembly	Approved by:*		Date:	05.08.2023

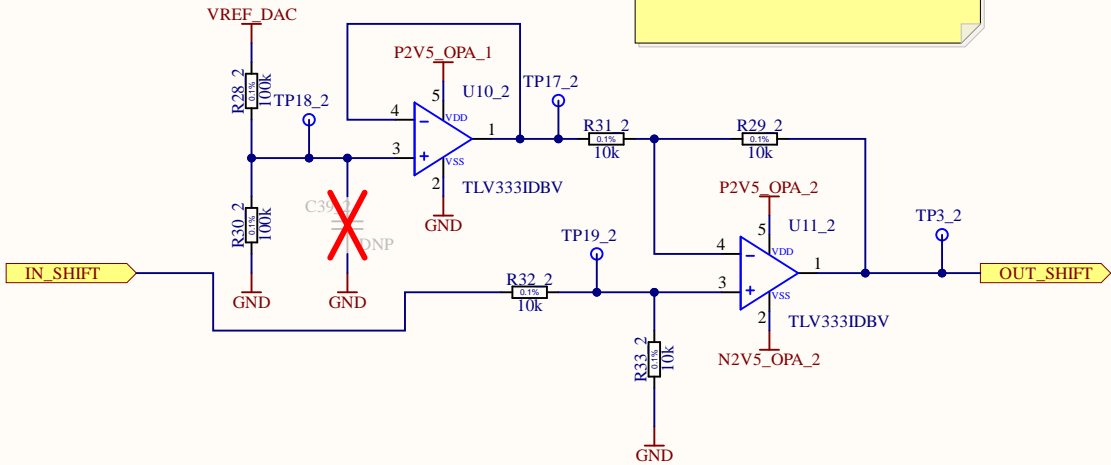
WEITI ISE  
ul. Nowowiejska 15/19  
00-665 Warszawa





△ Voltage divider + voltage follower  
Out = VREF\_DAC/2

△ Non-inverting op amp with inverting positive reference  
Input: 0...VREF\_DAC [V]  
Output: -VREF\_DAC/2...VREF\_DAC/2 [V]



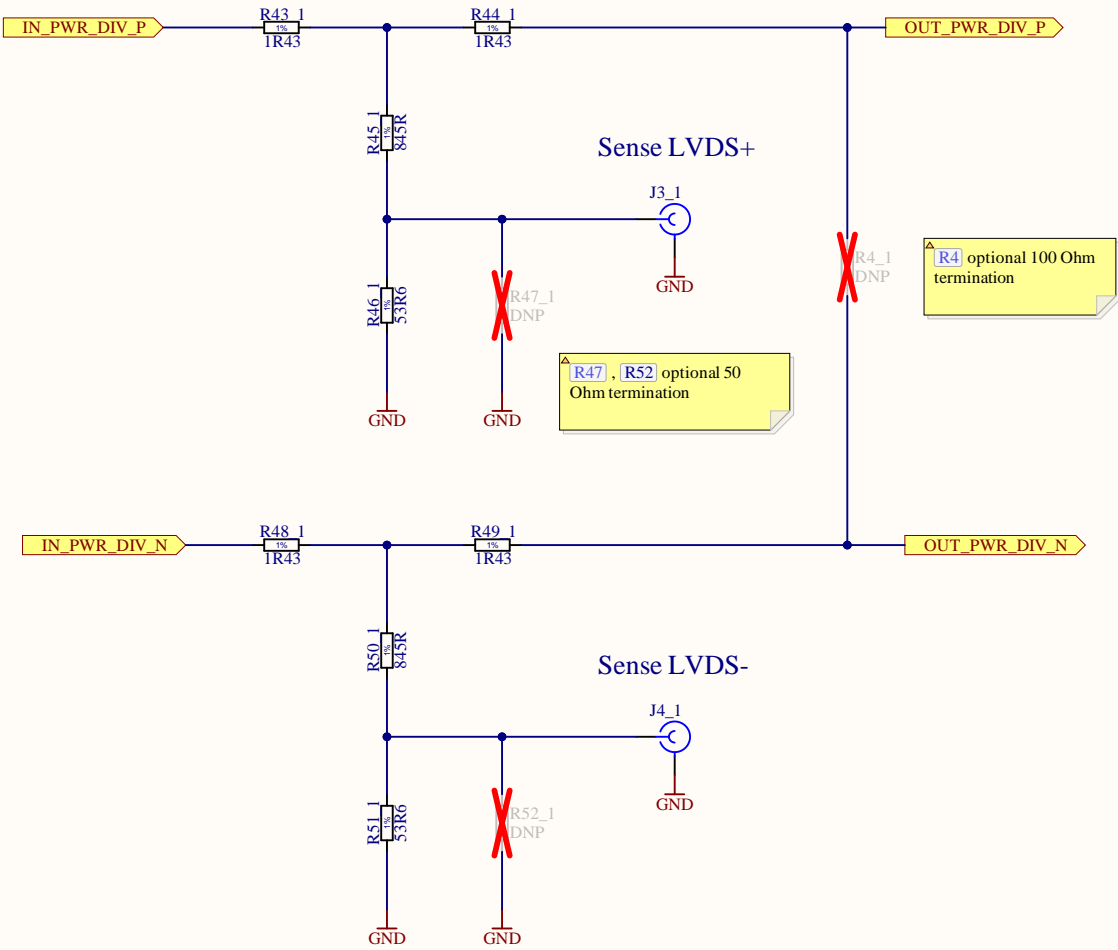
Project:	Time_Sampling_Oscilloscope.PrjPcb	Engineer:	Szymon Jedliński	Revision:	1.0	<i>WEITI ISE</i> <i>ul. Nowowiejska 15/19</i> <i>00-665 Warszawa</i>	
Title:	*	Drawn by:	Szymon Jedliński	Sheet:	5		
File:	Bipolar_Offset_Shifter.SchDoc	Checked by:	*	Total Sheet:	11		
Variant:	Basic Assembly	Approved by:	*	Date:	05.08.2023		

Resistive Unequal Power Divider  
S21 0.5 [dB]  
S31 31 [dB]  
<https://www.changpuak.ch/electronics/ResistivePowerSignalTap.php>

**Resistive Power Signal Tap Designer**  
aka RF Sampler, Resistive Unequal Power Divider

TO SOURCE ☐ R1 ☐ R2 ☐ TO LOAD  
S11 ☐ S21 ☐ TAP  
R3 ☐ R4 ☐

Mainline Loss, S21 [dB] 0.50 +0.1 -0.1  
Coupling, S31 [dB] 30.81  
System Impedance [Ω] 50.00  
R1, R2 [Ω] 1.439  
R3 [Ω] 842.368  
R4 [Ω] 53.056  
[CALCULATE]



Project:	Time_Sampling_Oscilloscope.PrjPcb	Engineer:	Szymon Jedliński	Revision:	1.0	WEITI ISE ul. Nowowiejska 15/19 00-665 Warszawa	
Title:	*	Drawn by:	Szymon Jedliński	Sheet:	6		
File:	Resistive_Unequal_Power_Divider.SchDoc	Checked by:	*	Total Sheet:	11		
Variant:	Basic Assembly	Approved by:	*	Date:	05.08.2023		

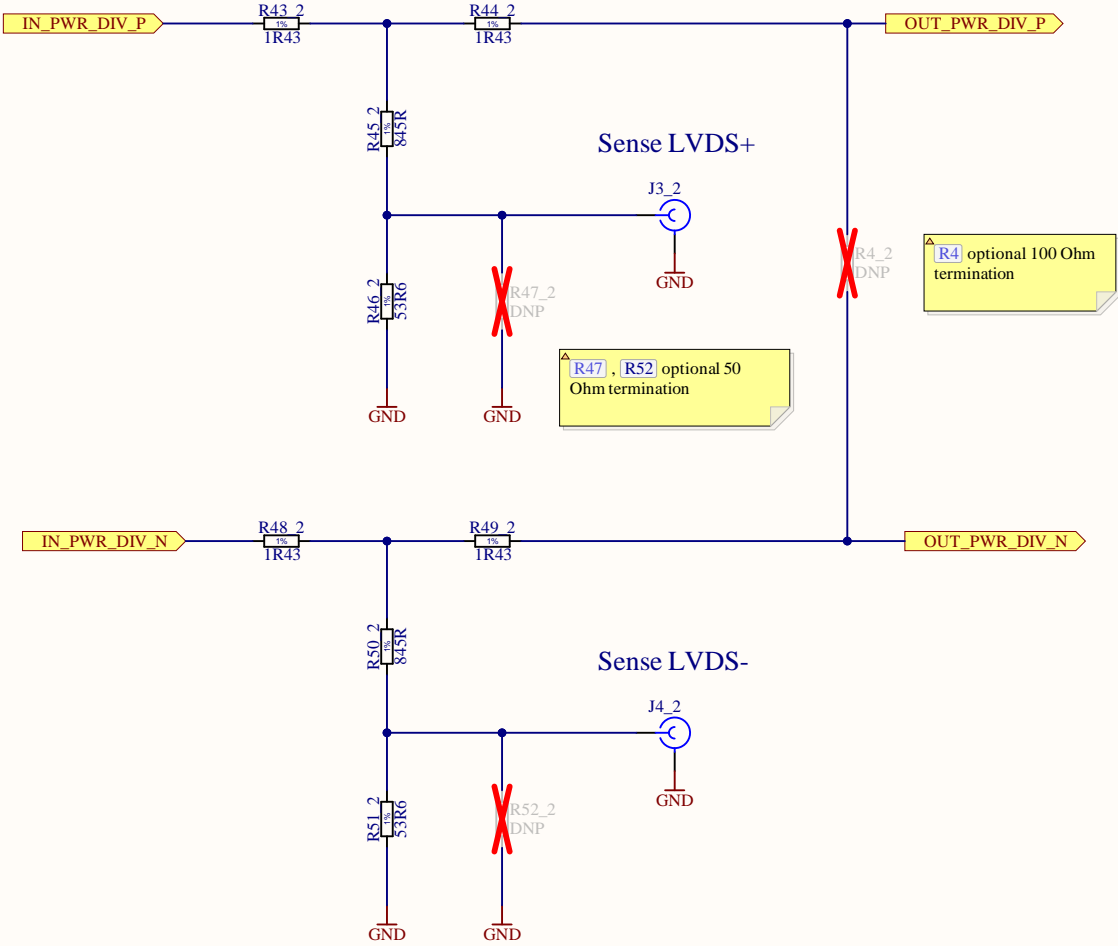


Resistive Unequal Power Divider  
S21 0.5 [dB]  
S31 31 [dB]  
<https://www.changpuak.ch/electronics/ResistivePowerSignalTap.php>

**Resistive Power Signal Tap Designer**  
aka RF Sampler, Resistive Unequal Power Divider

TO SOURCE ☐ R1 ☐ R2 ☐ TO LOAD  
S11 ☐ S21 ☐ TAP  
R3 ☐ R4 ☐

Parameter	Value
Mainline Loss, S21 [dB]	0.50
Coupling, S31 [dB]	30.81
System Impedance [Ω]	50.00
R1, R2 [Ω]	1.439
R3 [Ω]	842.368
R4 [Ω]	53.056



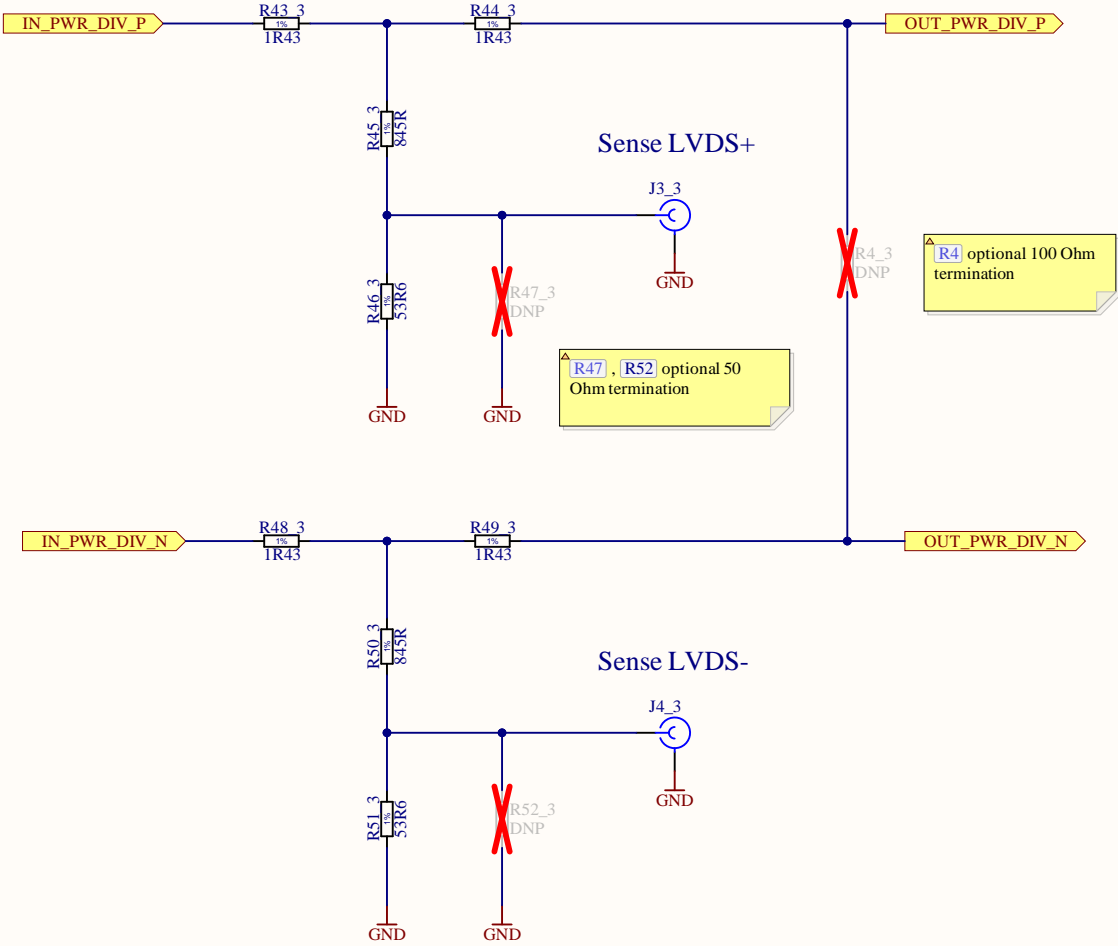
Project:	Time_Sampling_Oscilloscope.PrjPcb	Engineer:	Szymon Jedliński	Revision:	1.0	WEITI ISE ul. Nowowiejska 15/19 00-665 Warszawa	
Title:	*	Drawn by:	Szymon Jedliński	Sheet:	6		
File:	Resistive_Unequal_Power_Divider.SchDoc	Checked by:	*	Total Sheet:	11		
Variant:	Basic Assembly	Approved by:	*	Date:	05.08.2023		

Resistive Unequal Power Divider  
S21 0.5 [dB]  
S31 31 [dB]  
<https://www.changpuak.ch/electronics/ResistivePowerSignalTap.php>

**Resistive Power Signal Tap Designer**  
aka RF Sampler, Resistive Unequal Power Divider

TO SOURCE ☐ R1 ☐ R2 ☐ TO LOAD  
S11 ☐ S21 ☐ TAP  
R3 ☐ R4 ☐

Mainline Loss, S21 [dB] 0.50 +0.1 -0.1  
Coupling, S31 [dB] 30.81  
System Impedance [Ω] 50.00  
R1, R2 [Ω] 1.439  
R3 [Ω] 842.368  
R4 [Ω] 53.056  
[CALCULATE]



Project:	Time_Sampling_Oscilloscope.PrjPcb	Engineer:	Szymon Jedliński	Revision:	1.0	WEITI ISE ul. Nowowiejska 15/19 00-665 Warszawa	
Title:	*	Drawn by:	Szymon Jedliński	Sheet:	6		
File:	Resistive_Unequal_Power_Divider.SchDoc	Checked by:	*	Total Sheet:	11		
Variant:	Basic Assembly	Approved by:	*	Date:	05.08.2023		

A

B

C

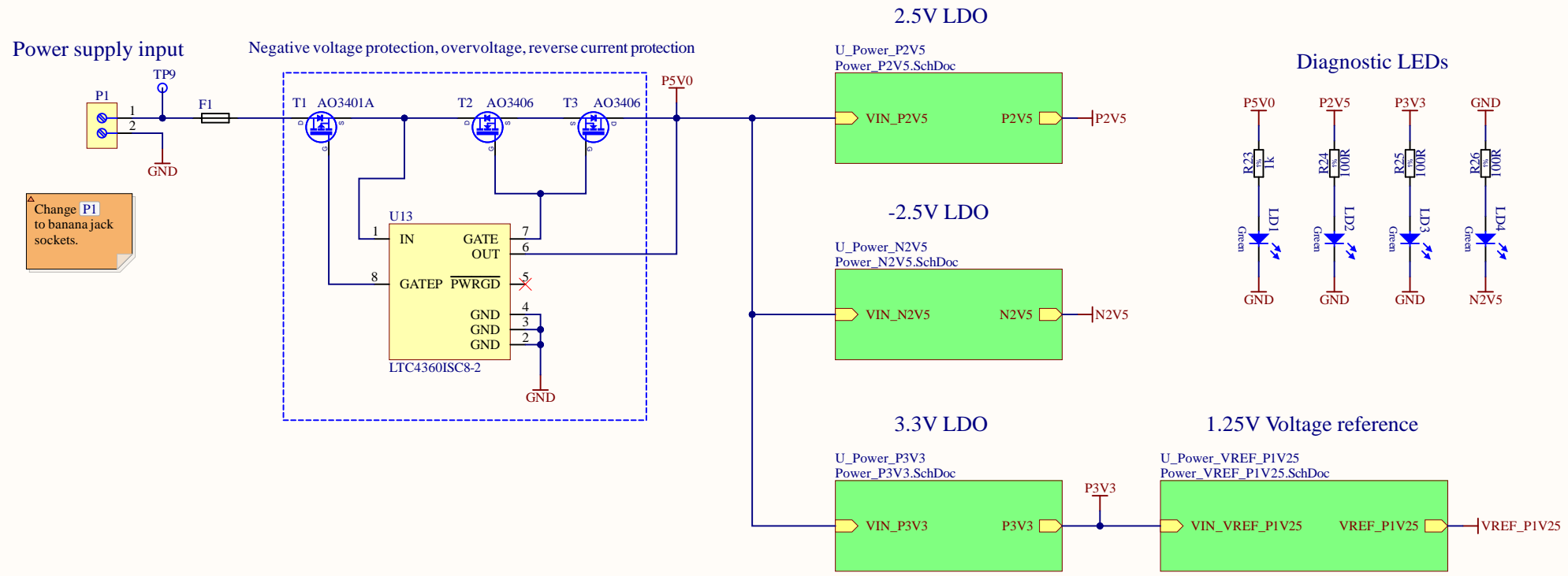
D

A

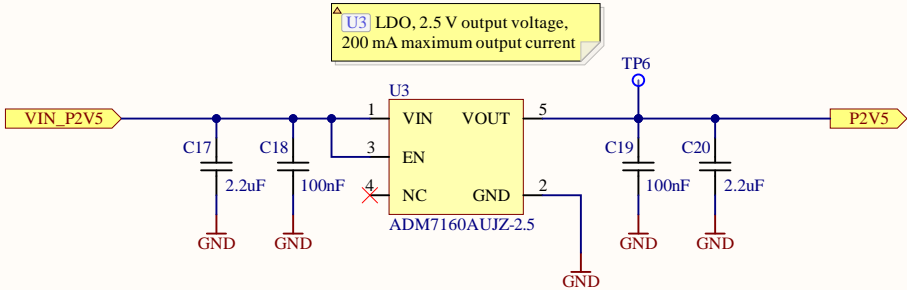
B

C

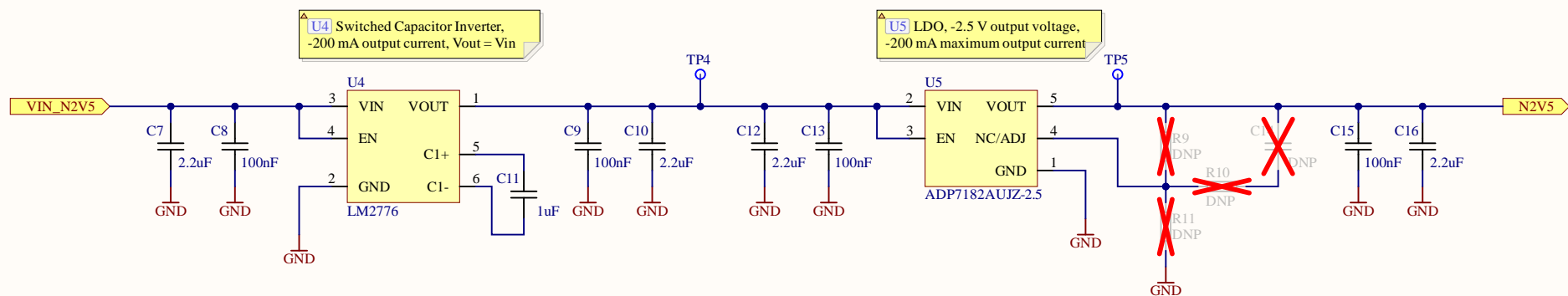
D




Project:	Time_Sampling_Oscilloscope.PrjPcb	Engineer:	Szymon Jedliński	Revision:	1.0	WEITI ISE ul. Nowowiejska 15/19 00-665 Warszawa	
Title:	*	Drawn by:	Szymon Jedliński	Sheet:	7		
File:	Power_Supply.SchDoc	Checked by:	*	Total Sheet:	11		
Variant:	Basic Assembly	Approved by:	*	Date:	05.08.2023		



Project:	Time_Sampling_Oscilloscope.PrjPcb	Engineer:	Szymon Jedliński	Revision:	1.0	<i>WEITI ISE</i> <i>ul. Nowowiejska 15/19</i> <i>00-665 Warszawa</i>	
Title:	*	Drawn by:	Szymon Jedliński	Sheet:	8		
File:	Power_P2V5.SchDoc	Checked by:	*	Total Sheet:	11		
Variant:	Basic Assembly	Approved by:	*	Date:	05.08.2023		



Project:	Time_Sampling_Oscilloscope.PrjPcb	Engineer:	Szymon Jedliński	Revision:	1.0	<i>WEITI ISE</i> <i>ul. Nowowiejska 15/19</i> <i>00-665 Warszawa</i>	
Title:	*	Drawn by:	Szymon Jedliński	Sheet:	9		
File:	Power_N2V5.SchDoc	Checked by:	*	Total Sheet:	11		
Variant:	Basic Assembly	Approved by:	*	Date:	05.08.2023		

A

A

B

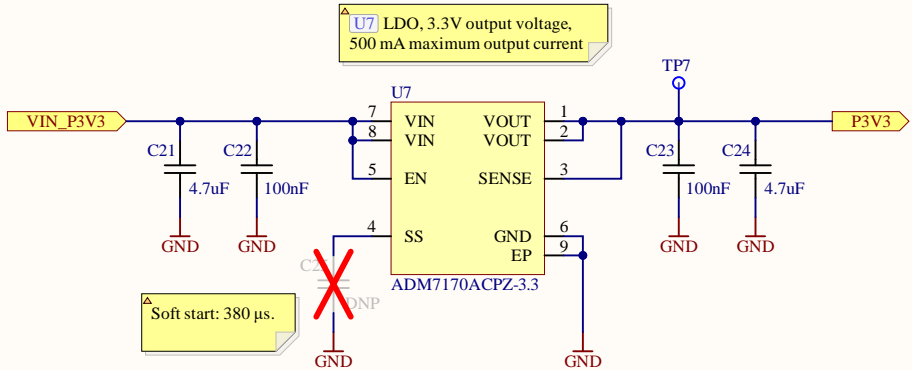
B


C

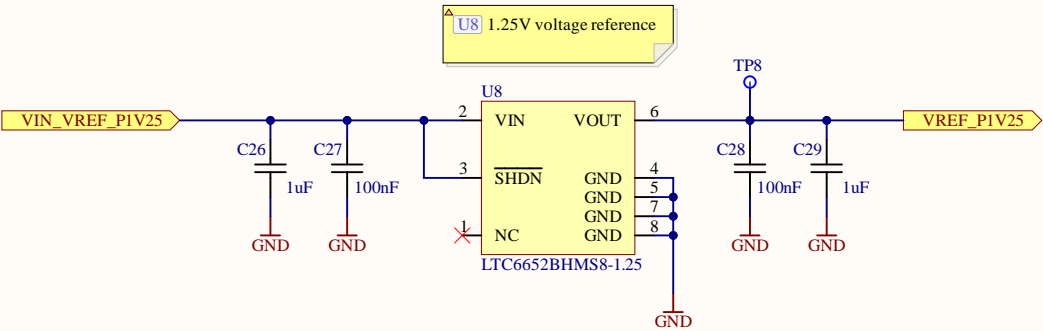
C


D

D



Project:	Time_Sampling_Oscilloscope.PrjPcb	Engineer:	Szymon Jedliński	Revision:	1.0	<i>WEITI ISE</i> <i>ul. Nowowiejska 15/19</i> <i>00-665 Warszawa</i>	
Title:	*	Drawn by:	Szymon Jedliński	Sheet:	10		
File:	Power_P3V3.SchDoc	Checked by:	*	Total Sheet:	11		
Variant:	Basic Assembly	Approved by:	*	Date:	05.08.2023		



Project:	Time_Sampling_Oscilloscope.PrjPcb	Engineer:	Szymon Jedliński	Revision:	1.0	<i>WEITI ISE</i> <i>ul. Nowowiejska 15/19</i> <i>00-665 Warszawa</i>	
Title	*	Drawn by:	Szymon Jedliński	Sheet:	11		
File:	Power_VREF_P1V25.SchDoc	Checked by:	*	Total Sheet:	11		
Variant:	Basic Assembly	Approved by:	*	Date:	05.08.2023		