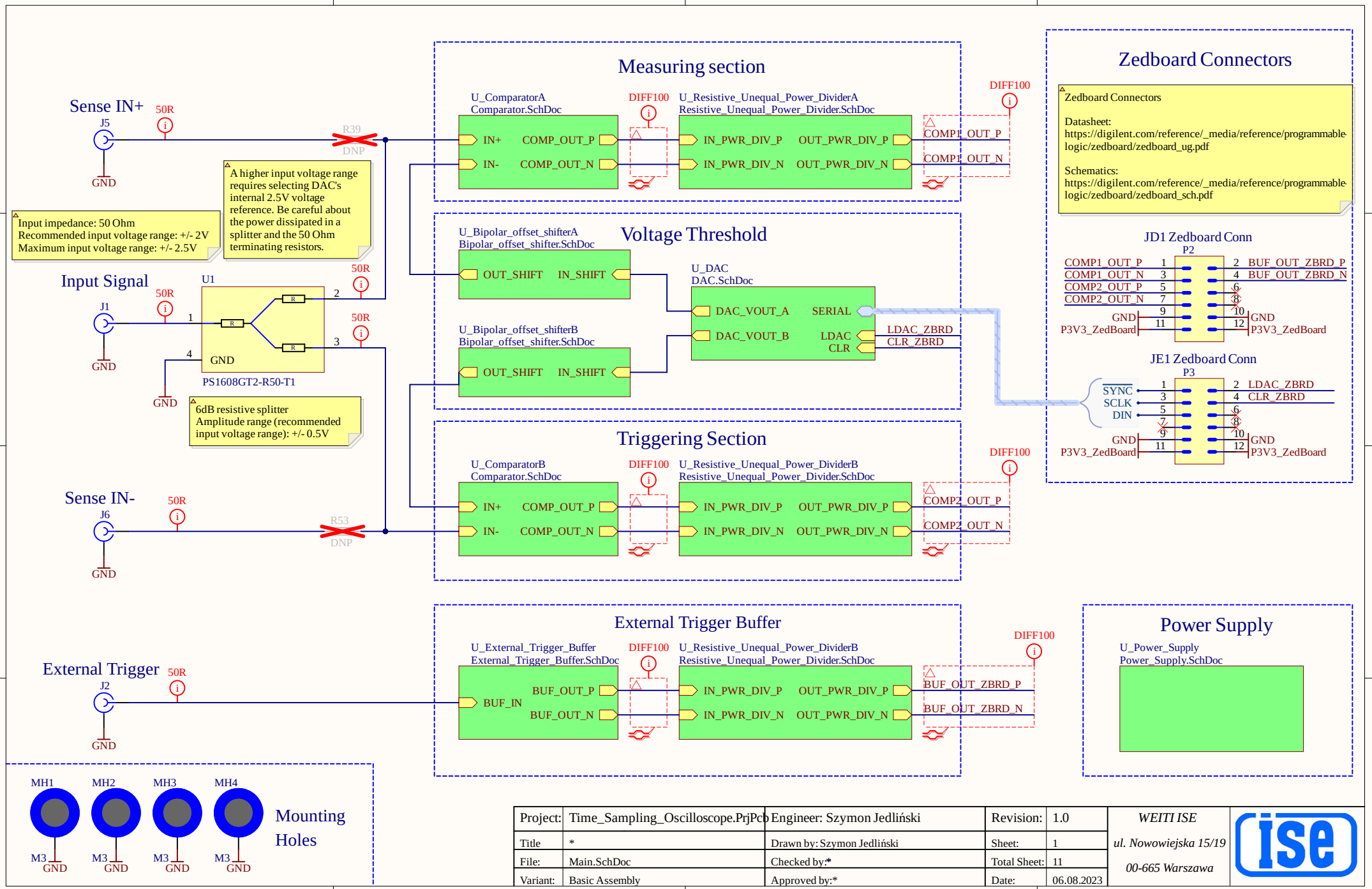
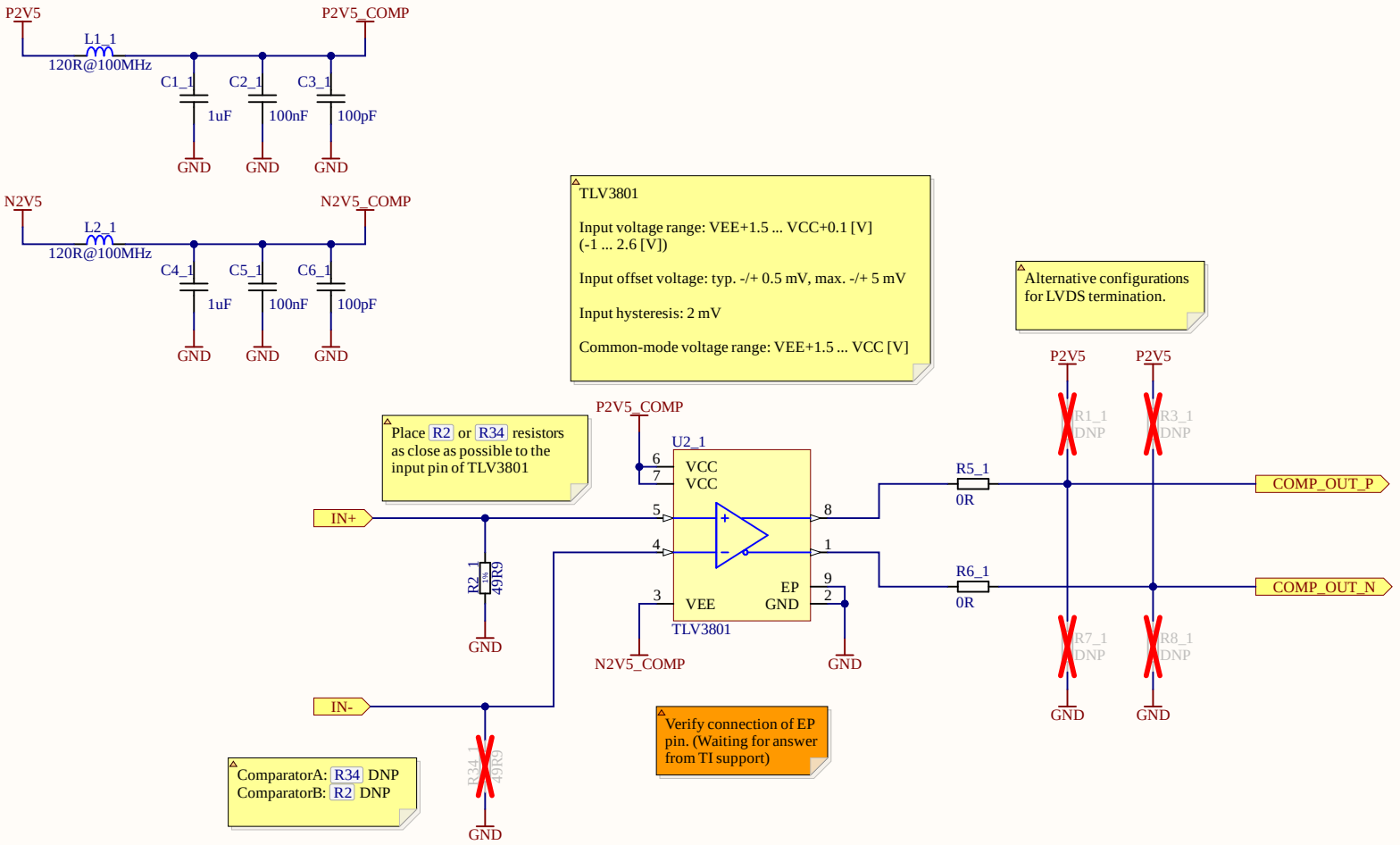
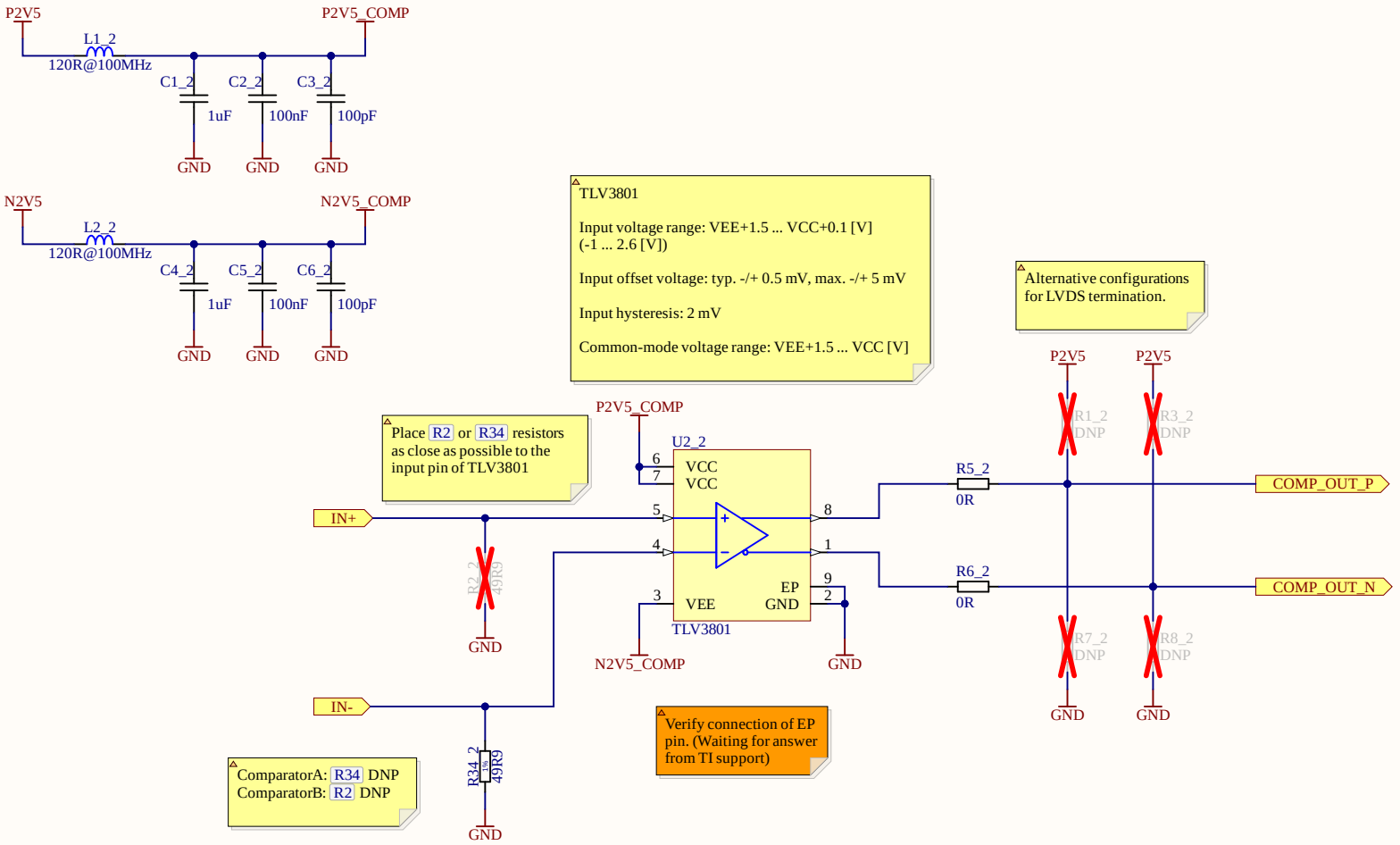
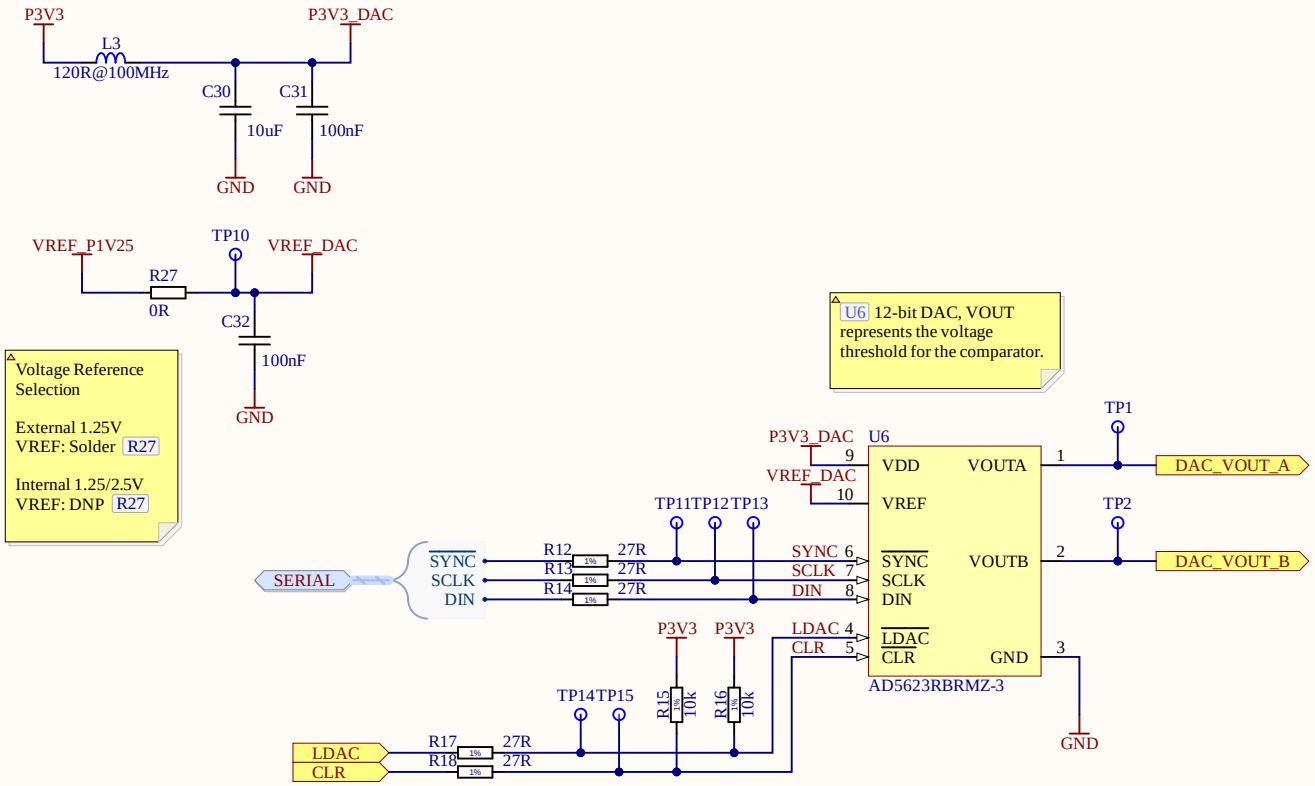

Sense IN+
J5
50R
GND
R39
DNP
Input impedance: 50 Ohm
Recommended input voltage range: +/- 2V
Maximum input voltage range: +/- 2.5V
A higher input voltage range requires selecting DAC's internal 2.5V voltage reference. Be careful about the power dissipated in a splitter and the 50 Ohm terminating resistors.
Input Signal
J1
U1
PS1608GT2-R50-T1
6dB resistive splitter
Amplitude range (recommended input voltage range): +/- 0.5V
Sense IN-
J6
R53
External Trigger
J2
Measuring section
U_ComparatorA
Comparator.SchDoc
DIFF100
U_Resistive_Unequal_Power_DividerA
Resistive_Unequal_Power_Divider.SchDoc
IN+
IN-
COMP_OUT_P
COMP_OUT_N
IN_PWR_DIV_P
IN_PWR_DIV_N
OUT_PWR_DIV_P
OUT_PWR_DIV_N
COMP1_OUT_P
COMP1_OUT_N
Voltage Threshold
U_Bipolar_offset_shifterA
Bipolar_offset_shifter.SchDoc
U_Bipolar_offset_shifterB
Bipolar_offset_shifter.SchDoc
OUT_SHIFT
IN_SHIFT
U_DAC
DAC.SchDoc
DAC_VOUT_A
DAC_VOUT_B
SERIAL
LDAC
CLR
LDAC_ZBRD
CLR_ZBRD
Triggering Section
U_ComparatorB
Comparator.SchDoc
U_Resistive_Unequal_Power_DividerB
Resistive_Unequal_Power_Divider.SchDoc
COMP2_OUT_P
COMP2_OUT_N
External Trigger Buffer
U_External_Trigger_Buffer
External_Trigger_Buffer.SchDoc
BUF_IN
BUF_OUT_P
BUF_OUT_N
BUF_OUT_ZBRD_P
BUF_OUT_ZBRD_N
Zedboard Connectors
Zedboard Connectors
Datasheet:
https://digilent.com/reference/_media/reference/programmable-logic/zedboard/zedboard_ug.pdf
Schematics:
https://digilent.com/reference/_media/reference/programmable-logic/zedboard/zedboard_sch.pdf
JD1 Zedboard Conn
P2
COMP1_OUT_P
COMP1_OUT_N
COMP2_OUT_P
COMP2_OUT_N
BUF_OUT_ZBRD_P
BUF_OUT_ZBRD_N
GND
P3V3_ZedBoard
JE1 Zedboard Conn
P3
SYNC
SCLK
DIN
LDAC_ZBRD
CLR_ZBRD
Power Supply
U_Power_Supply
Power_Supply.SchDoc
MH1
MH2
MH3
MH4
M3
Mounting Holes
Project: Time_Sampling_Oscilloscope.PrjPcb
Engineer: Szymon Jedliński
Revision: 1.0
Title *
Drawn by: Szymon Jedliński
Sheet: 1
File: Main.SchDoc
Checked by:*
Total Sheet: 11
Variant: Basic Assembly
Approved by:*
Date: 06.08.2023
WEITI ISE
ul. Nowowiejska 15/19
00-665 Warszawa



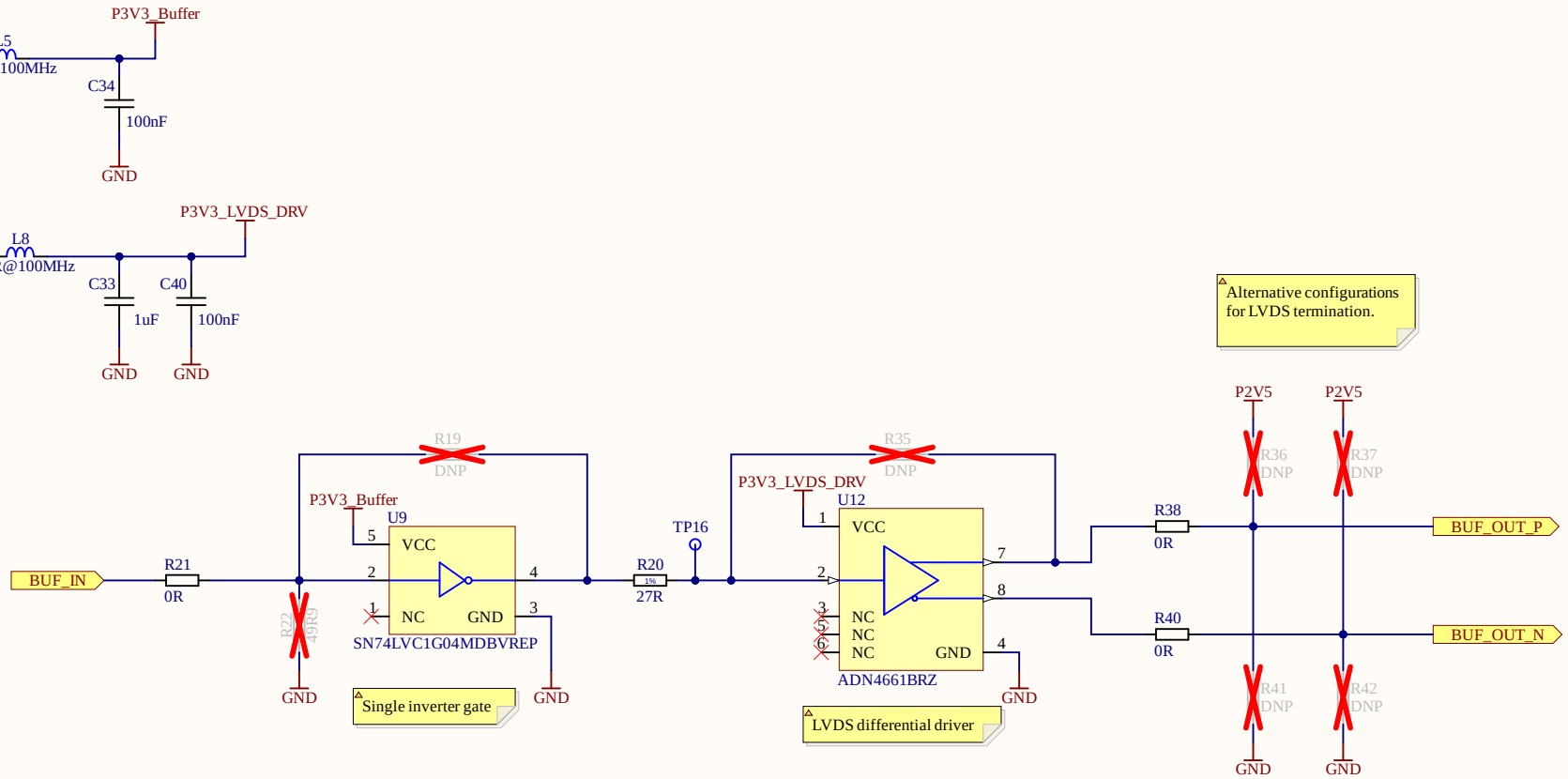
Project:	Time_Sampling_Oscilloscope.PrjPcb	Engineer: Szymon Jedliński	Revision:	1.0	*WEITI ISE*
Title	*	Drawn by: Szymon Jedliński	Sheet:	2	*ul. Nowowiejska 15/19*
File:	Comparator.SchDoc	Checked by:*	Total Sheet:	11	*00-665 Warszawa*
Variant:	Basic Assembly	Approved by:*	Date:	06.08.2023	



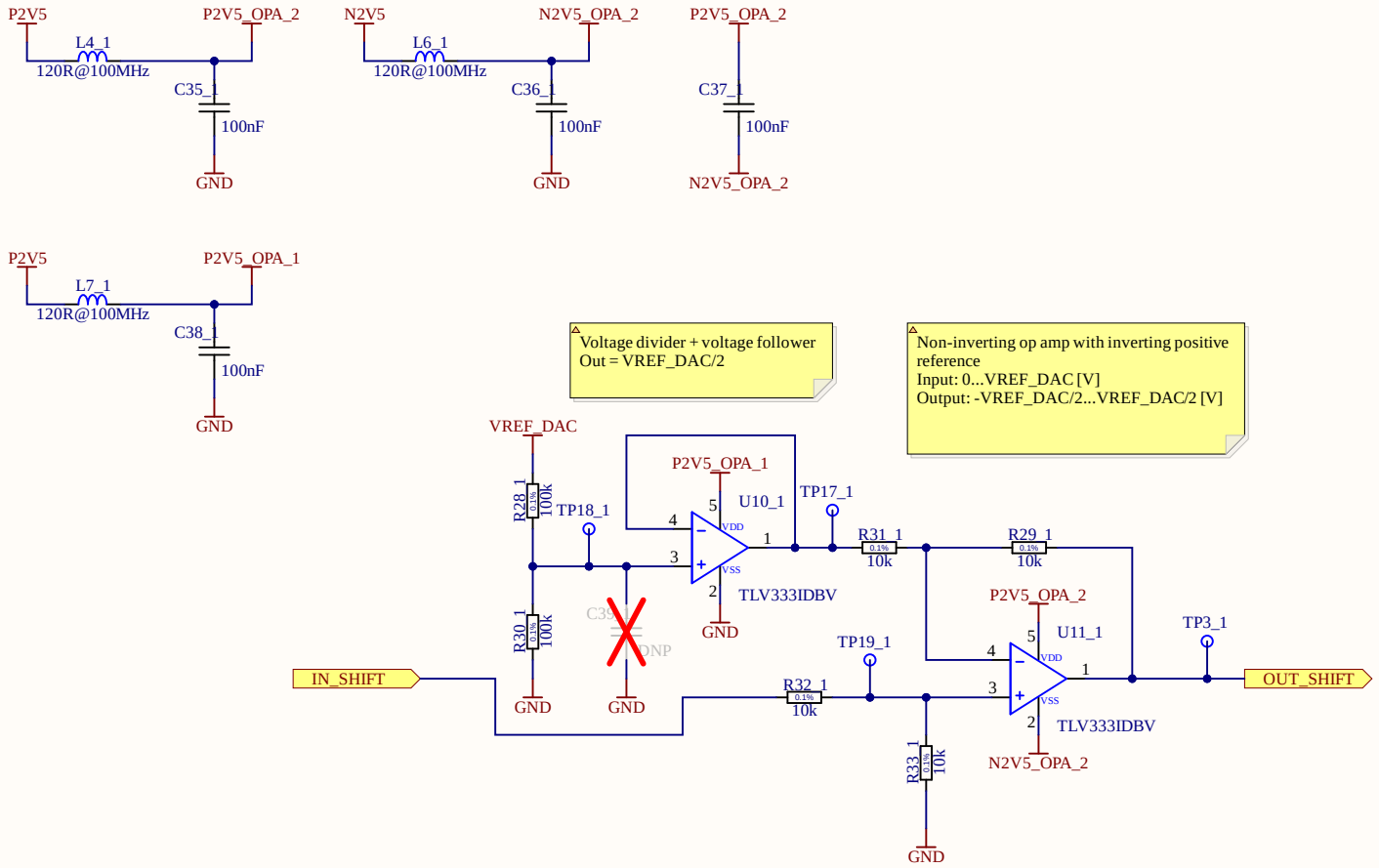
Project:	Time_Sampling_Oscilloscope.PrjPcb	Engineer: Szymon Jedliński	Revision:	1.0	*WEITI ISE*
Title	*	Drawn by: Szymon Jedliński	Sheet:	2	*ul. Nowowiejska 15/19*
File:	Comparator.SchDoc	Checked by:*	Total Sheet:	11	*00-665 Warszawa*
Variant:	Basic Assembly	Approved by:*	Date:	06.08.2023	



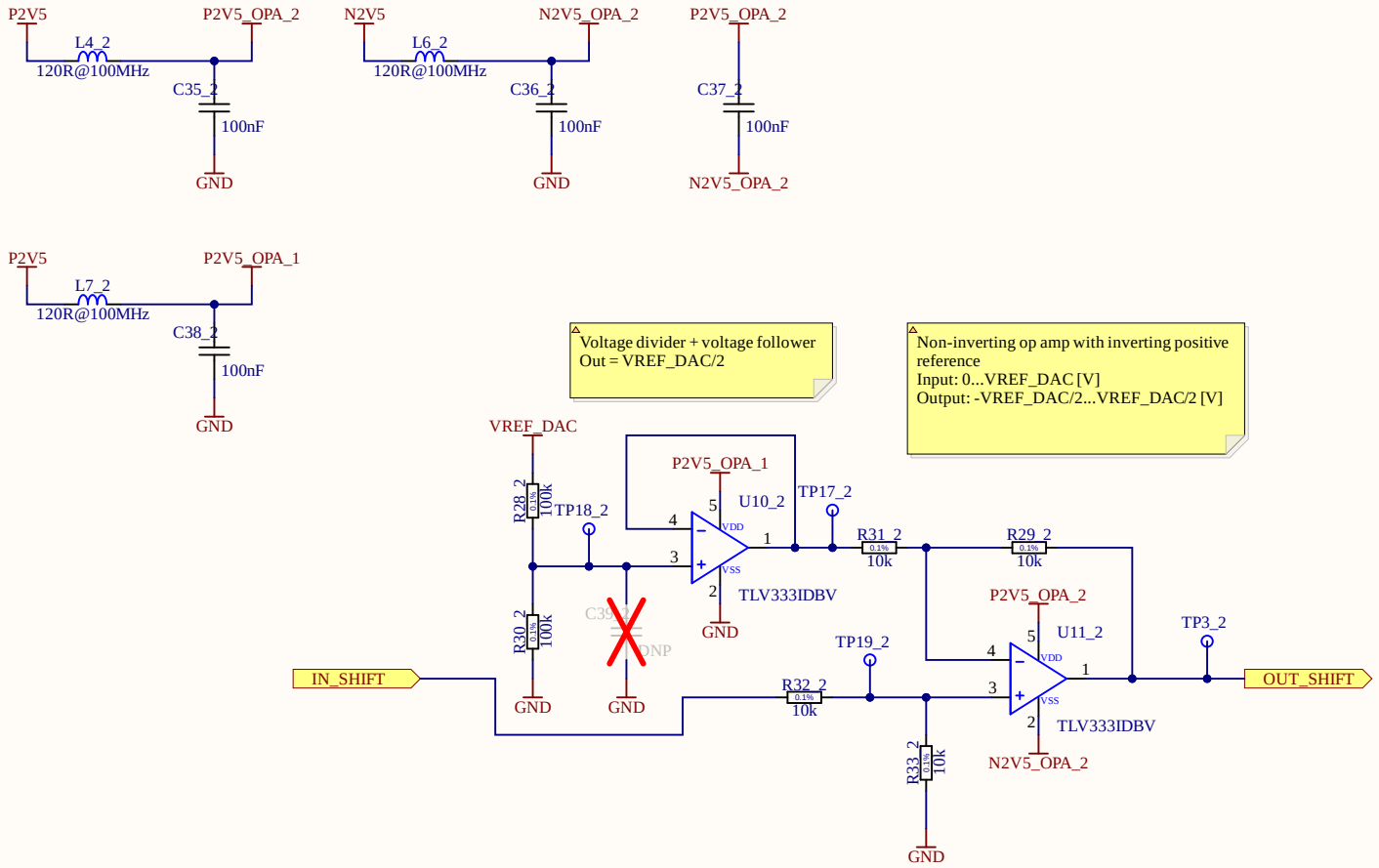
Project:	Time_Sampling_Oscilloscope.PrjPcb	Engineer: Szymon Jedliński	Revision:	1.0	*WEITI ISE*
Title	*	Drawn by: Szymon Jedliński	Sheet:	3	*ul. Nowowiejska 15/19*
File:	DAC.SchDoc	Checked by:*	Total Sheet:	11	*00-665 Warszawa*
Variant:	Basic Assembly	Approved by:*	Date:	06.08.2023	



Project:	Time_Sampling_Oscilloscope.PrjPcb	Engineer: Szymon Jedliński	Revision:	1.0	*WEITI ISE*
Title	*	Drawn by: Szymon Jedliński	Sheet:	4	*ul. Nowowiejska 15/19*
File:	External_Trigger_Buffer.SchDoc	Checked by:*	Total Sheet:	11	*00-665 Warszawa*
Variant:	Basic Assembly	Approved by:*	Date:	06.08.2023	



Project:	Time_Sampling_Oscilloscope.PrjPcb	Engineer: Szymon Jedliński	Revision:	1.0	*WEITI ISE*
Title	*	Drawn by: Szymon Jedliński	Sheet:	5	*ul. Nowowiejska 15/19*
File:	Bipolar_Offset_Shifter.SchDoc	Checked by:*	Total Sheet:	11	*00-665 Warszawa*
Variant:	Basic Assembly	Approved by:*	Date:	05.08.2023	



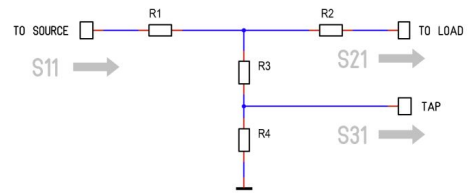
Project:	Time_Sampling_Oscilloscope.PrjPcb	Engineer: Szymon Jedliński	Revision:	1.0	*WEITI ISE*
Title	*	Drawn by: Szymon Jedliński	Sheet:	5	*ul. Nowowiejska 15/19*
File:	Bipolar_Offset_Shifter.SchDoc	Checked by:*	Total Sheet:	11	*00-665 Warszawa*
Variant:	Basic Assembly	Approved by:*	Date:	05.08.2023	

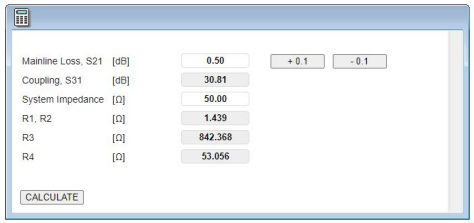
Resistive Unequal Power Divider
S21 0.5 [dB]
S31 31 [dB]

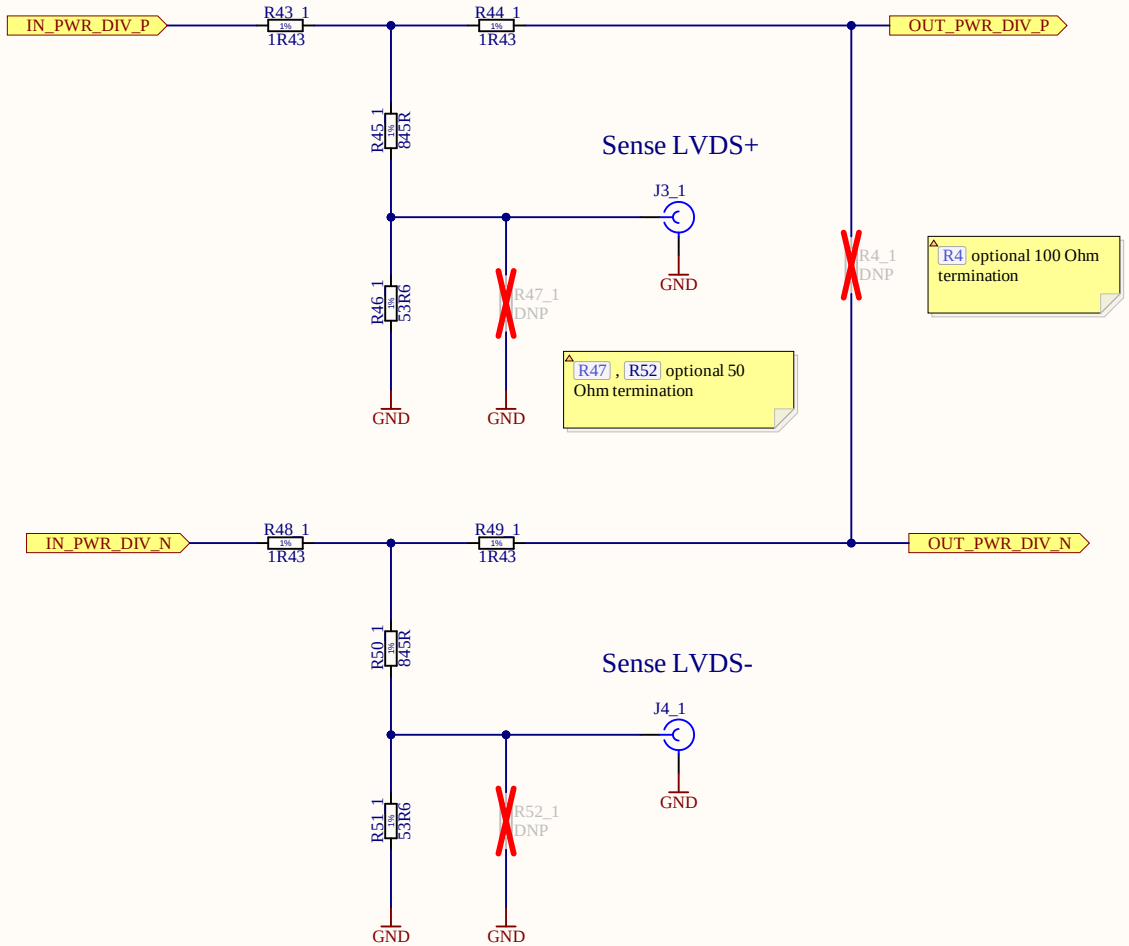
https://www.changpuak.ch/electronics/ResistivePowerSignalTap.php

Resistive Power Signal Tap Designer

aka RF Sampler, Resistive Unequal Power Divider







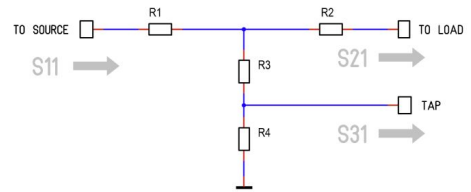
Project:	Time_Sampling_Oscilloscope.PrjPcb	Engineer: Szymon Jedliński	Revision:	1.0	*WEITI ISE*
Title	*	Drawn by: Szymon Jedliński	Sheet:	6	*ul. Nowowiejska 15/19*
File:	Resistive_Unequal_Power_Divider.SchDoc	Checked by:*	Total Sheet:	11	*00-665 Warszawa*
Variant:	Basic Assembly	Approved by:*	Date:	06.08.2023	

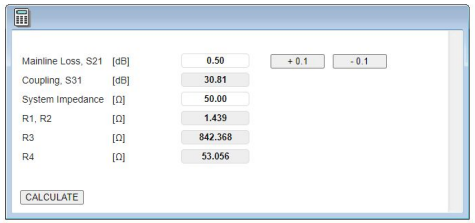
Resistive Unequal Power Divider
S21 0.5 [dB]
S31 31 [dB]

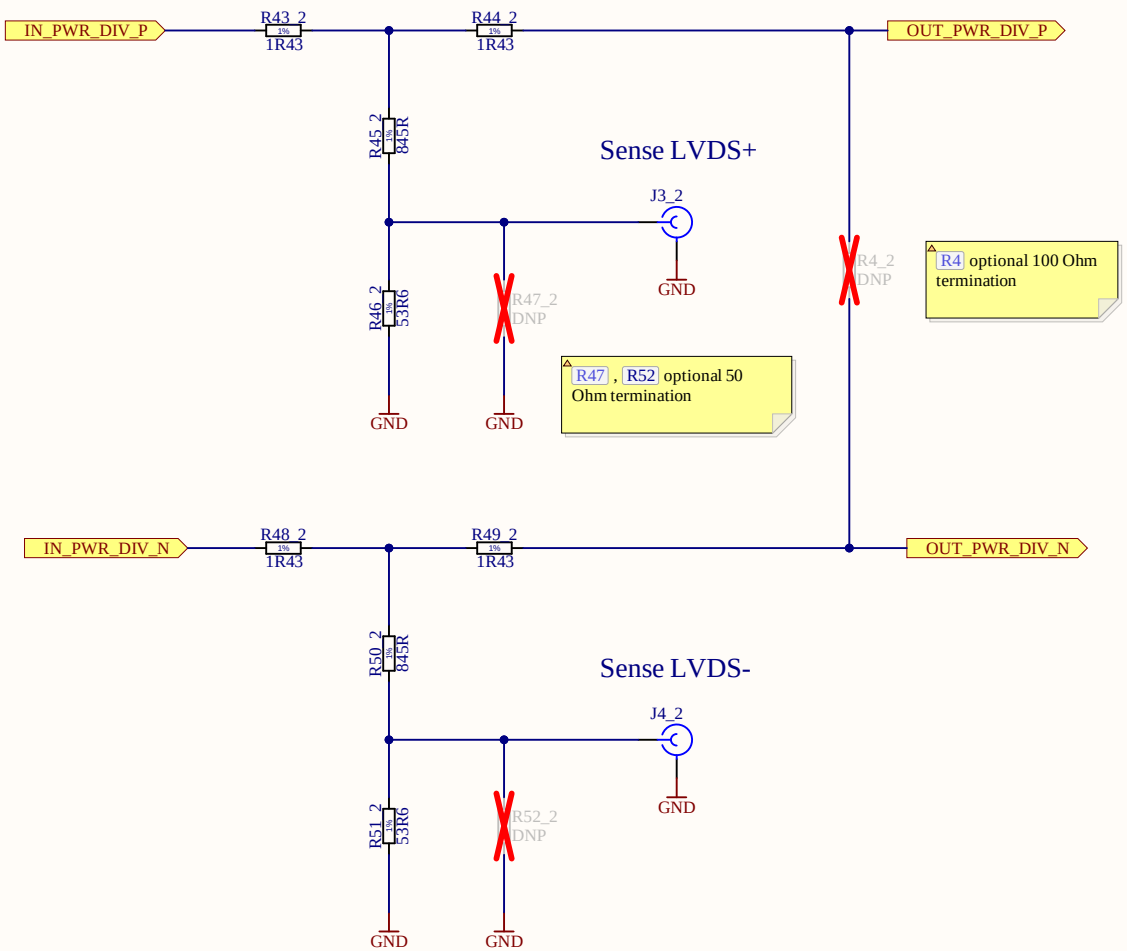
https://www.changpuak.ch/electronics/ResistivePowerSignalTap.php

Resistive Power Signal Tap Designer

aka RF Sampler, Resistive Unequal Power Divider







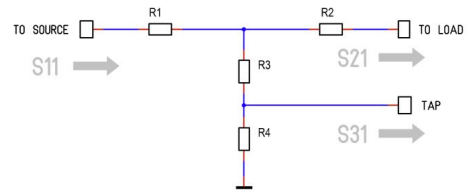
Project:	Time_Sampling_Oscilloscope.PrjPcb	Engineer: Szymon Jedliński	Revision:	1.0	*WEITI ISE*
Title	*	Drawn by: Szymon Jedliński	Sheet:	6	*ul. Nowowiejska 15/19*
File:	Resistive_Unequal_Power_Divider.SchDoc	Checked by:*	Total Sheet:	11	*00-665 Warszawa*
Variant:	Basic Assembly	Approved by:*	Date:	06.08.2023	

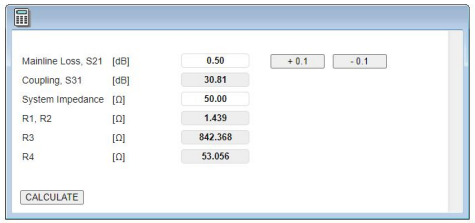
Resistive Unequal Power Divider
S21 0.5 [dB]
S31 31 [dB]

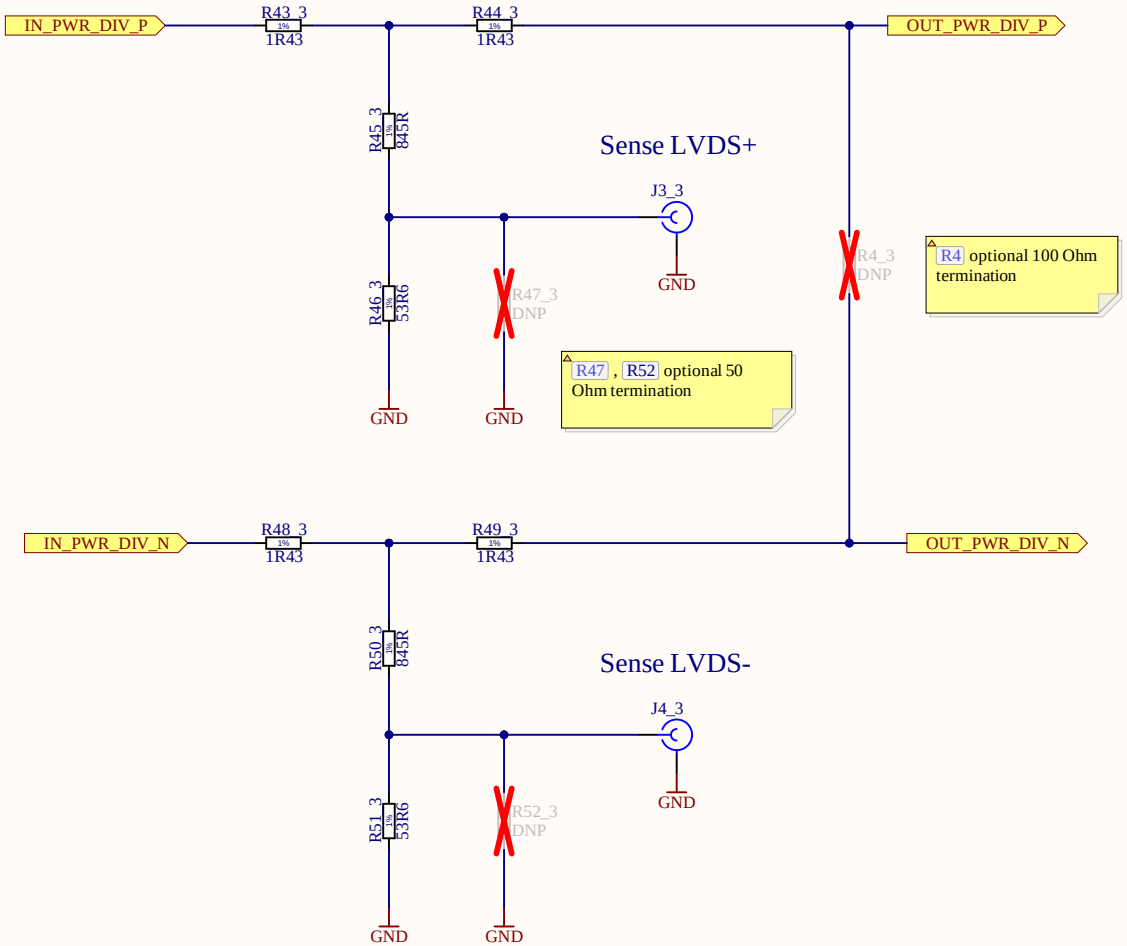
https://www.changpuak.ch/electronics/ResistivePowerSignalTap.php

Resistive Power Signal Tap Designer

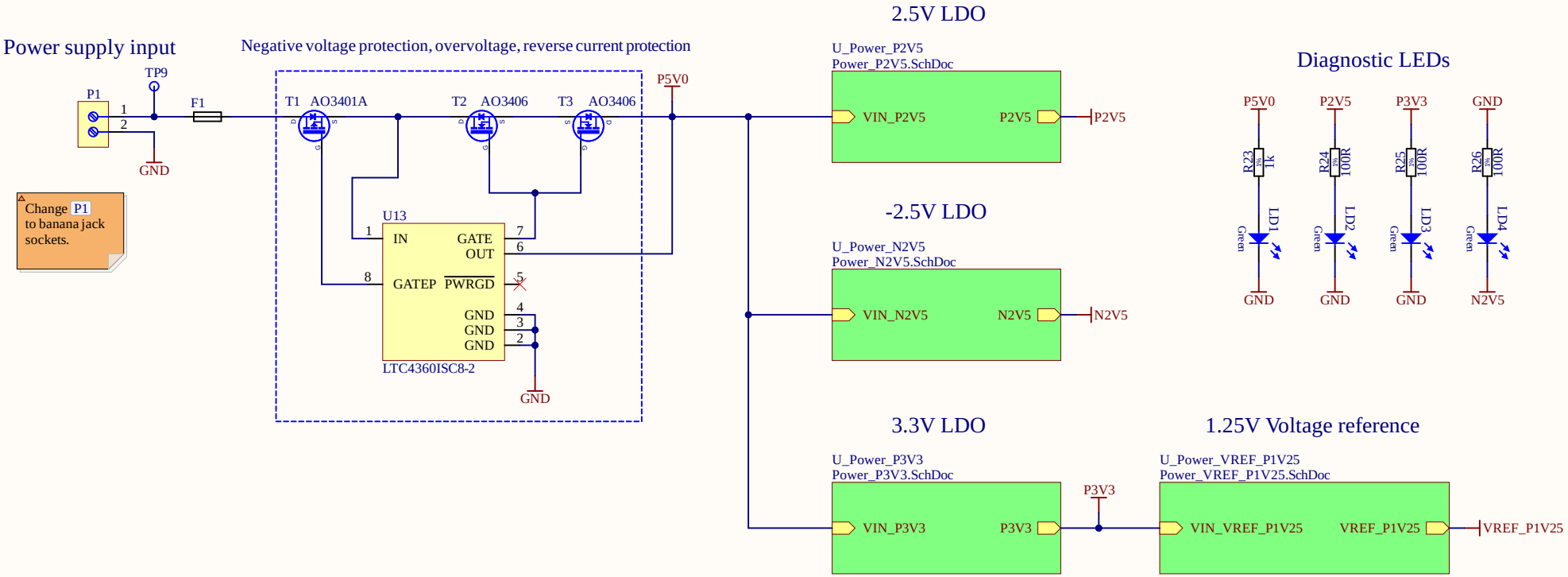
aka RF Sampler, Resistive Unequal Power Divider



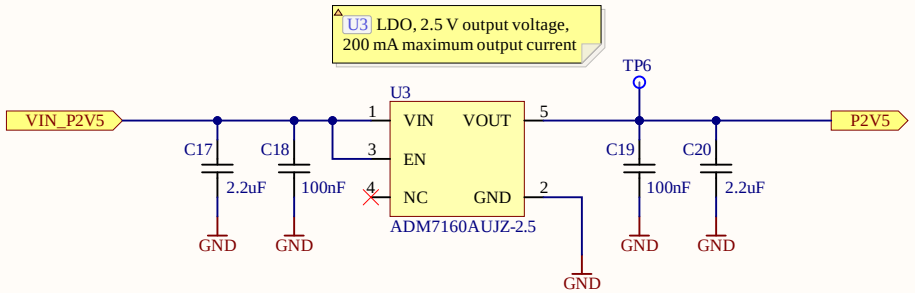




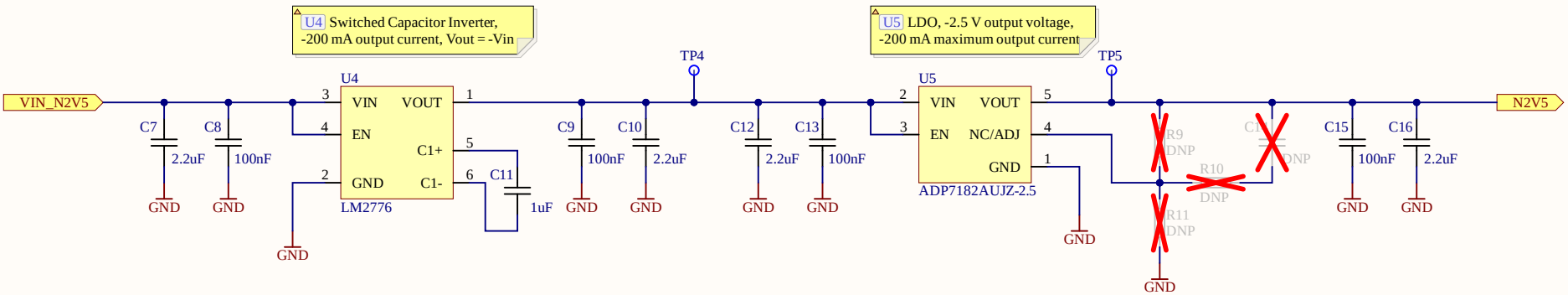
Project:	Time_Sampling_Oscilloscope.PrjPcb	Engineer: Szymon Jedliński	Revision:	1.0	*WEITI ISE*
Title	*	Drawn by: Szymon Jedliński	Sheet:	6	*ul. Nowowiejska 15/19*
File:	Resistive_Unequal_Power_Divider.SchDoc	Checked by:*	Total Sheet:	11	*00-665 Warszawa*
Variant:	Basic Assembly	Approved by:*	Date:	06.08.2023	



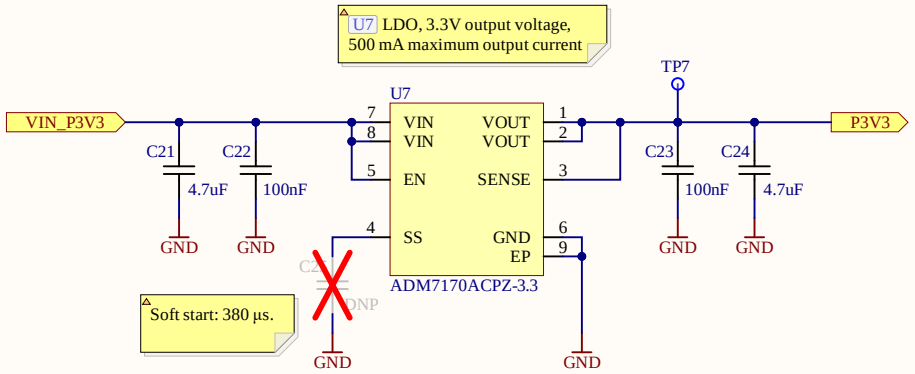
Project:	Time_Sampling_Oscilloscope.PrjPcb	Engineer: Szymon Jedliński	Revision:	1.0	*WEITI ISE*
Title	*	Drawn by: Szymon Jedliński	Sheet:	7	*ul. Nowowiejska 15/19*
File:	Power_Supply.SchDoc	Checked by:*	Total Sheet:	11	*00-665 Warszawa*
Variant:	Basic Assembly	Approved by:*	Date:	06.08.2023	



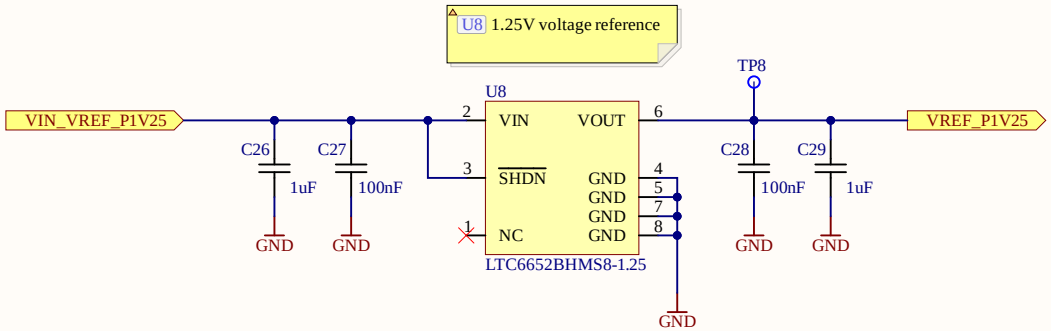
Project:	Time_Sampling_Oscilloscope.PrjPcb	Engineer: Szymon Jedliński	Revision:	1.0	*WEITI ISE*
Title	*	Drawn by: Szymon Jedliński	Sheet:	8	*ul. Nowowiejska 15/19*
File:	Power_P2V5.SchDoc	Checked by:*	Total Sheet:	11	*00-665 Warszawa*
Variant:	Basic Assembly	Approved by:*	Date:	06.08.2023	



Project:	Time_Sampling_Oscilloscope.PrjPcb	Engineer: Szymon Jedliński	Revision:	1.0	*WEITI ISE*
Title	*	Drawn by: Szymon Jedliński	Sheet:	9	*ul. Nowowiejska 15/19*
File:	Power_N2V5.SchDoc	Checked by:*	Total Sheet:	11	*00-665 Warszawa*
Variant:	Basic Assembly	Approved by:*	Date:	06.08.2023	



Project:	Time_Sampling_Oscilloscope.PrjPcb	Engineer: Szymon Jedliński	Revision:	1.0	*WEITI ISE*
Title	*	Drawn by: Szymon Jedliński	Sheet:	10	*ul. Nowowiejska 15/19*
File:	Power_P3V3.SchDoc	Checked by:*	Total Sheet:	11	*00-665 Warszawa*
Variant:	Basic Assembly	Approved by:*	Date:	06.08.2023	



Project:	Time_Sampling_Oscilloscope.PrjPcb	Engineer: Szymon Jedliński	Revision:	1.0	*WEITI ISE*
Title	*	Drawn by: Szymon Jedliński	Sheet:	11	*ul. Nowowiejska 15/19*
File:	Power_VREF_P1V25.SchDoc	Checked by:*	Total Sheet:	11	*00-665 Warszawa*
Variant:	Basic Assembly	Approved by:*	Date:	06.08.2023	