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T-Type Multilevel Converter Topologies: A Comprehensive Review

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Abstract
Renewable energy systems integration prefers DC–AC converters of high efficiency, low harmonic injection and small size. Multilevel converter (MLC) is preferred compared to two-level converter thanks to its low harmonic injection, even at low switching frequency values, and accepting high power as well as voltage levels. Among reduced switching devices count MLCs is the T-type topology. This article introduces a review of the different advanced topologies of T-type MLC in comparison with the conventional neutral point clamped converters. The operation of each topology, the design consideration and the performance in low-voltage applications such as AC drive systems, grid-tie integration of renewable energy and power train drive applications are discussed. In addition, the design considerations using enhanced semiconductor switches are elaborated. Different studies regarding MLCs—like common-mode voltage elimination or reduction, open-switch fault diagnosis, open- as well as short-circuit fault tolerance, and DC link capacitor voltage balancing for T-type topologies—are illustrated. Finally, recommendations for future work research directions are highlighted.

Keywords Multilevel converter · MLC · T-Type converter · Capacitor Balancing · Dual three-level T-type

Abbreviations

MLC	Multilevel converter
2L	Two-level
3L	Three-level
5L	Five-level
VSC	Voltage source converter
VSI	Voltage source inverter
MV	Medium voltage
PV	Photovoltaic
MPPT	Maximum power point tracking
NPC	Neutral point clamped
FCC	Flying capacitor converter
CHB	Cascaded H-bridge
DC	Direct current
AC	Alternating current
FACTS	Flexible AC transmission system
SVC	Static VAR compensator
EMI	Electromagnetic interference
IGBT	Isolated gate bipolar junction transistor
MOSFET	Metal oxide semiconductor field effect transistor
MPC	Model predictive control
CMV	Common-mode voltage
CMVE	Common-mode voltage elimination
PWM	Pulse width modulation
SHEPWM	Selective harmonic elimination PWM
Y-connected	Star connected
SVPWM	Space vector PWM
THD	Total harmonic distortion
PMSM	Permanent magnet synchronous machine
ANPC	Active neutral point clamped
PCB	Printed circuit board
SiC	Silicon carbide
Si	Silicon
ZSI	*Z*-source inverter
ST	Shoot-through
NP	Neutral point
CB-PWM	Carrier-based PWM

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1 Introduction

The rapid development in renewable energy integration requires high efficiency, low harmonic injection as well as small size grid-tie converters [1]. Two-level voltage source

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converter (2L-VSC) is preferred in low-voltage and low-power applications. However, this type of converter generates harmonic waveform that affects the performance of the connected load. The harmonics problem can be solved by adding passive power filter for specific harmonic orders. However, this solution is bulky and increases the converter size and weight. Another solution is to operate the 2L-VSC at high switching frequency levels, i.e., several tens of Kilohertz, in order to shift the high-frequency harmonic orders [1]. However, the high switching frequency affects negatively the converter switching loss as well as the overall efficiency. Multilevel converter (MLC) is a better alternative to 2L-VSC in order to decrease the harmonic contents without increasing switching frequency or adding huge passive filters to reduce the injected harmonics [2]. On the other hand, MLCs are preferred, compared to the classical 2L-VSC in many industrial applications, particularly for high-power and medium-voltage (MV) applications. Hence, MLC is more suitable for renewable energy integration systems. Figure 1 shows a block diagram of the basic photovoltaic (PV) as well as wind energy integration systems using an MLC which integrates the converted DC power to utility grid with the specified frequency and with low harmonic contents [1–3].

The basic power electronic converters used in the energy conversion of PV systems are the DC–DC, DC–AC and AC–DC converters. The DC–DC converter is used, with L (inductance) and C (capacitance) passive elements, as a boost converter to attain a load line on PV panel by controlling the boost input current (see Fig. 1a) in order to capture the maximum possible power from PV panels using maximum power point tracking (MPPT) techniques. Then the MLC (which is a DC–AC converter in this portion) is controlled to transfer the generated power and synchronize the converter to grid via a small L filter. For the wind energy system, the generated AC power from wind generator is rectified using controlled rectifier. The rectifier can be controlled in order to achieve the MPPT tracking (see Fig. 1b). Then, MLC is used, as an inverter, to convert the generated DC power to AC and synchronize it with grid [4]. More details on MPPT for PV and wind energy systems can be found in [5,6].

The most well-known, or conventional, topologies of MLCs are the neutral point clamped (NPC) converter, the flying capacitor converter (FCC) and the cascaded H-bridge (CHB) converter. Each of these converters has its own merits and demerits [7]. The common drawback of the different MLCs is the complexity of the power circuit, which is a result of the large number of switching elements. This problem has motivated researchers to develop more advanced multilevel VSC circuits with a smaller amount of switching devices to reduce the converter complexity and cost [7]. Numerous CHB-modified topologies have been introduced in [8–16]. These topologies reduce the amount of semiconductor devices compared to the conventional CHB converter. However, the converter still has the same drawback where isolated DC sources are required. In [17,18], a modified cascade transformer-based multilevel inverter is presented. This converter increases the number of voltage levels; however, it has a problem of complexity due to adding a transformer. It is observed that the modification and development in the NPC is little bit compared to the CHB power circuit. This results from the simplicity of using CHB MLC according to its modularity. In [19], an advanced configuration for the NPC is introduced to reduce the blocking voltage for the switches; however, the power circuit becomes more complicated. The T-type converter is one of the advanced NPC converter topologies that have the advantages of lower number of switching elements and higher efficiency compared to conventional NPC converter [20–23]. Then, T-type converter has been followed by many topologies in [24–33].

The target of this paper is to present a comprehensive review of the different T-type MLC topologies, discussing their evaluation compared to the NPC conventional topology. This paper is organized as follows: As the T-type converter is considered a modified topology from NPC MLC, an introduction about the conventional NPP MLC topology and its operation is discussed in Sect. 2. Then, in Sect. 3, the advanced three-level (3L) T-type MLC topology operation and construction are discussed. Efficiency evaluation of 3L T-type compared to conventional NPC and to 2L converters in recent studies is discussed. Moreover, the DC link capacitors voltage balancing studies are addressed as well. Then, in Sect. 4, the two main topologies of five-level (5L) T-type MLC are discussed. Firstly, modeling of dual 3L T-type topology is discussed. Then, efficiency evaluation and the effect of this topology harmonic content compared to those of 2L and 3L converters are addressed. This topology consists of two DC capacitors. A study for the dual 3L T-type converter capacitor balancing is addressed. Secondly, the 5L T-type topology modeling and operation are discussed. Then, a capacitor balancing study for this topology DC link is addressed. Some other T-type topologies are addressed at the end of Sect. 4. After illustrating the different T-type topologies, in Sect. 5, design considerations for T-type converters are discussed. Then, some important related studies for T-type converters and their applications are addressed. Section 6 presents the suitable applications based on the studies within this article and based on the converter production. Section 7 presents the future work and recommended studies for T-type MLCs. Finally, a conclusion is derived in Sect. 8.

2 Neutral Point Clamped Multilevel Converter

As mentioned above, NPC converter topology was the first proposed MLC [34]. This converter has been introduced

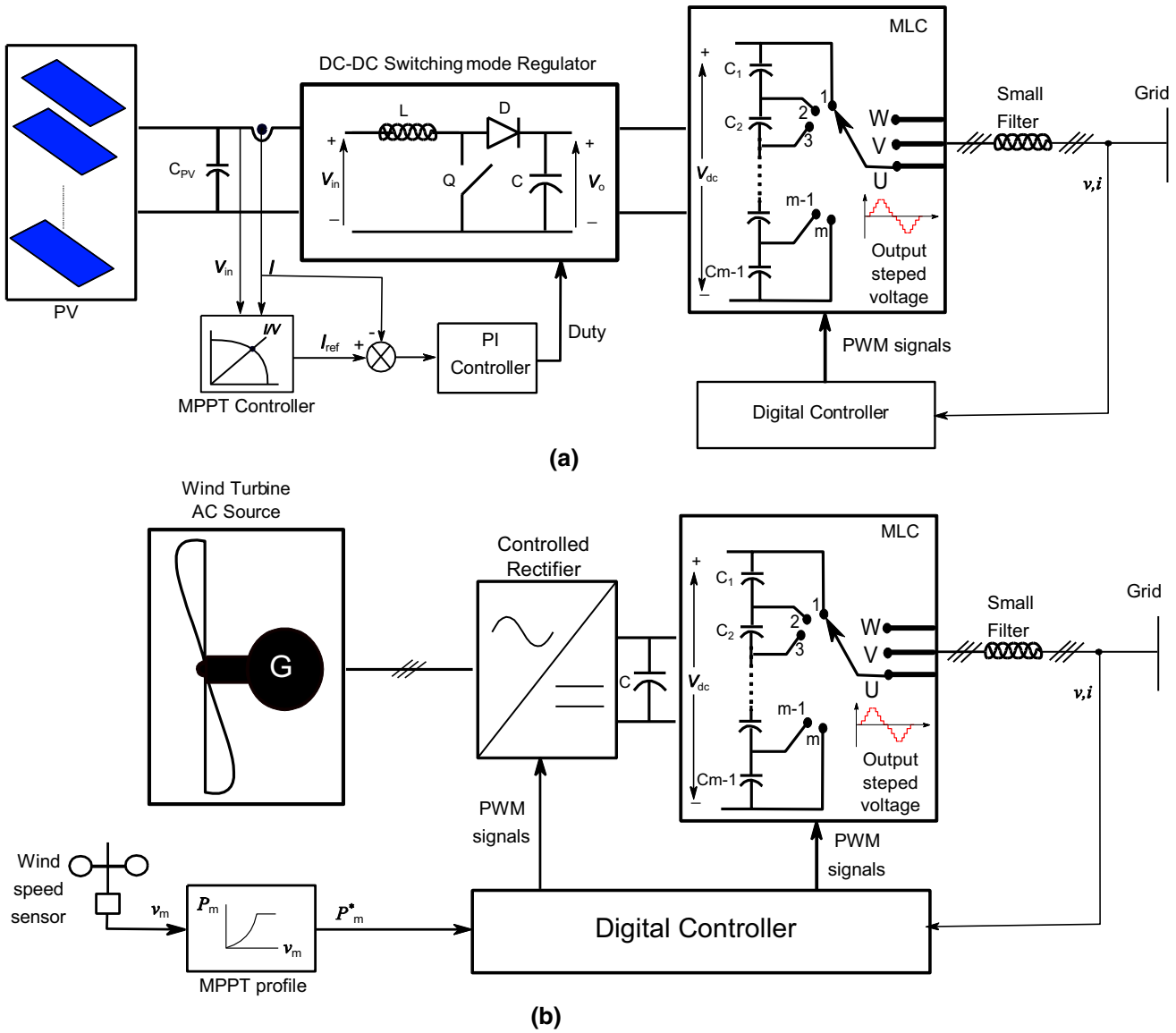

Fig. 1 Basic stages of **a** on-grid PV system using MLC and **b** wind energy system using MLC

in 1981 by Nabae, Takahashi, and Akagi. Then, a series of circuit modification and applications have been introduced in [35]–[48]. Figure 2 shows the circuit diagrams of a single-phase NPC converter for both 5L and 3L circuits. The single-phase circuit is described here for simplicity. However, the discussion in this paper will consider the three-phase converter topology. The possible switching states and the corresponding voltage levels for both 5L and 3L topologies are listed in Tables 1 and 2, respectively. The operation of this converter can be described as follows. For instance, for the 5L NPC, to attain the voltage level of point P_1, the switches Q_2, Q_3, Q_4 and $Q_{1'}$ have to be turned on. Hence, D_5 and D_6 will be forward-biased and forced to be on as well. Therefore, P_1 voltage level can appear on the output terminal.

For an n-level three-phase NPC converter, the number of required capacitors is $n-1$. The line to DC link midpoint 'O' voltage (here v_{UO}) can attain n different voltage levels, the line voltage attains $2n-1$ different voltage levels, and the Y-connected load phase voltage can obtain $4n-3$ different voltage levels. This topology is composed out of $6(n-1)$ semiconductor switches and $6(n-2)$ diodes for a three-phase circuit.

The main advantage of this topology is that the DC supply is commonly feed the converter three phases. On the other hand, the drawback of this topology is the increased number of clamping diodes particularly with high number of voltage levels.

The most well-known applications of the NPC converters are variable-speed AC drives [49–60], flexible AC transmis-

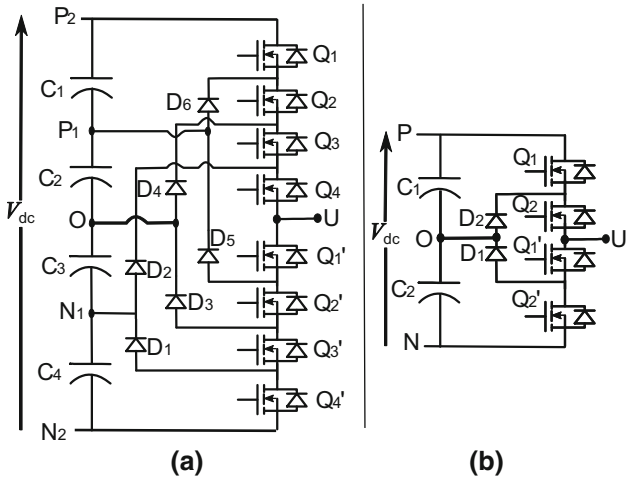

Fig. 2 NPC inverter circuit for single-phase **a** five-level converter and **b** three-level converter

Table 1 Possible switching states and voltage levels for 5L NPC inverter

Level	Q_1	Q_2	Q_3	Q_4	$Q_{1'}$	$Q_{2'}$	$Q_{3'}$	$Q_{4'}$	v_{UO} (V)
P_2	1	1	1	1	0	0	0	0	$V_{dc}/2$
P_1	0	1	1	1	1	0	0	0	$V_{dc}/4$
O	0	0	1	1	1	1	0	0	0
N_1	0	0	0	1	1	1	1	0	$-V_{dc}/4$
N_2	0	0	0	0	1	1	1	1	$-V_{dc}/2$

Table 2 Possible switching states and voltage levels for 3L NPC inverter

Level	Q_1	Q_2	$Q_{1'}$	$Q_{2'}$	v_{UO} (V)
P	1	1	0	0	$V_{dc}/2$
O	0	1	1	0	0
N	0	0	1	1	$-V_{dc}/2$

sion devices (FACTS) [61–65] and static VAR compensators (SVCs) [66,67].

3 3L T-Type MLC

For NPC MLCs with high number of levels, the number of clamping diodes increases the power circuit complexity and decreases the converter efficiency. Moreover, the large number of semiconductors, on the printed circuit boards (PCBs), increases the electromagnetic interference (EMI), particularly in high-power applications and relatively high switching frequencies. This results in ringing and overshoots in the converter output voltage. Hence, the topic of reducing the number of semiconductors in MLCs became an essential target for researchers. T-type MLC is a reduced NPC converter that eliminates the clamping diodes from the power circuit.

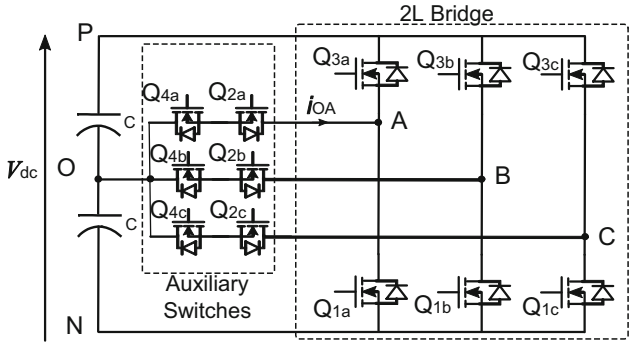

Fig. 3 Wiring diagram of three-phase 3L T-type MLC

The first T-type converter is proposed in 2010 by Schweizer in [68]. Then, many studies and modifications for this type of converter have been introduced in the several past few years in [20–33]. The following subsections describe the operation and summarize the research work performed using 3L T-type topology.

3.1 3L T-Type Converter Topology Description and Operation

The 3L T-type topology is shown in Fig. 3. It consists of a full-bridge 2L inverter connected to three anti-series branches of semiconductor switches named 'auxiliary switches' in this article. The idea in this topology is to clamp the DC link midpoint using these auxiliary switches and, hence, reducing the number of elements in the current paths. This increases the converter efficiency. Compared to 3L NPC, the current paths of the 3L T-type have lower number of semiconductor switches for achieving 'P' and 'N' voltage levels. For instance, to attain voltage level 'P' for phase-A, the current path, as shown in Fig. 4a, flows in Q_3. However, for the 3L NPC, to achieve the same voltage level 'P', the current flows through two switches Q_1, Q_2. Similar number of switches is used for the negative level 'N'. However, to attain voltage level 'O', two cascaded elements have to be used for both converters. Hence, the T-type topology reduces the conduction loss compared to the NPC MLC.

The operation of the T-type inverter is described as follows: In order to achieve the three voltage levels (of points P, N and O), a list of switching states is given in Table 3 and shown in Fig. 5. However, a modified switching pattern helps to reduce the switching stress of this topology. The following is a typical example to describe this modified switching pattern.

As shown in Fig. 4, if only one of the phase-A auxiliary switches, Q_2 or Q_4, is turned on, the current i_{OA} will be zero. Hence, no conduction loss results from turning on one of the auxiliary switches. Therefore, if the switch Q_2 is kept ON during attaining 'O' as well as 'P' levels, lower energy

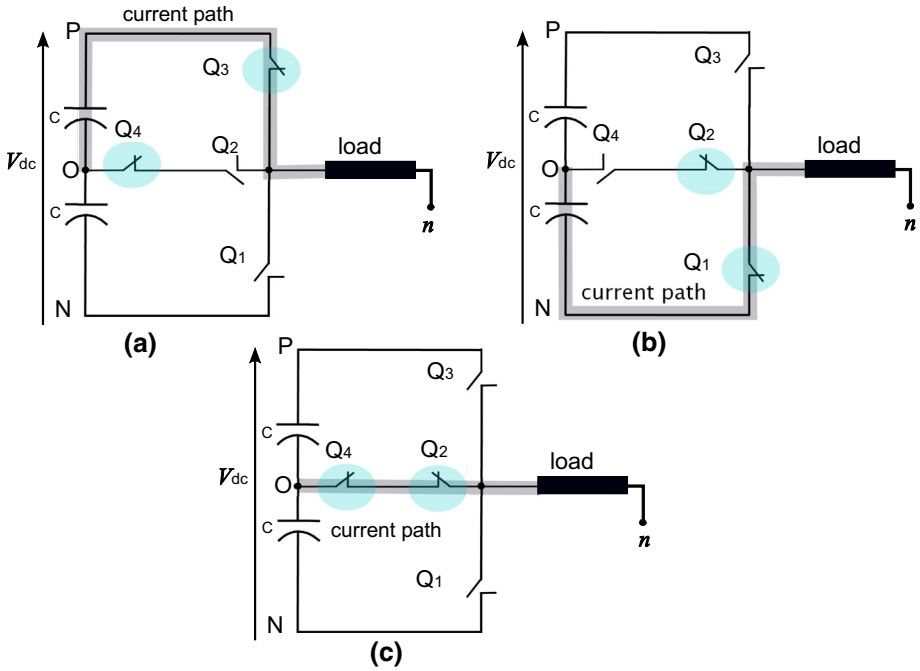

Fig. 4 Switching states wiring diagram for 3L T-type converter using modified switching pattern

Table 3 Possible switching states and voltage levels for 3L T-type inverter

Level	Q_1	Q_2	Q_3	Q_4	Phase voltage
P	0	0	1	0	$V_{dc}/2$
O	0	1	0	1	0
N	1	0	0	0	$-V_{dc}/2$

will be required to operate the converter. The same is also for Q_4 to achieve 'O' and 'N' voltage levels. Figure 6 shows the modified switching pattern for phase-A, while Table 4 gives the corresponding switching states. The modified switching states for one phase of a 3L T-type converter are shown in Fig. 4. It can be observed that, by applying the modified switching states, not only the conduction loss of the auxiliary switches is reduced, but also the switching loss will be reduced. This can reduce the converter switching stress and increase the semiconductor lifetime.

A comparison between the 3L T-type and NPC converters is given in Table 5. From the wiring diagram of the 3L T-type MLC, as shown in Fig. 3, it can be observed that the auxiliary semiconductor switches Q_{4a}, Q_{4b} and Q_{4c} are common-source MOSFETs or common emitter in case of IGBT semiconductor switches. This results in reducing the number of isolated DC power supplies used in driver circuits. Here, for 3L T-type topology, 8 isolated DC power supplies are required, while the corresponding 3L NPC, see Fig. 2b, requires 10 isolated DC power supplies for the driver circuits.

In addition, comparing the 3L T-type to the 3L NPC, 6 clamping diodes are removed from the later power circuit. On the contrary, the open-circuit voltage drop across the semiconductor switches in 3L T-type is higher than that in 3L NPC topology. For the modularity, it can be observed that the 3L T-type MLC is composed of two modules of bridges. The first is a 2L full-bridge, and the other auxiliary switches can be composed of three modules of anti-series switches. On the other hand, the 3L NPC MLC is composed of two

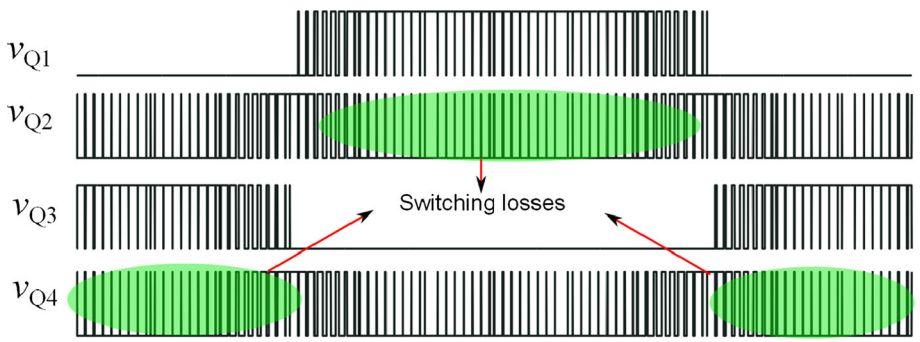

Fig. 5 Switching pattern for one phase of T-type semiconductor switches

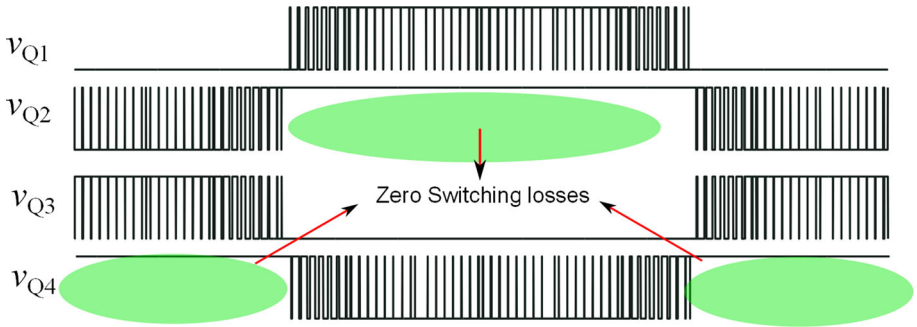

Fig. 6 Modified switching pattern for one phase of T-type switches

Table 4 Modified switching states and voltage for 3L T-type inverter

Level	Q_1	Q_2	Q_3	Q_4	Phase voltage	Wiring diagram
P	0	0	1	1	$V_{dc}/2$	Figure 4a
O	0	1	0	1	0	Figure 4c
N	1	1	0	0	$-V_{dc}/2$	Figure 4b

Table 5 Comparison between 3L T-type and NPC converters

Converter	3L T-type	3L NPC
No. of switches	12	12
No. of diodes	0	6
No. of driver isolated DC supplies	8	10
Max. switch voltage	V_{dc}	$V_{dc}/2$
Max. diode voltage	0	$V_{dc}/2$
Modularity	$2 \times$ 2L inverter	$2 \times$ 2L inverter + 6 diodes
Conduction loss	Lower	Higher

modules of 2L full-bridges connected in cascade and also connected to 6 power diodes.

3.2 3L T-Type Efficiency Evaluation

The 3L T-type MLC has been studied in many articles and companies application notes. Some of these articles illustrated the converter efficiency. The efficiency evaluation for the T-type drive system has been studied in [20,33,69]. It has been observed that the efficiency of the 3L T-type MLC is higher than that of NPC in frequency range lower than 7 kHz. The converter has been tested for a wide range of switching states and with two different machines. It can be observed that small rating drive systems only were elaborated. For power train and electric vehicles, the 3L T-type converter has been evaluated in [70,71]. These different studies confirm the superiority of the 3L T-type converter efficiency compared to the conventional 3L NPC. Another study for the 3L T-type converter has been introduced in [72] using reverse blocking (RB) switches instead of the auxiliary switches (Q_2, Q_4 in Fig. 7). The study reflects that this converter is more efficient than both 3L T-type with anti-series auxiliary branch and 2L converters. The circuit for the 3L RB T-type converter is shown in Fig. 7. A comparative study based on thermal analysis of the 3L T-type MLC has been introduced in [56]. The study investigated the converter loss involving the thermal analysis using PSIM simulation program. Similar trend is obtained from the studies in [73–76], which investigated the performance of 3L T-type MLC applied to renewable energy systems. The authors have replaced the auxiliary branch 'IGBT or MOSFET with the anti-parallel diode' by four MOSFETs instead. This modification makes two parallel paths for the DC link midpoint current and, hence, reduces the conduction loss of the T-type converter for the zero-vector. However, the number of semiconductor switches has increased. The loss calculations have been performed for different power ratings. The results show that the modification in the auxiliary branch increases the converter efficiency. However, the use of RB MOSFETs will be much better as the switches in the zero-vector current paths will be only one MOSFET. Hence, conduction losses for zero-vector will decrease compared to the topology in [20].

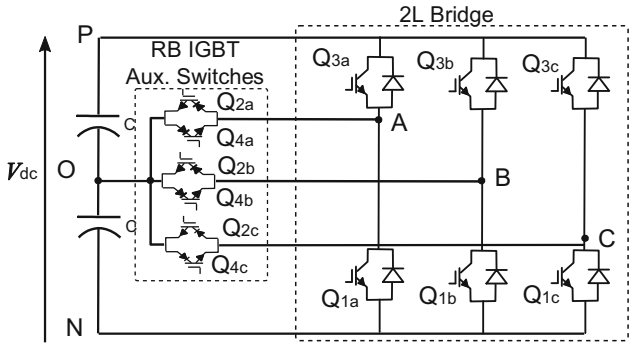

Fig. 7 Wiring diagram for 3L RB T-type MLC

The maximum efficiency operation of 3L T-type MLC has been investigated and compared with the 2L as well as the 3L NPC converters while supplying an interior permanent magnet synchronous machine (IPMSM) [77]. In this study, the authors proposed an algorithm to convert the 3L T-type topology into 2L topology during low-efficiency periods. However, the results showed fluctuations in the output volt-

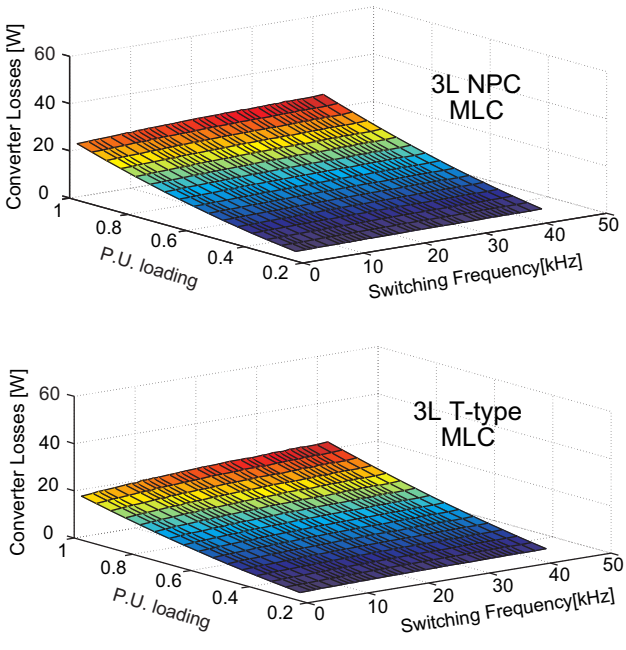

Fig. 8 Losses of 3L T-type and NPC MLCs. (Reproduced with permission from [90])

age levels. Moreover, the effect of the switching frequency change has not been considered. Summarizing the converter efficiency, Fig. 8 shows the converter losses for a wide range of switching states at different loading conditions of an IM drive system [78].

3.3 Neutral Point Voltage Control of 3L T-Type MLC

The neutral point of the 3L T-type MLC, similar to NPC MLC, needs to be controlled in order to keep the voltages of the two cascaded capacitors equal. The number of switching states of the 3L T-type converter is 27 as listed in Table 6. Applying space vector transformation to these switching states, the resultant vector diagram can be described as shown in Fig. 9 [79]. The idea of the capacitor balancing comes from changing the current switching state from P-type to N-type as listed in Table 6. For instance, applying a switching state, to achieve voltage level of point 'P' (P-type state), discharges

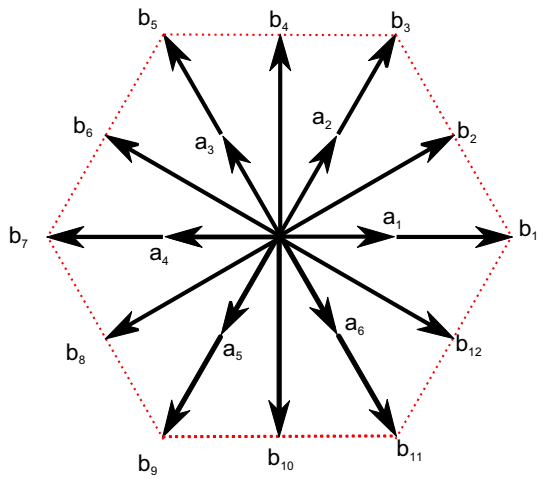

Fig. 9 Vector diagram for 3L T-type MLC

the upper capacitor and charges the lower one. Similarly, the upper capacitor charges by applying the switching state that achieves 'N' voltage level.

In [80], model predictive control (MPC) is used to control the neutral point voltage for balancing the DC link capacitors and reducing the common-mode voltage (CMV). Firstly, the cost function is used to balance the DC link capacitors and, hence, reduce the CMV by using only the higher values of outer hexagon vectors (b_2, b_4, b_6, b_8, b_{10} and b_{12}) which produce zero CMV. This point will be described later in this article in more detail. It is worth mentioning that the priority is given to balance the capacitors. Hence, the drawback of this technique is the absence of the CMV in the MPC cost function. Inclusion of the CMV and the switching state transitions in the cost function will effectively achieve the drive system requirements.

Neutral point balancing has been also studied based on a hysteresis control for the capacitor voltages in [81] and based on a selected harmonic elimination PWM (SHEPWM) technique in [82]. Both techniques succeeded in balancing the capacitor voltages. However, the mathematical computations for the later technique are very complex and time-consuming. In contrast, the study in [83] improves the calculations for the switching pulse intervals of SVPWM technique and reduces the capacitor voltage fluctuations at different loading power

Table 6 Vector classification and switching states of a 3L T-type MLC

Small vec.	States		Medium vec.	States	Large vec.	States	'O' vec.
	P_{type}	N_{type}					
a_1	POO	ONN	b_2	PON	b_1	PNN	PPP
a_2	PPO	OON	b_4	OPN	b_3	PPN	NNN
a_3	OPO	NON	b_6	NPO	b_5	NPN	OOO
a_4	OPP	NOO	b_8	NOP	b_7	NPP	
a_5	OOP	NNO	b_{10}	ONP	b_9	NNP	
a_6	POP	ONO	b_{12}	PNO	b_{11}	PNP	

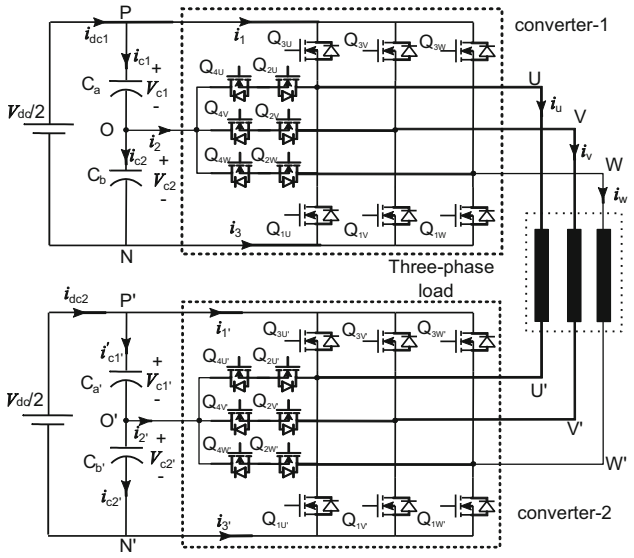

Fig. 10 Wiring diagram of a dual 3L T-type MLC

factor values. However, the switching frequency and the effects of the modulation index variations have not been considered in that study.

4 Advanced 5L T-Type MLCs

Several 5L T-type topologies have been proposed. Hereinafter, two different topologies of 5L T-type MLCs will be discussed in detail. Firstly, the dual 3L T-type as a 5L converter will be discussed. Then, the advanced topology of 5L T-type MLC will be discussed in detail. Some enhancements to these topologies will be also discussed.

4.1 Dual 3L T-Type MLC Operation-Based SVPWM

This topology has been introduced firstly in [33] in comparison with the NPC MLCs. The circuit diagram of the dual 3L T-type converter supplied by isolated DC sources and connected to a three-phase open-end load is shown in Fig. 10. A switching function model has been discussed for the dual 3L T-type MLC in [78]. This function is a mathematical representation for the VSC to give a clear vision of the converter switching states and the number of voltage levels. This study concluded that the presented topology could attain the same number of voltage vectors of the 5L MLCs with higher number of switching states (729 states instead of 125 for the conventional 5L MLCs).

4.1.1 Dual 3L T-Type MLC Modeling and Operation

The switching function model of this topology produces a phase voltage relation of the *Y*-connected load as [78]:

$$v_{UU'} = 2/3\,(m_U - m_{U'} - 1/2\,(m_V - m_{V'} + m_W - m_{W'}))\,, \quad (1)$$

Table 7 Modes of operation of a dual T-type: phase UU′

Converter-1	m_U	Point	Converter-2	m'_U	Point
Q_{3U}, Q_{4U}	1	P	Q'_{3U}, Q'_{4U}	1	P′
Q_{2U}, Q_{4U}	0	O	Q'_{2U}, Q'_{4U}	0	O′
Q_{1U}, Q_{2U}	−1	N	$Q'_{1U}, Q_{2U'}$	−1	N′

Table 8 Possible switching states for phase UU′ of the dual T-type

Converter I	Converter II	Points	V'_{UU}
Q_{3U}, Q_{4U}	$Q_{1U'}, Q_{2U'}$	P−N′	$+V_{dc}$
Q_{3U}, Q_{4U}	$Q_{2U'}, Q_{4U'}$	P−O′	$+V_{dc}/2$
Q_{2U}, Q_{4U}	$Q_{1U'}, Q_{2U'}$	O−N′	
Q_{3U}, Q_{4U}	$Q_{3U'}, Q_{4U'}$	P−P′	0
Q_{2U}, Q_{4U}	$Q_{2U'}, Q_{4U'}$	O−O′	
Q_{1U}, Q_{2U}	$Q_{1U'}, Q_{2U'}$	N−N′	
Q_{2U}, Q_{4U}	$Q_{3U'}, Q_{4U'}$	O−P′	$-V_{dc}/2$
Q_{1U}, Q_{2U}	$Q_{2U'}, Q_{4U'}$	N−O′	
Q_{1U}, Q_{2U}	$Q_{3U'}, Q_{4U'}$	N−P′	$-V_{dc}$

where m_X is the switching function to connect phase X to P, N or O as shown in Fig. 10. Here, X is U, V or W for converter-1, and U′, V′ or W′ for converter-2. The switching function can be 1, − 1 or 0 as clarified in Table 7.

By applying the switching function possibilities to (1), it has been observed that the vectors of a 5L MLC, Fig. 11, can be generated from this topology. The operation of the dual converter is described in Table 8. For MLCs, the number of possible switching states for an n-level three-phase converter equals n^3. Based on the converter switching states, the space vector is calculated by using the well-known space vector relation described in [79]. Unlike the conventional 5L MLCs with $5^3 = 125$ switching states, the dual 3L T-type topology is considered as a 5L converter with $(3^3)^2 = 729$ switching states and produces 61 different vectors, i.e., O, A_1–A_6, B_1–B_{12}, C_1–C_{18}, D_1–D_{24}. These vectors can be represented as shown in Fig. 11 which is a 5L vector diagram. The waveform of the line-to-line voltage for each converter v_{UV} and $v_{U'V'}$ is shown in Fig. 12, while the phase voltage $v_{UU'}$ is shown in Fig. 13. It is clear from the voltage level that this topology is equivalent to 5L MLCs. Another important issue in this topology is that the switching of this converter has been performed in such a way to reduce the switching stress on the dual converters as shown in Fig. 12. It can be seen that only one of the dual converters changes its switching state at the same instant (see Fig. 12a, b at the intervals T_x).

The dual 3L T-type topology has been studied in [33,78, 84] and compared with the 3L T-type and 5L NPC MLCs while supplying an IM drive system at different power and switching frequency ranges. Figure 14 shows the total converter loss where higher efficiency for the dual T-type

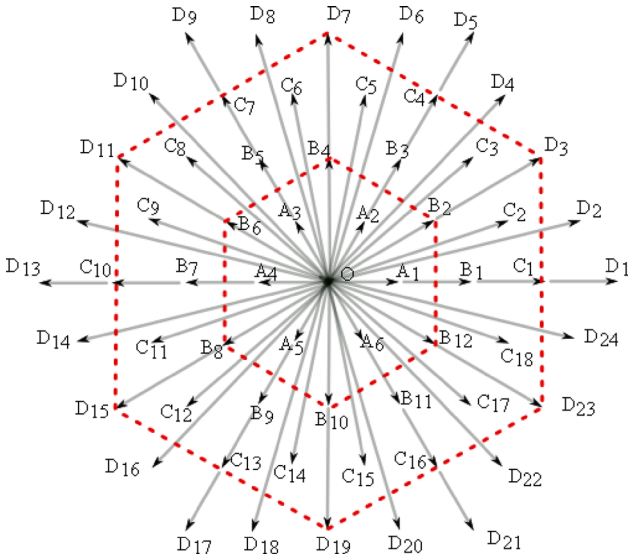

Fig. 11 Vector diagram for 5L MLC

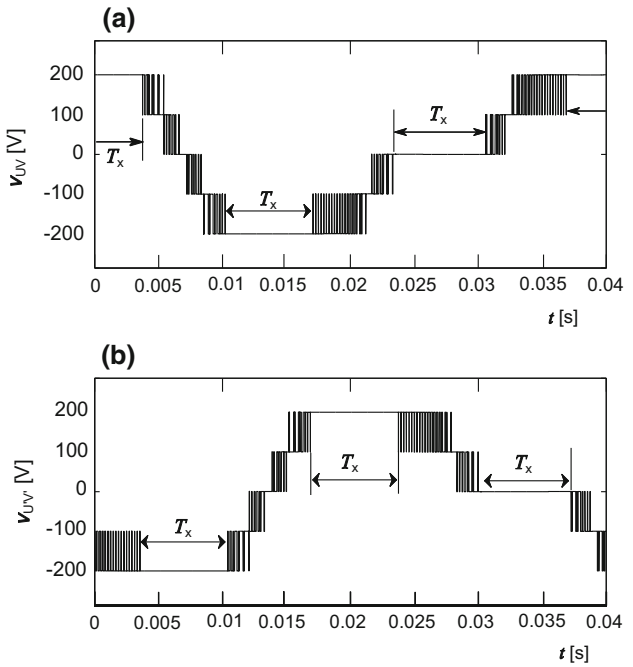

Fig. 12 Line-to-line voltages of dual 3L T-type MLC. **a** Converter-1 line-to-line voltage and **b** Converter-2 line-to-line voltage. (Reproduced with permission from [90])

converter can be observed. In [32], SVPWM computations for MLCs have been introduced and applied to the dual 3L T-type converter to study the magnetic losses of the load connected to MLCs.

The dual T-type topology has been examined with two isolated photovoltaic (PV) sources and connected to the grid [85,86]. It was observed that this topology is suitable for PV application. However, the capacitor balancing was overlooked and there was a lack of experimental verification.

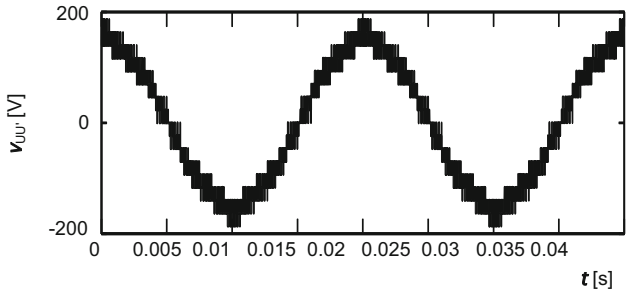

Fig. 13 Phase voltage of dual 3L T-type MLC. (Reproduced with permission from [90])

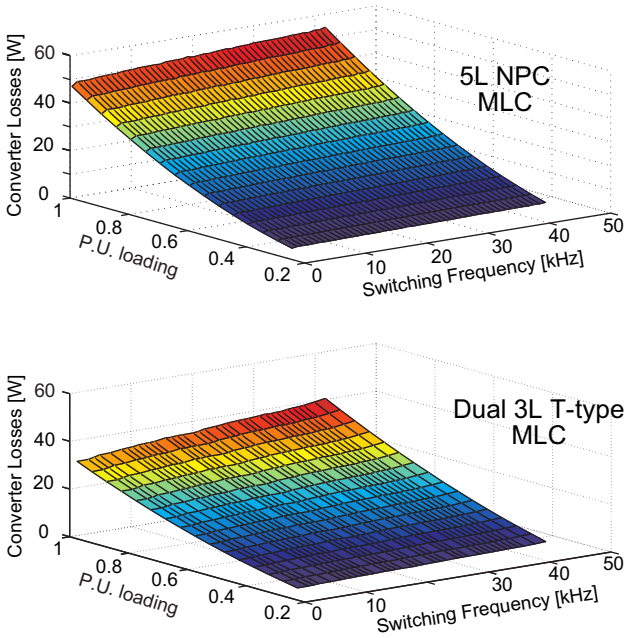

Fig. 14 Calculated converter total power loss for dual 3L T-type and 5L NPC MLCs. (Reproduced with permission from [78])

Also in [86], a common DC link for the dual converters has been used, which reduces the number of voltage levels and increases the total harmonic distortion (THD). A single-phase scheme of this topology has been introduced in [87,88] based on multistate switching cell. The conduction loss has been reduced as a result of the two parallel paths for the mid-point current. However, applying such an idea in three-phase topology will increase the number of used semiconductor devices substantially [75]. In [89], the same topology has been studied in energy storage system where the use of 5L inverter decreases the harmonic content and increases the power quality of the storage system.

The topology has been also studied in high-power traction application with a dual PMSM in [90]. This study reflected that the used PWM technique reduces the DC link capacitor voltage and current stresses on the DC link capacitor.

Table 9 Comparison between conventional 5L NPC and the proposed topology [90]

Converter	5L NPC	Dual 3L T-type
No. of switching states	125	729
No. of switches	24	24
No. of clamping diodes	18	–
No. of driver isolated DC supply	22	16
Voltage stress	$\left(\frac{1}{4} : \frac{3}{4}\right) V_{dc}$	$\left(\frac{1}{4} : \frac{1}{2}\right) V_{dc}$
Converter losses	High	Low (reduced by 35%)

However, the topology could be considered as 3L and not 5L.

From this survey and comparing to the 5L NPC, the advantages of the dual 3L T-type topology can be summarized as listed in Table 9. It can be concluded that the dual 3L T-type topology can reduce the converter cost and increase the converter efficiency.

4.1.2 Effect of Harmonics Reduction for Dual 3L T-Type MLC on Drive Losses

Besides the converter losses, the harmonic reduction in the converter output improves the drive system efficiency compared to lower levels MLCs. The effect of using 3L and dual 3L T-type MLCs, compared to conventional 2L converter, on the core losses in magnetic materials and electrical machines has been investigated [27,28,31,91]. The loss analysis has been investigated using 2D finite element method. Similar trends have been observed for the 3L T-type converters compared to the 2L one in [93,94] considering only the converter losses. These studies reflected that the use of higher levels of MLCs reduces the machine core loss as a result of harmonic reduction. An example for the effect of harmonics on the core loss of electrical machine can be described as shown in Fig. 15 [27]. The core loss, Fig. 15a, of a 150-kVA synchronous machine is calculated at different supply cases, i.e., sinusoidal supply, 3L T-type inverter and 5L T-type inverter, and at different switching frequency values, i.e., 1, 2.5, 5, 10 kHz. The corresponding voltage THD values for both 3L and 5L T-type converters are described in Fig. 15b. It can be observed that the 5L inverter contributes lower core loss and almost similar to sinusoidal supply even at low switching frequency (1 kHz). However, the core loss for 3L inverter case is affected by switching frequency increase. This gives the advantage of operating 5L converters at low frequency for AC drive applications, the issue that reduces the converter switching losses.

The effect of removing CMV on the drive losses has been investigated, and the use of higher multilevel converter is recommended in this case [30]. This article showed that the CMV elimination increases the harmonic contents and increases the connected machine core losses. The machine core loss, for the same synchronous machine in [27], at CMV elimination and at normal 3L and 5L supply is shown in Fig. 16 for half- and full-load conditions. It has been observed that the higher number of levels of the MLCs positively affects the drive efficiency at the expense of the cost. Hence, cost versus efficiency factor has to be investigated according to the specific application requirements.

4.1.3 Capacitor Balancing of Dual 3L T-Type MLC

As NPC and FCC MLCs, T-type MLC requires capacitor balancing. However, the capacitor balancing technique is topology dependent. This section describes the capacitor balancing of the dual 3L T-type MLC. Generally, MLC capacitor balancing can be performed either by using auxiliary circuit [93], or by modulation and control technique [92–99]. The dual 3L T-type MLC capacitor balancing has been studied once in [100] where the problem of the capacitor unbalance was attributed to the fluctuation of the DC link midpoints, O and O′, as shown in Fig. 10, due to non-uniform switching across the series-connected capacitors. The charging and discharging of the series-connected capacitors for similar intervals and currents can keep these capacitors balanced. Actually, the charging and discharging intervals depend on the switching pattern and the desired space vector. Therefore, the switching patterns have to be designed to keep these capacitors balanced. Applying the P-type or N-type switching states is the solution to balance the DC link capacitors. A study for the different switching states of the dual 3L T-type converter has been introduced in [74]. The switching state effects on the capacitor balancing are summarized in Table 10.

It was observed that the major effect group has too many switching states. A number of 480 major switching states can be used for balancing the two DC link capacitors. An advanced algorithm to balance the DC link capacitor voltage has been simulated using MATLAB\Simulink and implemented using Vertix2-Pro FPGA. The algorithm succeeded in balancing the capacitor voltages at different loading conditions.

4.2 5L T-Type MLC Description and Operation-Based SVPWM

The 5L T-type topology is an enhanced expanded topology to the 3L one. It has been firstly introduced in [24]. The circuit diagram for a three-phase 5L T-type MLC connected to a three-phase load is shown in Fig. 17. This converter is composed of three power modules, i.e., one 3L T-type and two 2L converter modules. A circuit with similar functionality and

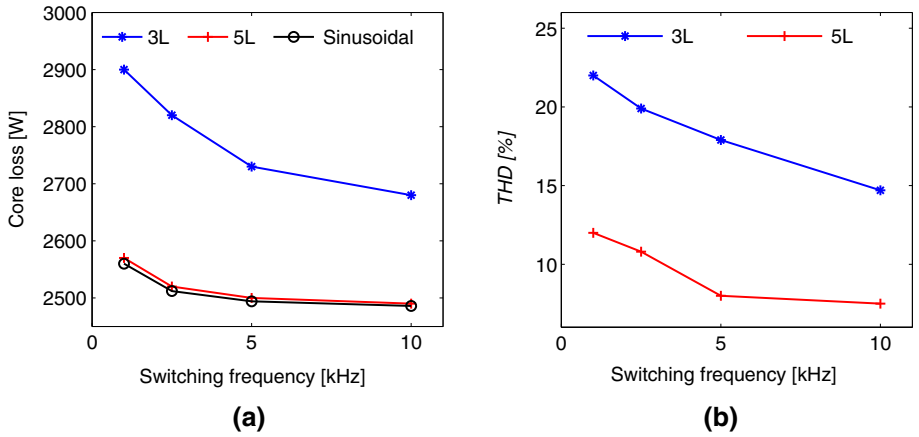

Fig. 15 Core losses and voltage THD values of 3L and 5L dual T-type MLCs

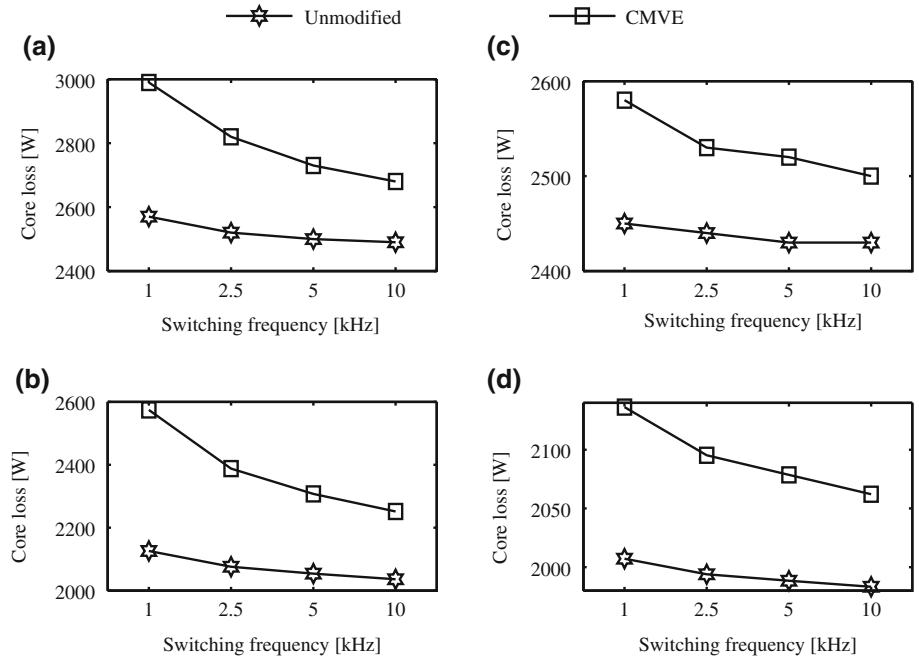

Fig. 16 Core losses due to CMVE and at unmodified case for **a** 3L full-load, **b** 3L half-load, **c** 5L full-load and **d** 5L half-load

Table 10 Vectors and corresponding switching states effect group

Vector	O	As	Bs	Cs	Ds
No effect	45	–	132	–	24
Major effect	–	216	84	156	24
Minor effect	–	–	48	–	–

different topology has been studied in [26] where the converter with different auxiliary branch bidirectional switches was introduced. The following subsections describe the 5L T-type operation, modeling and DC link capacitor balancing.

4.2.1 5L T-Type MLC Modeling and Operation

The operation of this topology can be described as follows. The switching states are listed in Table 11. It can be observed that switches Q_7 and/or Q_8 are used with all voltage levels in order to reduce the switching stress on the converter and hence reduce the switching loss. Such a switching mechanism was compared to the traditional switching as shown in Fig. 18.

As described earlier, the switching function model is used to clarify the converter output levels and voltage vectors. A switching function model has been introduced in [24]. The load *Y*-connected phase voltage 'v_{US}' of this topology can be described as:

$$v_{Us} = \frac{1}{12}\begin{pmatrix} 2m_{UP1} - 2m_{UN1} + 4m_{UP2} - 4m_{UN2} \\ -m_{VP1} + m_{VN1} - 2m_{VP2} + 2m_{VN2} \\ -m_{WP1} + m_{WN1} - 2m_{WP2} + 2m_{WN2} \end{pmatrix}. \quad (2)$$

Table 12 describes the switching function values for the 5L T-type MLC. Applying the switching function values in Table 11, the resultant voltage are of 17 levels, i.e.,

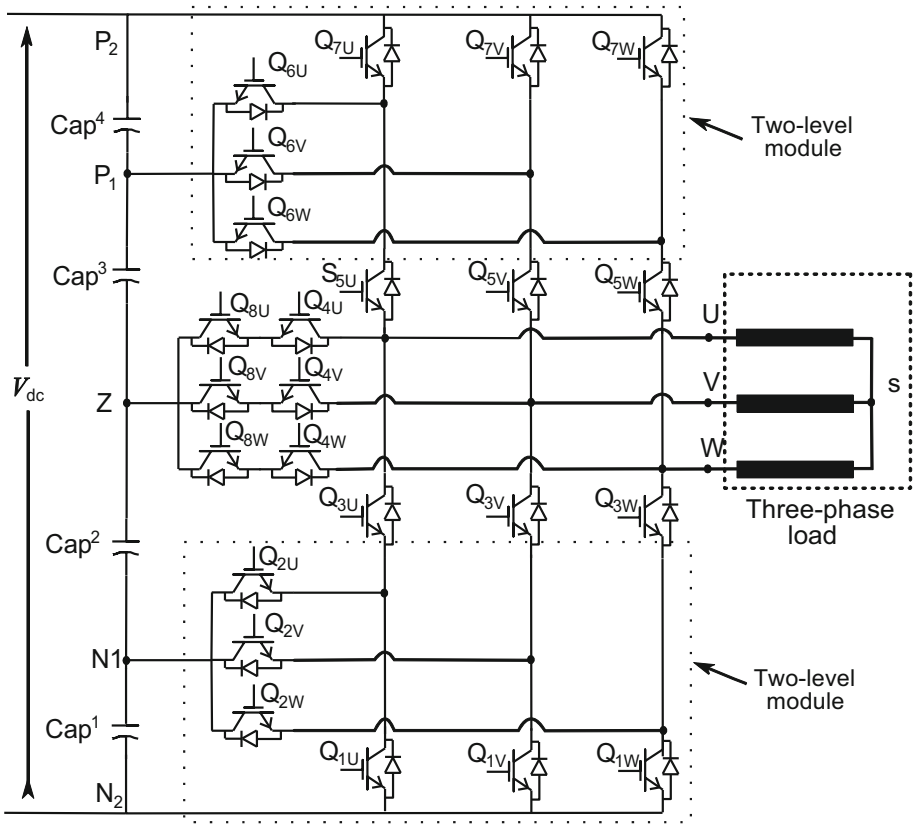

Fig. 17 Three-phase circuit of 5L T-type MLC

Table 11 Switching states and modes of operation of a 5L T-type: phase U

Converter-1	m_{UP2}	m_{UP1}	m_{UZ}	m_{UN1}	m_{UN2}	Point	v_{UZ} (V)
Q_{5U}, Q_{7U}, Q_{4U}	1	0	0	0	0	P_2	$V_{dc}/2$
Q_{5U}, Q_{6U}, Q_{4U}	0	1	0	0	0	P_1	$V_{dc}/4$
Q_{8U}, Q_{4U}	0	0	1	0	0	Z	0
Q_{2U}, Q_{3U}, Q_{8U}	0	0	0	1	0	N_1	$-V_{dc}/4$
Q_{1U}, Q_{3U}, Q_{8U}	0	0	0	0	1	N_2	$-V_{dc}/2$

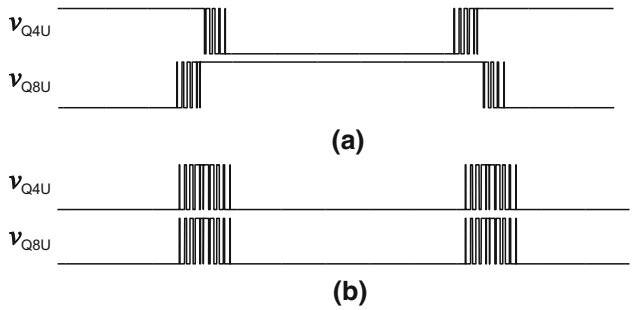

Fig. 18 Switching pulses for **a** lower stress and **b** traditional switching techniques for 5L T-type MLC

$\left\{\frac{8}{3}, \frac{7}{3}, 2, \frac{5}{3}, \frac{4}{3}, 1, \frac{2}{3}, \frac{1}{3}, 0, \frac{-8}{3}, \frac{-7}{3}, -2, \frac{-5}{3}, \frac{-4}{3}, -1, \frac{-2}{3}, \frac{-1}{3}\right\}$ $\frac{V_{dc}}{4}$ which are similar to 5L NPC MLC. On the other hand, by applying the switching possibilities to the SVPWM relation mentioned in [79], the resultant vectors can be represented by the hexagon shown in Fig. 11. A power loss study for the 5L T-type MLC has been presented in [24].

This topology compared to some other topologies has been studied while supplying a 40-kW drive system as a part of electric vehicle. Figure 19 shows a comparison between the 5L T-type losses and the corresponding 5L NPC, 3L T-type as well as 2L converters. It can be observed that the loss of the proposed 5L T-type converter is much lower than the corresponding 5L NPC. For instance, the losses decreased by 44% at 10 kHz switching frequency. Another study for the same converter has been introduced in [24,70] and for a prototype of 4-kW IM drive system where the same conclusion can be drawn. Figure 20 shows the total converter loss for the 5L T-type topology compared to the 5L NPC. It can be observed that, at a switching frequency of 5 kHz, the 5L T-type MLC reduces the converter loss by 42% compared to the 5L NPC. Table 12 shows a comparison between 5L T-type and 5L NPC MLCs. It can be observed that the 5L

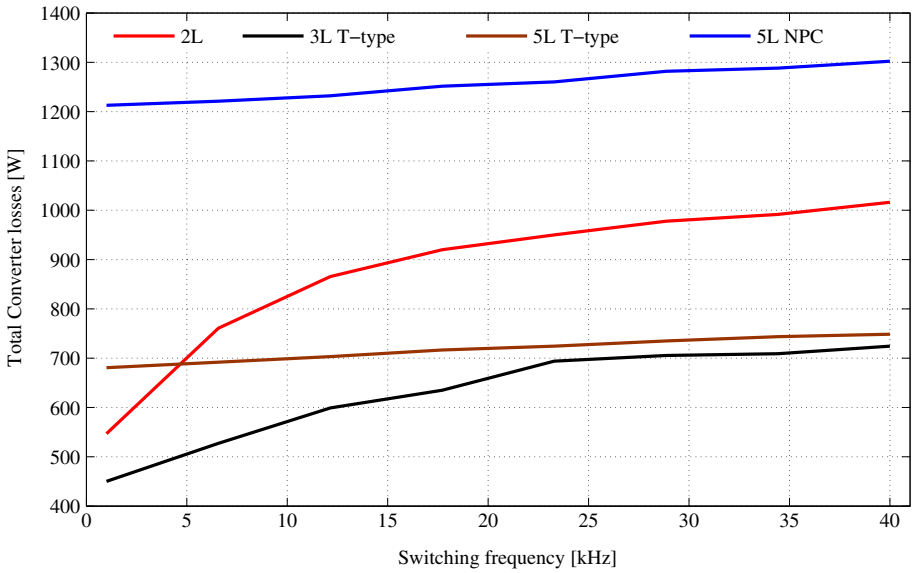

Fig. 19 5L T-type (T5) losses compared to 2L, 3L T-type and 5L NPC (DCC). Captured from [24]

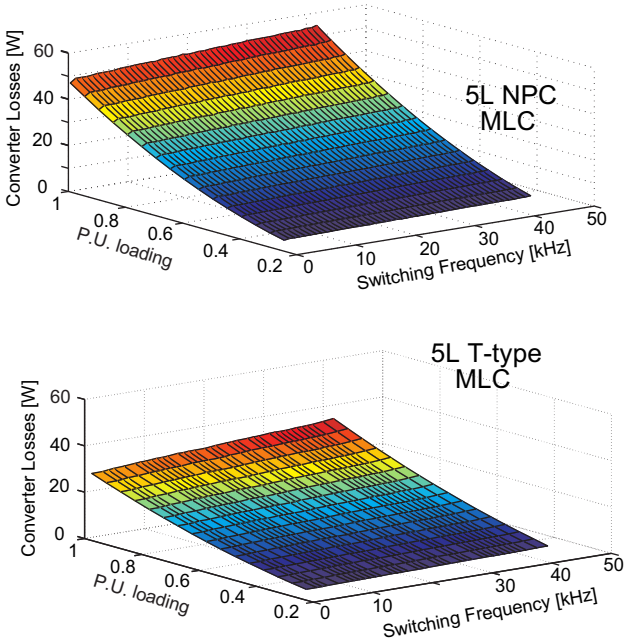

Fig. 20 Comparison between 5L T-type and 5L NPC losses at a wide range of switching frequencies. (Reproduced with permission from [90])

T-type topology reduces the number of switches and reduces the converter conduction loss.

4.2.2 Capacitor Balancing of 5L T-Type MLC

Only one study has addressed the issue of capacitor voltage balancing in this topology where an auxiliary circuit has been added [101]. Therefore, the converter complexity has increased by adding the capacitor balancing auxiliary circuit.

Table 12 Comparison between 5L NPC and 5L T-type MLCs

Converter	5L NPC	5L T-type
No. of switching states	125	125
No. of switches	24	24
No. of clamping diodes	18	–
No. of driver isolated DC supplies	22	16
Voltage stress	$\left(\frac{1}{4} : \frac{3}{4}\right) V_{\mathrm{dc}}$	$\left(\frac{1}{4} : \frac{3}{4}\right) V_{\mathrm{dc}}$
Converter losses	High	Low (reduced by 42%)

4.3 Other T-Type Topologies

Some other topologies have been introduced for single-phase MLCs. An active NPC (ANPC) has been proposed in [102]. It mixed the NPC and the FCC MLCs together in order to get 5L converter using two isolated DC power supplies. The circuit diagram is shown in Fig. 21. However, this topology requires separated DC supplies for the three-phase circuit, which increases the converter size and cost. Modified circuits of the ANPC have been introduced in [103,104]. These topologies reduced the number of semiconductors used and hence reduced the converter losses. However, it requires separated DC supplies for the three-phase circuit.

5 T-Type MLCs' Related Studies

Generally, MLCs are recommended in high-power and medium-voltage applications. Since the T-type topologies

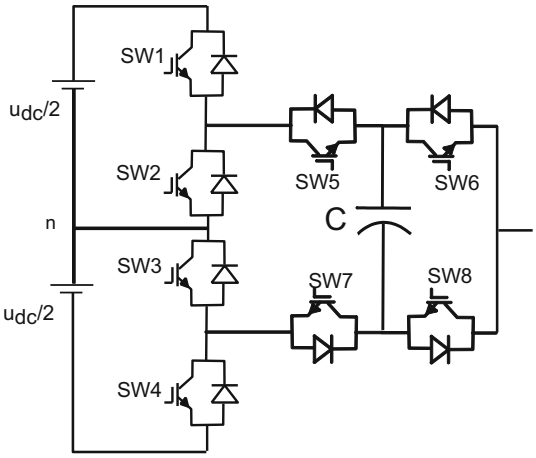

Fig. 21 5L ANPC converter circuit. (Reproduced with permission from [114])

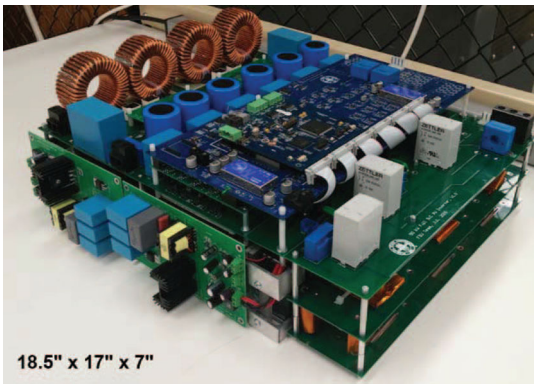

Fig. 22 50-kW SiC PV converter prototype. (Reproduced with permission from [86])

reduce the cost of MLCs, it can be used as well in LV applications.

Semikron and Fuji Electronics companies have designed 3L T-type power modules for low-power applications (like SKIP-35TMLI12F4V2 power module produced by Semikron [105] and 12MB150 VX-120-50 1200V, 50A power module produced by Fuji [71]) besides the design and production of the high-power modules of the same topology (like SKiM601TMLI12E4B, 1200 V 600 A power module). Mostly, the LV power modules are used in variable-speed drive applications. In addition, T-type topologies are considered promising MLCs for renewable energy application, particularly for PV grid integration. In this section, the different studies followed by the applications based on T-type MLCs will be discussed.

5.1 T-Type MLCs Design Considerations

In Fuji Electric, Semikron and Fairchild Semiconductor application notes [71,105,106], the EMI design issues for 3L T-type MLC have been discussed. Due to large commutation paths in the MLC PCBs compared to 2L converter circuits, the stray inductance increases and hence the ringing (voltage overshoots at the instant of level transition) appears. The voltage overshoot results from the energy stored in the stray inductance L_s, $E_s = \frac{1}{2}L_s i^2$, through the current path. This voltage overshoot is added to the DC link voltage and increases over the blocking voltage of the used semiconductors. Hence, the semiconductor devices may be damaged if the stray inductance minimization is not considered in the power circuit design. For that issue, most of the power modules are produced as a single-phase module in order to reduce the stray inductance due to short current paths.

The 3L T-type MLC has been implemented using silicon carbide (SiC) semiconductor MOSFET which is preferred to the silicon (Si) IGBT. Si IGBTs that support high breakdown voltage have considerably high on-resistance. This high on-resistance increases the IGBT conduction losses. IGBTs can achieve lower on-resistance than MOSFETs by injecting minority carriers into the depletion region that produces tail current at the turnoff transition. This transition delay increases the switching losses of the IGBT. SiC devices have much lower depletion resistance than Si devices. Hence, SiC MOSFETs have much lower loss than Si IGBTs. This enables the use of higher switching frequency, smaller passives, and smaller and less expensive heat sinks [107–111]. Moreover, SiC MOSFETs have smaller chip area and an ultralow recovery loss of body diodes. Many research articles have introduced 3L T-type MLC-based SiC semiconductor switches [111–115]. An important issue in the SiC T-type MLC design is that the transition periods are very small (can be several nanoseconds). This transition has the same effect of the high frequency that increases the impedance of the stray inductances and affects the voltage overshoots in the power PCBs. Therefore, the power and the driver PCBs have to be well designed by keeping current paths as short as possible. In addition, it is better to keep an appropriate distance between the drivers and the semiconductor device [108–110].

An example for a well-designed SiC-based T-type MLC is the prototype, shown in Fig. 22, of 50 kW which has been implemented and presented in [86]. In addition to the compact size, film and electrolytic capacitors are very close to the power circuit in order to reduce the stray inductance.

5.2 CMV Elimination/Reduction Using T-Type MLCs

CMV is a relatively high-frequency voltage that appears between the two isolated ground systems. In AC drives, this voltage appears between the machine neutral point and the connected inverter DC link midpoint [95]. Figure 23 describes the relation between the neutral point of two isolated systems and their relation to ground. In this figure, the

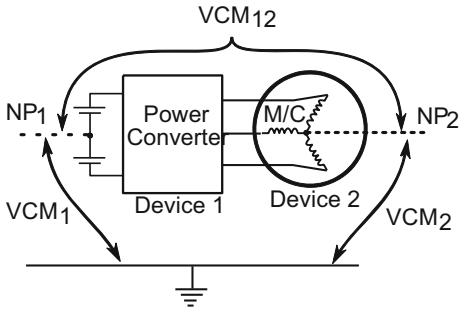

Fig. 23 Meaning of CMV of two connected power systems

CMV_{12} is considered the total CMV. The relation of the CMV for a three-phase system can be described as:

$$v_{\mathrm{CMV}} = 1/3\,(v_{AN} + v_{BN} + v_{CN})\,. \tag{3}$$

This voltage is considered as the third harmonic of a sinusoidal three-phase AC system. However, for the variable-speed drives, CMV is the third harmonic and its multiples. Hence, it is considered a relatively high frequency signal.

The CMV cannot be eliminated by using 2L inverter switching states. This results from the third harmonic component that exists at all the operating vectors of the 2L inverter. However, in MLCs, there are some vectors with zero 3rd harmonic components. If a converter is controlled to operate at these vectors, the CMV will not appear in the drive system. To clarify, here is an example for the 3L inverter.

The vector diagram of 3L MLC, shown in Fig. 9, has 19 vectors, i.e., 6 inner vectors, 12 outer vectors and zero-vector. Applying the CMV relation to the switching states of the 3L inverter, it can be observed that the even outer vectors (b_2–b_{12}) have zero CMV. Hence, if the 3L inverter is operated using these vectors, zero CMV will be attained. However, the voltage output of this converter will be similar to the 2L inverter. The vector diagram for the zero CMV of 3L inverter is shown in Fig. 9 in dotted line. Similarly, in 5L inverter, the hexagon of the zero CMV is shown in Fig. 11 in dotted line. It can be observed that two hexagons of vectors appear in 5L vector diagram, which reflects the flexibility of selecting the operating vector in CMV elimination.

There are some studies addressing CMV elimination or reduction in T-type topologies. A carrier-based PWM (CB-PWM) technique has been presented in [116,117] to reduce the CMV of the 3L T-type MLC. The carrier waveform has been generated as the sum of three carriers, with an f_s switching frequency and with a displacement from each other by 3 times f_s. This results in reducing the CMV considerably. It is important to note that, unlike SVPWM, the CMV cannot be eliminated fully using CB-PWM. MPC has been used to reduce the CMV of a 3L T-type inverter in [80] with SVPWM theory. However, the CMV voltage has not been fully eliminated as the CMV problem has been considered as a second priority where the capacitor balancing has the highest priority.

It is worthy to remind that the CMV elimination is important to reduce the bearing current and reduce the noise on the surrounding controllers. However, the elimination of the CMV increases the core loss of the connected machine. Hence, this loss has to be considered in drive system design [30].

5.3 *Z*-Source-Based T-Type MLCs

Z-source inverter (ZSI) is one of the promising converter topologies. It collects the advantages of the voltage source inverter (VSI) and current source inverter. It involves a two-port network composed of two capacitors and two inductors connected in an X-shape coupled to a VSI. The ZSI advantageously uses the shoot-through (ST) state, which controls the converter gain to operate the inverter as DC/AC buck–boost inverter [118–121].

The basic ZSI wiring is shown in Fig. 24a. Another topology with different passive element connections is shown in Fig. 24b and is called quasi-ZSI (QZSI).

The 2L inverter of the QZSI has been replaced by 3L T-type MLC in [122–124]. The topology has been tested in faulty as well as normal operating conditions in [124]. In [125], the converter has been studied while connected to PV panels as DC supply. The efficiency evaluation of the 3L T-type ZSI has been evaluated and compared to the use of step-up DC/DC converter followed by 2L inverter [124]. The study in [125] presented SVPWM to control the shoot-through (ST) period and the DC link midpoint voltage. It has been observed that the overall converter losses including the magnetic loss have not been studied for this topology.

5.4 Photovoltaic Grid-Tie T-Type MLC

According to the reports of Bloomberg New Energy Finance, 40 GW in 2013 and 52 GW in 2014, and 61 GW of solar installations were expected in 2015 [126]. Numerous articles have been involved T-type MLCs in renewable energy applications, particularly for PV grid integration. The advantages of using the T-type PV converter compared to the conventional 2L one are the lower harmonic contents, smaller filter size and lower converter losses [127–129].

PV is the most renewable energy application that has been studied with MLCs [141]. Generally, the grid integration of the PV sources has two different configurations, i.e., one- and two-stage configurations.

The one-stage configuration uses only DC/AC converter, while the two-stage configuration uses boost converter connected to a DC/AC converter. The boost converter aims to fulfill the MPPT and regulate the voltage of the DC link mid-

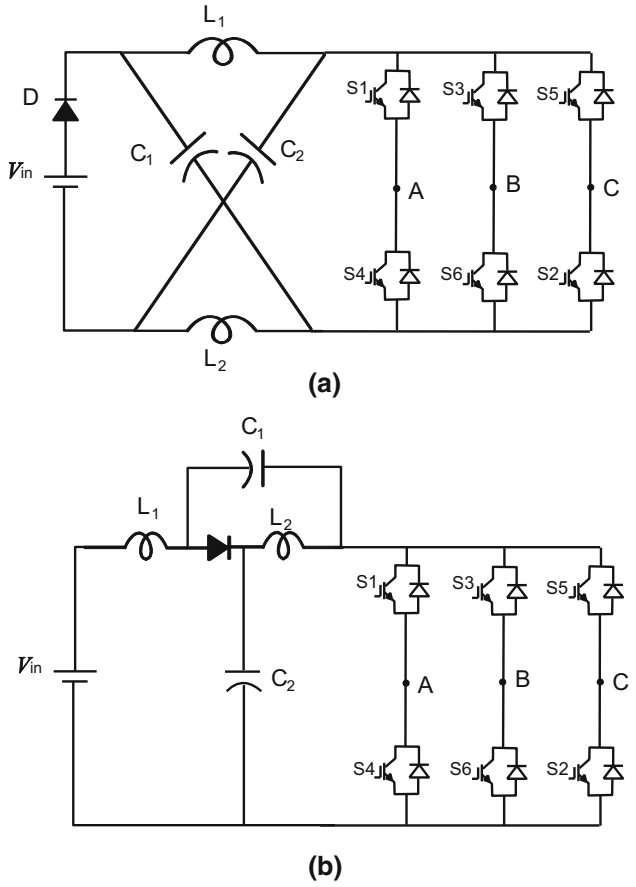

Fig. 24 Wiring diagram for **a** basic ZSI and **b** quasi-ZSI. (Reproduced with permission from [132])

point. The following are some of the research works that have been involved the T-type MLC into PV application either for a single- or for a three-phase circuit topology.

In [130,131], PV inverter-based 3L T-type inverter has been introduced. The first study considered the neutral point (NP) voltage balancing for low-voltage ride-through operation. It clarified that replacing the zero-vector by two opposite P- and N-type small vectors of equal duty cycle can reduce the NP voltage fluctuations. This way reduces the capacitor voltage unbalance; however, it increases the converter switching losses. The later study has been carried out using MPC. However, the switching frequency limit has not been considered, which increases the converter losses.

Single-phase 3L T-type MLC has been studied in many papers. An adaptive MPC is investigated in [131–134], for designing the interfacing filter of the grid-tie single-phase T-type inverter based on an online identification for the filter inductance. It was concluded that the 3L T-type is potential solution in grid-tie converter applications. The later study compares the T-type converter with 2L VSI equipped with boost converter. However, this study investigated the two converters at low power rating as well as at 100 MHz switching frequency. Actually, there is no need to operate MLCs at this high switching frequency range because MLCs reduce harmonic contents even at low switching frequency values (several kHz). On the other hand, the use of passive filter reduces the harmonic contents and the necessity for such high switching frequency is greatly reduced.

A maximum power extraction from PV system using T-type MLC has been investigated using MPC [135]. The study addressed the current control and the capacitor balancing only in the cost function. This method produces many harmonic orders in the output voltage. Moreover, the work was based on small sampling simulation time, which is difficult to be practically implemented using MPC. A three-phase two-stage 3L transformer-less PV system has been investigated [136]. The study fulfilled the capacitor balancing and MPPT using DC–DC chopper and an inverter controlled by CB-PWM technique. However, the output current is distorted with high harmonic contents.

One-stage PV inverter has been investigated in [137–139] using 3L T-type inverter. Generally, when PV modules are connected as separated DC link, the efficiency of the MPPT decreases particularly at partial shading condition. These articles presented an independent control of the two DC links for separate MPPT.

The study investigated the capacitor balancing by adding or subtracting the minimum calculated dwell switching period to the three-phase periods. The technique could balance the capacitor voltages. However, this technique will change the resultant space vector and hence affects the results accuracy.

5.5 Fault Diagnosis and Fault Tolerance for T-Type MLCs

Nowadays, the interest in power electronic converter reliability has increased because it affects greatly the cost and efficiency of the overall power systems [140]. Many research articles have studied the reliability of power conversion systems, particularly the fault detection and fault tolerance control of the power electronic semiconductor switches [140–144]. The semiconductor switches fault can be classified into two main categories, i.e., short-switch as well as open-switch faults [145]. The first category causes large overcurrent values and is difficult to be detected and cleared without an auxiliary hardware [145–148]. However, the open-switch fault causes a current distortion and affects the driver circuit as well as the other semiconductor switches in the converter circuit. Moreover, it degrades the performance of the overall power system [148]. Hence, it is important to investigate the open-switch faults of power electronic converters. Several studies been investigated the open-switch faults of the T-type MLCs.

The open-switch fault detection (OSFD) for the 3L T-type converter has been studied in different papers. The study in [149] investigated the OSFD using the criterion of the mass center of a histogram, which is a visual impression for the data distribution of the output. This method has succeeded in identifying the fault location. It has the advantage of being load dependent, as it requires only the three-phase voltage signals. However, it consumes time, more than one cycle to read data besides the time to calculate the histogram and make its analysis. In [150], an OSFD for an active T-type converter has been investigated where two auxiliary branches per phase are used. Each auxiliary branch contains two anti-series switches. This fault-tolerant mechanism has been implemented successfully to compensate the fault. However, the converter auxiliary branches raise the converter complexity and cost.

A fault-tolerant study for the three-phase T-type has been presented in [143,148]. The criterion of the fault detection was based on the average of the normalized phase current and the change of the neutral point voltage calculations. Similarly, the action for the fault tolerance takes several electrical periods. Similar fault detection has been investigated in [151–154] with different fault-tolerant techniques. These studies have compensated the open-switch fault by using alternative SVPWM switching states with satisfactory results. However, long compensation period is observed.

The 3L T-type OSFD has been studied while the converter is in rectification mode in [155–159]. The fault detection in [155,156] was based on the angle of the grid voltage which is the same as the current angle for the unity power factor control. The fault has been classified and controlled in order to keep the current undistorted by the converter reconfiguration using the possible SVPWM switching states. However, this approach takes long time for compensation. A comparison between different tolerance control techniques for the converter auxiliary switches (Q_2, Q_4 in Fig. 3) has been presented in [157,158]. The different techniques have been compared according to the current ripples, the switching losses, as well as the DC link voltage ripples. However, the vertical switches (Q_1, Q_3) have not been considered.

Studies in [159–161] investigated the fault tolerance of the 3L T-type MLC in both open circuit and short circuit based on adding auxiliary circuit shown in Figs. 25 and 26. However, the circuit becomes complex due to the consideration of the short-circuit fault. The idea was to compensate the circuit by an additional auxiliary branch using a back-to-back thyristors and two cascaded switching devices as shown in Fig. 25. The added circuit in [161] also could operate at normal healthy case in sharing currents and hence improve the thermal overload of the converter. This study has been extended in [162] to include a soft-switching using a quasi-zero-voltage switching and zero-current switching techniques applied to SiC MOSFET-based four-branch 3L T-type MLC. It has been concluded that the topologies in [161,162] compensate the open- and short-circuit faults properly. From this survey, it can be concluded that the three-phase 5L T-type MLC topologies have not been studied yet in faulty case.

6 Applications of T-Type MLC

T-type and NPC are similar in function, but topologically are different as has been declared in this article. Hence, the applications of NPC are valid for T-type MLC. However, on the other hand, the T-type converters have higher efficiencies. However, as the T-type converters are still not widespread in industry, we could not get their industrial participation till now. Fuji and Semikron are the well-known power electronics companies manufacturing T-type converters. These companies produce T-type converter with voltage ratings of 1200–1700 V and with the current range from 40 to 950 A which gives the ability to operate T-type MLCs in many applications like back-to-back converters for electrical drives, distributed renewable energy integration (PV

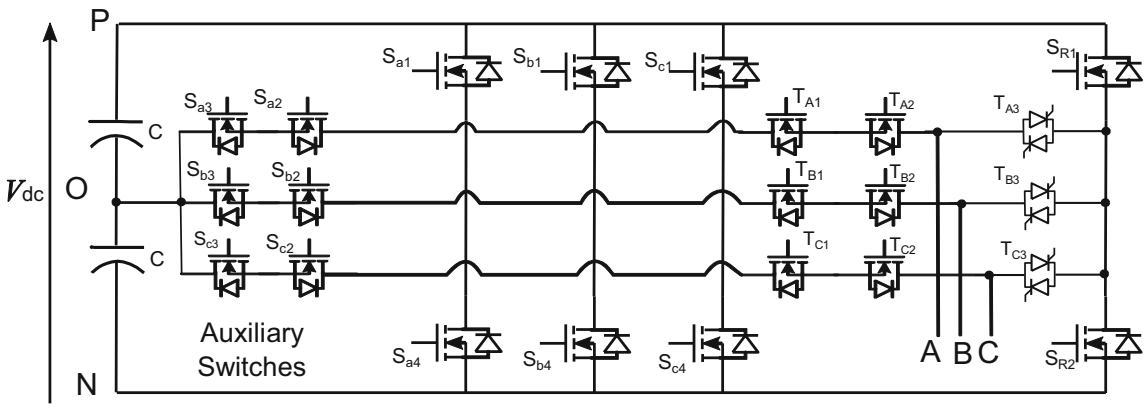

Fig. 25 Modified circuit diagram for fault tolerance of 3L T-type MLC

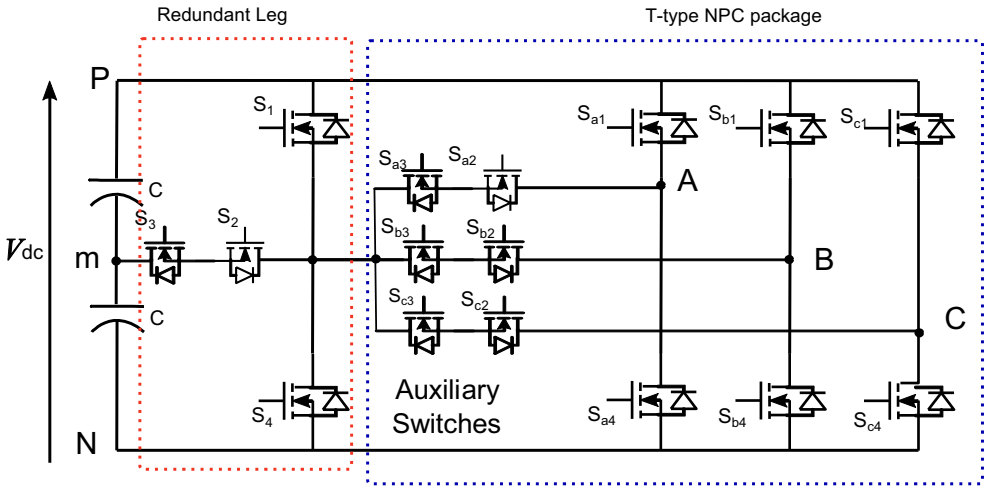

Fig. 26 Modified circuit for fault tolerance of 3L T-type MLC [86]

and wind power up to the level of rooftop power stations) and inverter modules for DC–AC conversion in electrical vehicles [163]. On the other hand, the availability of higher voltage levels of IGBTs gives the opportunity to implement the T-type converters for MV applications like in FACTS and SVC. Finally, the studies in this article reflected that the T-type converter is valid for all other conventional MLC applications and has higher efficiency.

7 Future Work

Although the 5L drive systems have better performance compared to 3L and 2L drive systems, the fault diagnosis and fault tolerance of these topologies have not been studied yet. Therefore, the authors plan to study the fault diagnosis and tolerance of 5L T-type converters. In addition, the authors are going to test the performance of the 5L T-type converters using advanced semiconductor technologies and for three-phase topologies in order to enhance their power circuit and reduce the EMI effects.

8 Conclusion

This paper introduces a comprehensive review of different T-type MLC topologies and their performance and applications. The 3L, the dual 3L and the 5L T-type MLC topologies have been presented and discussed. The operation, mathematical models and main applications for each of the aforementioned topologies have been summarized. The design aspects for the T-type MLCs, particularly for SiC power electronic devices, have been discussed. According to this review, it can be concluded that the T-type MLCs' performance is superior compared to conventional 2L and NPC converters.

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