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Hardware-in-the-Loop (HIL) to reduce the development cost of power electronic converters

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***Abstract* – This paper proposes a validation methodology for implementing solutions to challenges involved with power electronic converter design. Typically, the design process consists of first simulating the converter and then implementing it on hardware. Here, an intermediate step is added where the controller is connected to a real-time simulator before being connected to real hardware. This allows for virtual testing of scenarios that cannot be conducted with physical hardware without risking damage to the hardware. This technique will be demonstrated by implementing a new method of control, the drifting PWM, for a multilevel packed U-cell (PUC) converter. The drifting PWM allows for a slight variation in the switching state so that regulation of the auxiliary capacitor can be achieved. This method will be simulated offline and in real-time to demonstrate its long term reliability. Once fully functional, the controller is implemented on an FPGA board, from which it will control the real converter. Simulation results, as well as experimental results, are presented and compared. It is demonstrated that the HIL technique is a very effective tool for designing multilevel converter controllers.**

***Index Terms*--control, FPGA, HIL, power quality, multi-level converter, real-time simulation**

I. INTRODUCTION

Typically, the first step taken during industrial prototype development of power electronics is demonstrating the feasibility and performance of the proposed concept using offline simulation tools. However, offline simulation of complex power electronic systems with large numbers of switches can be very time consuming. In the case of complex systems that include several multi-level converters with hundreds of switches in series, the traditional solution is to connect the prototype controller to a full-scale or scaled-down analog model of the plant, enabling the performance of hundreds of tests in a reasonable amount of time, that closely resemble real operating conditions. This technique is commonly used to design and test fast power electronic systems using IGBTs under steady-state and faulty operating conditions.

Ideally, a researcher or engineer will spend most of their time focused on developing and testing new designs, as opposed to experimentation with real hardware, which can be time consuming to setup and perform. Scaled-down analog setups can be damaged and exhibit too many losses, leading to costly project delays. Furthermore, an analog setup may be impractical and very expensive when the power rating of the power electronic system increases, or if the complete system involves the interconnection of several power electronic converters interconnected to a complex electrical grid.

One alternative to using an analog setup is to connect the prototype controller hardware to a fully digital real-time simulator that is capable of emulating the complete plant in real-time. Leading manufacturers of large thyristor-based HVDC and FACTS systems have use the Hardware-in-the-Loop (HIL) testing method for the last 20 years. However, conventional real-time simulators used for power grid applications are not able to accurately simulate fast voltage-source converters with high-frequency PWM controls. These simulators also have difficulties simulating systems with a large number of switches, such as in modern multi-level modular converter (MMC) systems. For this reason, most power electronic manufacturers still use analog setups to test new voltage source converter (VSC) MMC topologies, as well as simpler 2-level and 3-level VSCs

However, the availability of modern digital simulators equipped with fast multi-core processors interfaced with FPGA chips, as well as new power electronic converter models and solvers with real-time interpolation, enable the design and testing of complex VSC systems using a virtual plant. Using HIL simulation, the prototype of the controller is tested on the simulated plant before being connected to the real converter. In HIL simulation, the controller's analog input and digital output converters are implemented as close as possible to the actual controller to emulate signal conversion delays. Control signals are connected to the analog and digital inputs of the virtual plant model.

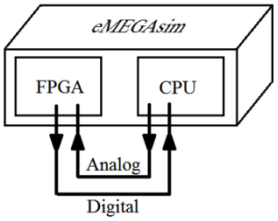

Figure 1 Basic HIL setup.

From the controller perspective, there is no difference between the real converter and the simulated one, as illustrated in Figure 1. Of course, there are time-step delays between the IGBT firing signals sent by the controller and the

current output by the real-time simulator. The total latency must therefore be kept to a minimum by using a very small time-step during simulation.

This technique allows testing of the controller, even if a prototype of the converter is not available. It can also be used to perform tests that would be harmful to the physical converter hardware, such as the response of the controller to overvoltage or overcurrent during fault conditions when some protection functions are out of service.

HIL simulation can also be used for statistical testing, such as Monte Carlo studies [1, 2]; which may require multiple iterations when different fault cases are simulated. Therefore, if these studies are performed in real-time, the required time for each case is greatly reduced.

Of course, fully digital simulators can only be used if the global accuracy is <good enough> for the testing of control and protection systems under all normal and faulty operating conditions. Simulation specialists must therefore conduct benchmark tests to verify the accuracy of the real-time simulators, which must use fixed step integration methods with time-step values in the range of 10 µs to 50 µs. Such time-step values are normally used for thyristor-based applications, but are too large for fast voltage source converters. The real-time simulator must use optimized models and solvers capable of simulating the effect of fast switching events occurring between simulation time-steps. Benchmark testing using conventional off-line simulation software with variable step solvers, or with very small time-step values, must be conducted. Results obtained using a real-time simulator can then be compared with those obtained using offline simulation software. Ideally, results should also be validated with an analog setup, if available, or during commissioning of the real hardware.

Over the last five (5) years, the HIL testing of fast 2-level and 3-level VSCs has been verified by leading power electronic manufacturers, such as Toyota (hybrid vehicle)[3], Mitsubishi, Converteam and Loher (Siemens). However, the use of real-time simulators for MMC systems is the new to industry because of the challenges faced when simulating systems with a very large number of switches in real-time.

This paper proposes the use of HIL testing for a seven-level VSC as an intermediate step to implementing a solution from offline simulation, to HIL simulation and then to real hardware implementation. This technique will be used to implement an FPGA-based controller for a PUC multilevel power converter [4],[5],[6]. In section II, the PUC power converter will be introduced. The method of control used will be discussed in section III. Section IV. illustrates the results obtained for each step of the implementation method, followed by a conclusion in Section V. .

II. PRESENTATION OF THE TOPOLOGY

The topology used in this paper, the packed U cell (PUC), was first introduced in [4]. The model is a hybrid of an H-bridge and a flying capacitor, as illustrated in Figure 2. Each cell is comprised of two switches and one capacitor. Using only two cells, it can reach 7 levels. By adding an additional cell, it can reach up to 15 levels and so on.

Theoretically, T_n and T_n' are always complementary, where n can be 1, 2 or 3. If T_n and T_n' are closed at the same time, it would result in short-circuiting of either C_{AUX} or C_{BUS}. The capacitors should never be short-circuited. Because of the inductance L, the circuit should never be open. The intrinsic diode of the MOSFET will allow the current to find a valid path. When only relevant switching cases are considered, there are only eight possible switching combinations. Each of these place the converter

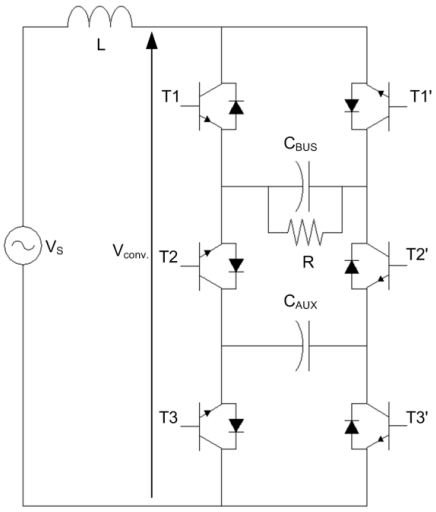

Figure 2 Hard switching equivalent circuit (7-level PUC rectifier).

in a different state, as shown in the Table 1. As can be observed, state 0 can be obtained by two different switch combinations, due to the symmetry of the circuit. In the command, both will be used to ensure even power dissipation across all the switches.

Table 1 Switching state of the converter

State	T1	T2	T3	T1'	T2'	T3'	Vconv.
0	0	0	0	1	1	1	0
1	0	0	1	1	1	0	V_{AUX}
2	0	1	0	1	0	1	$(V_{BUS}-V_{AUX})$
3	0	1	1	1	0	0	V_{BUS}
-3	1	0	0	0	1	1	$-V_{BUS}$
-2	1	0	1	0	1	0	$-(V_{BUS}-V_{AUX})$
-1	1	1	0	0	0	1	$-V_{AUX}$
0	1	1	1	0	0	0	0

By choosing the value at which V_{AUX} (voltage of C_{AUX}) will be regulated, 5 or 7 levels can be obtained. If V_{AUX} is half of

V_{BUS} , then only 5 levels are obtained, since switching states 1 and 2 have the same values, as do states -1 and -2. If V_{AUX} is regulated at one third of V_{BUS}, then 7 even voltage levels are obtained. The inductance L is a smoothing inductance, and is used as a boosting inductance in rectifier mode. The output voltage on V_{BUS} should be higher than the input voltage V_S. This topology offers lower THD and lower switching frequency, which result in a higher power efficiency. Also, the voltage stress on the power switches is reduced. As can be concluded from Table 1, T1 and T1' must sustain V_{BUS}, T2 and T2' (V_{BUS}-V_{AUX}) and T3 and T3' must sustain V_{AUX}. This allows for reduction of the total cost of the power switches.

III. Proposed Regulation

The previous section discussed how the value has been chosen at which C_{AUX} should be regulated. This section will discuss how the value is obtained. During states 1 and -1, the C_{AUX} is charged with the current flowing from V_S. State 2 and -2, C_{BUS} is charged by V_S and C_{AUX} is discharged. In states 3 and -3, C_{BUS} is still charging and C_{AUX} stays constant. Figure 3 a) shows a regular 7-level PWM, and Figure 3 b) illustrates the output state. In the case of the different carriers that produce the multilevel PWM, adding a small drift to the offset will result in a modification in the duration of each state. Considering the carrier between state 1 and state 2, if it drifts up, than state 1 will last longer. If it drifts too far up, than state 2 will eventually be completely ignored. For the waveforms between 0 and 1, and between 2 and 3, a drift down is required so that state 1 will last longer and state 2 will last shorter. By doing so, the overall duration of state 1 would be longer, and in turn the capacity would be charged, and V_{AUX} increased. Similar logic is applied when lowering V_{AUX}. Figure 3 c) thru Figure 3 f) shows the effect of drifts of 20% and 40% on the output waveform. When observing the effect on the output state, it can be seen that for a positive drift state 2 occurs more often, and therefore C_{AUX} is discharged.

Using a simple PI regulator, V_{AUX} is set to one third of V_{BUS} by adding a drift to the 7-level PWM. The output voltage of the converter is then regulated using a standard controller. The output is compared to a reference output. This generates a current reference, which is multiplied with a sinusoidal waveform synchronized with V_S. A feed-forward controller is then applied to the current to obtain the modulating signal.

IV. Results

The controller and the converter are tested first with a very small time-step using MATLAB/Simulink with the SimPowerSystems library. This enables the theory to be proven without having to overcome problems encountered when working with a real converter. Furthermore, the results obtained at this step will be used to validate the results obtained with the real-time simulator, and to select the appropriate time-step value yielding to acceptable results. The real controller will be executed on an FPGA board. Before connecting it to the real converter, functionality must be tested; this is done using a real-time simulator, and allows for the connection of the prototype, or the real controller hardware, to a simulated converter. This is accomplished using the eMEGAsim real-time digital simulator from Opal-RT, which enables the plant model to be distributed across multiple CPUs during simulation..The eMEGAsim simulator is also equipped with an FPGA development board. At this point, the controller is implemented on the FPGA, while the converter is implemented on one CPU. Voltage and current from the simulated converter are sent to the FPGA using an analog to digital converter, and the power switches from the converter are driven by the controller using digital input. This approach ensures that the controller exhibits the same behaviour as if it were connected to a real converter. This technique is called HIL simulation or Hardware-in-the-Loop simulation, and allows testing of the real controller, and verification of the stability of the command over a long period of time. Different scenarios can then be tested to fully test the controller and its protection systems, including misfiring of a gate signal, variation of

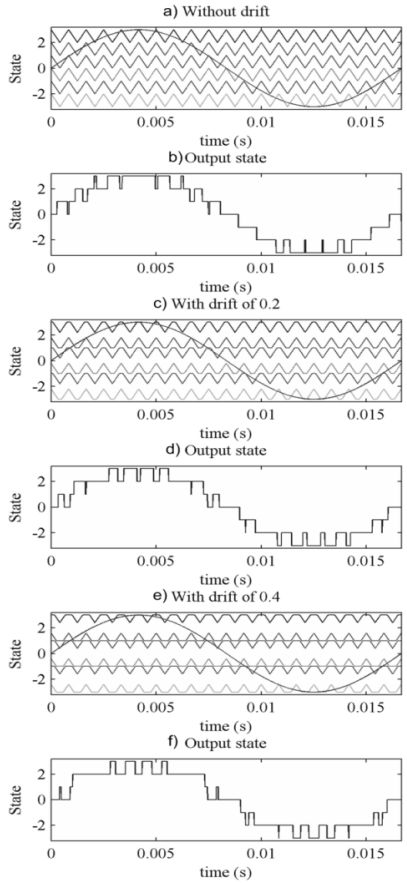

Figure 3 Variation of input converter voltage load for different drift.

input voltage, voltage unbalances or several fault conditions. The FPGA also has a very small computation time and a clock with a resolution of 10 ns to generate very precise firing pulses. In fact, most industrial MMCs are now implemented on FPGA chips because of their speed and flexibility. The simulator architecture is therefore very close to real controller architecture, enabling the development of practical control prototypes. Once the HIL testing and control optimization using the virtual plant are terminated, the FPGA board is connected to the real 1.5kW converter to conduct the final validation. The results obtained in offline simulation and in HIL real-time simulation can then be verified with a real setup for a few critical cases. Additional tests with the virtual plant in HIL mode can then be performed for more complex operating conditions and systems with several high-power converters that would be too complex or expensive to test with an analog setup. Table 2 illustrates the value for each component used in simulation and in the prototype.

Table 2 Components of the converters

Component	Value
C_{BUS}	4.5 mF
C_{AUX}	680 µF
L	3 mH
R	20-27
V_S	0-120 V

During the experimentation, V_S is set to 90 V_{RMS}. The desired output voltage is 120 V_{DC}, changing to 130 V_{DC} between the 1st and 3rd seconds, and then returning to 120 V_{DC}. R is 27 Ω for 2 seconds and 20 Ω after. Figure 4 a) shows input voltage V_S and the current I_S. V_{BUS} and V_{AUX} are shown in Figure 4 b). Figure 5 illustrates the response of the system when the voltage output drops from 130V to 120V. Similar results, obtained from the real-time simulation and the real converter, are outlined in Figure 6 to Figure 9. Table 3 synthesizes the results for the THD of the current for the different methods tested

Table 3 Synthesis of the results

	THD during experimentation time (s)			
	0-1	1-2	2-3	3-4
Offline simulation	8.12%	6.86%	5.16%	6.31%
HIL simulation	7.02%	6.90%	6.28%	6.35%
Real hardware	7.53%	7.30%	6.51%	6.63%

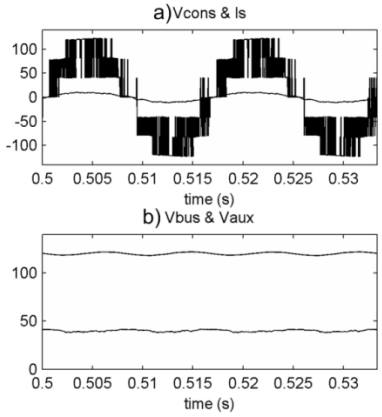

Figure 4 Offline simulation results showing converter generated voltages and current.

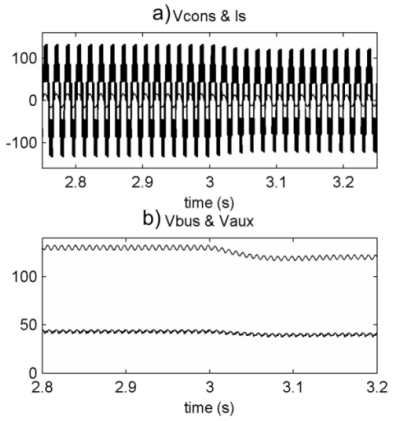

Figure 5 Offline simulation results showing converter generated voltages and current for variation of output voltage reference.

V. CONCLUSION

The presented method of control has been proven efficient both in simulation and in practice for steady-state operating conditions. Low THD is achieved without any filtering and all harmonics are around the modulating frequency, which is about 10 times the frequency of the desired output. Using HIL simulation enables implementation with the real converter and has been used to demonstrate the stability of the controller over a long period of time. When compared together, the results are very similar. For the offline simulation, the difference in the time-step explains a lower THD. Since it has a time-step of 20µs, some of the harmonics were not considered in the THD computation. For the real converter, the differences are mainly due to switching, since the power switches in this case are not ideal. The real-time simulation enables verification of the stability of the proposed regulation. Also, using the HIL method contributes to the resolution of

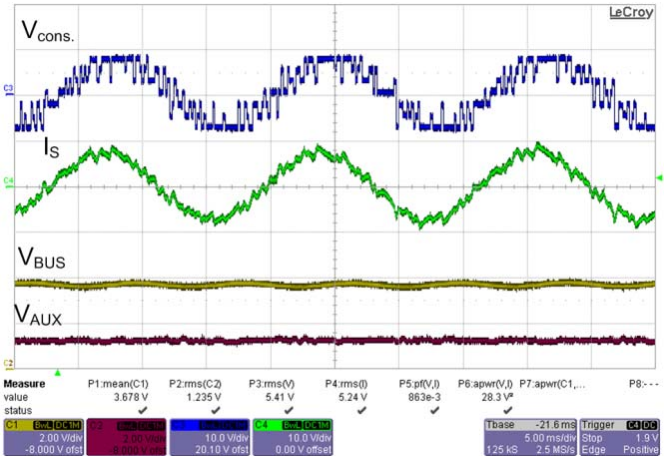

Figure 6 HIL simulation results, V_{CONV}130 V/div, I_S 10 A/div, V_{BUS} 65 V/div, V_{AUX} 65 V/div.

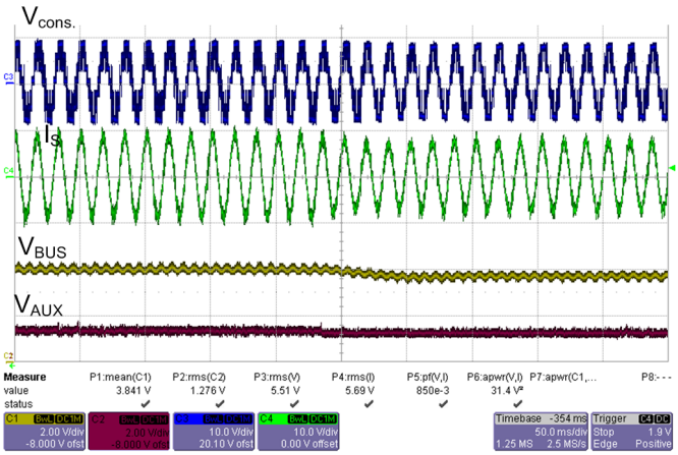

Figure 7 HIL simulation results for variation of output voltage reference, V_{CONV}130 V/div, I_S 10 A/div, V_{BUS} 65 V/div, V_{AUX} 65 V/div.

some of the problems encountered during the design of the controller. HIL simulation reduces the source of error, ensuring that the converter will behave the way it should, which is not always the case with a real design on the first attempt. Future work will focus on the analysis of the controller and stresses on components under large disturbances and fault conditions.

VI. ACKNOWLEDGEMENT

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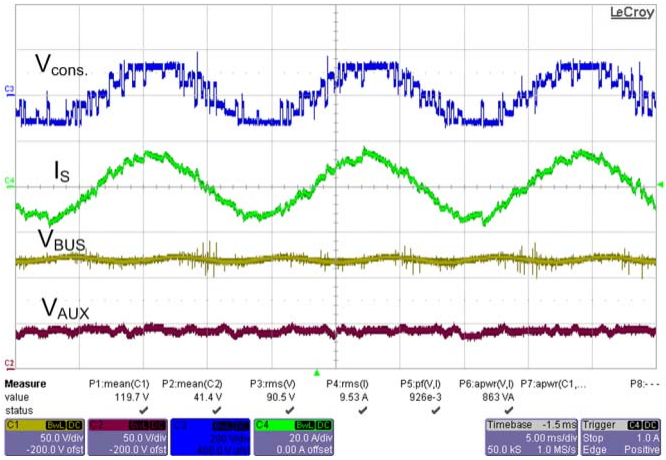

Figure 8 Experimental results, V_{CONV} 200 V/div, I_S 20 A/div, V_{BUS} 50 V/div, V_{AUX} 50 V/div.

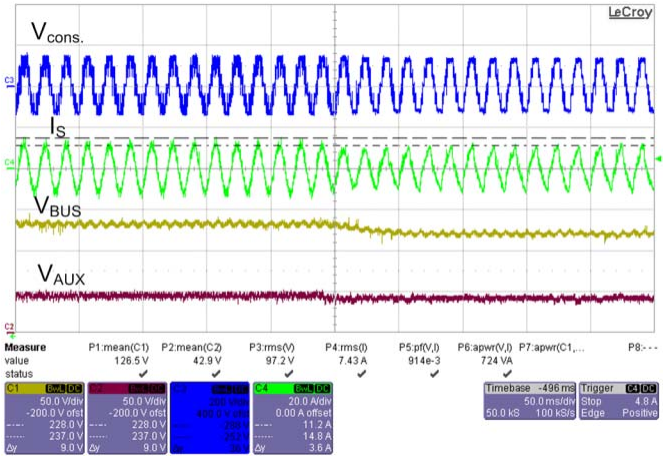

Figure 9 Experimental results for variation of output voltage reference, V_{CONV} 200 V/div, I_S 20 A/div, V_{BUS} 50 V/div, V_{AUX} 50 V/div.

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VIII. BIOGRAPHIES

Kamal Al-Haddad (S'82-M'88-SM'92-F'07) was born in Beirut, Lebanon, in 1954. He received B.Sc.A. and M.Sc.A. degrees from the University of Québec à Trois-Rivières, Trois-Rivières, QC, Canada, in 1982 and 1984, respectively, and A Ph.D. degree from the Institut National Polythechnique, Toulouse, France, in 1988. From June 1987 to June 1990, he was a Professor with the Engineering Department, Université du Québec à Trois-Rivières. Since June 1990, he has been a Professor with the Electrical Engineering Department, École de Technologie Supérieure (ETS), Montreal, QC, where he has been the holder of the Canada Research Chair in Electric Energy Conversion and Power Electronics since 2002. He has supervised more than 60 Ph.D. and M.Sc.A. students working in the field of power electronics. He was the Director of graduate study programs at the ETS from 1992 to 2003. He is a Consultant and has established very solid link with many Canadian industries working in the field of power electronics, electric transportation, aeronautics, and telecommunications. He is the Chief of ETS-Bombardier Transportation North America division, a joint industrial research laboratory on electric traction system and power electronics. He is the Co-author of the Power System Blockset software of Matlab. He has co-authored more than 250 transactions and conference papers. His fields of interest are in high efficient static power converters, harmonics and reactive power control using hybrid filters, switch mode and resonant converters including the modeling, control, and development of prototypes for various industrial applications in electric traction, power supply for drives and telecommunications. Prof. Al-Haddad is a fellow member of the Canadian Academy of Engineering, a life member of the Circle of Excellence of the University of Quebec and received the outstanding researcher award from ETS in 2000. He is active in the IEEE Industrial Electronics society where he is Vice President for Publication, an AdCom member and serves as an Associate Editor of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS.

Luc-André Grégoire was born in Joliette, Canada, on December 8 1981. He received a B.Ing degree (2008) from École de Technologie Supérieure (ETS), Montréal, Qc, Canada. He has also received a M.Ing degree (2010) under the supervision of professor Al-Haddad at Groupe de Recherche en Électronique de Puissance et Commande Industrielle (GREPCI-ETS). In 2009, Mr. Grégoire joined Opal-RT Technologies as a Simulation Specialist. His main fields of interest are renewable energy, power converters and energy efficiency.

Girish Nanjundaiah was born in Shimoga, Karnataka, India in 1971. He graduated from the Karnataka University, Dharwad in year 1993. He has been involved with Mathematical Modeling, Simulation and Real Time Operating Systems since 1993. He started Opal-RT operations in India in 2004 and has been handling the Indian market since then, with particular emphasis on vertical markets including Automotive, Aerospace, Transportation and Electrical Engineering in Academic Circles.