A New Multilevel Inverter Using Switched Capacitor Unit with Reduced Components

P. Venugopal and V. Sumathi

Abstract In the present paper, single phase multilevel inverter using switched capacitor units is proposed. The switched capacitor unit (SCU) is used in the multilevel inverter will increase the dc supply voltage at the input without using transformer by operating the capacitors in parallel and in series. The SCU comprises one dc source, two semiconductor switches, power diode, and capacitor. The proposed topology does not require the charge balancing operations, which results reducing the cost of the overall circuit. In addition to that, it does not required H-bride module to alter the polarity of the output voltage, which will lead to minimum required semiconductor power switches. The proposed topology is compared with the conventional similar architectures in terms of power semiconductor switches, power diodes, dc power supplies. Finally, to confirm the proposed architecture performance, simulation results are presented.

Keywords Multilevel inverter · dc voltage sources · Power switches
Output voltage levels · Charging and discharging

1 Introduction

Nonconventional energy sources such as wind turbine and photovoltaic systems have been accepted as a valuable replacement for fossil fuels for the reason that their consistent response and commercial profits in recent years. So as to manage boundless utilizing these renewable energy sources, the overall system output performance need to be improved through increasing the quality of power output, reducing the total losses, eliminating the filter at output, and reducing the size of the

P. Venugopal (✉)
School of Electronics Engineering, VIT University, Vellore, Tamil Nadu, India
e-mail: venugopal.p@vit.ac.in

V. Sumathi
School of Electrical Engineering, VIT University, Chennai, Tamil Nadu, India
e-mail: vsumathi@vit.ac.in

S. S. Dash et al. (eds.), *Artificial Intelligence and Evolutionary Computations in Engineering Systems*, Advances in Intelligent Systems and Computing 668,
https://doi.org/10.1007/978-981-10-7868-2_63

transformer [1]. To achieve this, multilevel inverters have gain more attention because of their high quality of output power, reduced harmonic distortion, higher magnitude of the fundamental component, high efficiency, lower switching losses, and less dv/dt. These advantages mentioned above are the motivation for the changeover from the conventional two-level converter to multilevel converters [2, 3]. In actuality, the multilevel inverter (MLI) intends to produce the stepwise voltage waveform at the output by integrating dc source values connected with its terminals. The output voltage levels increases by increasing the number of dc links at the input [4]. Considering the different topologies of MLI, the dc power supplies can be isolated or interconnected. Three primary structures of the multilevel inverters have been exhibited: diode clamped, flying capacitor, and cascaded multilevel inverter [5]. In spite of the majority of the specified benefits, MLIs have a few disadvantages over the classical two-level inverter topology. In multilevel inverter architectures, increasing the output voltage levels results increasing the circuit complexity, which decreases reliability and efficiency [6, 7]. The fundamental condition for producing high number of voltage levels is to utilize various dc voltage sources,for example, transformers or capacitors with combination of several switching components [8].

In the literature, Researchers have attempted to overcome these previously mentioned limitations by introducing the recently proposed MLI structures [9]. In spite of that, producing more number of voltage levels at the output, with least number of separated dc sources and other components, for example, gate driver circuit and power semiconductor switches in like manner, is considered a key features for investigators [10, 11]. A best approach to lessening the number of essential dc voltage sources is to utilize the capacitors. However, the previous mentioned approach requires a separate voltage balancing circuit for preclude the problem of discharging [12, 13]. Discharging problems can be reduced by switching states repetitions. In this approach, large number of semiconductor switches is required to achieve more number of voltage levels [14, 15]

To reduce the count of essential switches and gate drivers, Dargahi [16] presented a novel technique in FCMCs to balance the charge. These FCMCs can generate output voltage of 19-level, power semiconductor switches of 18, 5 capacitors, and two dc power supplies. However, this architecture requires no less than two number of voltage sensors to follow the voltage performance of every capacitor under working conditions. Moreover, this design generates a abnormal voltage ripples with increased levels of voltage at the output and is not possible to increase the output levels further as desired. To resolve the problem of discharging the alternative methodology is to use the modulation methods accompanied by lessening of duty cycle rate for every capacitor. Nevertheless such designs are only apt for a definite amount of voltage levels and the ability of extending the topology is not possible [17, 18].

The other alternative approach is, using the switched capacitor in multilevel inverter, in which charge balancing processes for eliminating the additional dc sources are not required, consequently overall cost will reducing [19–21]. This approach, not only transfers the large power from input to output, but also produces

more number of output voltage levels. Because of this advantage, a few enhanced architectures were introduced by various authors [22–26]. Notwithstanding, H-bridges are used to change the polarity of the voltage waveform in these topologies and the cascaded procedure keeping in mind the end goal to generalized the topologies and achieve the more number of the levels at the output voltage which results high conduction losses in power switches [27, 28].

Taking into account the study situation previously mentioned, a novel MLI using switched capacitor converter is presented. This topology generates increased number of output voltage levels compared to the topologies mentioned in the literature. Moreover, this architecture can be extended to further levels by adding the basic units. H-bridges are not used in this topology, which results reduce the cost, complexity of the circuit. A far reaching, comparison has been done with the recently proposed structures, which can demonstrate the upsides of proposed MLI using switched capacitor structure in various perspective, such as the switch count, number of dc sources, and voltage levels at output. To examine the proposed structure, simulation has been done using MATLAB/SIMULINK and the results are verified to confirm performance of the proposed structure.

2 Proposed MLI Using SCU

In order to generate more number of levels compared to [15–17], a novel structure has been introduced, which utilizes the switched capacitor unit. The basic structure of switched capacitor converter is shown in Fig. 1a. The switched capacitor converter contains a capacitor, power diode, dc power supply, and two power semiconductor switches. The capacitor will be charged to the voltage Vdc when turned ON the switch Sb. The capacitor will be discharged when turn ON the switch Sa. Figure 1b shows the operations of charging and Fig. 1c shows the operation of discharging of capacitor.

The basic architecture of proposed multilevel Inverter is shown in Fig. 2, which contains two Switched capacitor units, six power semiconductor switches. The number of switches and power diodes required in the proposed topology can be stated as following equations;

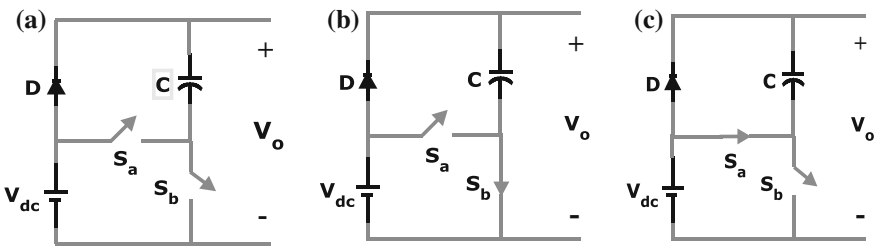

Fig. 1 **a** Basic switched capacitor unit **b** capacitor charging circuit **c** capacitor discharging circuit

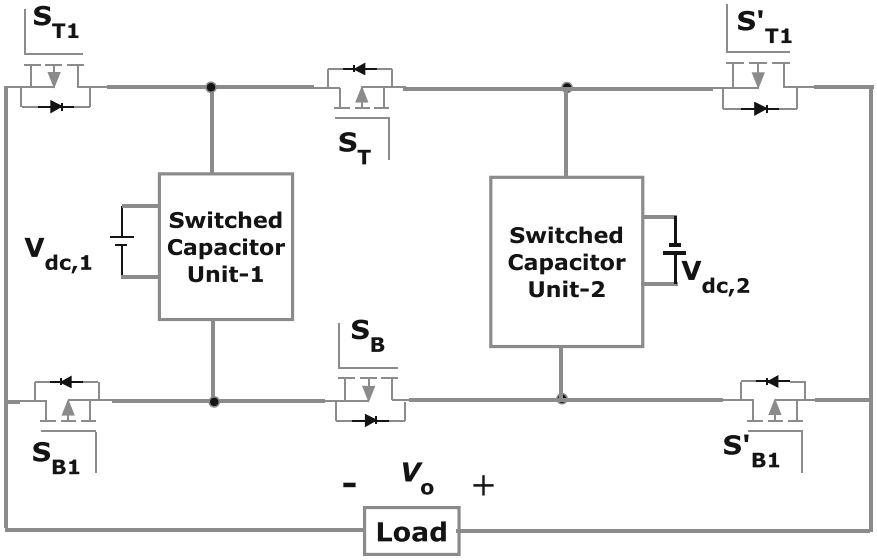

Fig. 2 The basic proposed switched capacitor multilevel inverter

$$N_{\text{Switch}} = 8k + 2 \tag{1}$$

$$N_{\text{diode}} = 2k \tag{2}$$

In the basic proposed topology, 2 switched capacitor converters are used, therefore 2 dc sources and $2k$ (k is the half of the isolated dc sources) capacitors required. To generate maximum number of output levels 2 dc sources ae in asymmetric in nature. The mathematical expression for the dc source of second switched capacitor unit is given by,

$$V_{\text{dc},2} = (1 + 2^k) V_{\text{dc},1} \tag{3}$$

The asymmetrical proposed topology will produce maximum voltage levels at output can be expressed as following,

$$N_{\text{level}} = 1 + 2^{k+2} + 2^{2k+1} \tag{4}$$

The seventeen levels proposed inverter is shown in Fig. 3, which has 10 power switches, 2 capacitors, 2 diodes, and 2 isolated power supplies. The value of DC sources of first SC unit and second SC unit are Vdc and 3 Vdc. The switching pattern of the s17 level topology is given in Table 1. For example, if the value of Vdc is 10 V, and then the maximum voltage obtained at load is 80 V. Each step size is 10 V. To get 80 V at the output side S_{B1}, S_1, S_T, S'_1, S'_{B1} should be turned

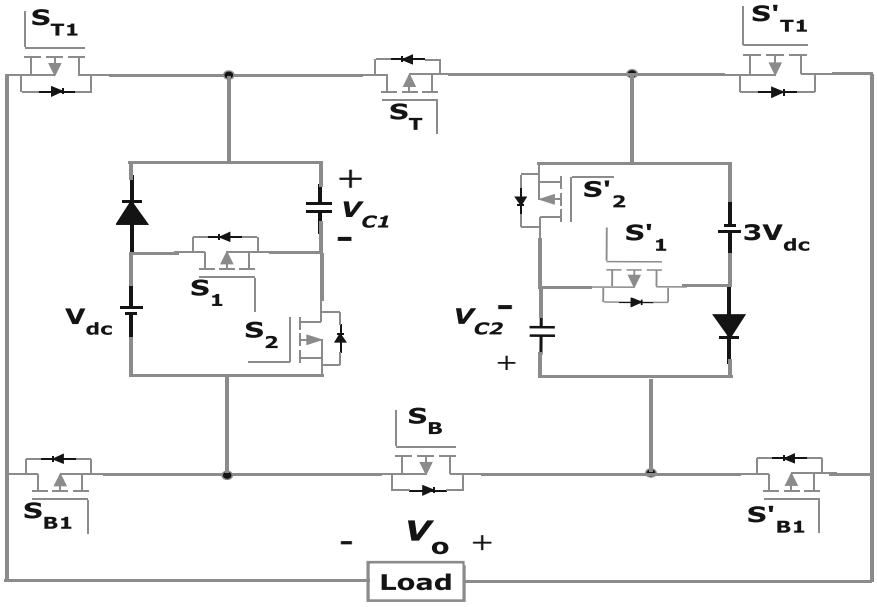

Fig. 3 Proposed 17-level multilevel inverter

ON. During this period both the capacitors are in discharging mode. When switches S_{B1}, S_2, S_T, S'_1, S'_{B1} are turn ON simultaneously, the voltage at output will be 70 V with capacitor C1 charging and C2 discharging.

The proposed topology can be extended to further levels by adding SCUs and switches. For instant, by adding the one SC unit and two switches to the basic topology, will produce 49 level output. Hence, 49 level inverter require 14 switches, 3 DC sources, 3 capacitors, and 3 diodes. 49-level inverter is shown in Fig. 4. For example, the switches S_{B1}, S_{T2}, S_T, S'_{T1} alongside the internal power switches of SCU-2 and SCU-3 and internal power switch of SCU-1 must be turn ON. So as to generate 9th level of output, switches of S_{B1}, S_{B2}, S_T, S'_{T1} along with internal power switches of SCU-3 and SCU-2 and turn ON the SCU-1 switches which are in parallel. The switching sequence is given in Table 2. To create higher number of voltage levels at the output side with regard to further levels, the value of additional dc power sources of individually SC unit can be implemented by the given expressions:

$$V_{\mathrm{dc},j} = 2(V_{\mathrm{dc},j-1} + V_{\mathrm{dc},r(j-1)}) + 1. \tag{5}$$

$$V_{\mathrm{dc},rj} = 2(V_{\mathrm{dc},j} + V_{\mathrm{dc},r(j-1)}) + 1. \tag{6}$$

Table 1 Switching sequence and capacitor charging and discharging states of seventeen level multilevel inverter

Switching states	ON switches	Vo	C1	C2
1	S_{B1}, S_1, S_T, S'_1, S'_{B1}	4Vdc + vc1 + vc2	D	D
2	S_{B1}, S_2, S_T, S'_1, S'_{B1}	4Vdc + vc2	C	D
3	S_{T1}, S_2, S_T, S'_1, S'_{B1}	3Vdc + vc2	C	D
4	S_{B1}, S_1, S_T, S'_2, S'_{B1}	4Vdc + vc2	D	C
5	S_{B1}, S_2, S_T, S'_2, S'_{B1}	4Vdc	C	C
6	S_{T1}, S_2, S_T, S'_2, S'_{B1}	3Vdc	C	C
7	S_{B1}, S_1, S_T, S'_2, S'_{T1}	Vdc + vc1	D	C
8	S_{B1}, S_2, S_T, S'_2, S'_{T1}	Vdc	C	C
9	S_{B1}, S_2, S_B, S'_2, S'_{B1}	0	C	C
10	S_{T1}, S_2, S_B, S'_2, S'_{B1}	−Vdc	C	C
11	S_{T1}, S_1, S_B, S'_2, S'_{B1}	−Vdc−vc1	D	C
12	S_{B1}, S_2, S_B, S'_2, S'_{B1}	−3Vdc	C	C
13	S_{T1}, S_2, S_B, S'_2, S'_{B1}	−4Vdc	C	C
14	S_{T1}, S_1, S_B, S'_2, S'_{B1}	−4Vdc−vc2	D	C
15	S_{B1}, S_2, S_B, S'_1, S'_{B1}	−3Vdc−vc2	C	D
16	S_{T1}, S_2, S_B, S'_1, S'_{B1}	−4Vdc−vc2	C	D
17	S_{T1}, S_1, S_B, S'_1, S'_{B1}	−4Vdc−vc1−vc2	D	D

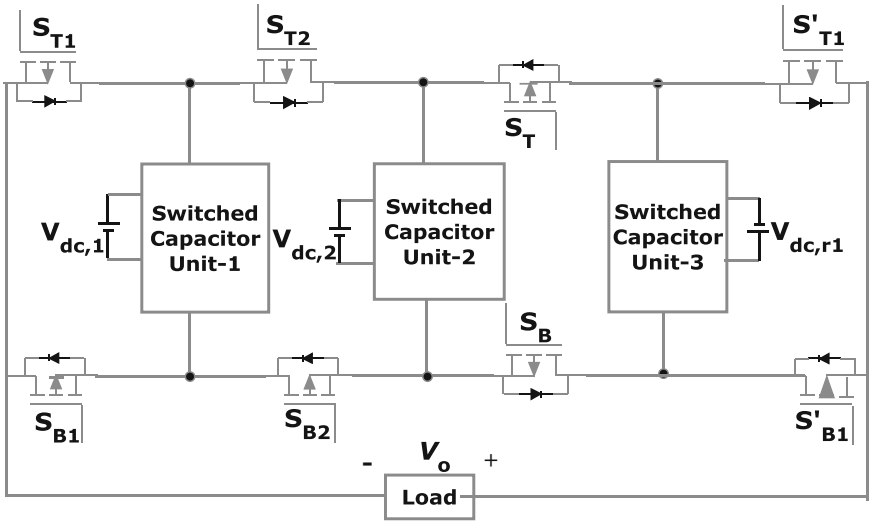

Fig. 4 49-level multilevel inverter

Table 2 Different states of switching of 49 level inverter

Switching states	ON switches	V_o
1	S_{B1}, S_{T2}, S_T, S'_{T1}	1, 2
2	$S_{T1,}$ S_{T2}, S_T, S'_{B1}	3, 6
3	S_{B1}, S_{T2}, S_T, S'_{B1}	4, 5, 7, 8
4	S_{B1}, S_{B2}, S_T, S'_{T1}	9, 18
5	S_{T1}, S_{B2}, S_T, S'_{B1}	10, 11, 13, 14, 19, 20, 22, 23
6	S_{B1}, S_{B2}, S_T, S'_{B1}	12, 15, 21, 24
7	S_{T1}, S_{B2}, S_T, S'_{T1}	16, 17

3 Comparative Study

The proposed multilevel inverter using switched capacitor structure is compared with some of flying capacitor multilevel inverter topologies which have been introduced recently. Comparison is done based on the voltage levels at output, number of power switches and dc sources and required number of capacitors. The proposed-structure is compared with the present topologies [15–17] from various observations is provided in Table 3. Clearly, as for the measures of extent of count of levels of the voltage at output over the number of required devices, the recommended structure requires minimum number of devices in contrast with their relevant architectures. For example, 18 and 20 semiconductor switching components to produce 17, 19, 7 levels of voltage at output, respectively, while proposed architecture requires just 10 control switches for its 17-level topology. In addition to that, recommended structure in [15–17] need 16, 18, and 20 power diodes to produce 17, 19, 7 levels of voltage at output, respectively, while recommended architecture needs just 12 control switches for its 17-level topology.

Table 3 Comparison of 17-level inverter with topologies [15–17]

Key parameters	[15]	[16]	[17]	Proposed SCMLI
Nlevel	17	19	7	17
NIGBT	16	18	20	10
Ndiode	16	18	20	12
Ncap	4	4	4	2
Nsource	1	2	2	2
Charge balance requirement	Yes	Yes	Yes	No

4 Simulation Results

To analyze the performance of recommended switching capacitor based multilevel inverter, the simulation and experimental results of 17-level inverter are presented. MATLAB/Simulink has been used for simulation. In addition to that, the hardware prototype of 17-level inverter with 80 V has been developed. The FPGA spartan-3e has been used to produce the gating pulses. For the present structure fundamental switching frequency method is used. The MOSFETs used are IRF-840, 500 V, 8A, and Ron is 0.85 Ω and Power diodes used are FR107, 700 V, and 50 Ω. Capacitors have been used with 4700 μF and 50 V. The prototype has been tested on R-L load with the magnitude of 0.5 mH and 500 Ω for all the studies. In this topology, the values of dc sources are unequal and are 10 and 30 V. According to this present topology produces the maximum voltage at the output will be 80 V. R-L load have been used for both simulation and experimental tests. The simulation results of

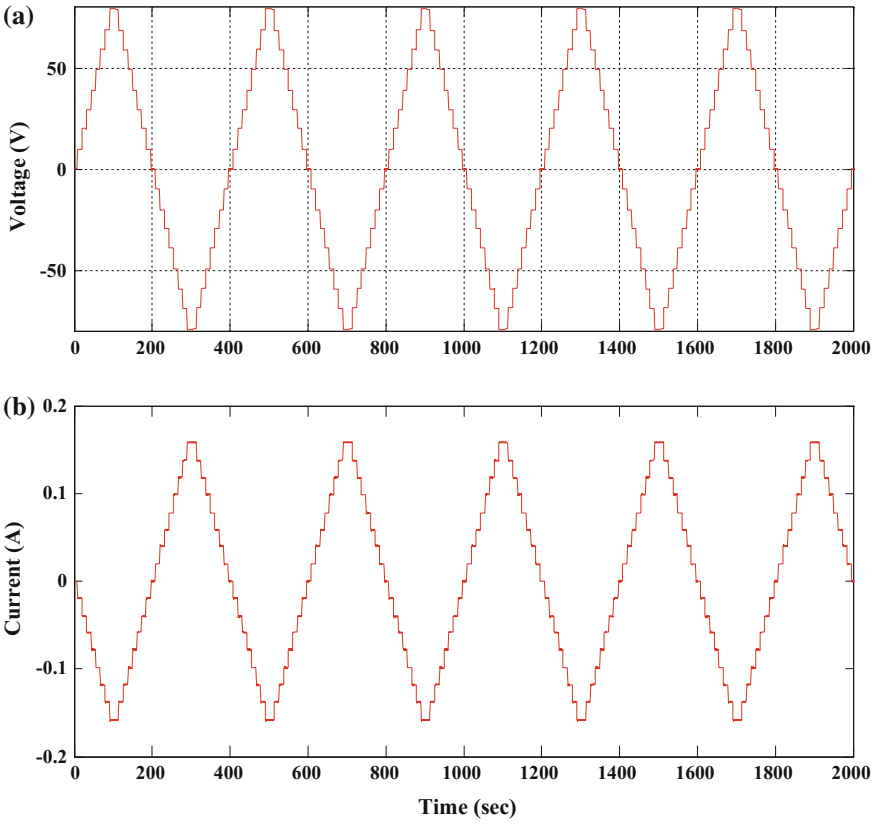

Fig. 5 Simulation waveforms of 17-level multilevel inverter **a** output voltage wave form **b** current waveform

proposed multilevel inverter which produces 17-level have shown in Fig. 5a, b. It is observed that the output voltage is 80 V and current is 950 mA.

5 Concluding Remarks

In this paper, a novel topology using switched capacitor converter has been proposed for multilevel inverters to produce seventeen voltage levels at the output. The basic topology can be extended to any number of levels at the output for example by adding one switched capacitor converter unit to the seventeen level multilevel inverter, the voltage levels at the output are 49. Similarly, to produce 137 levels at the output, two switched capacitor converter units should be added to the basic proposed multilevel inverter. The proposed topology has been compared with several existing topologies in the literature from the various points of observation. Based on these comparisons, the proposed structure requires less number of power switches, DC sources, and diodes. Consequently, the size and cost of the proposed structure will be reduced in comparison with the conventional similar topologies. At last, the viability and performance of recommended 17-level switched capacitor multilevel inverter have been confirmed through simulation results.

References

1. J. Chavarria, D. Biel, F. Guinjoan, C. Meza, J.J. Negroni, Energy balance control of PV cascaded multilevel grid-connected inverters under level-shifted and phase-shifted PWMs. IEEE Trans. Ind. Electron. **60**, 98–111 (2013)
2. A.L. Batschauer, S.A. Mussa, M.L. Heldwein, Three-phase hybrid multilevel inverter based on half-bridge modules. IEEE Trans. Ind. Electron. **59**, 668–678 (2012)
3. S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. Franquelo, B. Wu, J. Rodriguez, M. Perez, J. Leon, Recent advances and industrial applications of multilevel converters. IEEE Trans. Ind. Electron. **57**, 2553–2580 (2010)
4. E. Babaei, S. Alilu, S. Laali, A new general topology for cascaded multilevel inverters with reduced number of components based on developed H-bridge. IEEE Trans. Ind. Electron. **61**, 3932–3939 (2014)
5. M.R. Banaei, E. Salary, New multilevel inverter with reduction of switches and gate driver. Energy Convers. Manage. **52**, 1129–1136 (2011)
6. A. Ajami, M.R.J. Oskuee, A. Mokhberdoran, H. Shokri, Selective harmonic elimination method for wide range of modulation indexes in multilevel inverters using ICA. J. Central South Univ. **21**, 1329–1338 (2014)
7. R. Stala, A natural DC-link voltage balancing of diode-clamped inverters in parallel systems. IEEE Trans. Ind. Electron. **60**, 5008–5018 (2013)
8. K.K. Gupta, A. Ranjan, P. Bhatnagar, L.K. Sahu, S. Jain, Multilevel inverter topologies with reduced device count: a review. IEEE Trans. Power Electron. **31**, 135–151 (2015)
9. A. Mokhberdoran, A. Ajami, Symmetric and asymmetric design and implementation of new cascaded multilevel inverter topology. IEEE Trans. Power Electron. **29**, 6712–6724 (2014)
10. K.K. Gupta, S. Jain, Comprehensive review of a recently proposed multilevel inverter. IET Power Electron. **7**, 467–479 (2014)

11. K.M. Tsang, W.L. Chan, Single DC source three-phase multilevel inverter using reduced number of switches. IET Power Electron. **7**, 775–783 (2014)
12. M. Khazraei, H. Sepahvand, K.A. Corzine, M. Ferdowsi, Active capacitor voltage balancing in single-phase flying-capacitor multilevel power converters. IEEE Trans. Ind. Electron. **59**, 769–778 (2012)
13. K. Sano, H. Fujita, Voltage-balancing circuit based on a resonant switched-capacitor converter for multilevel inverters. IEEE Trans. Ind. Appl. **44**, 1768–1776 (2008)
14. B.P. McGrath, D.G. Holmes, Analytical modeling of voltage balance dynamics for a flying capacitor multilevel converter. IEEE Trans. Power Electron. **23**, 543–550 (2008)
15. P. Roshankumar, R.S. Kaarthic, K. Gupakumar, J.I. Leon, L.G. Franquelo, A seventeen-level inverter formed by cascading flying capacitor and floating capacitor H-bridge. IEEE Trans. Power Electron. **30**, 3471–3478 (2015)
16. V. Dargahi, A.K. Sadigh, M. Abarzadeh, S. Eskandari, K. Corzine, A new family of modular multilevel converter based on modified flying capacitor multicell converters. IEEE Trans. Power Electron. **30**, 138–147 (2015)
17. V. Dargahi, A.K. Sadigh, M. Abarzadeh, M.R.A. Pahlavani, A. Shoulaie, Flying capacitor reduction in an improved double flying capacitor multicell converter controlled by a modified modulation method. IEEE Trans. Power Electron. **27**, 3875–3887 (2012)
18. H. Sepahvand, J. Liao, M. Ferdowsi, K. Corzine, Capacitor voltage regulation in single dc source cascade H-bridge multilevel converters using phase shift modulation. IEEE Trans. Ind. Electron. **60**, 3619–3626 (2013)
19. A.M.Y.M. Ghias, J. Pou, V.A. Agilidis, Voltage balancing method for stacked multicell converters using phase disposition PWM. IEEETrans. Ind. Electron. **62**, 4001–4010 (2015)
20. B. Axelrod, Y. Berkovich, A. Ioinovici, A cascade boost switched capacitor-converter two-level inverter with an optimized multilevel output waveform. IEEE Trans. Circuits Syst. I. **52**, 2763–2770 (2005)
21. M.S.W. Chan, K.T. Chau, A newswitched-capacitor boostmultilevel inverter using partial charging. IEEE Trans. Circuits Syst. II. Exp. Briefs **54**, 1145–1149 (2007)
22. Y. Hinago, H. Koizumi, A switched-capacitor inverter using series/parallel conversion with inductive load. IEEE Trans. Ind. Electron. **59**, 878–887 (2012)
23. J. Liu, K.W.E Cheng, Y. Ye, A cascaded multilevel inverter based on switched-capacitor for high-frequency ac power distribution system. IEEE Trans. Power Electron. **22**, 4219–4230 (2014)
24. E. Babaei, F. Sedaghati, Series-parallel switched-capacitor based multilevel inverter. in *Proceedings of International Conference on Electrical Machines and Systems*, 2011, pp 1–5
25. Y. Ye, K. Cheng, J. Liu, K. Ding, A step-up switched-capacitor multilevel inverter with self voltage balancing. IEEE Trans. Ind. Electron. **61**, 6672–6680 (2014)
26. E. Babaei, S.S. Gowgani, Hybrid multilevel inverter using switchedcapacitor units. IEEE Trans. Ind. Electron. **61**, 4614–4621 (2014)
27. R.S. Alishah, D. Nazarpour, S.H. Hosseini, M. Sabahi, Reduction of power electronic elements in multilevel converters using a new cascade structure. IEEE Trans. Ind. Electron. **62**, 256–569 (2015)
28. E. Babaei, M.F. Kangarlu, M. Sabahi, Extended multilevel converters: an attempt to reduce the number of independent dc voltage sources in cascade multilevel converters. IET Power Electron. **7**, 157–166 (2014)