Arab J Sci Eng (2014) 39:1117–1127
DOI 10.1007/s13369-013-0696-9

RESEARCH ARTICLE - ELECTRICAL ENGINEERING

Improvement of Multilevel Inverters Topology Using Series and Parallel Connections of DC Voltage Sources

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Received: 15 March 2012 / Accepted: 9 July 2013 / Published online: 11 September 2013

Abstract This paper proposes a new topology for multilevel inverters based on series and parallel {R1–7} connection's of the dc voltage sources. Series and parallel {R1–7} connections ability of the proposed topology make it capable of increasing the number of voltage levels and the output current, respectively. The proposed topology is optimized from the viewpoint of number of switches, number of dc voltage sources, and maximum blocked voltage by switches. The optimal topologies with minimum number of switches and dc voltage sources are computed to produce the maximum number of output voltage levels with minimum blocked voltage by switches. In addition, a new algorithm for the determination of magnitudes of dc voltage sources is presented. Furthermore, to verify the theoretical aspects, the proposed topology is compared with some of the new presented multilevel inverters. The performance of the proposed multilevel inverter is verified by the simulation and experimental results of a single-phase 25-level inverter.

Keywords Multilevel inverter · Series and parallel connections of dc voltage sources · Standing voltage

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الخلاصة

تقترح هذه الورقة العلمية طوبولوجيا جديدة للمحولات متعددة المستويات على أساس اتصالات متسلسلة وموازية و{7-R1} من مصادر جهد دس. إن قدرة اتصالات {7-R1} المتسلسلة والموازية للطوبولوجيا المقترحة تجعلها قادرة على زيادة عدد مستويات الجهد والانتاج الحالي على التوالي. وتم تحسين الطوبولوجيا المقترحة من وجهة نظر عدد المحولات، وعدد مصادر جهد دس والحد الأقصى للجهد المسدود من المحولات. وتم أيضاً حساب الطبولوجيات (البنيات) الأمثل مع الحد الأدنى لعدد مفاتيح ومصادر جهد دس من أجل إنتاج أكبر عدد ممكن من مستويات انتاج التيار الكهربائي مع الحد الأدنى من الجهد المسدود من المحولات. وتم -إلى جانب ذلك - تقديم خوارزمية جديدة لتحديد مقادير مصادر جهد دس. وعلاوة على ذلك، ومن أجل التحقق من الجوانب النظرية تمت مقارنة الطوبولوجيا المقترحة مع بعض المحولات متعددة المستويات الجديدة المقدمة. وتم التحقق من أداء المحول متعدد المستويات المقترح من قبل نتائج المحاكاة والنتائج التجريبية لمحول مرحلة واحدة على مستوى 25.

Abbreviations

V_{dc}	Isolated dc voltage source
m	Number of dc voltage sources connected in parallel
n	Number of dc voltage sources for the extended unit
n_j	Number of dc voltage sources for the jth unit
$N_{step,j}$	Number of voltage levels for the jth unit
V_j	Magnitude of dc voltage source used in jth unit
v_o	Output voltage
$v_{o,j}$	Output voltage of the jth unit
$V_{o,max}$	Maximum output voltage
I_j	Nominal current of the dc voltage source used in jth unit
$I_{o,j}$	Nominal output current of jth unit
k	Number of units
N_{IGBT}	Number of IGBTs
N_{step}	Number of voltage levels
N_{dc}	Number of dc voltage sources

V_{switch}	Standing voltage
$V_{\text{switch},j}$	Standing voltage of jth unit
c	Constant value
C_k^m	Number of $m$combinations from k numbers
R	Load resistance
L	Load inductance

1 Introduction

The concept of multilevel inverters was introduced in 1975 [1], and the term "multilevel" began with the three-level inverter [2]. Multilevel inverters are such converters that generate the desired output voltage by synthesizing from several levels of dc voltage sources as inputs. By increasing the number of dc voltage sources on the input side, the output voltage of inverter becomes more similar to a sinusoidal waveform. Multilevel inverters have lower switching losses, higher efficiency, and more electromagnetic compatibility in comparison with the conventional two-level inverters [3–5].

Three main topologies of multilevel inverters have been presented. These are diode clamped multilevel inverter [2], flying capacitor multilevel inverter [6], and cascaded H-bridge multilevel inverter [7].

This paper focuses on cascaded multilevel inverters. The cascaded multilevel inverters have received more attention due to their easier control and modular structure. These types of inverters are created by connecting several single-phase H-bridge inverters in series. A major disadvantage of these inverters is requirement of high number of isolated dc voltage sources and switches. To reduce the number of dc voltage sources, some new configurations have been presented [8,9]. Asymmetrical cascade multilevel inverters, which resulted from supplying the cascaded H-bridge cells with different values of dc voltages, provide a higher number of levels [10,11]. Although low-voltage switches can be utilized in a multilevel inverter, each switch requires a gate driver and protection circuit. This causes the overall system to be more expensive and complex. Recently, some attempts have been done in this area, and some new optimal topologies with the reduced number of switches have been presented [12–16]. In some of them, the cascaded multilevel inverter needs bidirectional power switches with the capability of blocking voltage in both directions. It should be noted that in all mentioned topologies, the multilevel inverters use only series connection of dc voltage sources. The presented multilevel inverter in [17] uses series and parallel connections.

In this paper, a new topology of cascaded multilevel inverter based on the basic unit presented in [17] is proposed. There is no need of bidirectional power switches in the proposed topology. In addition, the proposed topology provides the ability of series and parallel connections of dc voltage sources. The proposed topology needs less number of power switches in comparison with the structures presented in [12,13,17].

A new algorithm for calculating the magnitude of required dc voltage sources is proposed to generate all levels (odd and even) at the output. In order to produce the maximum number of output voltage levels with the minimum blocked voltage by power switches, the optimal number of switches and dc voltage sources is computed. In addition, the comparison results between the proposed multilevel inverter and the presented multilevel inverters in [12–17] are given. Finally, the simulation and experimental results are presented to verify the abilities of the proposed multilevel inverter.

2 Basic Topology

The basic structure of multilevel inverter recommended in [17] is shown in Fig. 1a. This basic unit consists of two dc voltage sources with three power switches (S_{a1}, S_{b1}, and S_{c1}). Each switch is composed of an isolated gate bipolar transistor (IGBT) with anti-parallel diode. When the switch S_{a1} is turned on, V_1 and V_2 are connected in series and $V_1 + V_2$ is produced at the output. In a similar manner, when the switches S_{b1} and S_{c1} are turned on $v_o = V_1 = V_2$ can be generated at the output. It is clear that the switch S_{a1} operates in a complementary mode with the switches S_{b1} and S_{c1}. It means that when S_{a1} is on, S_{b1} and S_{c1} must be off, and when S_{b1} and S_{c1} are on, S_{a1} must be off. Otherwise, a short circuit will occur across the dc voltage sources. Because of parallel connection between dc voltage sources, the magnitude of the dc voltage sources should be identical ($V_1 = V_2 = V_{\text{dc}}$). The typical output waveform of v_o is shown in Fig. 1b.

Figure 2 shows the extended unit of the basic unit shown in Fig. 1a. Due to parallel connection of dc voltage sources in the extended unit, the magnitude of these sources must be chosen as follows:

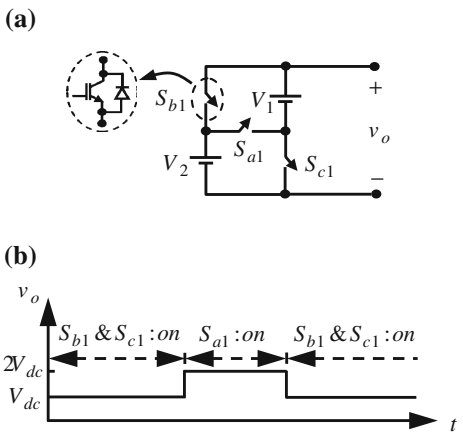

Fig. 1 **a** Basic unit of multilevel inverter recommended in [17], **b** typical output waveform of basic unit

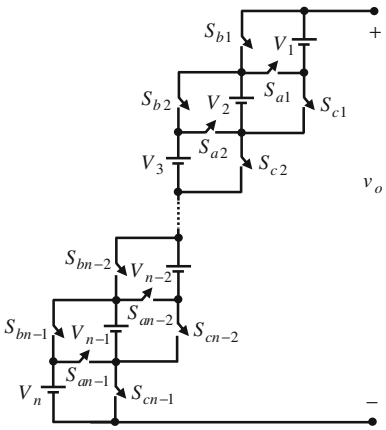

Fig. 2 Extended unit presented in [17]

$$V_i = V_1 = V_{\text{dc}} \quad i = 1, 2, \ldots, n \tag{1}$$

It should be noted that the structure demonstrated in Fig. 2 can produce only positive voltage levels at the output. In Fig. 2, the output voltage is given by

$$v_{\text{o}} = (n + 1 - m)\ V_1 \quad m \neq 0 \tag{2}$$

The possible number of voltage levels in Fig. 2 can be calculated by

$$N_{\text{step}} = n \tag{3}$$

If the nominal current of each dc voltage source is considered I_1, the output current in Fig. 2 will be maximum when all of the dc voltage sources are connected in parallel ($m = n$) and will be minimum when at least one of them are connected in series with the others ($m \neq n$):

$$I_{\text{o,max}} = nI_1 \tag{4}$$

$$I_{\text{o,min}} = I_1 \tag{5}$$

The maximum output voltage and number of used IGBTs for this structure can be calculated by (6) and (7), respectively.

$$V_{\text{o,max}} = \sum_{j=1}^{n} V_j = V_1 + V_2 + \cdots + V_n = nV_{\text{dc}} \tag{6}$$

$$N_{\text{IGBT}} = 3(n - 1) \tag{7}$$

3 Proposed Topology

As mentioned, the structure shown in Fig. 2 is capable of producing only positive voltage levels at the output. To produce positive and negative voltage levels, an H-bridge can be used at the output of the extended unit. In order to obtain more levels of voltage, k extended units have been used in series by H-bridges, as shown in Fig. 3. In the topology illustrated in Fig. 3, the first unit, second unit, …, and

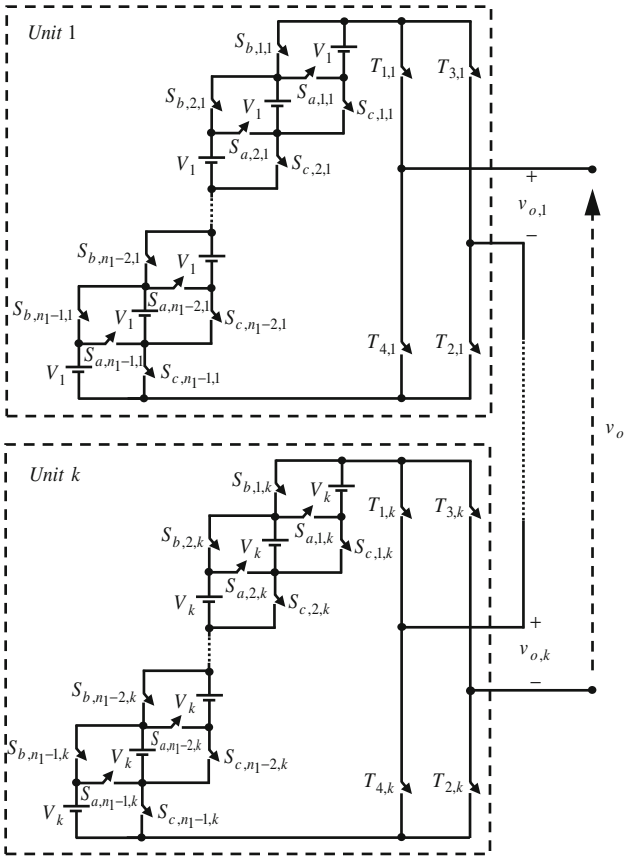

Fig. 3 Proposed topology

the kth unit have $n_1, n_2, \ldots, n_k$ dc voltage sources with magnitude of $V_1, V_2, \ldots, V_k$ and nominal currents of $I_1, I_2, \ldots, I_k$, respectively.

The topology shown in Fig. 3 requires multiple dc sources. In some systems, the dc voltage sources may be available through renewable energy sources such as photovoltaic panels or fuel cells, or with energy storage devices such as capacitors or batteries. When ac voltage is already available, multiple dc sources can be generated using isolated transformers and rectifiers [12].

The number of output voltage levels of each unit can be calculated as follows:

$$N_{\text{step},j} = (2n_j + 1) \quad j = 1, 2, \ldots, k \tag{8}$$

The nominal output current of each unit in Fig. 3 can be obtained as follows:

$$I_{\text{o},j} = bI_j \tag{9}$$

where b is the first integer number less than the non-integer number a. a is defined as follows:

$$a = \left| \frac{V_j n_j}{v_{\text{o},j}} \right| \tag{10}$$

It should be noted that if a is obtained an integer number, b will be assumed equal to integer a.

Due to series connection of the units in Fig. 3, the nominal output current of the proposed topology will be equal to the nominal output current of the unit with the minor current.

In Fig. 3, the maximum number of values for v_o is calculated by following equation:

$$N_{\text{step}} = \prod_{j=1}^{k} (2n_j + 1) \tag{11}$$

The maximum output voltage of the proposed topology can be evaluated by

$$V_{o,\max} = \sum_{j=1}^{k} (n_j \times V_j) \tag{12}$$

The number of IGBTs of proposed topology is calculated by

$$N_{\text{IGBT}} = \sum_{j=1}^{k} (3n_j + 1) \tag{13}$$

In order to have unequal values for v_o in Fig. 3 and produce linear levels, the values of the dc voltage sources in each unit must be chosen according to the following algorithm:

Unit 1:

$$V_1 = V_{\text{dc}} \tag{14}$$

Unit 2:

$$V_2 = (2n_1 + 1)V_{\text{dc}} \tag{15}$$

Unit 3:

$$\begin{aligned} V_3 &= 2(n_1 V_1 + n_2 V_2) + V_{\text{dc}} \\ &= [4n_1 n_2 + 2(n_1 + n_2) + 1]\, V_{\text{dc}} \end{aligned} \tag{16}$$

Unit k:

$$V_k = \left(2 \times \sum_{j=1}^{k-1} n_j V_j\right) + V_{\text{dc}} \tag{17}$$

4 Optimal Structures

In this section, in order to produce the maximum number of output voltage levels with minimum blocked voltage by switches, the optimal number of switches and dc voltage sources is calculated. It should be noted that in all extracted equations, the values of dc voltage sources have been chosen according to the proposed algorithm expressed by (14) to (17).

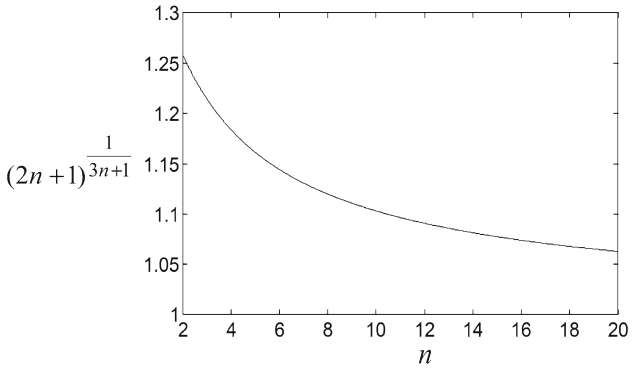

Fig. 4 Variation of $(2n+1)^{\frac{1}{3n+1}}$ versus n

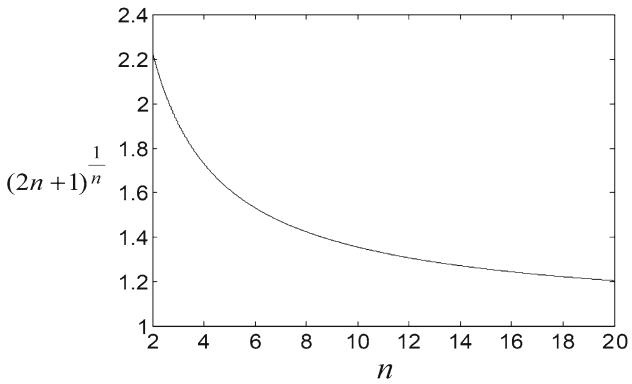

Fig. 5 Variation of $(2n+1)^{\frac{1}{n}}$ versus n

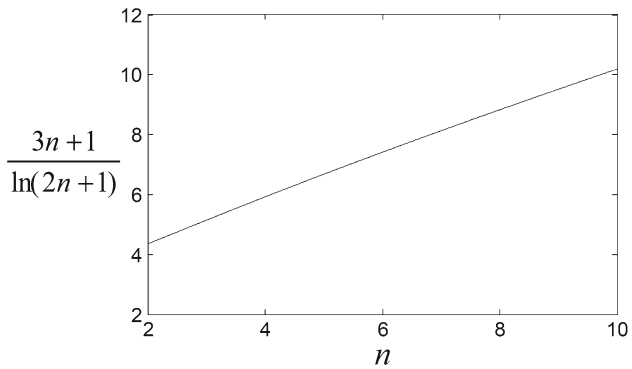

Fig. 6 Variation of $\frac{3n+1}{\ln(2n+1)}$ versus n

4.1 Optimal Structure for Maximum Number of Voltage Levels with Constant Number of Switches

The purpose of this subsection is to maximize the number of voltage levels at the output for a constant number of switches. The number of switches for proposed topology shown in Fig. 3 is given by

$$\begin{aligned} N_{\text{IGBT}} &= \sum_{j=1}^{k} (3n_j + 1) \\ &= 3(n_1 + n_2 + \cdots + n_k) + k = c \end{aligned} \tag{18}$$

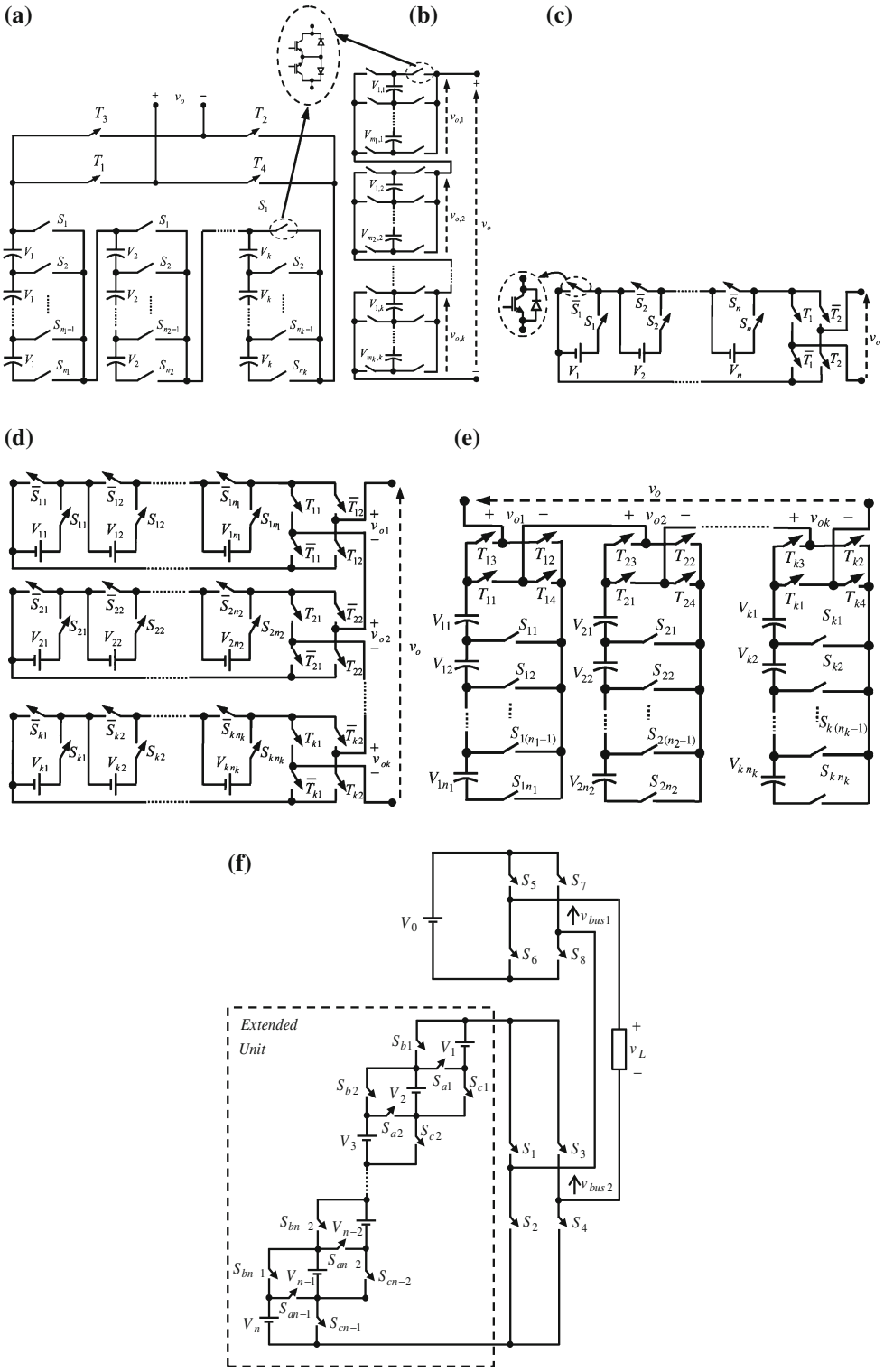

Fig. 7 Presented topologies in **a** [12], **b** [13], **c** [14], **d** [15], **e** [16], **f** [17]

From (18), it can be concluded that

$$n_1 + n_2 + \cdots + n_k = \frac{N_{\text{IGBT}} - k}{3} = c \tag{19}$$

Considering (11) and (19), the number of voltage levels in (11) will be maximum when the following condition being satisfied:

$$n_1 = n_2 = \cdots = n_k = n \tag{20}$$

From (19) and (20), k returns as follows:

$$k = \frac{N_{\text{IGBT}}}{3n + 1} \tag{21}$$

Now, the value of n must be determined. Considering (11) and (20), the maximum number of voltage levels will be

$$N_{\text{step}} = (2n+1)^k \tag{22}$$

Considering (21) and (22), it is clear that

$$N_{\text{step}} = (2n+1)^{\frac{N_{\text{IGBT}}}{3n+1}} \tag{23}$$

Equation (23) will be maximum when $(2n+1)^{\frac{1}{3n+1}}$ picks its maximum value. Figure 4 shows the variation of $(2n+1)^{\frac{1}{3n+1}}$ versus n. From this figure, it is evident that the maximum number of voltage levels is obtained for $n=2$. In other words, for producing the maximum number of voltage levels at the output of structure shown in Fig. 3, each unit of the proposed topology must have two dc voltage sources.

4.2 Optimal Structure for Maximum Number of Voltage Levels with Constant Number of DC Voltage Sources

The number of dc voltage source is expressed with N_{dc} and calculated as follows:

$$N_{\text{dc}} = \sum_{j=1}^{k} n_j = n_1 + n_2 + \cdots + n_k \tag{24}$$

Considering (20), the number of dc voltage sources will be

$$N_{\text{dc}} = nk = c \tag{25}$$

The above equation results:

$$k = \frac{N_{\text{dc}}}{n} \tag{26}$$

From (22) and (26), the number of voltage levels can be written as:

$$N_{\text{step}} = (2n+1)^{\frac{N_{\text{dc}}}{n}} \tag{27}$$

Equation (27) will be maximum when $(2n+1)^{\frac{1}{n}}$ picks its maximum value. Figure 5 shows the variation of $(2n+1)^{\frac{1}{n}}$ versus n. As shown in Fig. 5, the maximum number of voltage levels is obtained for $n=2$.

4.3 Optimal Structure for Minimum Number of Switches with Constant Number of Voltage Levels

To satisfy this objective, the relation between N_{step} and N_{IGBT} should be obtained. From (23), N_{IGBT} can be written as follows:

$$N_{\text{IGBT}} = \ln(N_{\text{step}}) \times \frac{3n+1}{\ln(2n+1)} \tag{28}$$

Since N_{step} is constant, N_{IGBT} will be minimum when $\frac{3n+1}{\ln(2n+1)}$ tends to minimum. Figure 6 shows the variation of $\frac{3n+1}{\ln(2n+1)}$ versus n. This figure shows that the minimum value of N_{IGBT} occurs in $n=2$.

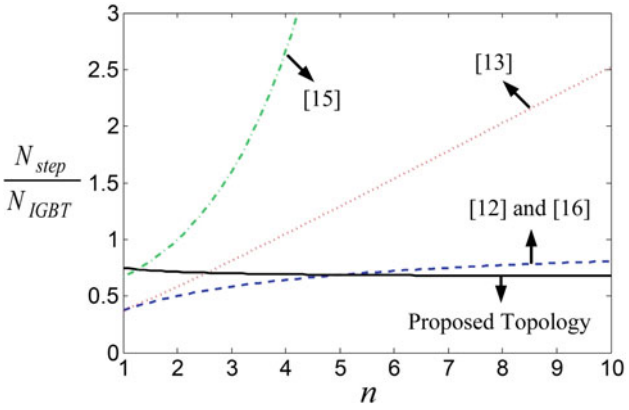

Fig. 8 Comparison of $\frac{N_{\text{step}}}{N_{\text{IGBT}}}$ for theproposed topology and the structures presented in [12–16] for an extended unit with n dc voltage sources

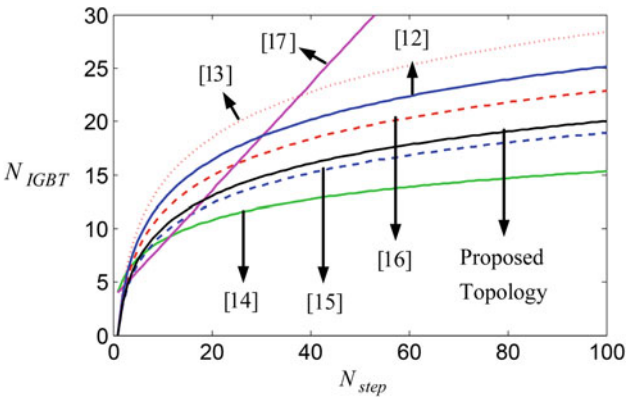

Fig. 9 Comparison of the required number of IGBTs to realize N_{step} voltages in the proposed topology and the structures presented in [12–17]

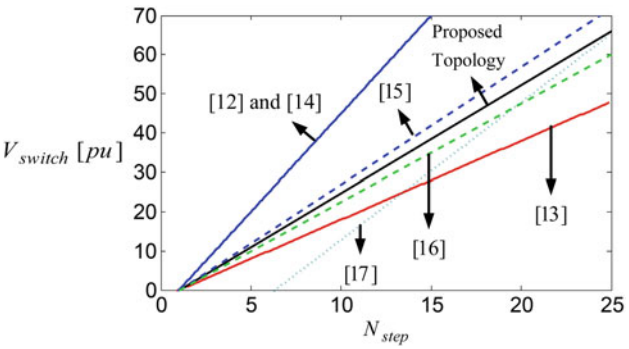

Fig. 10 Standing voltages on switches to realize N_{step} voltages in the proposed topology and the structures presented in [12–17]

4.4 Optimal Structure for Minimum Standing Voltage of Switches with Constant Number of Voltage Levels

Voltage and current ratings of the switches in a multilevel inverter play important roles in the total cost of the inverter. In all topologies, the currents of all switches are equal to the rated current of the load. This is, however, not the case

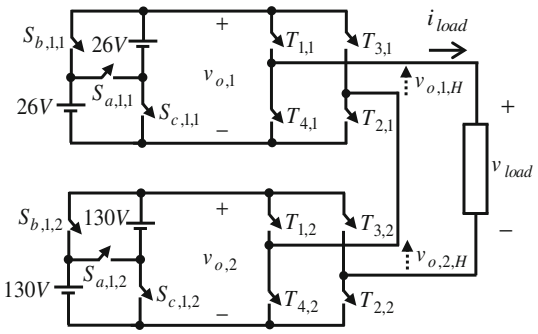

Fig. 11 25-level inverter based on proposed topology

Table 1 Switching look-up table for multilevel inverter shown in Fig. 11

v_{Load} (pu) (26 V = 1 pu)		−12	...	−1	0	1	...	12
Switches state	$S_{a,1,1}$	1	...	0	0	0	...	1
	$S_{a,1,2}$	1	...	0	0	0	...	1
	$T_{1,1}$	0	...	0	0	1	...	1
	$T_{2,1}$	0	...	0	1	1	...	1
	$T_{3,1}$	1	...	1	0	0	...	0
	$T_{4,1}$	1	...	1	1	0	...	0
	$T_{1,2}$	0	...	0	0	0	...	1
	$T_{2,2}$	0	...	1	1	1	...	1
	$T_{3,2}$	1	...	0	0	0	...	0
	$T_{4,2}$	1	...	1	1	1	...	0

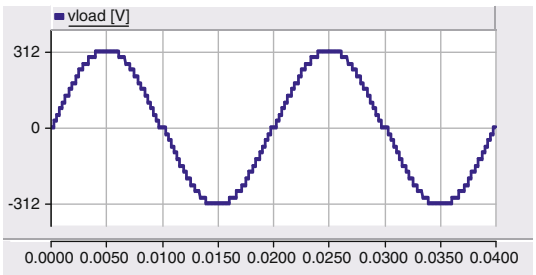

Fig. 12 Output voltage of 25-level inverter

for the voltage [12]. Hence, there is a need for a criterion to evaluate the multilevel inverter from the viewpoint of blocked voltage by power switches and the total cost of system. This criterion has been captioned as "standing voltage" in [12]. The standing voltage is equal to the sum of all blocked voltage by power switches in a converter. In this section, the objective is to find the structure with the minimum standing voltage and maximum number of voltage levels at the output.

The standing voltage or peak value of the blocked voltage by the switches is equal to the sum of the blocked voltage by switches S_a, S_b, and S_c and the H-bridge switches (T_1–T_4) for all units. The value of this voltage is given by:

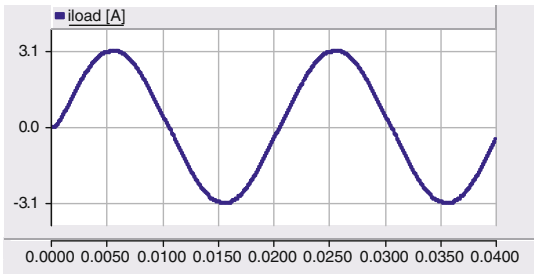

Fig. 13 Output current of 25-level inverter

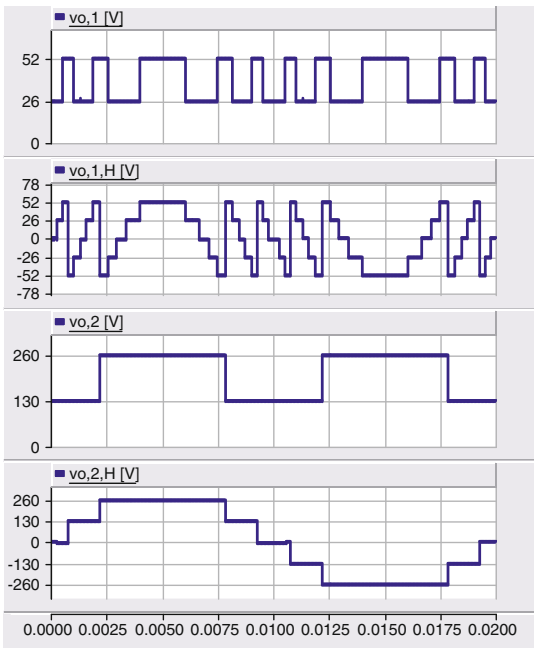

Fig. 14 Output voltage for each section of the 25-level inverter

$$V_{\text{switch}} = \sum_{j=1}^{k} V_{\text{switch},j} \tag{29}$$

The peak value of the blocked voltage by switches in the first unit ($V_{\text{switch},1}$) can be evaluated by follows:

$$V_{\text{switch},1} = 3(n_1-1) \times V_1 + 4n_1V_1 = (7n_1-3)V_1 \tag{30}$$

The peak value of the blocked voltage by switches in the second unit ($V_{\text{switch},2}$) is calculated by

$$V_{\text{switch},2} = 3(n_2-1) \times V_2 + 4n_2V_2 = (7n_2-3)V_2 \tag{31}$$

And finally, the peak value of the blocked voltage by switches in the kth unit ($V_{\text{switch},k}$) is obtained as follows:

$$V_{\text{switch},k} = 3(n_k-1) \times V_k + 4n_kV_k = (7n_k-3)V_k \tag{32}$$

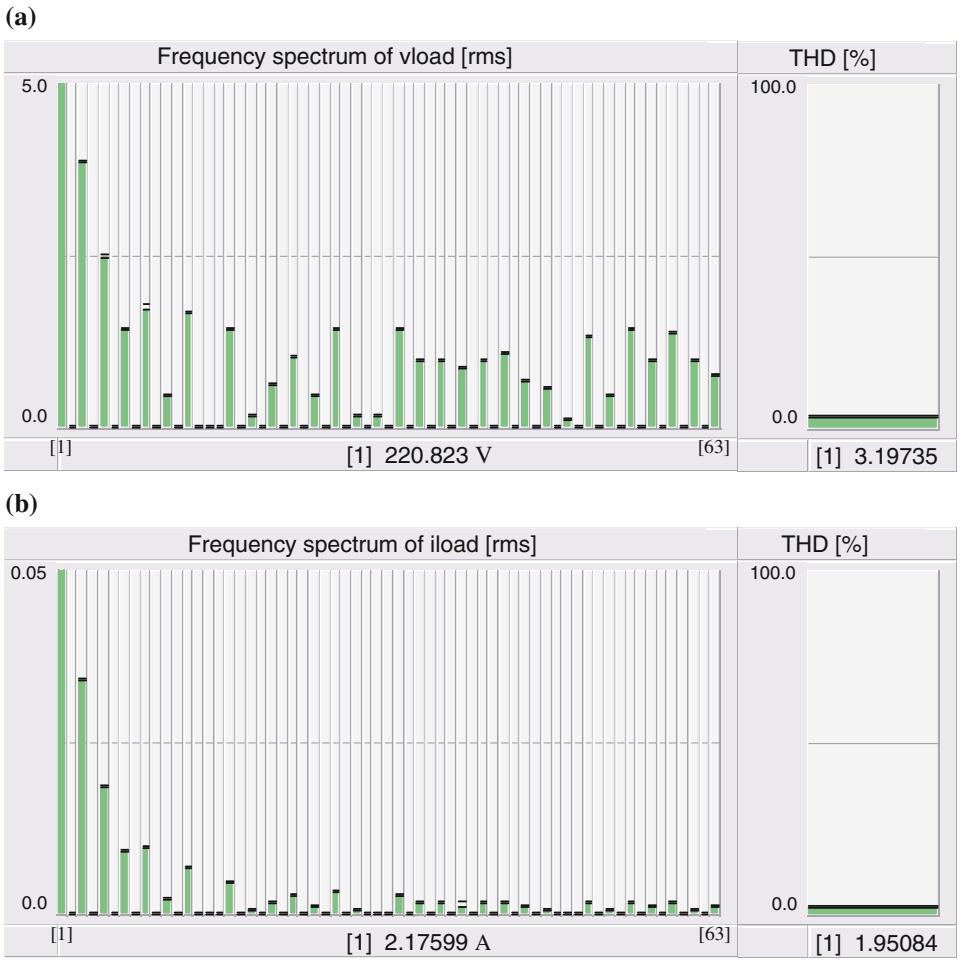

Fig. 15 Frequency spectrum and THD of 25-level inverter, **a** output voltage, **b** output current

From (20) and (29), can be written as:

$$V_{\text{switch}} = (7n-3) \times \sum_{j=1}^{k} V_j = (7n-3) \times (V_1 + V_2 + \cdots + V_k) \tag{33}$$

The voltages V_1–V_k in (33) have been represented using the proposed algorithm for determination of dc voltage sources values (14–17). Considering (14)–(17), (20) can be simplified as follows:

$$\begin{aligned} V_1 &= V_{\text{dc}} \\ V_2 &= (2n+1)V_{\text{dc}} \\ V_3 &= (4n^2+4n+1)V_{\text{dc}} \\ &\vdots \\ V_k &= \left(2^{k-1}n^{k-1} + 2^{k-2}C_{k-1}^{k-2}n^{k-2} + 2^{k-3}C_{k-1}^{k-3}n^{k-3} + \cdots + 1\right) V_{\text{dc}} \end{aligned} \tag{34}$$

The symbol C_k^m in (34) is defined by

$$C_k^m = \binom{k}{m} = \frac{k!}{m!(k-m)!} \tag{35}$$

Now, (33) can be rewritten as follows:

$$\begin{aligned} V_{\text{switch}} = (7n-3)V_{\text{dc}} \times \Bigg\{ & k + 2n \times \left[\binom{1}{1} + \binom{2}{1} + \cdots + \binom{k-1}{1} \right] + 2^2 n^2 \times \left[\binom{2}{2} + \binom{3}{2} + \cdots + \binom{k-1}{2} \right] \\ & + 2^3 n^3 \times \left[\binom{3}{3} + \binom{4}{3} + \cdots + \binom{k-1}{3} \right] \\ & + \cdots + 2^{k-1} n^{k-1} \times \binom{k-1}{k-1} \Bigg\} \end{aligned} \tag{36}$$

It must be mentioned that n is a positive integer number and its minimum value is $n = 2$. With the consideration of the voltages V_1–V_k presented in (34), V_{switch} in (33) will be minimum when each V_1–V_k tends to minimum. Therefore, V_{switch} will be minimum when $n = 2$. Choosing $n = 2$, the proposed multilevel inverter will be capable of producing the maximum number of voltage levels with minimum number of switches, dc voltage sources, and blocked voltage by switches. In other words, all the optimization conditions can be satisfied by utilizing a uni-

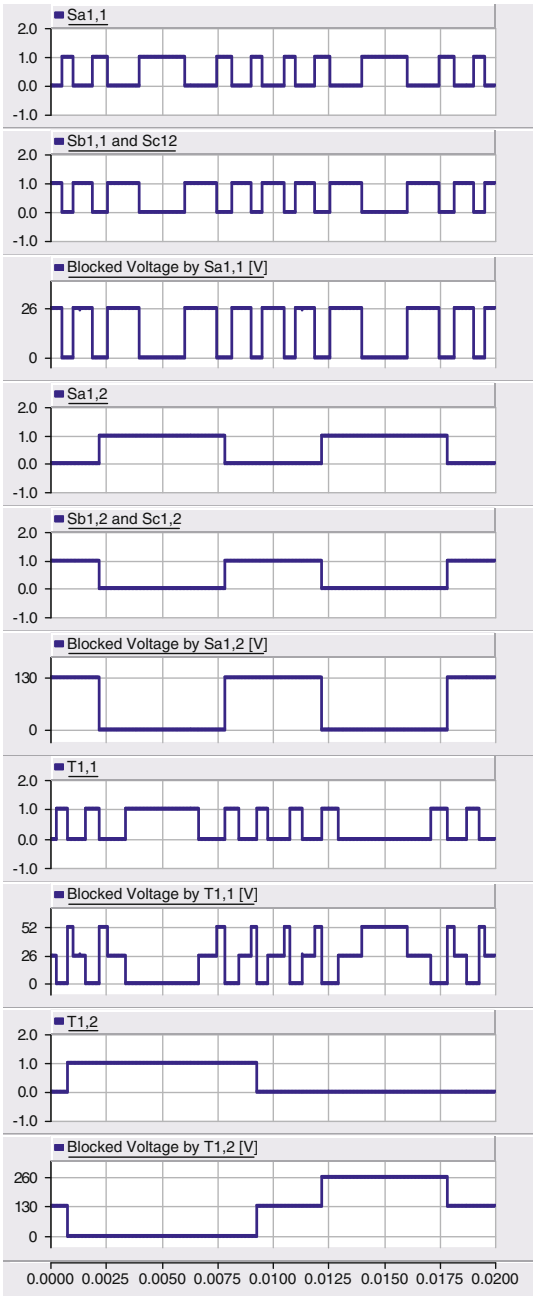

Fig. 16 Switching state and blocked voltage by switches of 25-level inverter

form structure. Satisfaction of all optimization limits by choosing $n = 2$ is an advantage for proposed multilevel inverter.

5 Comparison of the Proposed Topology with Other Topologies

For revelation of the abilities of proposed multilevel inverter, the comparison results between the proposed topology

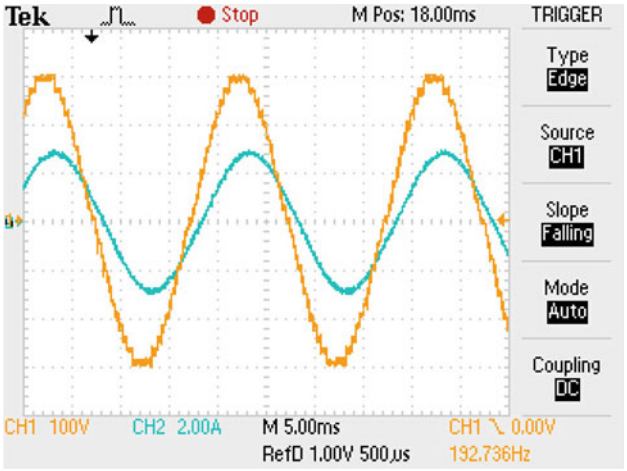

Fig. 17 Experimental output voltage and current of 25-level inverter

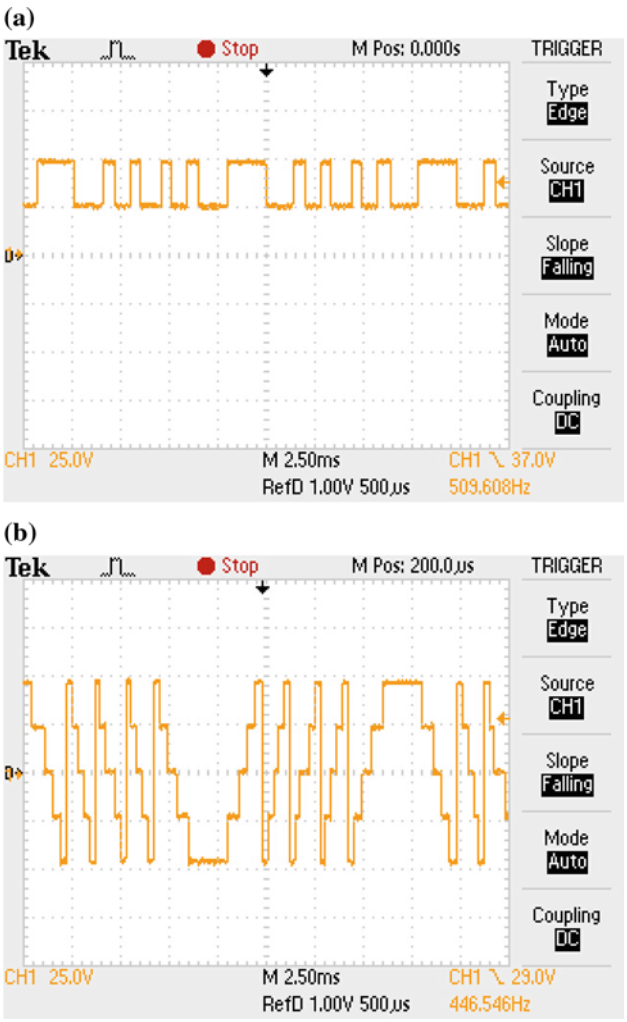

Fig. 18 Experimental output voltages of 25-level inverter, **a** first unit, **b** first H-bridge

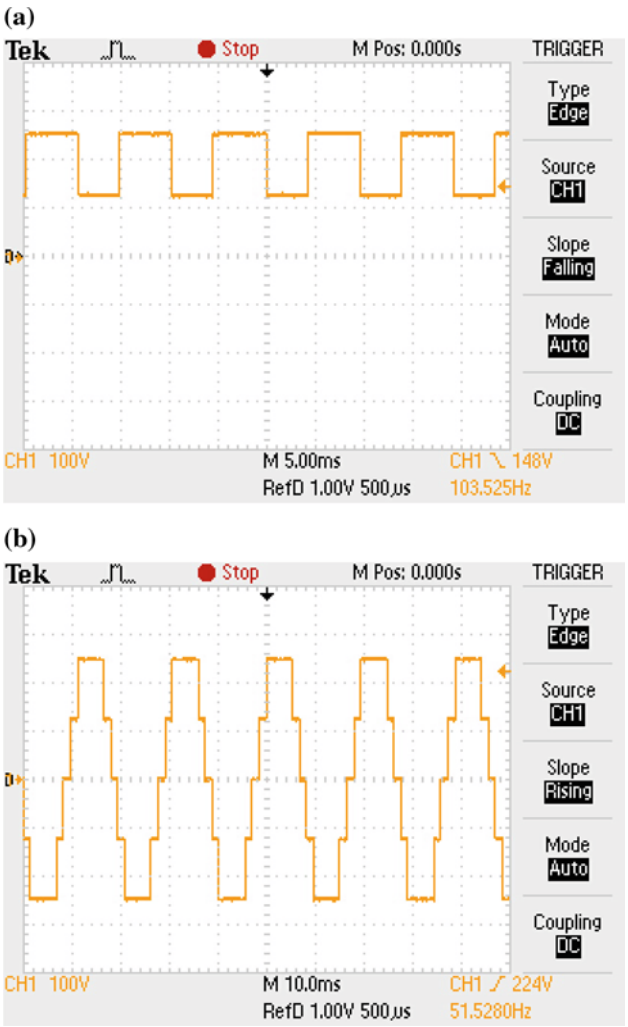

Fig. 19 Experimental output voltages of 25-level inverter, **a** second unit, **b** second H-bridge

and those presented in [12–17] (Fig. 7a–f) are given. It is important to note that in the presented topologies in [12,13,16] the bidirectional power switches have been utilized.

Figure 8 compares the ratio of $\frac{N_{\text{step}}}{N_{\text{IGBT}}}$ for proposed topology with those presented in [12,13,15,16] for an extended unit with n dc voltage sources. This figure illustrates that the proposed topology without the units cascading has no advantage against the mentioned topologies except parallel connection of the dc voltage sources. Because of the nonmodular structure of the topologies recommended in [14,17], this comparison will not be meaningful for these topologies.

Figures 9 and 10 show the variation of number of required IGBTs and standing voltage on power switches versus the number of voltage levels, respectively.

6 Simulation and Experimental Results

In order to verify the performance of the proposed multilevel inverter, the simulation has been done for the single-phase 25-level output voltage. Figure 11 shows the simulated 25-level inverter circuit. The simulated multilevel inverter has been set to produce a 50 Hz, staircase 25-level voltage waveform with the maximum value of $220\sqrt{2}$ V. PSCAD/EMTDC software has been used for simulation. In this paper, the fundamental frequency switching scheme has been used for producing the desirable voltage levels at the output. Table 1 shows the switching look-up table for producing different voltage levels. In this table, 0 and 1 represent the off and on states of switches, respectively. As been noted in Sect. 2, the switches S_b and S_c operate in a complementary mode with S_a. Therefore, the states of $S_{b,1,1}$, $S_{c,1,1}$, $S_{b,1,2}$, and $S_{c,1,2}$ have not been shown in Table 1. It should be noted that there are several switching patterns for the generation of the different voltage levels. These patterns can be used for some ideas such as minimizing the total harmonic distortion (THD) and selective harmonic elimination. But these goals are not the objective of this paper.

Figures 12 and 13 show the simulated output voltage and current of the proposed 25-level inverter, respectively. The R–L load ($R = 100\Omega$ and $L = 55$ mH) has been used for the simulation. Since the R–L load has the low-pass filtering feature, the load current shown in Fig. 13 is more similar to sinusoidal waveform.

The simulated output voltage of each unit ($v_{\text{o},1}$ and $v_{\text{o},2}$) and each H-bridge ($v_{\text{o},1,\text{H}}$ and $v_{\text{o},2,\text{H}}$) are shown in Fig. 14. Each unit output voltage consists of the positive voltage levels. The H-bridges generate zero and negative voltage levels and combine the voltage levels to produce the desirable output waveform. Considering (12) and (14)–(17), to produce $220\sqrt{2}$ V at output, the magnitude of dc voltage sources in the first and second units must be chosen 26 and 130 V, respectively.

Figure 15a, b shows the frequency spectrums of the output voltage and current, respectively. As shown in Fig. 15, the output voltage and current of the 25-level inverter are very close to a pure sinusoidal waveform. The THDs of output voltage and current are 3.2 and 1.95 %, respectively.

Figure 16 shows the switching states and blocked voltages by the switches. The complementary operation of $S_{b,1,1}$ and $S_{c,1,1}$ with $S_{a,1,1}$, and also $S_{b,1,2}$ and $S_{c,1,2}$ with $S_{a,1,2}$ can be seen in Fig. 16. This behavior makes the switches control simpler. Figure 16 also shows the blocked voltage by switches. Considering (36) with $k = 2$, $n = 2$, and $V_{\text{dc}} = 26$V, the maximum blocked voltage by switches will be 1716 V. This value is the sum of the blocked voltages of all switches in the multilevel inverter.

The experimental study has been done for proposed 25-level inverter with the R–L load ($R = 100\Omega$ and $L =$

55 mH) mentioned in simulation. The IGBTs of the prototype are BUP306D with internal anti-parallel diodes. The 89C52 microcontroller by ATMEL Company has been used to generate the switching patterns.

Figure 17 shows the experimental output voltage and current waveforms respectively. The output voltage of first unit ($v_{o,1}$) and its H-bridge ($v_{o,1,H}$) is shown in Fig. 18. Figure 19 shows the output voltages for second unit ($v_{o,2}$ and $v_{o,2,H}$), also. As can be seen, the experimental results have good agreement with the simulation.

7 Conclusion

In this paper, a structure for improvement of the multilevel inverter presented in [17] that operates on the base of the series and parallel connections of the dc voltage sources was proposed. In the proposed topology, the capability of series and parallel connections of the dc voltage sources increases the number of voltage levels and the output current, respectively. The optimal number of switches and dc voltage sources was calculated in order to have maximum number of voltage levels at the output with minimum blocked voltage by switches. It was shown that the proposed topology is in the optimal state from the viewpoint of the number of switches and dc voltage sources, the maximum number of voltage levels, and the blocked voltage by switches when $n_1 = n_2 = \cdots = n_k = n = 2$ and this is an advantage for the proposed multilevel inverter. In addition, a new algorithm was proposed for the determination of the magnitudes of dc voltage sources also. The ability of the proposed topology in agreement of desired output voltage was verified by simulation and experimental of a 25-level inverter based on proposed topology.

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