

A Modified Space Vector PWM Approach for Nine-Level Cascaded H-Bridge Inverter

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Received: 6 June 2017 / Accepted: 29 May 2018
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Abstract

This paper presents a modified space vector pulse width modulation (MSVPWM) technique for nine-level cascaded H-bridge (CHB) inverter. Based on a modular structure and absence of capacitor balancing problems, CHB inverter topology is preferred. Nowadays, space vector PWM (SVPWM) control scheme has achieved higher attention among different PWM techniques. In general, SVPWM method is realized based on disintegrating higher-level hexagons into a number of two-level hexagons. Compared to conventional SVPWM technique, the proposed MSVPWM technique reduces the computational burden and memory requirement involved in the realization of nine-level SVPWM. This is achieved by reducing the number of two-level hexagons without losing the inverter output voltage profile. Also a further modified space vector pulse width modulation technique is presented, which greatly reduces the computation efforts. The proposed SVPWM techniques are applied to a nine-level CHB inverter by using MATLAB/SIMULINK software tool and are compared with carrier-based sinusoidal pulse width modulation (SPWM) technique to validate the proposed techniques. The proposed SVPWM schemes produce lower harmonic distortion and higher DC bus utilization compared to SPWM technique. To verify the practicality of the proposed SVPWM techniques, experimental results are presented on nine-level CHB inverter.

Keywords Cascaded H-bridge (CHB) · Pulse width modulation (PWM) · Two-level hexagon · Harmonic distortion · Nine-level inverter

1 Introduction

In conventional two-level inverter, output voltage with lower harmonic is obtained by increasing the switching frequency, which causes higher switching losses, and voltage stress on the switches is high due to less number of steps in output voltage. This drawback in two-level inverter increases the interest

on the multilevel inverters (MLIs). Multilevel idiom starts through the three-level cascaded H-bridge (CHB) inverter introduced by Baker and Bannister [1]. In 1980, neutral point clamped (NPC) MLI was proposed by Baker [2,3]. Nabae et al. [4] published an article pertaining to the execution of pulse width modulation (PWM) for three-level performance in 1981. The flying capacitor (FC) MLI was introduced by Meynard et al. [5].

Nowadays, MLIs are extensively used in industries for requirement of medium-voltage and high-power applications [6]. MLIs have more number of switches and DC sources to produce the stair case waveform, which is nearer to sinusoidal waveform to obtain lower harmonic distortion [7]. The merits of MLIs over the conventional two-level inverter are lower dv/dt stress on the power switches, higher fundamental output voltage, lower inverter switching loss, common mode voltage, electromagnetic interference and harmonic distortion. Owing to these merits, MLIs has a wide range of applications in FACTS, electric vehicles, HVDC, PV systems etc. Both NPC and FC topologies are similar in

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Fig. 1 Configuration of a three-phase cascaded H-bridge inverter and **b** H-bridge cell with source

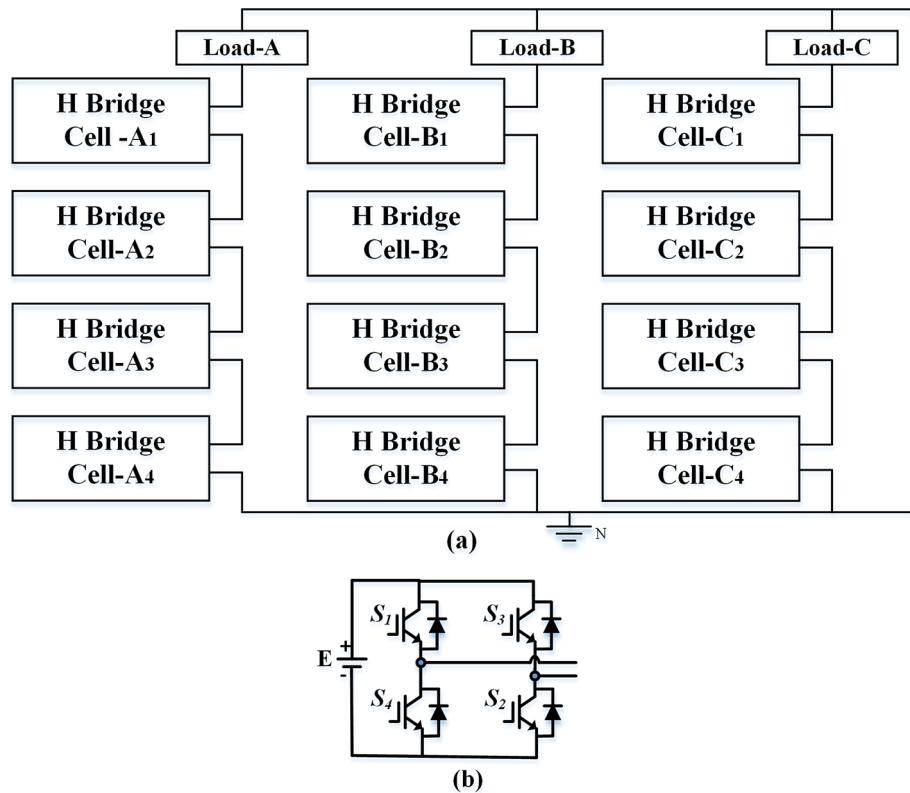


Fig. 2 Decomposition of nine-level SVD into five-level SVDs

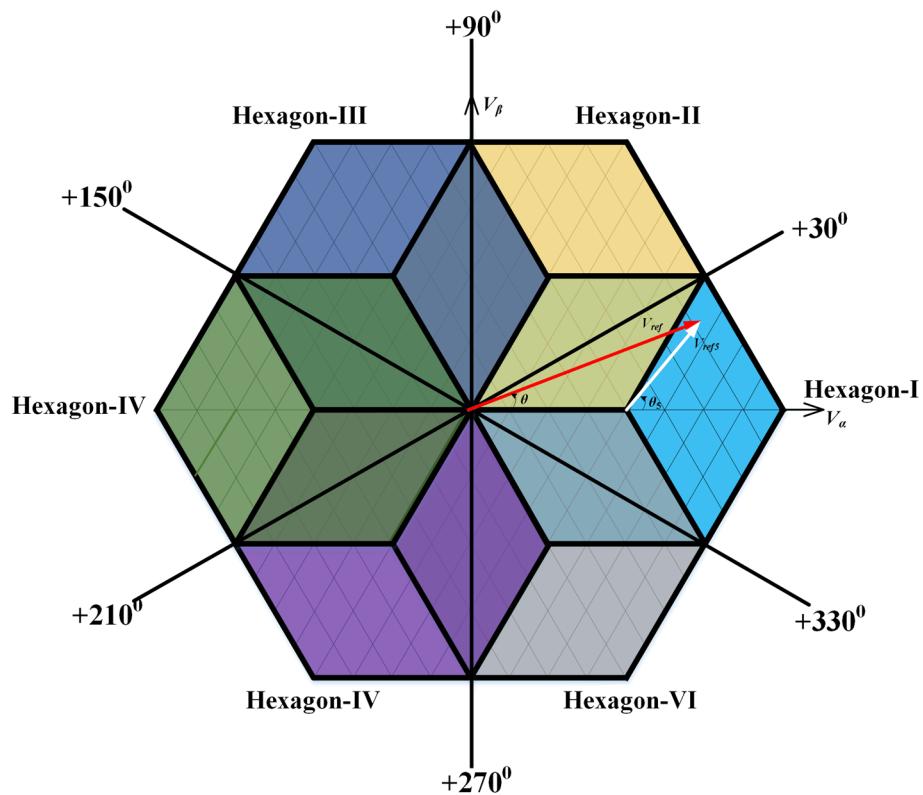


Table 1 Selection of five-level hexagons from nine-level SVD

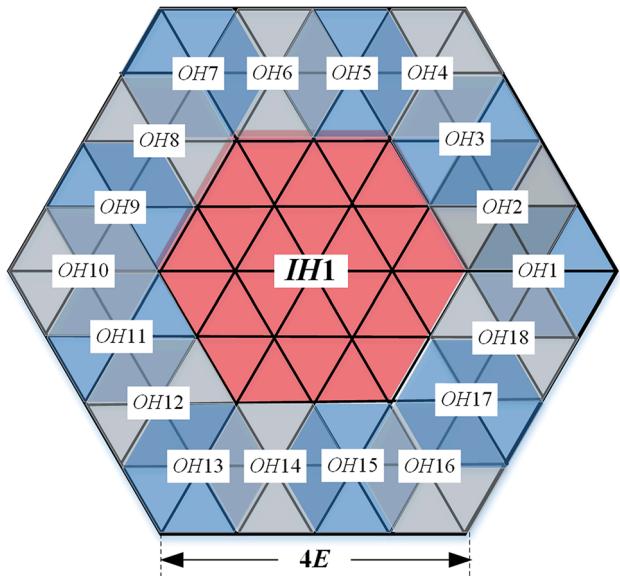
Hexagon no.	Range of θ
I	330°–30°
II	30°–90°
III	90°–150°
IV	150°–210°
V	210°–270°
VI	270°–330°

Table 2 Mapping of $V_{\text{ref}5}$ from $V_{\text{ref}9}$

Hexagon no.	$V_{5\alpha}$	$V_{5\beta}$
I	$V_{9\alpha} - 4E$	$V_{9\beta}$
II	$V_{9\alpha} - 4E \cos(\pi/3)$	$V_{9\beta} - 4E \sin(\pi/3)$
III	$V_{9\alpha} - 4E \cos(2\pi/3)$	$V_{9\beta} - 4E \sin(2\pi/3)$
IV	$V_{9\alpha} + 4E$	$V_{9\beta}$
V	$V_{9\alpha} - 4E \cos(4\pi/3)$	$V_{9\beta} - 4E \sin(4\pi/3)$
VI	$V_{9\alpha} - 4E \cos(5\pi/3)$	$V_{9\beta} - 4E \sin(5\pi/3)$

design, but the only difference is NPC has diodes in ladder form and FC has capacitors in ladder form. Both NPC and FC require more number of power components to produce higher inverter levels and also they have voltage imbalance problems. In CHB topology, H-bridge cells are linked in series fashion and each cell requires a separate DC source which forms the modular topology. This CHB topology is useful for both three-phase and single-phase power conversion. Among three basic MLI topologies, CHB MLIs are highly suitable for PV applications [8,9]. The structures of three-phase nine-level cascaded H-bridge inverter operating in symmetric mode is shown in Fig. 1. Each phase requires four H-bridge to obtain nine-level. To generate $2n + 1$ level, each phase requires n -bridges to be series connected. Each H-bridge requires separate DC source. Hence, for three-phase nine-level CHB inverter requires twelve separate DC sources with same magnitude; this property makes the CHB inverter to be used widely in renewable energy applications.

Generally inverter modulation strategies for MLIs are mainly multicarrier level shifted sinusoidal pulse width modulation (SPWM) [10] and space vector pulse width modulation (SVPWM) [11]. SPWM technique is easier to implement, but, however, SVPWM technique gives higher DC bus utilization, lower harmonic content, lower common mode voltage [12,13], and allows balancing the capacitor voltage problems with the help of redundant switching state [14]. Digital implementation of SVPWM is easier. Hence, SVPWM is preferred PWM technique for industrial applications. The steps required to implement the SVPWM [15] are finding the sector in which reference voltage V_{ref} lies; followed by selection of a triangle in a particular sector based on V_{ref} location, calculation of switching dwell

**Fig. 3** Resolution of five-level SVD into two-level hexagons

times and selection of optimal switching instants to generate pulses to the inverter circuit. Realization of SVPWM for MLI is not so easy because complexity increases with the increase in the inverter levels.

Various SVPWM techniques have been presented in the literature in order to reduce the burden of mathematical computations. The higher-level hexagons are disintegrated into basic two-level hexagons, and the conventional approach is adopted thereafter. A SVPWM technique in [16] is implemented for three-level inverter, in which three-level hexagon is decomposed into six two-level hexagons. The origin of three-level hexagon is shifted to respective two-level hexagon to realize three-level SVM as same as in the case of two-level SVM approach. In [17], generalized SVM is done for n -level inverter by using the euclidean vector approach. A fractal theory-based SVM approach for MLI is presented in [18], which involves the finding the triangle in which reference signal tip lies by triangularisation algorithm. In [19], initially five-level space vector hexagon disintegrated into six three-level hexagons, and further three-level hexagon is reduced to six two-level hexagons. In [20], seven-level SVPWM initially decomposed of six four-level hexagons and then four-level hexagon is composed into two-level hexagon and the normal conventional procedure applied to realize SVPWM for the seven-level inverter. Figure 2 shows the space vector diagram(SVD) for nine-level inverter, which means inverter phase output voltage levels vary from $+P_4$ (corresponding to positive peak level) to $-N_4$ (corresponding to negative peak level). In general, for N -level inverter: the total numbers of switching instants are N^3 . Out of N^3 , $(3N^2 - 3N + 1)$ are independent switching instants and remaining are redundancy switching instants [20]. In N -



Fig. 4 Selection of hexagons (inner/outer) in the five-level SVD

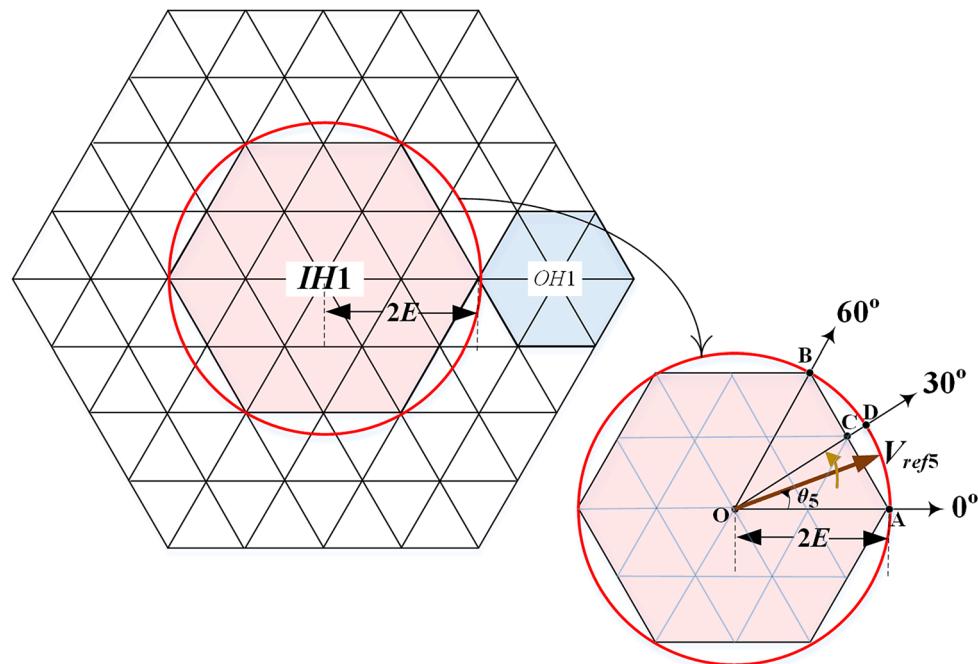


Table 3 Selection of two-level hexagons from five-level SVD

Hexagon no.	Range of θ
OH1	345°–15°
OH2	15°–30°
OH3	30°–45°
OH4	45°–75°
OH5	75°–90°
OH6	90°–105°
OH7	105°–135°
OH8	135°–150°
OH9	150°–165°
OH10	165°–195°
OH11	195°–210°
OH12	210°–225°
OH13	225°–255°
OH14	255°–270°
OH15	270°–285°
OH16	285°–315°
OH17	315°–330°
OH18	330°–345°

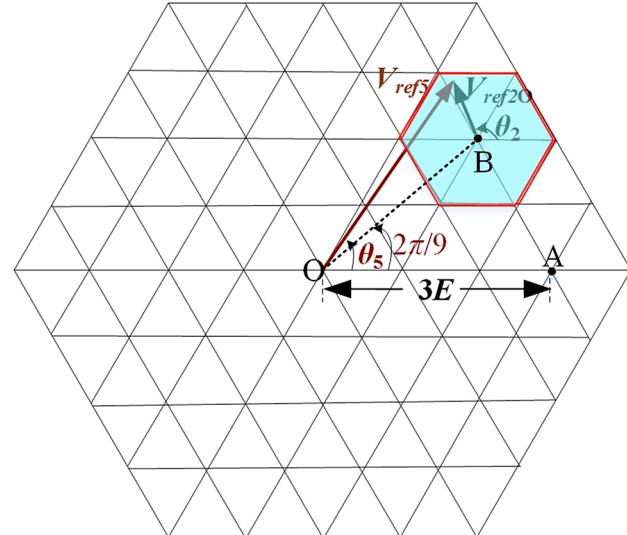


Fig. 5 Five-level hexagon with V_{ref5} and V_{ref2} in two-level hexagon (OH3)

level SVD, it has $(N - 1)$ layers and $(N - 1)^3$ triangles. So, for 9-level inverter: it has $9^3 = 729$ switching instants. Among 729 switching instants, 217 are independent switching instants; remaining 512 are redundancies switching instants. It has 8 layers and 512 triangles in the space vector diagram.

The proposed MSVPWM technique significantly reduces the computational burden involved without losing the inverter

output voltage profile. The number of two-level hexagons that are required for nine-level inverter is reduced from 1296 to 144 count. A Further Modified Space Vector Pulse Width Modulation (FMSVPWM) technique is also presented, which greatly reduces the computation efforts by further reducing from 144 to 108 two-level hexagons. The proposed two SVPWM techniques are evaluated for nine-level inverter and are compared with well-known carrier-based SPWM technique to validate the presented techniques. An experimental verification has been done to validate the proposed SVPWM techniques.



2 Proposed MSVPWM Technique

The MSVPWM technique depends on the idea of reducing the high-level SVD into two-level hexagons. The nine-level SVD is shown in Fig. 2. Initially, nine-level SVD is reduced into 6 five-level hexagons, which is shown in Fig. 2. The midpoint of first five-level hexagon (Hexagon-I) is along zero degree axes, and then the midpoint of each succeeding five-level hexagon is deviated by 60° . The suitable hexagon is selected based on the value of angle θ to remove the overlapping among the adjoining hexagons. Table 1 shows the selection of five-level hexagons based on the angle θ of reference signal V_{ref} .

As soon as five-level hexagons is selected, a new reference vector $V_{\text{ref}5}$ is required, which comes from centre of selected five-level hexagon, so that the vector tips of both V_{ref} and $V_{\text{ref}5}$ coincide. Consider an example, the tip of V_{ref} lies in Hexagon-I shown in Fig. 2. Here, the mapped reference vector $V_{\text{ref}5}$ from Hexagon-I and reference signal V_{ref} coincide with their tips as shown in Fig. 2. Mathematically, the real and imaginary components of the vector $V_{\text{ref}5}$ are calculated from V_{ref} as shown below

$$V_{5\alpha} = V_{9\alpha} - 4E \quad (1)$$

$$V_{5\beta} = V_{9\beta} \quad (2)$$

Here, $V_{5\alpha}$, $V_{5\beta}$ and $V_{9\alpha}$, $V_{9\beta}$ are the components of $V_{\text{ref}5}$ and V_{ref} along real (α) and imaginary (β) axes, respectively. Similar analysis can be done for reference vector V_{ref} mapping to other five-level hexagons, which is shown in Table 2. The problem of nine-level SVM reduced to five-level by calculating the $V_{\text{ref}5}$ vector.

Then, the next step is to divide the five-level into two-level hexagons. Resolving five-level hexagon to two-level hexagon is shown in Fig. 3, which is having outer 18 and inner one three-level hexagon, which has six two-level hexagons. All the six inner two-level hexagons in a five-level SVD form one three-level hexagon, which is shown in Fig. 3. So, each five-level hexagon has a total of 24 two-level hexagons. Selections of inner and outer two-level hexagons are based on the value of angle θ_5 and reference voltage $V_{\text{ref}5}$. Suppose if vector $V_{\text{ref}5}$ magnitude value is more than magnitude $2E$, then outer two-level hexagons are selected and if vector $V_{\text{ref}5}$ magnitude value is less than the magnitude $2E$ then inner two-level hexagons are selected.

As the reference vector length is constant for the particular modulation index (M) value, whose locus is in the form of circle but, the length between the centre point (O) and a side of a hexagon (AB) varies if θ_5 varies from 0° to 60° as shown in Fig. 4.

Suppose, if vector $V_{\text{ref}5}$ magnitude varies from $1.726E$ (corresponding M value is 0.5) to $1.99E$ (corresponding M value is 0.579) at an angle of 30° , although the tip of the

Table 4 Mapping of $V_{\text{ref}20}$ from $V_{\text{ref}5}$

Hexagon no.	$V_{2\alpha o}$	$V_{2\beta o}$
OH1	$V_{5\alpha} - 3E$	$V_{5\beta}$
OH2	$V_{5\alpha} - 2.6E\cos(\pi/9)$	$V_{5\alpha} - 2.6E\sin(\pi/9)$
OH3	$V_{5\alpha} - 2.6E\cos(2\pi/9)$	$V_{5\alpha} - 2.6E\sin(2\pi/9)$
OH4	$V_{5\alpha} - 3E\cos(\pi/3)$	$V_{5\alpha} - 3E\sin(\pi/3)$
OH5	$V_{5\alpha} - 2.6E\cos(4\pi/9)$	$V_{5\alpha} - 2.6E\sin(4\pi/9)$
OH6	$V_{5\alpha} - 2.6E\cos(5\pi/9)$	$V_{5\alpha} - 2.6E\sin(5\pi/9)$
OH7	$V_{5\alpha} - 3E\cos(2\pi/3)$	$V_{5\alpha} - 3E\sin(2\pi/3)$
OH8	$V_{5\alpha} - 2.6E\cos(7\pi/9)$	$V_{5\alpha} - 2.6E\sin(7\pi/9)$
OH9	$V_{5\alpha} - 2.6E\cos(8\pi/9)$	$V_{5\alpha} - 2.6E\sin(8\pi/9)$
OH10	$V_{5\alpha} + 3E$	$V_{5\alpha}$
OH11	$V_{5\alpha} - 2.6E\cos(10\pi/9)$	$V_{5\alpha} - 2.6E\sin(10\pi/9)$
OH12	$V_{5\alpha} - 2.6E\cos(11\pi/9)$	$V_{5\alpha} - 2.6E\sin(11\pi/9)$
OH13	$V_{5\alpha} - 3E\cos(4\pi/3)$	$V_{5\alpha} - 3E\sin(4\pi/3)$
OH14	$V_{5\alpha} - 2.6E\cos(13\pi/9)$	$V_{5\alpha} - 2.6E\sin(13\pi/9)$
OH15	$V_{5\alpha} - 2.6E\cos(14\pi/9)$	$V_{5\alpha} - 2.6E\sin(14\pi/9)$
OH16	$V_{5\alpha} - 3E\cos(5\pi/3)$	$V_{5\alpha} - 3E\sin(5\pi/3)$
OH17	$V_{5\alpha} - 2.6E\cos(16\pi/9)$	$V_{5\alpha} - 2.6E\sin(16\pi/9)$
OH18	$V_{5\alpha} - 2.6E\cos(17\pi/9)$	$V_{5\alpha} - 2.6E\sin(17\pi/9)$

vector lies in the outer level hexagon but according to the algorithm, we are selecting the inner three-level hexagon. This is happening because only $V_{\text{ref}5}$ magnitude is considered to find the inner or the outer level hexagon, to make the proposed algorithm simple. By doing this, the change in the voltage harmonic distortion is very less as modulation index varying from 0.5 to 0.579. It is possible to select the particular hexagon as M varies from 0.5 to 0.579 at an angle 30° , by considering both magnitude and phase angle of the vector $V_{\text{ref}5}$, which makes the algorithm complex, as the distance between the centre point (O) and a side of a hexagon (AB) is varied with respect to the angle θ_5 . For the modulation indices varies from $M = 0$ to 0.499 and $M = 0.5789$ to 1.0, the proposed algorithm selects the correct hexagon where the tip of the reference vector lies.

The selection of particular outer two-level hexagon among eighteen outer two-level hexagons in a five-level SVD is carried out based on the value of angle θ_5 shown as given in Table 3.

Meanwhile, if one of the outer two-level hexagons is selected, then a new reference vector, say $V_{\text{ref}20}$, is required, which comes from centre of selected outer two-level hexagons. Here, the tips of both $V_{\text{ref}5}$ and $V_{\text{ref}20}$ coincide. Consider an example, tip of $V_{\text{ref}5}$ lies in outer two-level hexagon-3 (OH3) shown in Fig. 5. Mathematically, the vector $V_{\text{ref}20}$ is calculated from $V_{\text{ref}5}$ as given below.

$$V_{2\alpha o} = V_{5\alpha} - 2.6E\cos(2\pi/9) \quad (3)$$

$$V_{2\beta o} = V_{5\beta} - 2.6E\sin(2\pi/9) \quad (4)$$



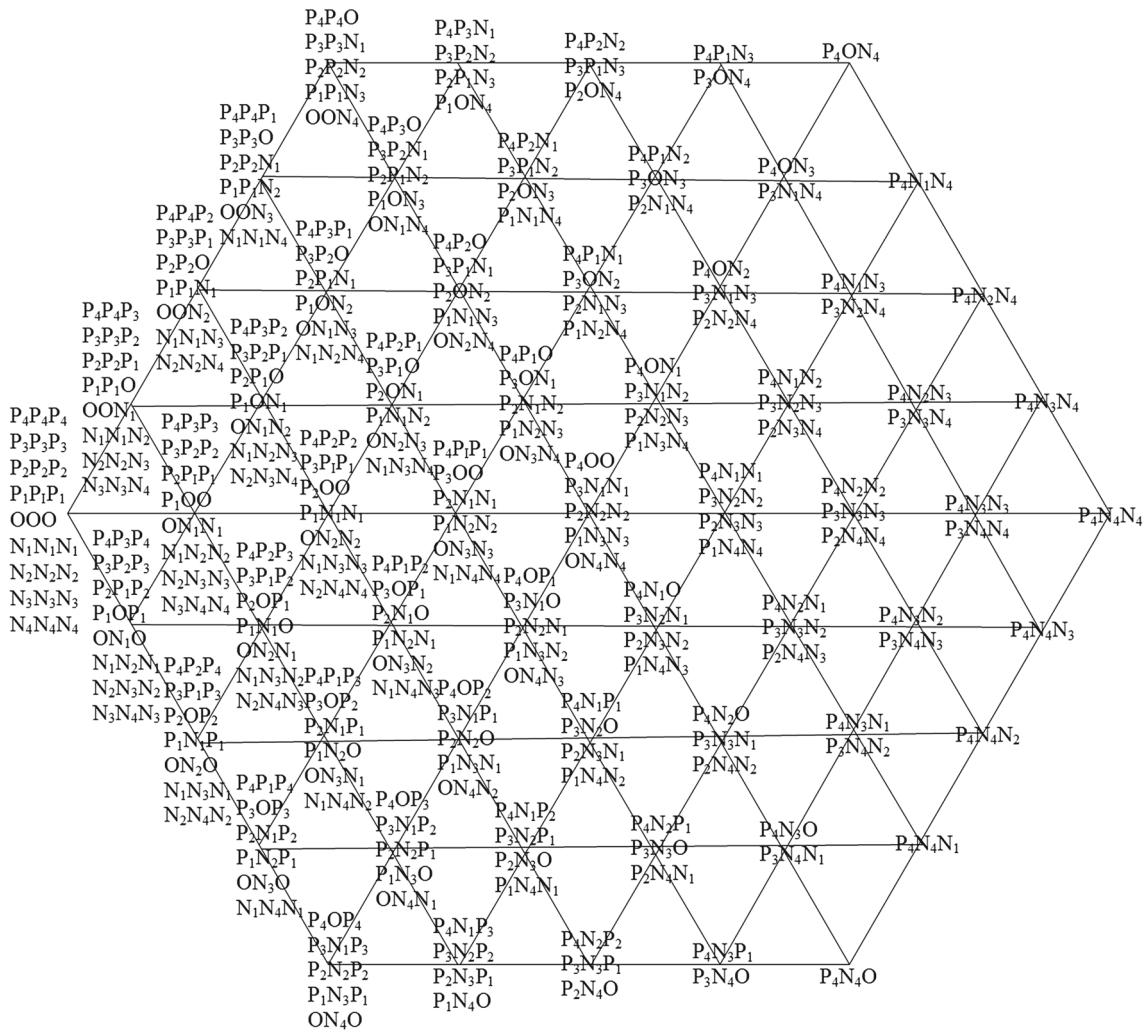


Fig. 6 Five-level hexagon-I with available stationary vectors

Here, $V_{5\alpha}$, $V_{5\beta}$ and $V_{2\alpha o}$, $V_{2\beta o}$ are the components of V_{ref5} and V_{ref2o} along real (α) and imaginary (β) axes, respectively. The relations (3) and (4) can be obtained as follows:

From Fig. 4, it is clear that

$$\overline{V_{ref5}} = \overline{OB} + \overline{V_{ref2o}} \quad (5)$$

Then

$$\overline{V_{ref2o}} = \overline{V_{ref5}} - \overline{OB} \quad (6)$$

Length of $OA = 3E$

Length of $OB = 2.6E$

The vector \overline{OB} makes an angle $2\pi/9$ with the line \overline{OA} (α -axis)

The component \overline{OB} along with the α -axis is obtained as $2.6E\cos(2\pi/9)$ and the component \overline{OB} along with the β -axis is obtained as $2.6E\sin(2\pi/9)$. Then, the voltage component along α -axis for the new reference vector V_{ref2o} is

$V_{5\alpha} - 2.6E\cos(2\pi/9)$ and voltage component along β -axis of the new reference vector V_{ref2o} is $V_{5\alpha} - 2.6E\sin(2\pi/9)$.

Consecutively Similar analysis can be done for V_{ref5} mapping to other 17 outer two-level hexagons in a five-level SVD, which is shown in Table 4. Figure 6 shows the five-level hexagons-I with all the possible switching instants. It is shown in Fig. 6 that, from the outer layer to the inner layer, number of space vector redundancies is increasing. The centre of nine-level SVD has maximum number of space vectors, which has eight redundancies.

Similarly, if the inner three-level hexagon is selected, which is a combination of six two-level hexagons, then a new reference vector, say V_{ref2i} , is required, which comes from the centre of selected inner two-level hexagons. Here, the tips of both V_{ref5} and V_{ref2i} coincide. The selection of the inner two-level hexagons in a three-level hexagon based on the value of θ_5 is shown in Table 5. Consider an example, tip of V_{ref5} lies in the inner three-level hexagon in the five-level SVD, which has a combination of 6 two-level hexagons. In Fig. 7,

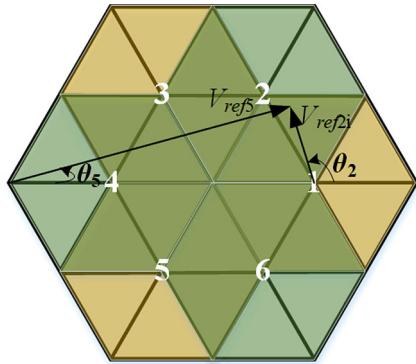
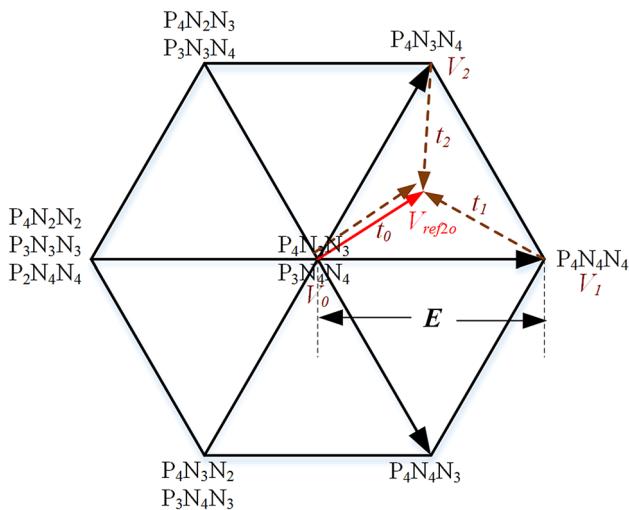
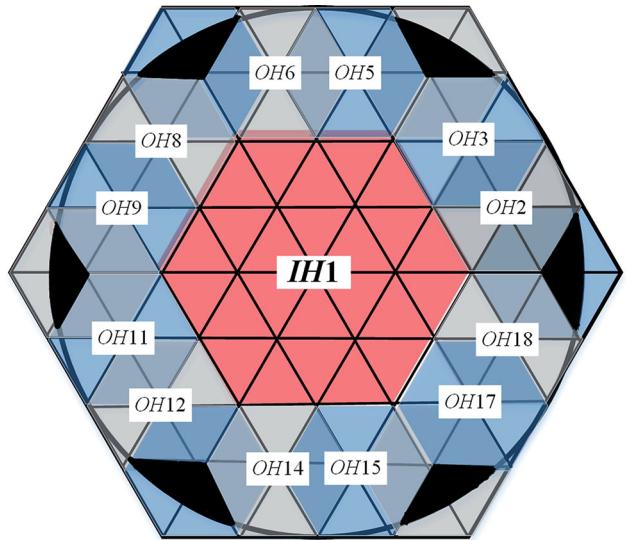


Table 5 Selection of two-level hexagons from three-level SVD

Hexagon no.	Range of θ
1	330°–30°
2	30°–90°
3	90°–150°
4	150°–210°
5	210°–270°
6	270°–330°

Table 6 Mapping of $V_{\text{ref}2i}$ from $V_{\text{ref}5}$

Hexagon no.	$V_{2\alpha i}$	$V_{2\beta i}$
1	$V_{5\alpha} - E$	$V_{5\beta}$
2	$V_{5\alpha} - E \cos(\pi/3)$	$V_{5\beta} - E \sin(\pi/3)$
3	$V_{5\alpha} - E \cos(2\pi/3)$	$V_{5\beta} - E \sin(2\pi/3)$
4	$V_{5\alpha} + E$	$V_{5\beta}$
5	$V_{5\alpha} - E \cos(4\pi/3)$	$V_{5\beta} - E \sin(4\pi/3)$
6	$V_{5\alpha} - E \cos(5\pi/3)$	$V_{5\beta} - E \sin(5\pi/3)$

**Fig. 7** Resolution of three-level SVD into two-level hexagons and reference vector mapping**Fig. 8** Two-level hexagon (OH1) with reference $V_{\text{ref}2}$ and stationary vectors**Fig. 9** Five-level SVD for $M = 1$ with inscribed circle**Table 7** Selection of two-level hexagons from five-level SVD

Hexagon no.	Range of θ
OH2	0°–30°
OH3	30°–60°
OH5	60°–90°
OH6	90°–120°
OH8	120°–150°
OH9	150°–180°
OH11	180°–210°
OH12	210°–240°
OH14	240°–270°
OH15	270°–300°
OH17	300°–330°
OH18	330°–360°

the $V_{\text{ref}5}$ tip lies in two-level hexagon-1. Mathematically, the vector $V_{\text{ref}2i}$ is calculated from $V_{\text{ref}5}$ as shown below.

$$V_{2\alpha i} = V_{5\alpha} - E \quad (7)$$

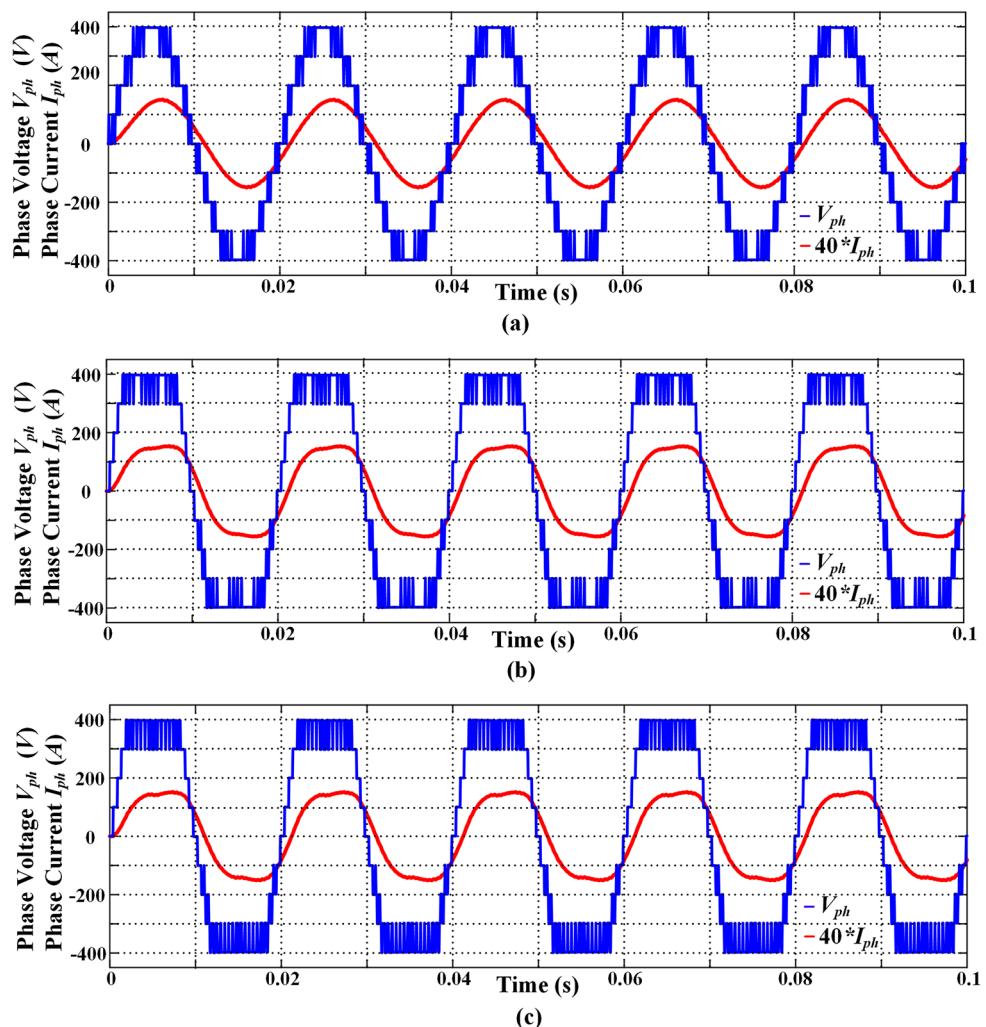
$$V_{2\beta i} = V_{5\beta} \quad (8)$$

Here, $V_{5\alpha}$, $V_{5\beta}$ and $V_{2\alpha i}$, $V_{2\beta i}$ are the components of $V_{\text{ref}5}$ and $V_{\text{ref}2i}$ along real (α) and imaginary (β) axes, respectively. Consecutively Similar analysis can be done for $V_{\text{ref}5}$ mapping to other five inner two-level hexagons in a five-level SVD is given in Table 6. Hence, the problem of nine-level SVM reduced to two-level hexagon by finding the $V_{\text{ref}2}$ vector.



Table 8 Simulation parameters

Parameter	Value
Three-phase R load	$100 \Omega/\text{ph}$
Three-phase L load	$110 \text{ mH}/\text{ph}$
Three-phase IM (1 HP)	
Stator resistance (R_s)	14.05Ω
Stator inductance (L_s)	$0.76744 H$
Rotor resistance (R_r)	8.3Ω
Rotor inductance (L_r)	$0.76744 H$
Mutual inductance (L_m)	$0.724 H$
Rotor inertia (J)	0.0088 kg m^2
Friction coefficient (B)	0.0001
Number of poles (P)	4
Sampling time (T_S)	2100 s
DC supply (E)	100 V
System frequency	50 Hz

Fig. 10 Nine-level phase voltage and phase current at unity modulation index using **a** SPWM, **b** MSVPWM and **c** FMSVPWM techniques

3 Calculation of Dwell Times and Switching Sequence Design

Similar to a conventional two-level hexagon, the dwell times, and switching instants are calculated. Every two-level hexagon has six sectors, and reference vector in each sector is realized by using the available three switching states. The time applied for each switching state is calculated based on volt-sec-balancing method. Let us consider the mapped reference vector V_{ref20} lies in outer two-level hexagon (OH1) in five-level hexagon-I as shown in Fig. 8.

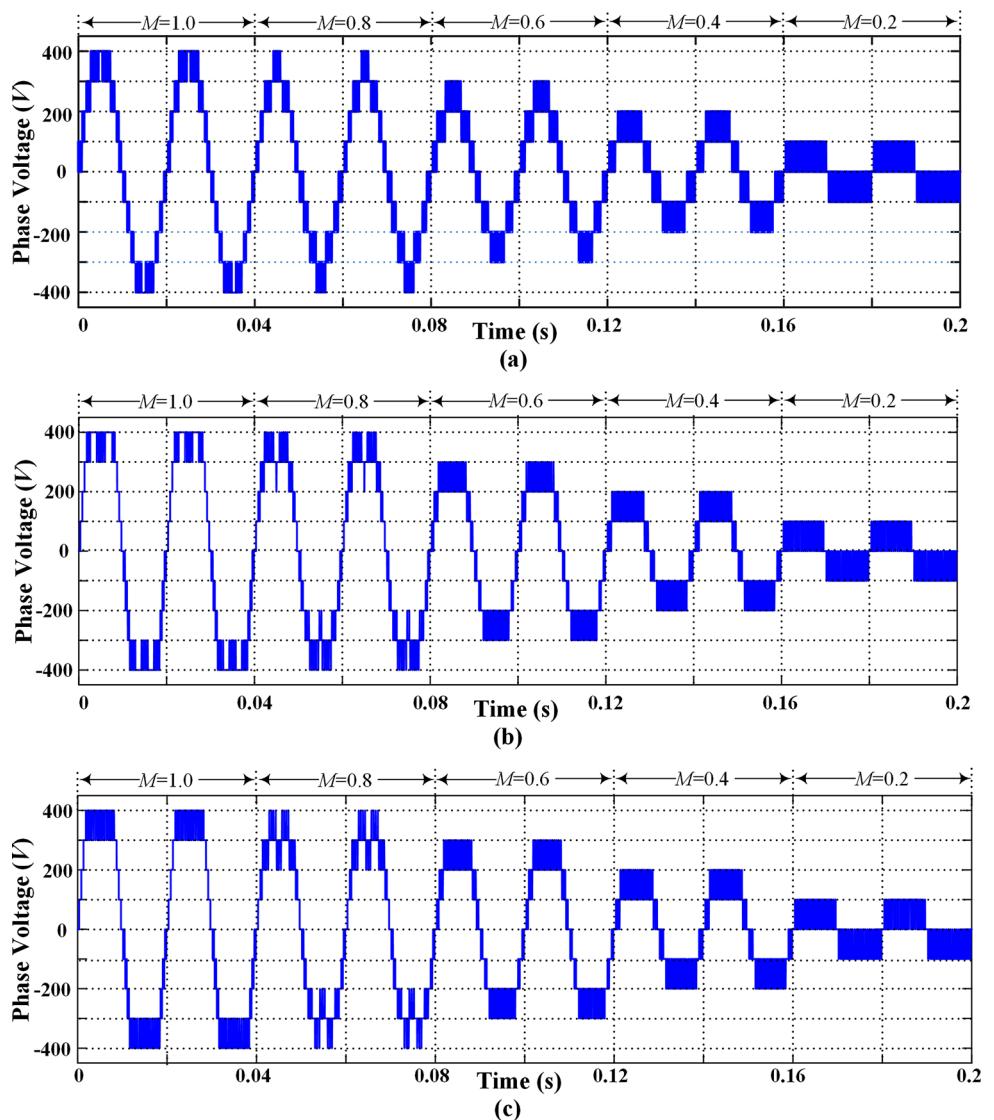
In Fig. 8, $P_4N_4N_4$ acts as an active switching state (V_1); $P_4N_3N_4$ acts as an active switching state (V_2) and $P_3N_4N_4$ or $P_4N_3N_3$ are considered as zero switching states (V_0). The dwell times for switching states V_1 , V_2 , and V_0 are T_1 , T_2 , and T_0 respectively.

The expressions to calculate dwell times for V_1 , V_2 , and V_0 are as follows

$$T_1 = T_s^* M^* \sin(60 - \theta) \quad (9)$$



Fig. 11 Nine-level phase voltage at different values of modulation index using **a** SPWM, **b** MSVPWM and **c** FMSVPWM techniques



$$T_2 = T_s^* M^* \sin(60) \quad (10)$$

$$T_0 = T_s - T_1 - T_2 \quad (11)$$

where M is modulation index, whose values varies from 0 to 1 and its expression is given by

$$M = \frac{\sqrt{3} V_{\text{ref}}}{E} \quad (12)$$

Another important step is to design the switching sequence from two active switching states and one zero switching state. This method uses seven segment switching sequence. Designing of switching sequence is such that there should be only one leg change from one switching instant to the next switching state. The seven segment switching instants with dwell timings: If the $V_{\text{ref}2}$ vector lies in sector-I, it is preferred as

$$(P_3N_4N_4)^*T_0/4, (P_4N_4N_4)^*T_1/2, (P_4N_3N_4)^*T_2/2, (P_4N_3N_3)^*T_0/2, \\ (P_4N_3N_4)^*T_1/2, (P_4N_4N_4)^*T_2/2, (P_3N_4N_4)^*T_0/4.$$

And if the $V_{\text{ref}2}$ vector lies in sector-III, it is preferred as

$$(P_3N_4N_4)^*T_0/4, (P_3N_3N_4)^*T_1/2, (P_3N_3N_3)^*T_2/2, (P_4N_3N_3)^*T_0/2, \\ (P_3N_3N_3)^*T_1/2, (P_3N_3N_4)^*T_2/2, (P_3N_4N_4)^*T_0/4.$$

4 Further Modified SVPWM (FMSVPWM) Technique

An FMSVPWM scheme is also recommended for SVM of nine-level inverter. This scheme again reduces the number of two-level hexagons to take part in realization of nine-level SVD. In this scheme, initially nine-level SVD is resolved



Fig. 12 Nine-level line voltage at different values of modulation index using **a** SPWM, **b** MSVPWM and **c** FMSVPWM techniques

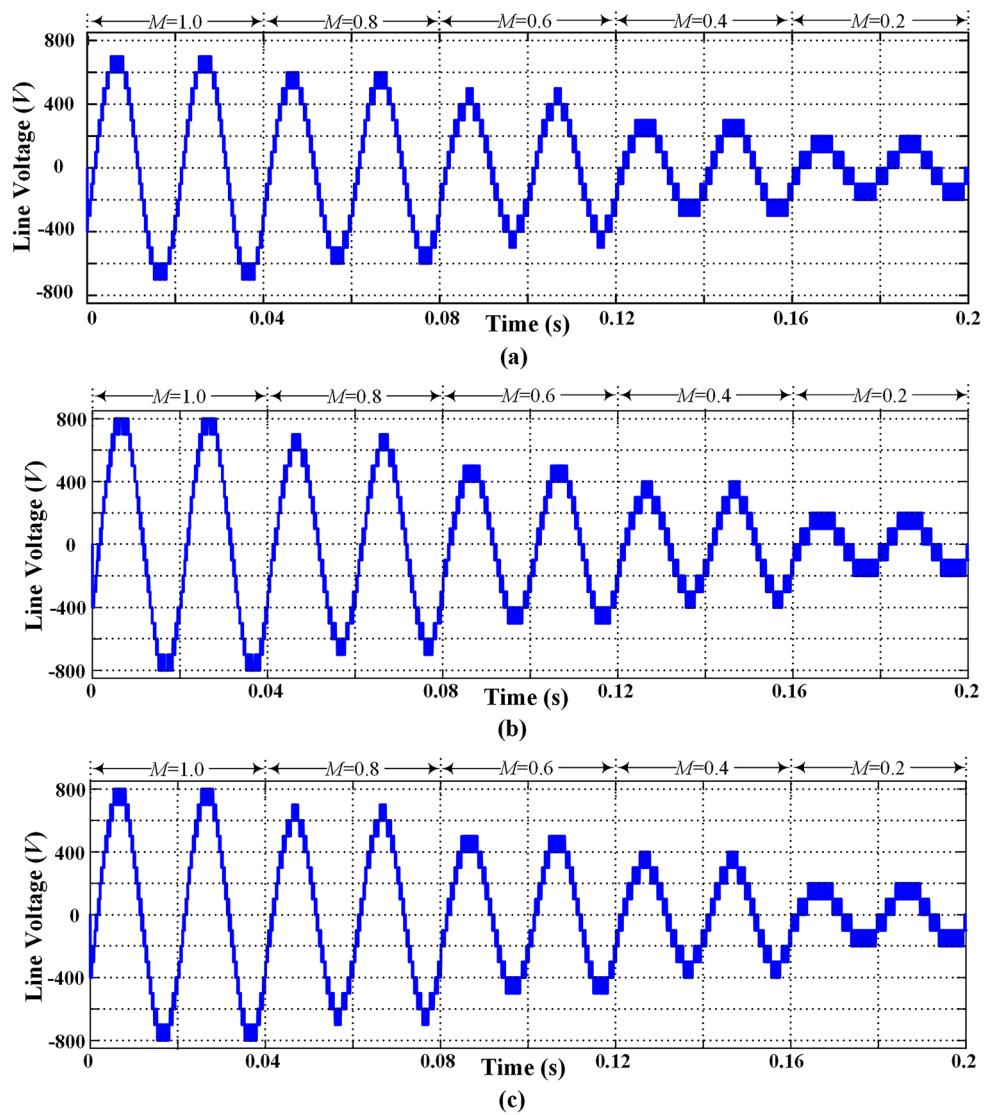


Table 9 Line voltage harmonic distortion at different modulation indices

Modulation index (M)	Line voltage harmonic distortion (%)		
	SPWM	MSVPWM	FMSVPWM
1.0	9.70	8.65	9.58
0.8	10.91	9.88	10.23
0.6	13.26	12.24	12.24
0.4	21.93	18.6	18.6
0.2	42.19	38.43	38.43

into 6 five-level hexagons as same as in MSVPWM technique and then each five-level is divided into 18 two-level hexagons. So, the numbers of two-level hexagons to be considering are reduced from 144 to 108 for nine-level SVM. The radius of a biggest circle which is inscribed in a hexagon is corresponds to the unity modulation index. The five-level

Table 10 Fundamental line RMS voltage value at different modulation indices

Modulation index (M)	Fundamental line rms voltage (V)		
	SPWM	MSVPWM	FMSVPWM
1.0	486.2	562.3	545.2
0.8	389.6	450.8	434.4
0.6	293.5	336.9	336.9
0.4	194.9	224.5	224.5
0.2	96.7	111.7	111.7

SVD with a circle is shown in Fig. 9. Even for unity modulation index, only 12 outer hexagons are taking part, and the dark shaded portion in the five-level SVD is left neglected. Hence, the number of two-level hexagons are considering is reduced to 108 for SVM of nine-level inverter. Suppose if the reference voltage lies in the dark shaded portion, then one



Table 11 Phase voltage harmonic distortion at different modulation indices

Modulation index (M)	Phase voltage harmonic distortion (%)	
	MSVPWM	FMSVPWM
1.0	21.23	22.17
0.8	25.88	26.59
0.6	30.37	30.37
0.4	39.70	39.70
0.2	67.71	67.71

Table 12 Phase current harmonic distortion at different modulation indices

Modulation index (M)	Phase current harmonic distortion (%)	
	MSVPWM	FMSVPWM
1.0	17.85	17.9
0.8	18.67	18.7
0.6	18.97	18.97
0.4	19.29	19.29
0.2	20.81	20.81

of the nearest outer hexagon is selected based on V_{ref2} and angle θ_2 . The selection of outer twelve two-level hexagons in a five-level SVD based on the value of V_{ref5} and angle θ_5 is shown in Table 7 and the selection of inner two-level hexagons are same as in MSVPWM technique. Compared to MSVPWM scheme, reduction in complexity is obtained by slightly increased in THD for modulation index greater than 0.77. If the modulation index less than or equal to 0.77, then both MSVPWM and FMSVPWM give the same results.

5 Simulation Results

Both MSVPWM and FMSVPWM techniques are applied to nine-level inverter and are simulated using MATLAB/SIMULINK. A star-connected three-phase RL-load and

three-phase induction motor (IM) are connected to the three-phase CHB inverter for analysing the load voltage and currents. The simulation results obtained from the proposed techniques are verified within phase disposition (IPD) SPWM technique. The parameters used for simulation are listed in the Table 8. Figure 10 shows the nine-level inverter phase voltage and phase current for different control strategies at the unity modulation index. The phase voltage across the load and its line voltage at various modulation indices using SPWM, MSVPWM and FMSVPWM techniques are shown in Figs. 11 and 12, respectively.

Table 9 gives the line voltage THD at different modulation indices for different modulation strategies. Table 10 gives the fundamental rms voltage value for different modulation strategies at different modulation indices. The harmonic distortion in phase voltages for different values of M

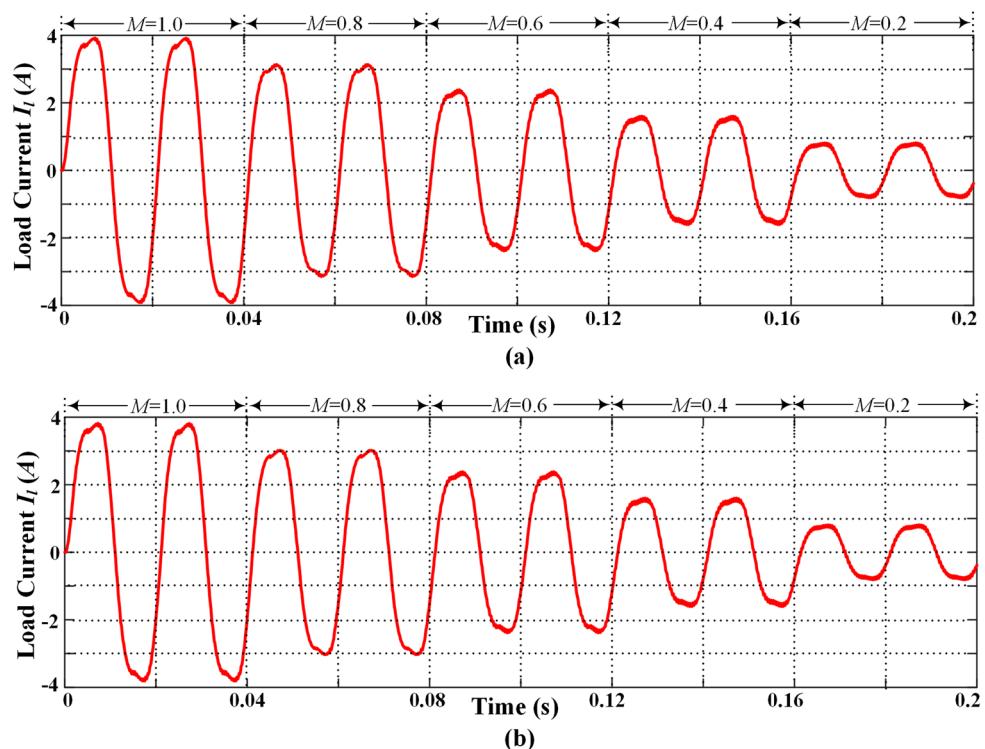
Fig. 13 Nine-level load current at different values of modulation index using **a** MSVPWM and **b** FMSVPWM techniques

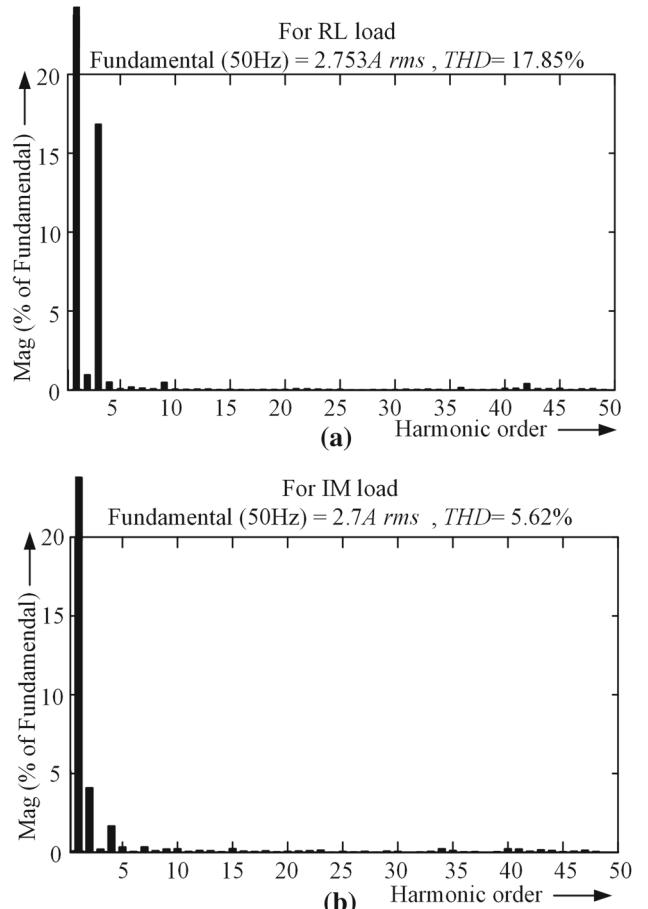
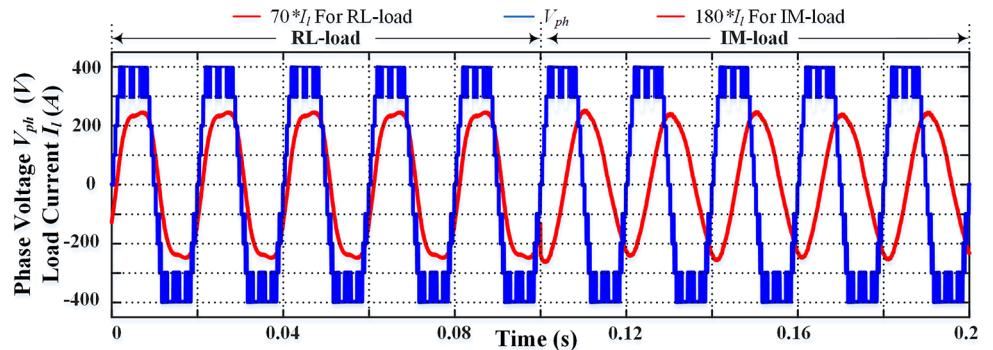
Table 13 Switching losses for three different modulation schemes

Modulation scheme	Switching losses (W)
SPWM	7.47
MSVPWM	5.96
FMSVPWM	6.24

using MSVPWM and FMSVPWM techniques are shown in Table 11. The load current at different values of modulation indices for the RL-load using MSVPWM and FMSVPWM techniques is shown in Fig. 13. Table 12 shows the load current harmonic distortion at different modulation indices using proposed techniques. Switching losses are calculated for different modulation techniques by incorporating the characteristics of IGBT from the datasheet [21] in the thermal model of IGBT. Table 13 shows the switching losses using SPWM, MSVPWM and FMSVPWM techniques. As the switching sequence pattern is designed in such a way that, there is only one leg change from one switching instant to the next switching instant, which reduces the switching frequency and then leads to reduction in switching losses. From Table 13, it is clear that the both the proposed modulation techniques produce lower switching losses compared to SPWM technique.

The reactance of the load assists in filtering out the harmonics, so that the nature of the load current waveform becomes nearly sinusoidal with a phase shift from the corresponding phase voltage with less THD. Figure 14 shows the nine-level inverter phase voltage and phase current at $M = 1$ using MSVPWM techniques for both RL-load and induction motor (IM) load. The harmonic spectra of load current for RL load and IM load are shown in Fig. 15a, b respectively. It is seen that the harmonic distortion in load current is high for RL load compared to IM load.

The effect of sampling frequency on the line voltage harmonic distortion is shown in Fig. 16, which shows that the harmonic distortion in the output voltage decreases with the increase in the sampling frequency. But if an inverter operates at a higher sampling frequency, then the inverter

Fig. 14 Nine-level phase voltage and phase current at unity modulation index using MSVPWM technique for dynamic load**Fig. 15** Frequency spectra at unity modulation index using a MSVPWM technique with **a** RL load and **b** induction motor load

produces higher switching losses, which is undesirable. So, it is recommended to operate the MLIs at an optimal sampling frequency.

6 Hardware Results

The experimental setup for the three-phase nine-level CHB inverter to validate the proposed SVPWM techniques is



Fig. 16 Effect of sampling frequency with respect to line voltage harmonic distortion

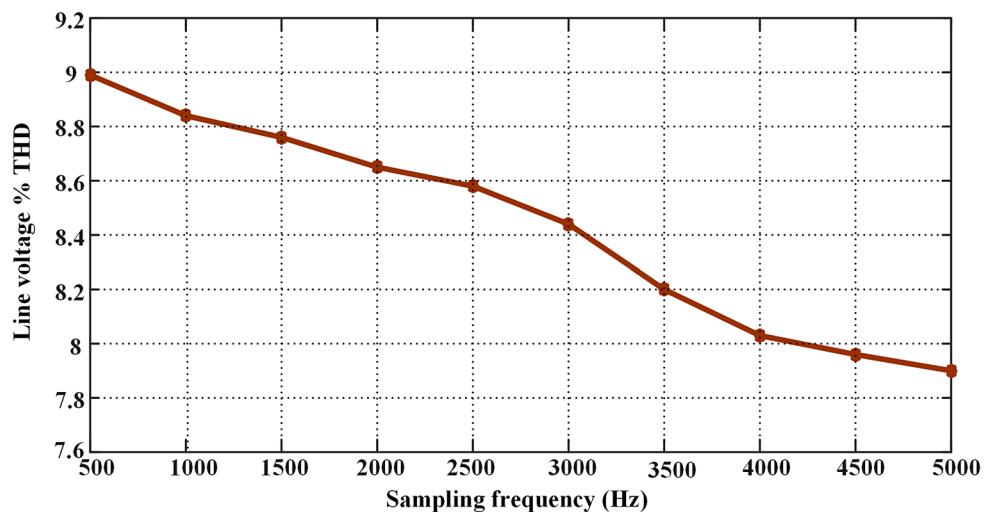
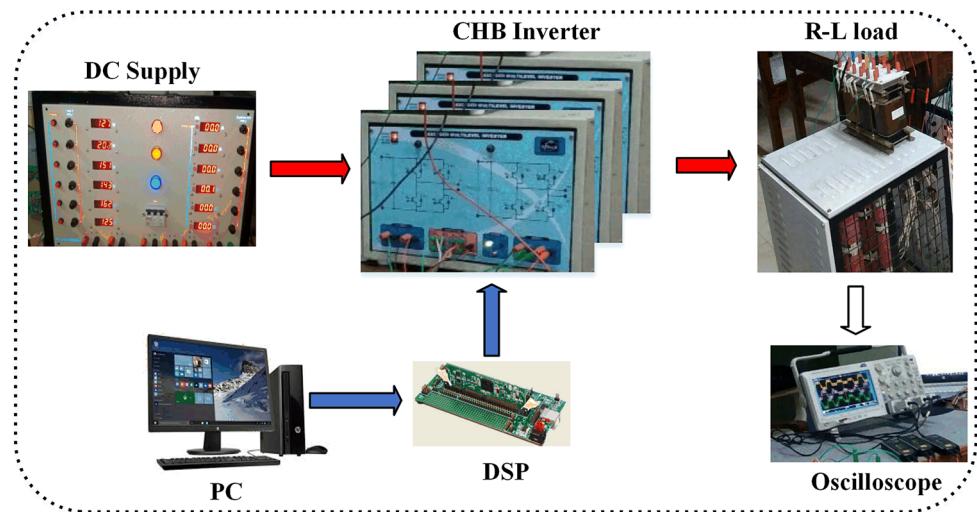


Fig. 17 Hardware setup



depicted in Fig. 17. Two different RL-loads are considered for the analysis; one is high-impedance load (HIL), and other is low-impedance load. (LIL) The load parameter values for high-impedance load are same as the load parameters considered for the simulation. Each H-bridge cell is excited with a DC source (E) of 50 V and sampling time (T_s) for the modulation techniques is 2100 s. The inverter gate pulses are generated by using DSP processor. The nine-level phase voltage, phase current and line voltage at unity modulation index using MSVPWM technique for HIL are shown in Fig. 18a–c, respectively. The line voltage at $M = 0.8$ using MSVPWM technique for HIL is shown in Fig. 19. The frequency spectra for nine-level phase and line voltage at unity modulation index using MSVPWM technique for HIL are shown in Fig. 20a, b, respectively.

The nine-level phase voltage and phase current at unity modulation index using FMSVPWM technique for HIL are as shown in Fig. 21a–c, respectively. The nine-level line voltage at $M = 1$ using FMSVPWM technique for HIL is shown in Fig. 21c. The nine-level line voltage at $M = 0.8$ using FMSVPWM technique for HIL is shown in Fig. 22. The frequency spectra for nine-level phase voltage at unity modulation index using FMSVPWM technique for HIL are shown in Fig. 23. The frequency spectrum for the current waveforms shown in Figs. 18b and 21b is shown in Fig. 24a, b, respectively.

The load current for low-impedance load is adjusted in such a way that it is ten times than the high-impedance load. The phase current at $M = 1$ using MSVPWM and FMSVPWM techniques for LIL is shown in Fig. 25. Its respective frequency spectrum is shown in Fig. 27. Similarly, the phase current at $M = 0.8$ for LIL using



Fig. 18 Experimental waveforms for nine-level CHB inverter at unity modulation index with HIL using proposed MSVPWM technique **a** phase voltage, **b** phase current and **c** line voltage

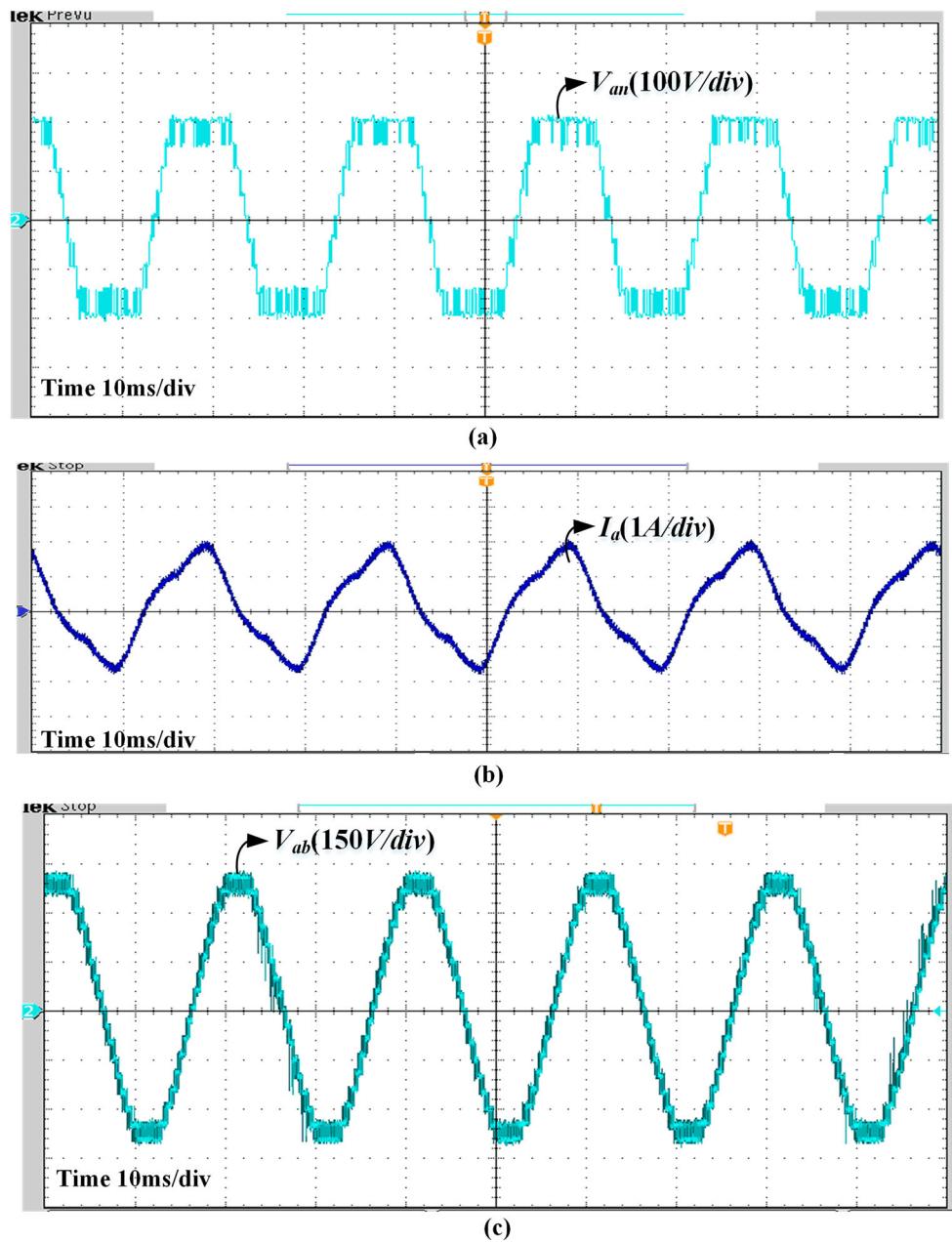
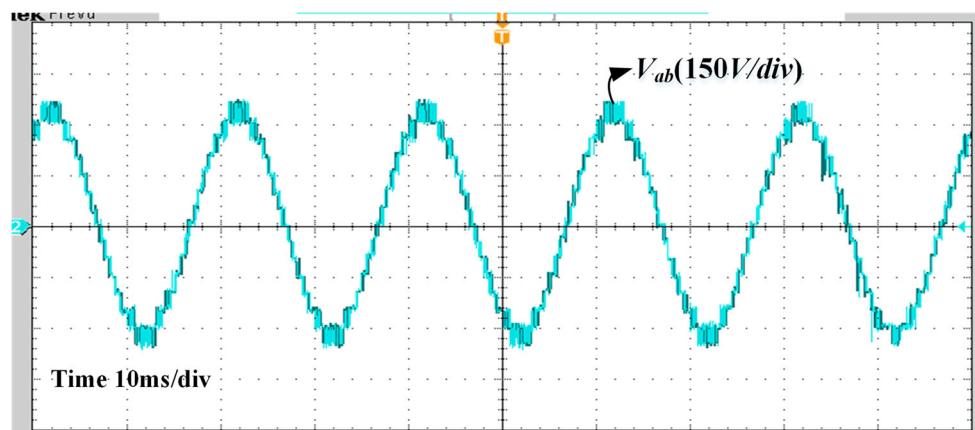


Fig. 19 Experimental waveform for nine-level CHB inverter at $M = 0.8$ with HIL using proposed MSVPWM technique



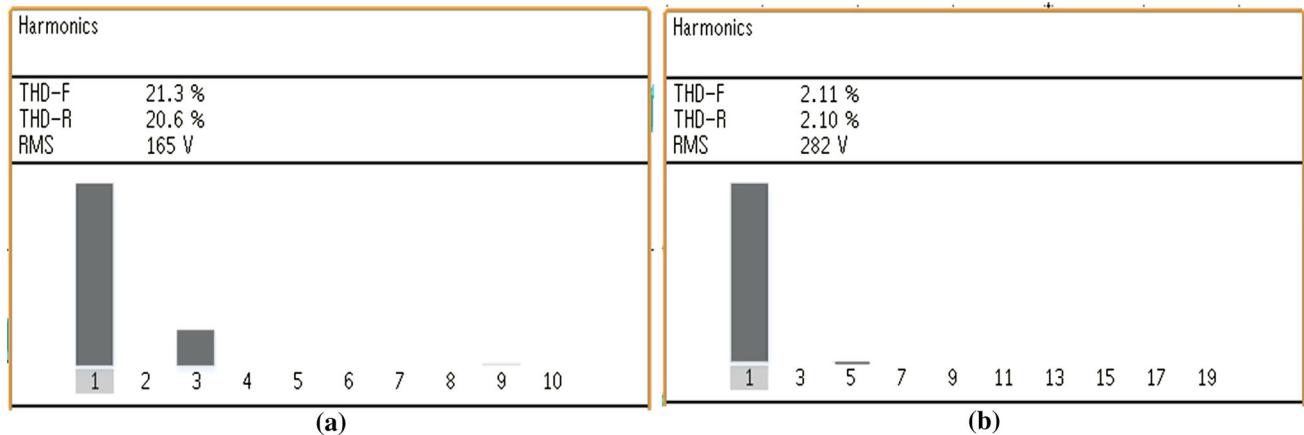
**Fig. 20** Frequency spectra at unity modulation index with HIL using MSVPWM technique **a** phase voltage and **b** line voltage

Fig. 21 Experimental waveforms for nine-level CHB inverter at unity modulation index with HIL using proposed FMSVPWM technique **a** phase voltage, **b** phase current and **c** line voltage

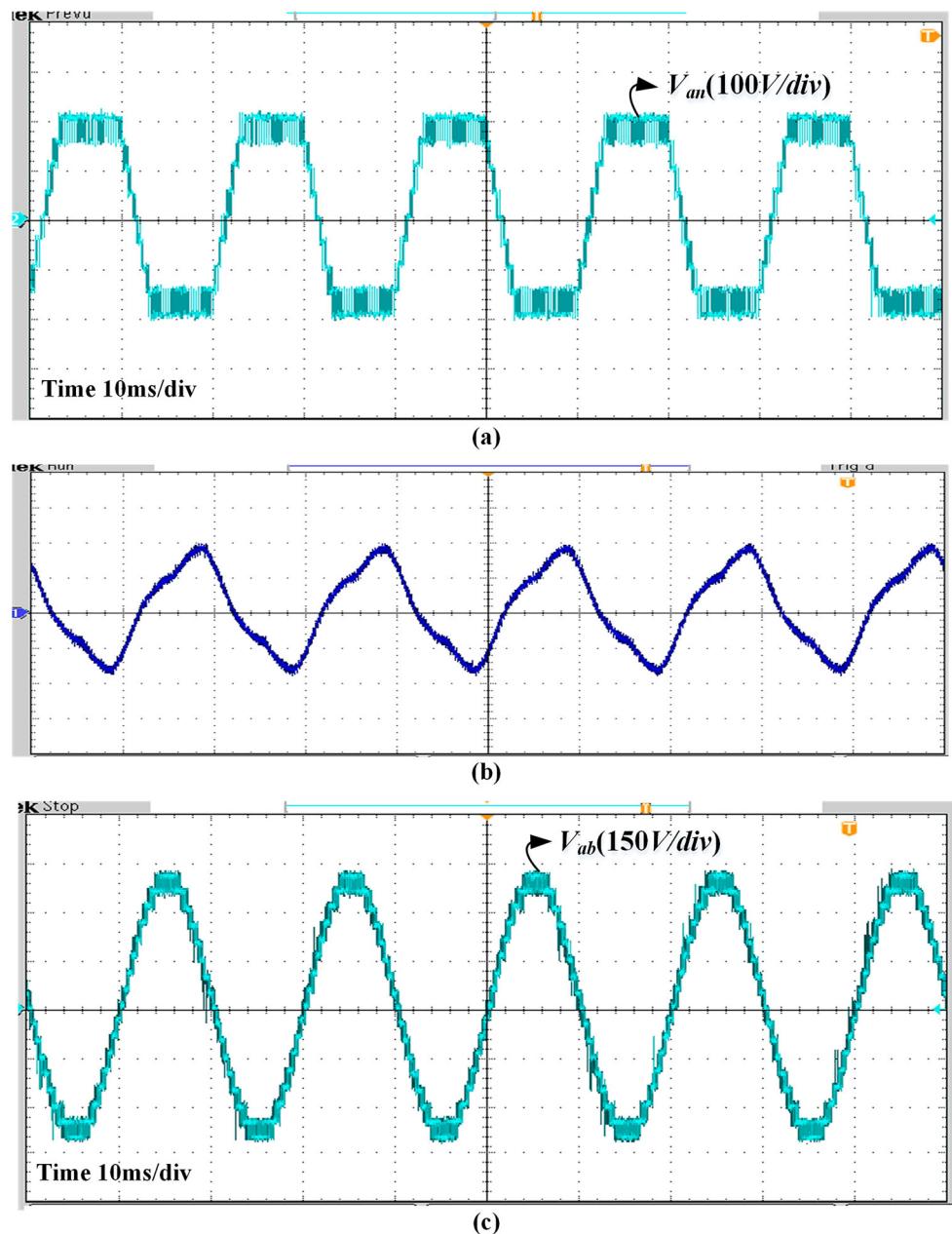


Fig. 22 Experimental waveform for nine-level CHB inverter at $M = 0.8$ with HIL using proposed FMSVPWM technique

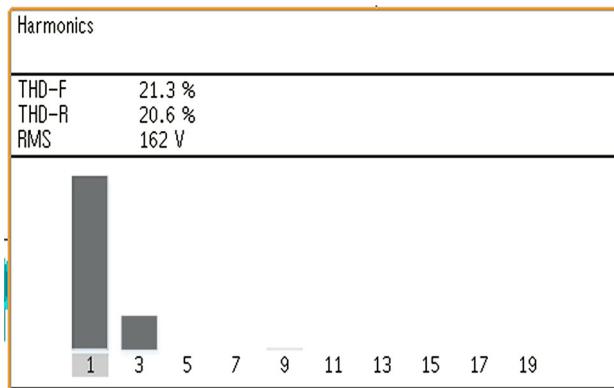
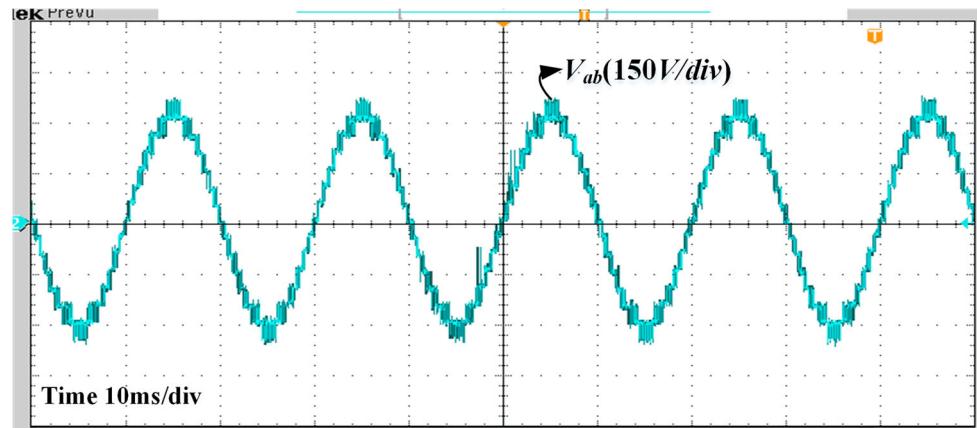


Fig. 23 Frequency spectra for phase at unity modulation index with HIL using FMSVPWM technique

MSVPWM and FMSVPWM techniques is shown in Fig. 26. Its respective frequency spectrum is shown in Fig. 28. It is obvious that the THD of load current for LIL is lower compared to high-impedance load. Thus, the obtained results

for HIL are quite similar than the results obtained from simulation.

7 Conclusion

The proposed MSVPWM techniques greatly reduce the computational burden and the system memory requirements by minimizing the number of two-level hexagons to be considered from 1296 to 144 in order to realize the SVPWM of nine-level inverter. This technique is reliable to any inverter topology, and it can be generalized for any inverter levels. And also FMSVPWM scheme is presented, which again reduces the count of two-level hexagons to be considered to realize nine-level SVM from 144 to 108. Simulation analyses have been done on nine-level CHB inverter at different modulation indices and are compared with carrier-based SPWM technique. The proposed SVPWM schemes gives lower harmonic distortion and higher DC bus utilization. Experimental results are also presented to validate the proposed SVPWM

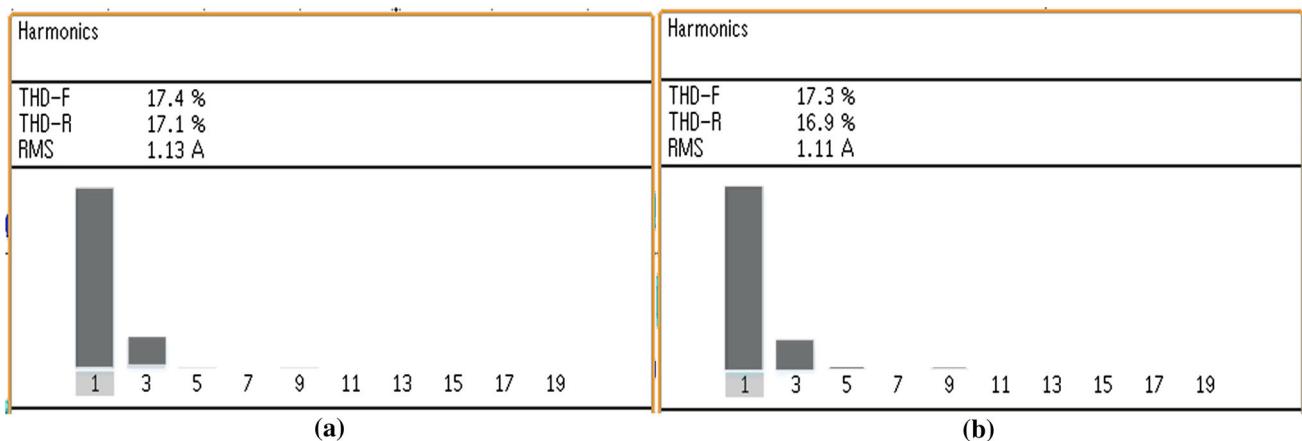


Fig. 24 Load current frequency spectra at unity modulation index with HIL using **a** MSVPWM and **b** FMSVPWM techniques



Fig. 25 Nine-level load current at unity modulation index with LIL using **a** MSVPWM and **b** FMSVPWM techniques

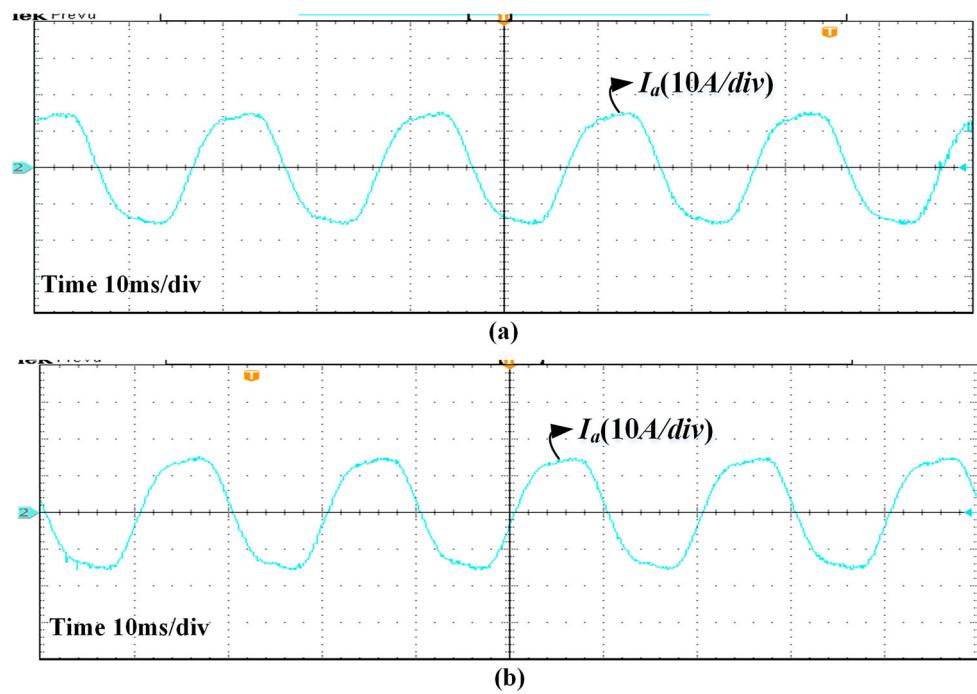
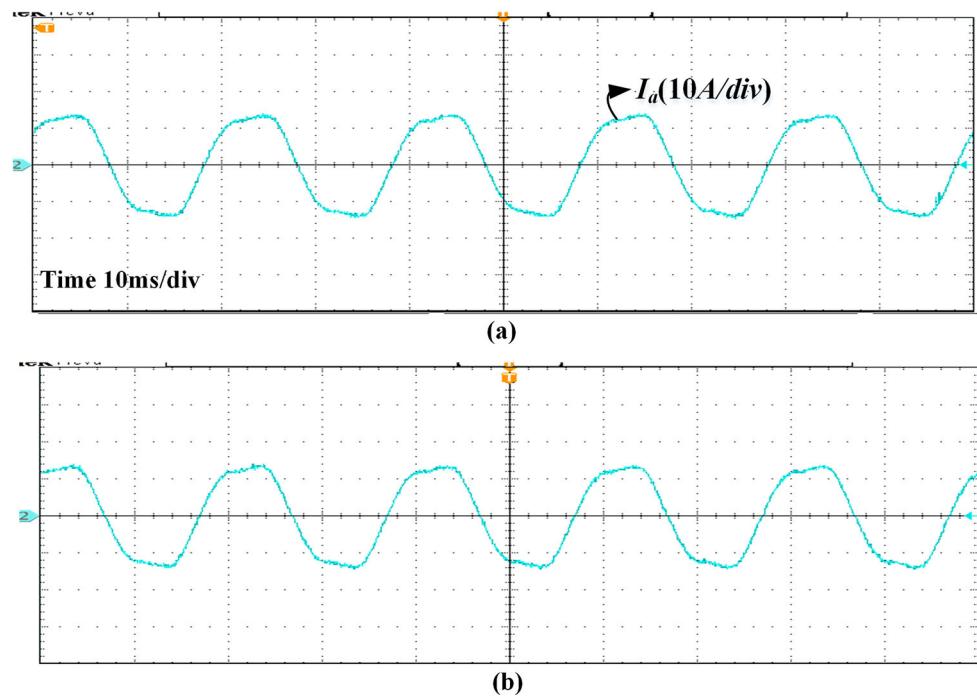


Fig. 26 Nine-level load current at 0.8 modulation index with LIL using **a** MSVPWM and **b** FMSVPWM techniques



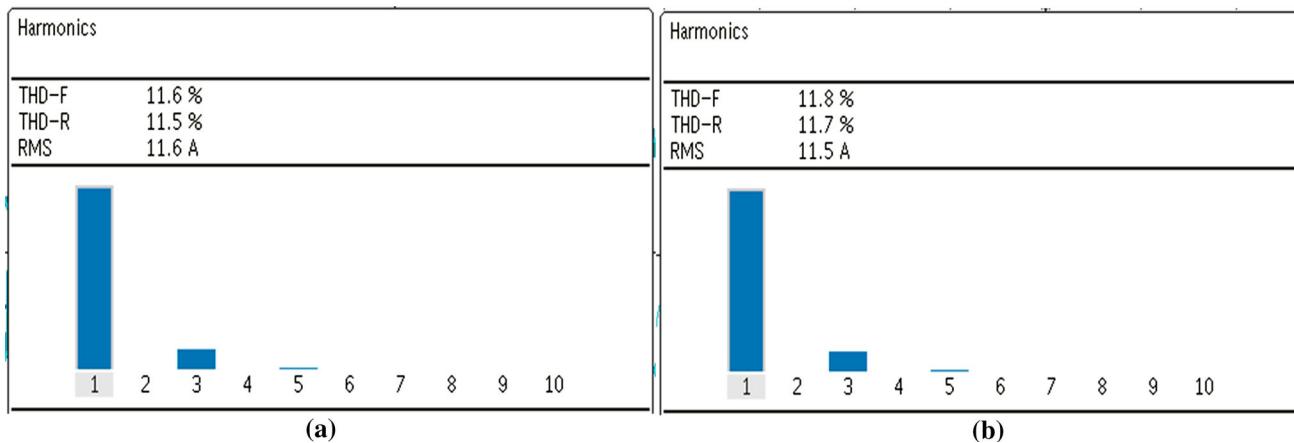


Fig. 27 Load current frequency spectra at unity modulation index with LIL using **a** MSVPWM and **b** FMSVPWM techniques

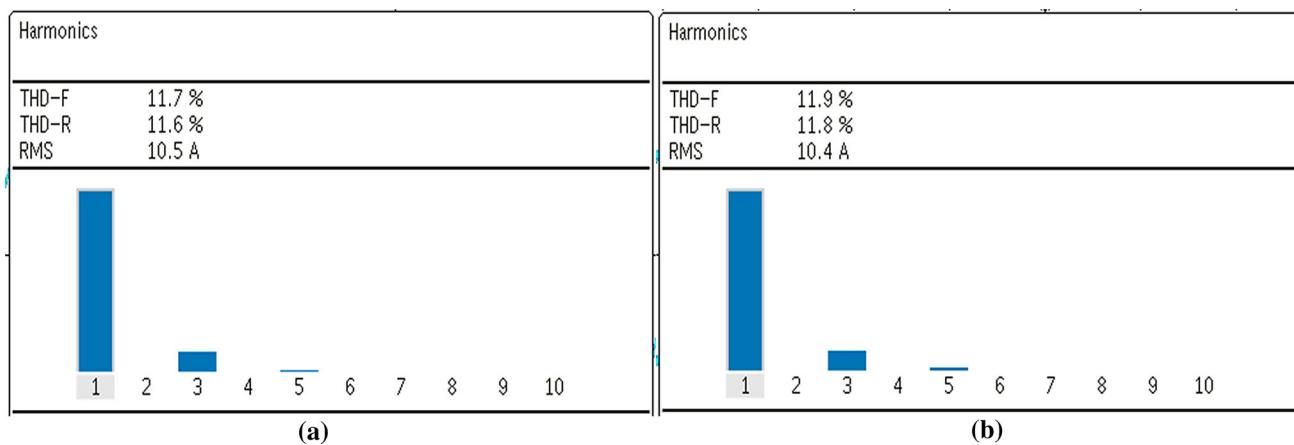


Fig. 28 Load current frequency spectra at 0.8 modulation index with LIL using **a** MSVPWM and **b** FMSVPWM techniques

control strategies. Both simulation and hardware results are presented at the different load conditions. Thus, the proposed two SVPWM techniques give the satisfactory results by reducing the complexity in realization of SVPWM for multilevel inverters.

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