# Optimization of WiFi Communication System using Low Power Ring Oscillator Delay Cell

Kh Shahriya Zaman
*Department of Electrical, Electronic and Systems Engineering*
*University Kebangsaan Malaysia*
Bangi, Malaysia
kh.shahriya.zaman@gmail.com

Mamun Ibne Reaz
*Department of Electrical, Electronic and Systems Engineering*
*University Kebangsaan Malaysia*
Bangi, Malaysia
mamun@ukm.edu.my

Fahmida Haque
*Department of Electrical, Electronic and Systems Engineering*
*University Kebangsaan Malaysia*
Bangi, Malaysia
fahmida32@yahoo.com

Norhana Arsad
*Department of Electrical, Electronic and Systems Engineering*
*University Kebangsaan Malaysia*
Bangi, Malaysia
noa@ukm.edu.my

Sawal Hamid Md Ali
*Department of Electrical, Electronic and Systems Engineering*
*University Kebangsaan Malaysia*
Bangi, Malaysia
sawal@ukm.edu.my

***Abstract*— Modern systems rely on wireless communication for data transmission and system control. Power dissipation and circuit area are crucial factors for such communication systems in portable devices. Ring oscillators are the popular choice for voltage-controlled oscillator (VCO) architecture for Phase locked loop (PLL). This is because ring oscillators exhibit wider tuning range and consume less area on chip. This paper presents a low power ring oscillator designed for wireless application at 5 GHz in the ISM band. A 3-stage starved current voltage-controlled ring oscillator was implemented with 0.13 µm CMOS technology using ELDO Spice simulator from Mentor Graphics. With supply voltage of 1.2V, the power dissipation is 1.08 mW and the phase noise is -78 dBc/Hz at 1 MHz additionally, the proposed ring oscillator with new delay cell layout size occupied 7.1 by 11.7 µm$^2$.**

***Keywords*— ring oscillator, starved current, voltage-controlled oscillator, low power, phase noise***

## I. Introduction

Every wireless technology from cell phones to automatic gate uses radio frequency to communicate. Many devices share frequencies that cause interference as they transmit or receive signal among them [1]. The demand for high frequency processor with low power consumption is increase rapidly [2]-[5]. Short range wireless communication is held by Wi-Fi which are corresponding to the IEEE 802.11a and 802.11b work around 5 GHz and 2.4 GHz respectively. Nowadays, 5 GHz band used in the Wi-Fi networks for media streaming and transferring music, picture and video to help address the digital noise that come with the signal [6, 7].

In the wireless communication system, VCO plays an important role in the RF subsystem [8]. VCO use to generate local oscillator frequency to up convert and down convert the input signal. Low phase noise, low power consumption and high frequency swing are the desired characteristic need to have in the VCO design. The ring oscillator and the LC oscillator are the two types of architectures for VCO. The core of VCO is utilizes an inverter-type ring oscillator, which is supplied by a current from the voltage-to-current converter.

In terms of performance, ring oscillators are better than relaxation oscillators. Although relaxation oscillators attain wider tuning range, they are less power efficient. The LC oscillator consume large area in a die, it has low tuning range and the phase noise performance is depending on the quality factor. Thus, ring oscillator is preferable to be used in due to their compact size, digital compatibility and ease of porting.

In this paper, a 3-stage ring oscillator has been proposed in 0.13µm CMOS technology process using Mentor Graphic simulation software. The ring oscillator is designed for 5 GHz operating frequency with low power dissipation that improved the performance of the device. Besides, the circuit enhanced its phase noise performance and the area occupied is reduced significantly.

## II. Methodology

Basically, there are many types of delay cells, that can be implemented in the ring oscillator circuit. Some designers used starved current, differential and source follower delay cells depending on the critical parameter that they considered in their design. In this work, the starved current ring oscillator is adopted due to several reasons. This circuit with starved delay cell provides better frequency linearity, where the frequency is dependent on device parameter and process [9, 10]. This topology is widely used as the tuning range and power efficiency of the current starved ring oscillator can be improved due to the delay cell used. Minimum value of voltage supply and the current tail used in this type of circuit in order to achieve low power consumption. In addition, the implementation of his circuit is simpler compare to other circuits.

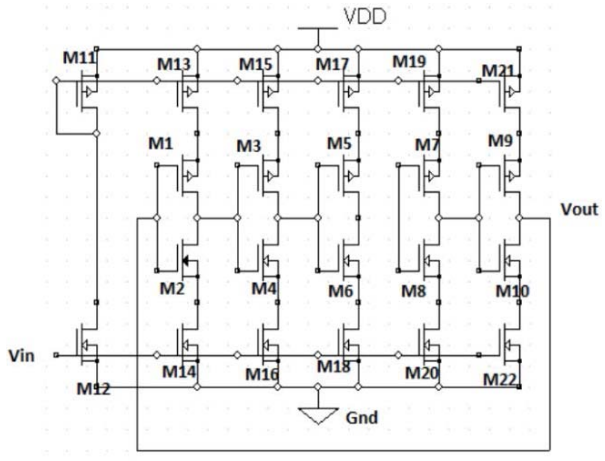


Fig. 1. Schematic diagram for the voltage-controlled ring oscillator based on current starved delay cell [11].

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### A. Current Starved Delay Cell

The supply voltage (VDD) to a ring oscillator circuit fluctuates in real time. This voltage fluctuation also affects the output frequency. Thus, supply current at each inverter ensures that the stability of the output frequency. A current starved delay cell being utilized in a voltage-controlled ring oscillator is shown in Fig. 1. The design contains 5 stages of ring oscillator, where the NMOS transistor are used as current sources and the PMOS transistors are used in the delay cell. Current limiter circuits (M1 and M2) are necessary in such structure in order to limit the PMOS inverter current. This implementation with delay cells improves the tuning range, increases the frequency linearity and decreases the power consumption of the circuit [10].

### B. Proposed Starved Current Ring Oscillator

Initially, a 3 stages ring oscillator is used to estimates the oscillation frequency. The output frequency is unstable when the ring oscillator circuit solely depend on voltage supply, VDD. This is because when the voltage supply of 1.2 V varies by ±10%, the output frequency may vary. Hence, current is introduced to each inverter instead of $V_{DD}$ to overcome this problem. A schematic of the voltage-controlled ring oscillator containing current starved delay cell is illustrated in Fig. 2. Each delay cell was connected with PMOS and NMOS transistors whereby its supply current to each inverter instead of $V_{dd}$. Hence, it stabilize the output frequency as the ring oscillator is not independent to $V_{dd}$ supply voltage. For instance, M7 and M8 transistor was connected at the first stage of the inverter (M1 and M2) and they act as current source to M1 and M2. At this point, the inverter is said to starved for current as M7 and M8 limit the current go through M1 and M2. M13 and M14 are act as current mirrored and was set by input control voltages. The current mirrored is supplied to each of the current source stage.

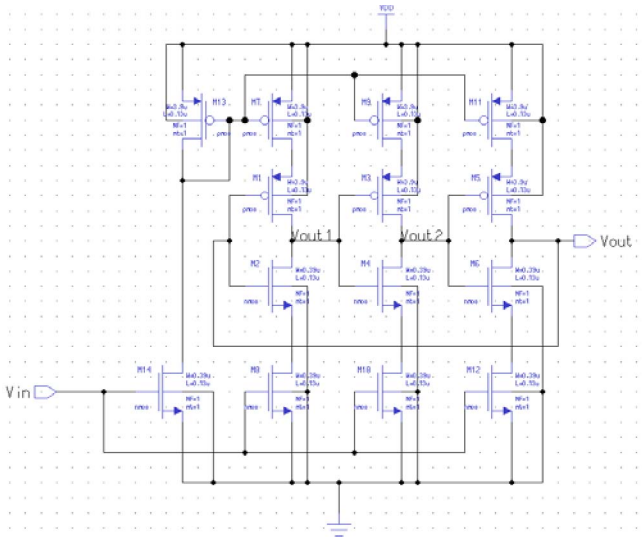


Fig. 2. The schematic of ring oscillator with starved current circuit.

## III. Results and Comparison

The proposed starved current ring oscillator is designed in 0.13 µm TSMC CMOS technology and performance of the circuit is validated using ELDO Spice simulator of Mentor Graphic software. The frequency is set at 5 GHz at room temperature. For the improvement, the voltage control of the proposed circuit, is set to be very low. Fig. 3 shows the output frequency waveform of the proposed circuit with new delay cell at an input control voltage 1.2 V. The nominal oscillation frequency is 4.9139 GHz presents the oscillator start-up due to parasitic capacitance [12]. This proposed circuit gives low power dissipation where the value is 1.088 mW as is one of the most important criteria in VCO design for wireless communication application. However, the phase noise obtained from this proposed circuit is -78 dBc/Hz at 1 MHz as present in Fig. 4. This value is almost close to the acceptable range, which is within -107 to -110 dBc/Hz when using 1 MHz offset frequency with around 0.95 Vpp single ended voltage swing, as reported in [13].

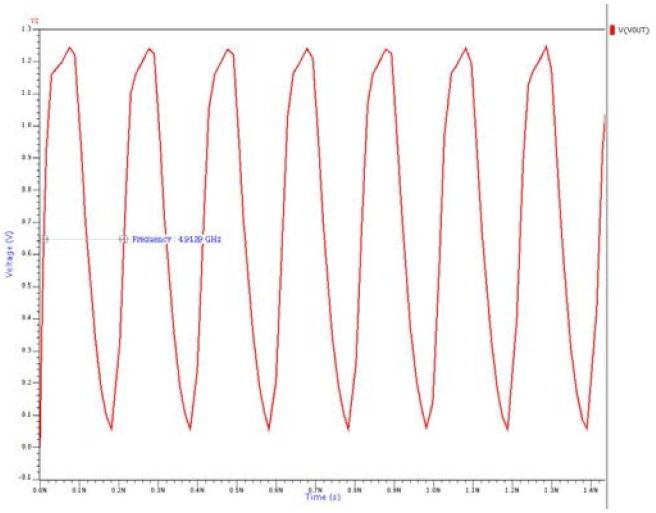


Fig. 3. The output frequency waveform of proposed circuit.

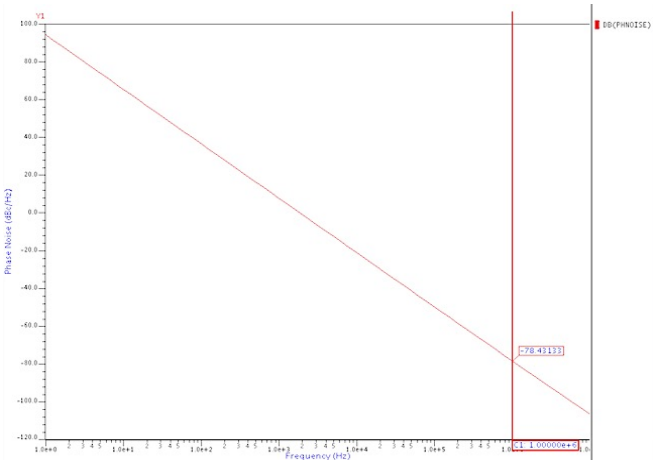


Fig. 4. The output phase noise of the proposed circuit.

In addition, the tuning frequency of the proposed circuit from 1.25 to 4.92 GHz with a tuning voltage from 0.6 to 1.2 V and is said to be linear as illustrated in Fig. 5. The output frequency is increased up to 4.92 GHz as the control voltage of the current increased through the inverter and by fixing the control voltage for the resistance and capacitances. As mentioned earlier, IEEE 802.11a protocol operate at 5 GHz and the proposed VCRO works reliably on this frequency range.

The layout of the proposed circuit is presented in figure 6 and the area consume for the core layout is approximately 7.1 × 11.7 µm$^2$. Table I tabulated the performance comparison of various VRO with different implementation. It is observed

that the proposed circuit has low power dissipation with the same power supply of 1.2 V and wide frequency rage.

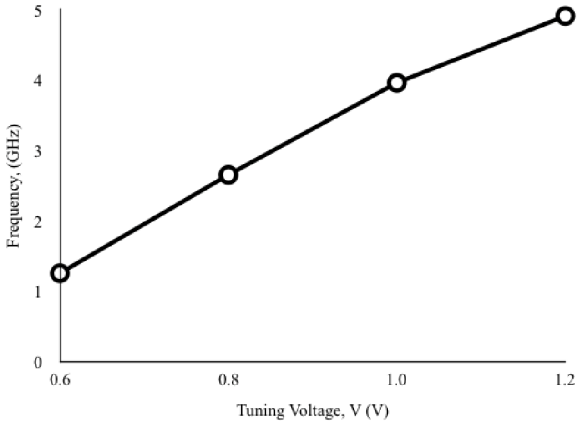


Fig. 5. Simulated voltage tuning versus oscillation frequency.

TABLE I. SUMMARY RESULTS OF CURRENT STARVED RING OSCILLATOR PERFORMANCE AND COMPARISON WITH OTHER WORKS.

| [Reference] (Technology) | Frequency (MHz) | Supply Voltage (V) | Power Dissipation (mW) | Phase Noise (dBc/Hz) | VCO Type |
|---|---|---|---|---|---|
| This work (0.13 µm) | 5000 | 1.2 | 1.088 | -78 @ 1 MHz | RO |
| [14] (0.13 µm) | 10000 | 1.2 | 3.182 | | RO |
| [15] (0.13 µm) | 640 - 650 | 1.2 | 1.44 | -96 @ 100 kHz | LC |
| [16] (0.13 µm) | 402 - 405 | 0.65<br>1 | 0.65<br>1 | -111@ 1 MHz<br>-127 @ 1 MHz | LC |
| [17] (0.13 µm) | 28.24 - 358.88 | 1.3 | 0.591 | -118 @ 1MHz | RO |

## IV. CONCLUSION

This paper presented a 3 stages current starved ring oscillator simulated in ELDO Spice simulator (Mentor Graphic). This circuit was designed with oscillation frequency of 5 GHz and low power consumption as presented in Table I. Thus, this proposed circuit is suitable to work with IEEE 802.11a protocol. On the other hand, the layout of the ring oscillator is designed using 0.13 µm CMOS technology and the area consumption of this layout is about 7.09 x 11.0 µm$^2$ as illustrated in Fig. 6.

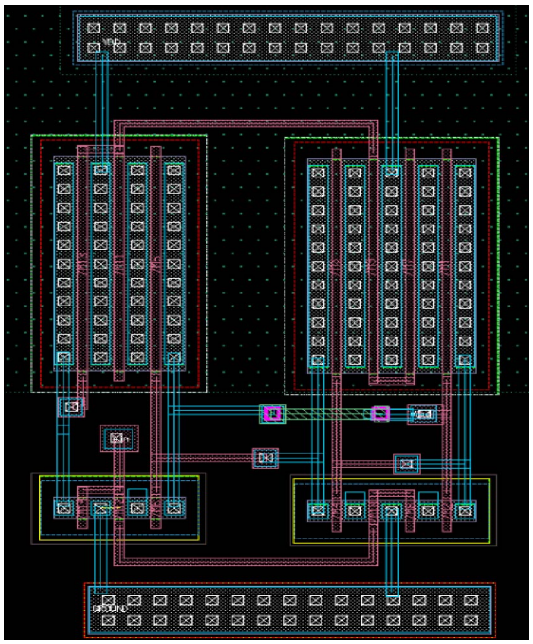

Fig. 6. The layout of proposed circuit.

## ACKNOWLEDGMENT

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## REFERENCES

[1] D. M. M. Rahaman, M. S. Islam, J. Sampe, and S. H. M. Ali, "An architecture of ULP energy harvesting power conditioning circuit using piezoelectric transducer for wireless sensor network: A review," Asian Journal of Scientific Research, vol. 8, no. 1, p. 1, 2015.

[2] J. Uddin, M. B. I. Reaz, M. A. Hasan, A. N. Nordin, M. I. Ibrahimy, and M. A. M. Ali, "UHF RFID antenna architectures and applications," Scientific Research and Essays, vol. 5, no. 10, pp. 1033–1051, 2010.

[3] Y. Mohd, M. K. Khaw, and M. B. I. Reaz, "Radio frequency identification: Evolution of transponder circuit design," Microwave Journal, vol. 49, no. 6, p. 56, 2006.

[4] K. H. Yeo, S. H. M. Ali, P. S. Menon, and M. S. Islam, "Comparison of CMOS rectifiers for micropower energy harvesters," in 2015 IEEE Conference on Energy Conversion (CENCON), 2015, pp. 419–423.

[5] A. M. Moubark, M. A. Mohd Ali, H. Sanusi, and S. M. Ali, "FPGA implementation of low power digital QPSK modulator using verilog HDL," JApSc, vol. 13, no. 3, pp. 385–392, 2013.

[6] M. B. I. Reaz, F. Mohd-Yasin, S. L. Tan, H. Y. Tan, and M. I. Ibrahimy, "Partial encryption of compressed images employing FPGA," in 2005 IEEE International Symposium on Circuits and Systems, 2005, pp. 2385-2388 Vol. 3, doi: 10.1109/ISCAS.2005.1465105.

[7] M. B. I. Reaz, F. Choong, and F. Mohd-Yasin, "VHDL modeling for classification of power quality disturbance employing wavelet transform, artificial neural network and fuzzy logic," Simulation, vol. 82, no. 12, pp. 867–881, 2006.

[8] M. Hsu and P. Chen, "5GHz Low Power CMOS LC VCO for IEEE 802.11a Application," in Proceedings of the Asia-Pacific Microwave Conference 2011, pp. 263–266, 7-10 Dec. 2010, Yokohama.

[9] M. Kulkarni and K. Hosur, "Design of a Linear and Wide Range Current Starved Voltage Controlled Oscillator," International Journal Cybern. Informatics (IJCI), vol. 2, no. 1, pp. 23–30, 2013.

[10] M. Bhardwaj and S. Pandey, "Design and performance analysis of wideband CMOS Voltage Controlled Ring Oscillator," in Electronics and Communication Systems (ICECS), 2015 2nd International

Conference on, 2015, no. ICECS 2015, pp. 142–145, 26-27 Feb. 2015, Coimbatore.

[11] Z. Kazemi, M. Bin, I. Reaz, and F. H. Hashim, "Low Power Five Stage Current Starved Voltage Controlled Oscillator in 0.18µm CMOS Technology towards Green Electronics," in International Conference on Advances in Science, Engg., Technology & Natural Resources (ICASETNR-15), 2015, pp. 27–29, 27-28 Aug., 2015 Kota Kinabalu.

[12] N. Bako and A. Baric, "A low-power, temperature and supply voltage compensated current starved ring oscillator," Microelectronics Journal, vol. 44, no. 12, pp. 1154–1158, 2013.

[13] H. Li, S. Member, and H. Rein, "Millimeter-Wave VCOs With Wide Tuning Range and Low Phase Noise, Fully Integrated in a SiGe Bipolar Production Technology," IEEE Journal Solid-State Circuits, vol. 38, no. 2, pp. 184–191, 2003.

[14] F. Taghizadeh-Marvast, M. A. Mansouri-Birjandi, and M. J. Taghizedeh-Marvast, "10 GHz Voltage Controlled Ring Oscillator for High Speed Application in 130nm CMOS Technology," Australian Journal Basic Appl. Sci., vol. 6, no. 8, pp. 17–22, 2012.

[15] A. Italia and G. Palmisano, "A 1.2-mW CMOS Frequency Synthesizer with Fully-Integrated LC VCO for 400-MHz Medical Implantable Transceivers," in 2009 IEEE Radio Frequency Integrated Circuits Symposium, 2009, pp. 333–336, 7-9 June 2009, Boston, MA.

[16] T. Khan and K. Raahemifar, "A Low Power Current Reused Quadrature VCO for Biomedical Applications," in 2009 IEEE International Symposium on Circuits and Systems, 2009, pp. 669–672, 24-27 May 2009, Taipei.

[17] V. J. Patel and M. L. Patel, "Low Power Wide Frequency Range Current Starved CMOS VCO in 180nm, 130nm and 90nm CMOS Technology," International Journal of Engineering Research and Development, vol. 7, no. 4, pp. 80–84, 2013.