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A Portable GPS Signal Simulator Design Based on ZYNQ

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***Abstract*—Aiming at the problems of a large volume, high price, and complex operation of traditional global positioning system (GPS) signal simulator, a low-cost and portable GPS signal simulator based on ZYNQ is designed, which can simulate and generate multiple satellite signals. Compared with the common digital signal processing (DSP) and field programmable gate array (FPGA) combination technical solutions, ZYNQ adopts ARM + FPGA mode. In this mode, ARM and FPGA can achieve efficient coupling through an advanced extensible interface (AXI) on-chip bus interface, with a faster communication speed and more stable data transmission. The ARM module is responsible for receiving the scene information sent by the host computer as the information processing part, and generating the navigation message in the real time. The FPGA module is used as the signal processing part to process the data of multiple satellites in parallel. The intermediate frequency (IF) signal is modulated by the direct digital synthesis (DDS) technology and sent to the digital-analog converter (DAC) to generate the analog IF signal. The experimental results show that the GPS L1 frequency satellite signal is successfully simulated, and the error between the positioning coordinates and the preset coordinates is within a reasonable range, which verifies the feasibility of the design scheme.**

Keywords-component; Signal simulation; GPS signal; ZYNQ

I. INTRODUCTION

GPS signal simulator is a kind of test equipment to simulate satellite navigation signal. At present, the design of simulator is generally divided into pure software realization and hardware and software cooperative realization. In a pure software implementation, data and signals are simulated by MATLAB, System view, and other scientific computing software. The advantage is that the data are controllable and adjustable, easy to modify and update. However, the data are all controlled by the computer, there are higher requirements for the computer's memory and central processing unit (CPU) performance [1]. Cooperative implementation of software and hardware is the current mainstream implementation scheme, the outstanding advantage is that it can generate analog signals in real time, and compared with pure software implementation, it does not need to reconfigure every time, and can complete long-term simulation test. However, there are strict requirements for signal timing alignment, and the overall design is more complex [2]. The GPS signal simulator proposed in this paper belongs to the hardware and software cooperative realization scheme.

In the software and hardware co-design scheme, [3] proposed a dual-mode signal simulator design for GPS and BeiDou navigation satellite system based on "CPU+GPU", which reduced the requirements of sampling rate and the time cost of simulation. However, graphic processing unit (GPU) had high requirements for the computer graphics card, so it was not universal. [4] proposed a Galileo / GPS signal simulator design based on the "DSP+FPGA" architecture. The algorithm had adjustable initial parameters, good real-time performance, and a fast calculation speed. What was not good enough was that the DSP system need to use a special high-performance processing engine to calculate specific satellite signal parameters, so that when DSP cooperated with FPGA, it needed to call the customized processing engine and application programming interface (API). The performance was limited by the input/output (I/O) interface, which limited the comprehensive processing ability of the composite system to a certain extent. [5] proposed a multi-channel data analogy acquisition algorithm based on "ARM+FPGA", which had low cost and high stability. However, the communication interface between ARM and FPGA was complex, the interconnection bandwidth was limited, and the overall hardware design was difficult.

To solve these problems, this paper proposes a portable GPS signal simulator based on an "ARM+FPGA" programmable system on a chip of ZYNQ. ZYNQ-7000 chip with relatively smaller resources is selected, which includes two parts: a program system (PS) and a program logic (PL). The two parts are connected through the advanced extensible interface, AXI bus is integrated into a single chip. The high-performance standard AXI interface makes the communication bandwidth of PS and PL higher and the data transmission efficiency higher. The advanced microcontroller bus architecture (AMBA) interconnection mechanism also ensures that there will be no I/O bottleneck problem that reduces the system performance. Besides, PS supports multiplexed I/O (MIO), and the interface is flexible, which reduces the difficulty of hardware design.

II. SYSTEM DESIGN

A. System structure

The whole GPS signal simulator consists of a baseband part and a radio frequency (RF) part [6]. The baseband part is mainly composed of ZYNQ and DAC modules. Among them,
the ARM module is mainly used to select visible stars, generate navigation data, calculate data parameters, control parameters, time delay, and Doppler shift, etc. In addition, it needs to send updated information to FPGA in real time. FPGA module generates IF signal based on the data provided by ARM. RF part is composed of local oscillator module, modulation module, and attenuation channel. Actually, the original RF signal is usually not needed, only the baseband signal is used for data

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processing and analysis, to verify the accuracy and effectiveness of the design. Therefore, this paper focuses on the ARM and FPGA modules of the baseband. The overall framework of the system is shown in Fig. 1.

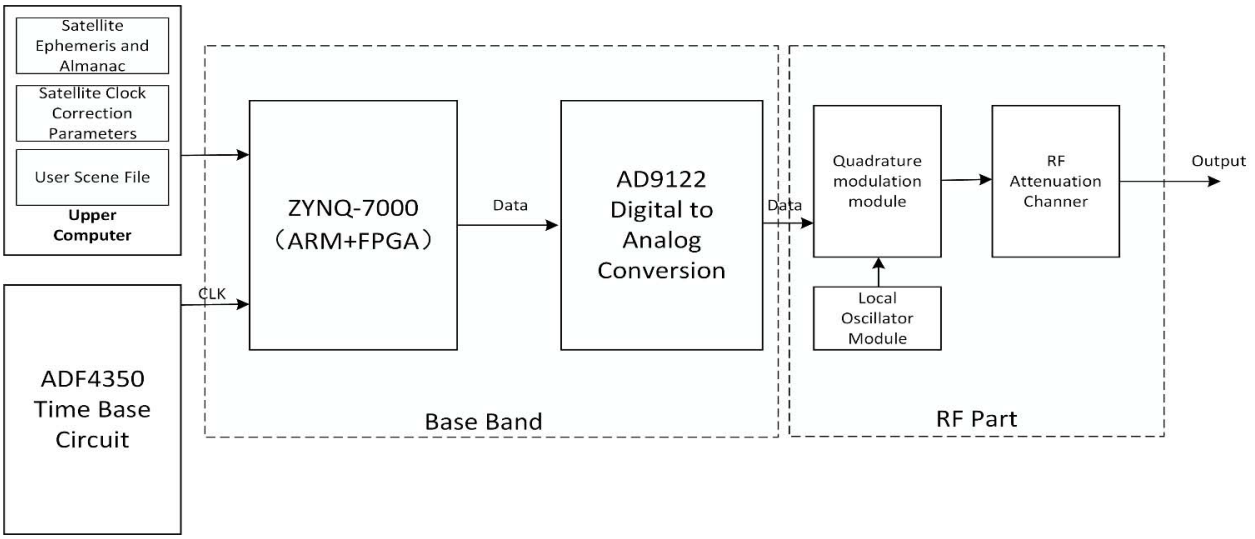

Fig. 1. System Architecture

The operation process of the system is as follows: First of all, the host computer configures the scene file and sets the user trajectory, satellite ephemeris, almanac data and other data. The scene file contains parameters such as signal simulation time, local time, user location, and other parameters. Then start ZYNQ to complete the initialization of basic modules such as memory management unit (MMU), phase locked loop (PLL), general interrupt unit (GIC), and internal interrupts [7]. The ARM begins to process the information sent by the upper computer, analyzes the satellite ephemeris and almanac, gets the approximate position value of the simulated satellite, calculates the relative elevation value with the user's position, selects the visible satellite according to the set elevation threshold value. According to the specification of the satellite interface control file, the navigation message is provided to FPGA as data parameter. At the same time, it is necessary to calculate the time delay values and Doppler frequency of each satellite according to the position information of the selected satellites and generate the control parameters required by the FPGA. After receiving the data parameters and control parameters provided by ARM through data ping-pong operation, FPGA generates a digital IF signal by DDS, which is converted into an analog IF signal by the DAC module. Finally, the intermediate frequency signal is converted into the radio frequency signal and transmitted through the RF part.

B. ARM Module Algorithm

The main function of arm module is to generate navigation information and calculate satellite parameters according to the current user trajectory and the satellite almanac input by upper computer. The specific algorithm flow is as follows: First of all, ARM reads the initial parameters and ephemeris files set by the upper computer, converts the local time to GPS time according to the data in the file, and converts the user coordinates to World Geodetic System 1984 (WGS-84) coordinates. Then, according to whether the relative elevation angle between the satellite and the user is bigger than the set threshold, the visibility of the satellite is judged, and then the navigation information is compiled and the error model is established to calculate the time delay and Doppler shift of the satellite. Finally, the generated data parameters, control parameters and navigation information are sent to FPGA.

C. FPGA Module Design

FPGA is responsible for receiving data parameters, control parameters, and navigation messages from the ARM, and generating IF signals of multiple satellites, which is the key module of the entire design. In this design, FPGA uses 6 channels to simulate 6 satellites and generate GPS L1 frequency signal. The implementation of FPGA IF signal generation is shown in Fig. 2.

As shown in the Fig. 2, the overall process of IF signal generation is: After the ARM sends data to FPGA, FPGA selects satellite channel to be simulated according to the data address, and extracts core data such as navigation message, control words, initial carrier phase, and initial code phase. The code control word is sent to the numerically controlled oscillator (NCO) module to generate the C/A code; the carrier control word is sent to the carrier NCO module to generate the IF carrier signal. The pseudo code and navigation message are spread spectrum modulation and then modulated with the IF carrier signal by binary phase-shift keying (BPSK) to generate digital IF signal[8]. Finally, analog IF signal is generated by the DAC module.

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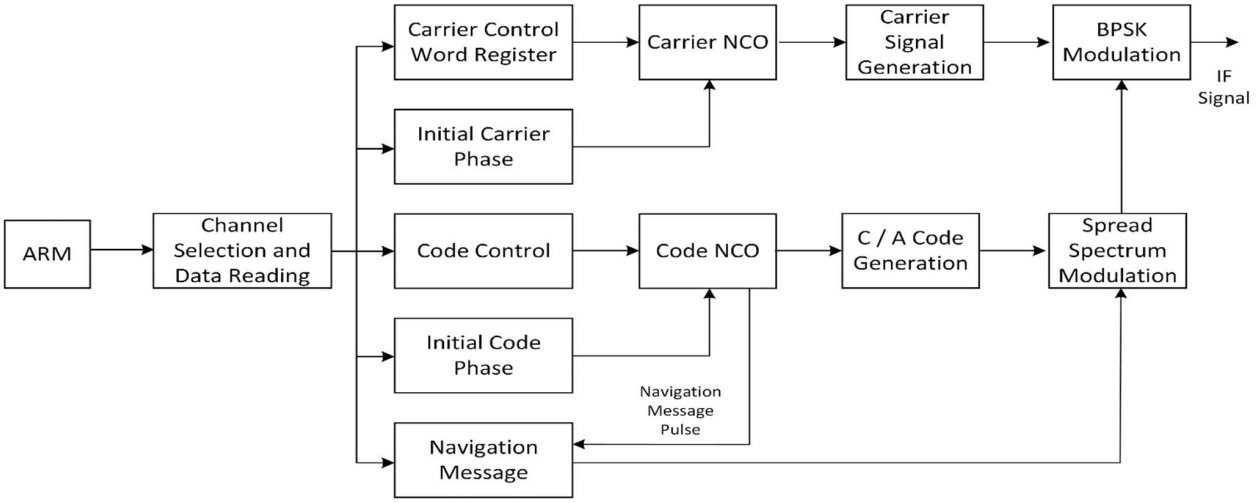

Fig. 2. FPGA IF Signal Generation

It can be seen that the carrier NCO and code NCO are the core parts of the FPGA module. Among them, DDS technology is the key to the carrier NCO module. It can achieve the purpose of frequency synthesis by changing the rate of change of the phase, and is generally used to simulate the Doppler frequency shift and phase frequency shift of the carrier. In addition, the code NCO is divided into carry output and most significant bit (MSB) output. In practical applications, due to the high dynamics of the GPS receiver, the Doppler shift cannot be ignored, so the frequency of the control word will change with the frequency of the C/A code. In view of this, if the MSB output is selected, the phase jitter of the output signal will not be determined, but the phase jitter of the carry output signal is determined, and the magnitude can be predicted by calculation. Therefore, this design uses the carry output of the accumulator as a clock to drive the code generator.

III. EXPERIMENT AND ANALYSIS

The simulated IF signal of GPS signal simulator is the final output of the main control board, and then the satellite simulated IF signal is up converted into corresponding RF signal through the mixer module. Therefore, whether the IF signal of satellite simulation is correct or not is directly determines the success or failure of satellite signal simulator system design. The frequency of the IF signal simulated in this design is 39.42MHz, and Fig. 3 is the spectrum diagram of the analog IF signal measured by the spectrometer.

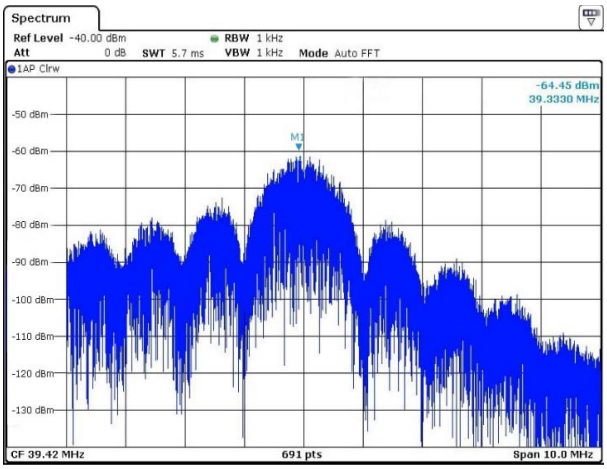

Fig. 3. Spectrum of analog IF signal

In view of the fact that the frequency of common open frequency point L1 of GPS satellite navigation system is 1575.42MHz, and the up conversion local oscillator frequency of this simulator is 1536MHz. Therefore, for this system, the criteria and parameters for evaluating the correctness of the generated analog satellite signal frequency are: The sum of the output IF signal frequency and the local oscillator frequency of the RF part should be equal to the standard frequency value of GPS L1 frequency point, namely 1575.42MHz. The measurement results of the spectrometer are shown in Fig. 4. It can be seen that the center frequency is 1.575442GHz, that is 1575.442MHz. The error with the expected result is in a reasonable range, which proves the rationality of the design.

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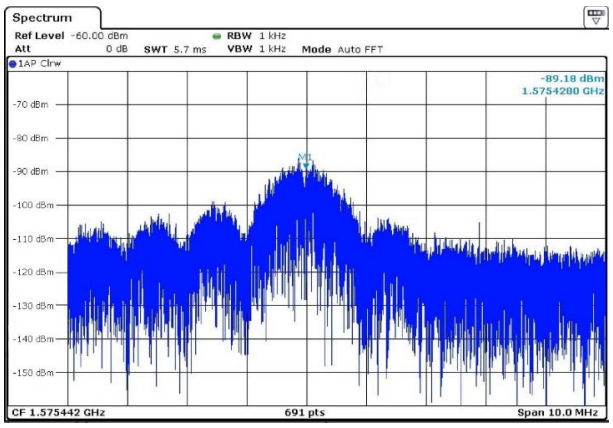

Fig. 4. Signal spectrum of GPS L1 frequency point

Besides, the simulation navigation signal generated by the simulator is observed through the software receiver, and the results are shown in Fig. 5.

It can be seen from the Fig. 5 that the GPS simulator has successfully simulated the six satellites, including 2, 6, 12, 14, 15, and 24. The longitude and latitude are 118.189156 and 24.496077 respectively, and horizontal dilution of precision (HDOP) is 1.9, position dilution of precision (PDOP) is 3.3. PDOP values less than 6 are generally considered to be valid data. In theory, the smaller the PDOP value, the higher the reference value of the satellite signal. Good HDOP values and PDOP values both show the validity of positioning data.

The initial coordinates are set to Building NO.39, Xiamen Software Park, and its longitude and latitude information is 118.189127 east longitude and 24.496038 north latitude. According to the error calculation formula, the difference between longitude and latitude is 0.000029 and 0.000039 respectively. After converting to the degree, minute and second system, the difference is 0.00174 minutes and 0.00234 minutes respectively. Since the total meridian length of the earth is about 40008km, that is 1 degree is about 111 km, and 1 minute is about 1.85 km. The calculated longitude error is 3.219 m, the latitude error is 4.329 m, and the positioning accuracy error is in a reasonable range, which shows that the design can correctly simulate the GPS satellite signal.

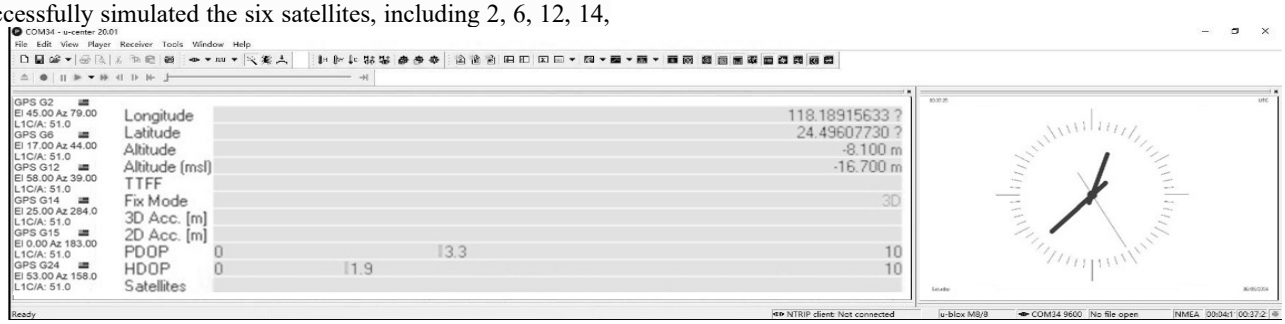

Fig.5. Acquisition signal diagram of software receiver

IV. Conclusion

This paper mainly introduces a portable GPS signal simulator based on ZYNQ. Through the efficient AXI interface between ARM and FPGA, the I/O bottleneck problem of traditional DSP/ARM and FPGA is solved, and the hardware design difficulty is reduced to a certain extent, and the comprehensive performance of the system is improved. In the experimental results, the positioning accuracy error of several meters also proves that the design can meet the test requirements of most GPS receivers.

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