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High-performance Zynq FPGA-based wireless sensor node for vibration monitoring systems

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***Abstract*—Vibration-based condition monitoring of rotating machinery is considered as the most effective strategies of early fault detection and maintenance. Wired solutions in the traditional vibration analyses and surveillance systems suffer considerably from several disadvantage such as low mobility and high cost of installation and maintenance. The technological progresses led in the last decades in the fields of microelectronics, micromechanics and wireless technologies have brought a new generation of ad hoc networks called wireless sensor networks (WSN) that presents significant challenges and offers economic practical solutions. The use of the WSN in the vibration analysers is useful to monitor and analyse the vibration of rotating machinery as well as early fault detection. However, the vibration analyser WSN based must meet several requirements such as high-performance processing capabilities with a high sampling rate and low power consumption. System-on-chip (SoC) designs based on FPGA circuit is an attractive approach to increase performance and decrease costs during industrial equipment monitoring process. In the present work, we designed and implemented a high-performance wireless node for vibration analysing based on Xilinx Zynq FPGA platform. The proposed node collects a tri-axes vibration data and performs FFT computations of maximum 16384 points. FFT results are then transferred to the base station through an Xbee module. The experimental results showed that the node achieves the requirements of high-sampling rate up to 50 kHz, where the relative error between the computed frequency by the FFT of the node and the real frequency of the generated signal can be reduced to less than 0.1%.**

Keywords—FPGA, SoC, Vibration monitoring, WSN, ZynqFPGA

I. INTRODUCTION

Wireless Sensor Networks include a sensing system, embedded processing system, and wireless communication infrastructure, making them favoured in distributed monitoring due to its low cost, helping industries to face the increasing competitiveness [1][2]. In most cases, wireless sensor nodes, which are the basic elements of a WSN, need to embrace the required resources to allow the infrastructure-less distributed monitoring. Most of the existing typical wireless sensor nodes designs based on low-cost and low-power modules, resulting very limited nodes in terms of communication and processing capability, and inappropriate to industrial applications that require a very high sampling frequency [3].

In the present work, we designed and implemented a high-performance wireless sensor node for vibration analysing, based on Xilinx Zynq@-7000 System on Chip FPGA circuit. In Addition to the main processor, an FFT co-processor as an IP-core is involved in the overall system. In order to ensure a wireless link between the different nodes of the network, we opted an Xbee RF module for wireless communication.

The rest of this paper is organized as follows: In section 2, we present the design structure of the proposed node and its main subsystems. In section 3, we discuss its implementation on a low cost platform which hosts a Zynq-7000 FPGA device. In section 4, we present some experimental results and finally we ended this paper by a conclusion in section 5.

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II. Design Structure of the Node

The wireless sensor nodes, commonly known as "motes" [4] or simply wireless nodes, are the central element of a wireless sensors network. The main subsystems of the node are detection and acquisition, processing and storage, communication, and power supply. Additional optional features may be incorporated into the design of the node, such as the localization system. The choice of technologies for the implementation of the nodes is generally determined by the design constraints imposed by the application [5]. The designer has a multitude of options to decide how to design and implement these subsystems into a single programmable node. Subsystems can be physically independent, as is the case when the node is designed with components available on the market or can be integrated as a SoC.

Using the FPGA circuit as a reconfigurable platform can improve the processing performances of many systems [6], including the WSN nodes [7]. In this case, the design of a node can benefit from the technologies of reconfigurable platforms in several aspects. Not only the design flexibility is exploited to develop customized hardware accelerators, but also the ability to prototype new processor architectures as required by the target application. However, the design cost and implementation remains one of the limitations of reconfigurable platforms, which restrict its use in real world application domains, often limiting the platforms realized for experimental purposes.

Figure 1 shows an overview of the designed system of a wireless sensor node for vibration monitoring. The system hardware architecture is based on the Xilinx Zynq 7010 FPGA which embeds a dual-core Cortex-A9 ARM processor at a maximum CPU clock of 650 MHz as processing system (PS), in addition to Xilinx programmable logic (PL), all in a single FPGA device. The PL and PS are connected via AXI Bus [8].

An FFT co-processor is created on the PL part of the device using the Xilinx AXI DMA core. Data from the acquisition phase are stored in the main system memory before being transferred to the FFT core for processing, via the AXI DMA. Once the FFT processing is done, the data is sent back to main memory using the AXI DMA core. Information passing between the PS and PL using the high speed AXI4 ACP (Accelerator Coherency Port) to maximize performance.

For the proposed node, we integrated an Xbee transceiver module on the proposed node through UART interface to add communication ability in order to transfer data to the base station. The Xbee module is based on the IEEE 802.15.4 standards and operates at 2.4 GHz frequency with maximum data rate of 250 kbps. The module offers indoor communication range up to 100 m and outdoor line of sight range up to 1500 m [9].

In addition, the wireless node is equipped with a 12-bit ADCS7476MSPS analog-to-digital converter. The inputs have a "Sallen key" anti-aliasing filter, with a maximum sampling rate of one million samples per second, which can be controlled easily via an SPI link. Also, sensors such as accelerometers is also used.

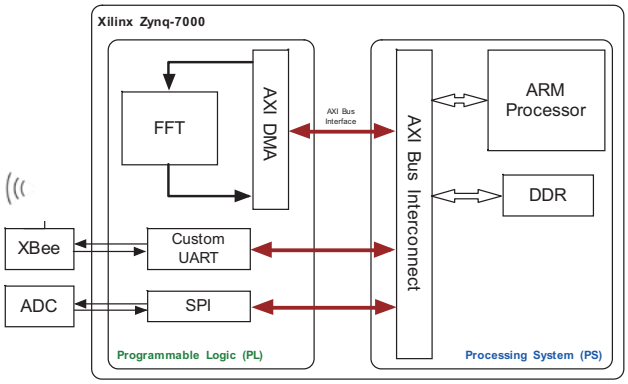

Fig. 1. The designed node architecture

III. Hardware Implementation

In this work, the Digilent Zybo Board is chosen as the development board for the implementation of the proposed node. It contains a Xilinx Zynq-7000 All Programmable System on Chip (c7z010-1clg400c), which consists of a dual-core ARM Cortex-A9 MPCore based PS and an Artix-7 FPGA as PL. The system offers the flexibility and the scalability of the FPGA, also will provide performance, power, and ease of use typically associated with ASIC and application specific standard product (ASSP).

The PL makes use of the second version of the Advanced Extensible Interface (AXI4) bus protocol, which is part of the ARM Advanced Microcontroller Bus Architecture (AMBA).

The Xilinx Vivado design suite tools were used to configure and program the ARM Cortex-A9 processor, where the frequency has been set to 100 MHz. After the place and route of the implemented architecture on the target FPGA board, the synthesis report of resource utilization, time and operating frequency are detailed in Table I.

TABLE I. Synthesis Results of the Nodes Implementation.

Resources	Used / Available	% Utilisation
Number of slices	7414 / 17600	42.13
Number of flip flop	12433 / 35200	35.32
Number of bonded IOBs	22 / 100	22.00
Number of BRAM	37 / 60	61.67
DSP Slices	54 / 80	67.50
Estimated total on-chip Power	1.6 W	
Maximum operating frequency	100 MHz	

The synthesis results show that a maximum of 62% of BRAM resources is used for the implementation and this for a reconfigurable FFT IP core of 16384 points. It can be noted that the energy consumed is also high compared to a wireless sensor network application, which represents a disadvantage in

the proposed node. Hence, we can benefit from the advantage of using the standby mode of the hard processor to overcome the problem of energy consumption in the node, especially for vibration monitoring applications, where the sensor node can perform measurements periodically, and then back to standby mode in most time.

To estimate this power consumption, we assumed that the node is powered by a DC battery of 5 V. The results obtained from the average current and power consumption are shown in Table II. Given that the capacity of the selected lithium battery is 2600 mAh, the service lifetime of the node can be estimated and the results are given in Table II.

TABLE II. POWER CONSUMPTION RESULTS.

Operational mode	Current (mA)	Power (mW)	Lifetime (h)
Full operation	333	1666	7
Standby	8	40	325

In the operational mode, the node can operate continuously for about 7 hours. In this case, the sensor node periodically performs a measurement every 3 s, which is very high for the majority of monitoring applications. When the modules:

ARM processor, RF module and ADC enter standby mode, the current consumption is only 8 mA, which increases the lifetime to 325 hours. Therefore, this standby mode helps to extend this duration. In fact, it depends mainly to the monitoring plan. For example, with a periodicity of monitoring of 1 minute (3 s in operational mode and 57 s in standby), it goes from 7 hours to more than 107 hours (the second point on the graph of figure 2). The limit of 325 hours can also be reached with a periodicity of one hour.

IV. EXPERIMENTAL RESULTS

In order to estimate the performance and the overhead introduced by the re-configurability of the FFT block, we tested the node for different configurations. The steps are depicted by the flowchart in Figure 3. When the node is powered up, the program starts by initializing the internal registers and the definition of constants and variables necessary for the calculation. Subsequently, the XBee module's Uart is configured with a baud rate of 115200 bps, the node's processor then sends the message “node ready” to the sink node and ends the initialization phase by switching the Zynq processor to the sleep mode to reduce energy consumption. Receiving a request for data acquisition from the sink, the Xbee module wakes up the processor that starts by reading the FFT’s number of points required. Then, the acquisition of the necessary data starts and calculates the FFT.

Finally, the node transmits via XBee module the result of the data processing and sets off a delay of one second before returning to sleep mode waiting for a new acquisition request.

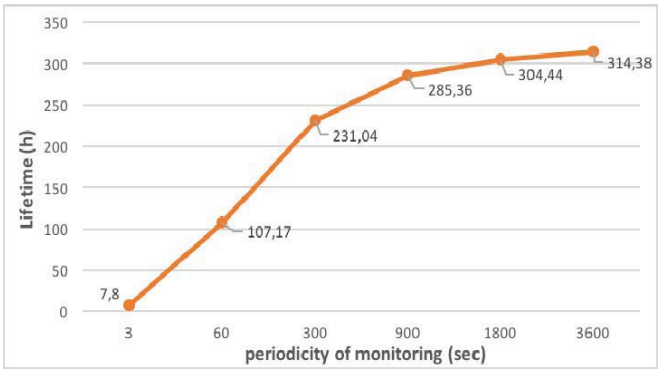

Fig. 2. Estimated lifetime of the node

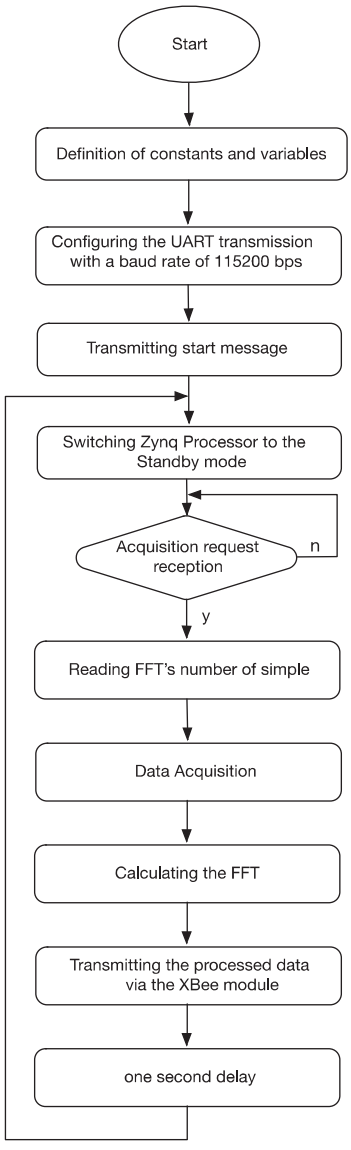

Fig. 3. Flowchart of the node process

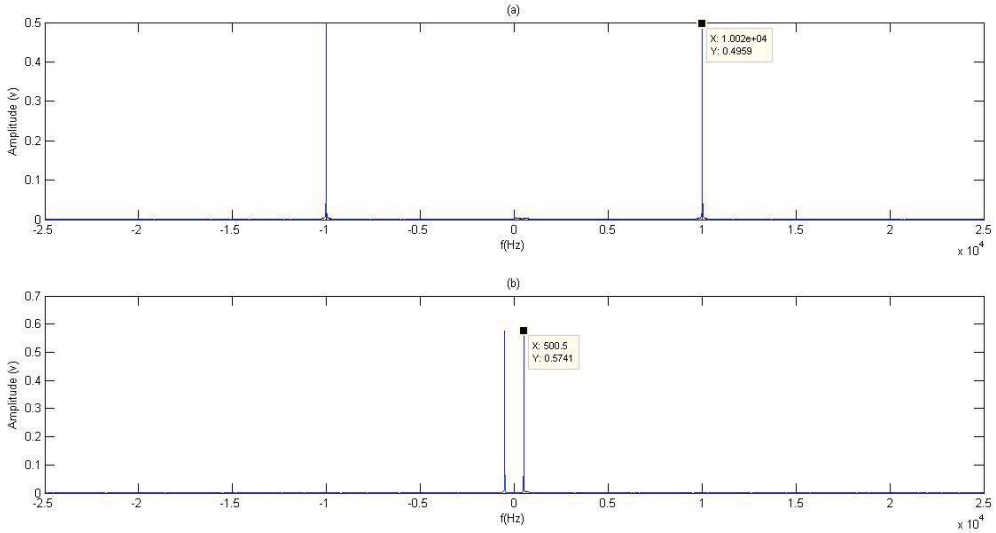

Fig. 4. Spectral representation (a) 10 kHz, (b) 500Hz

To evaluate the acquisition performance of the wireless sensor node made for high frequency signals and a high sampling rate, we used Digilent's "Analog Discovery 2" multifunction instrument to generate two sinusoidal signals with different frequencies (500 Hz, 10 kHz) and with the same amplitude (1 V).

The sampling rate of the node is set at 50 kHz. Once the acquisition operation is complete, a spectral analysis (a 16384-point FFT) of the collected data is performed in the FFT block of the sensor node. At the end of this step, data processed were transmitted to a PC via the sink node proposed in [7], and traced using the Matlab software as shown in figure 4. The results show that the relative error between the frequency of the generated signal and that of detected by the sensor node is relatively small, around 0.2 % for the signal of 10 kHz (figure 4a) and 0.1 % for the signal of 500 Hz (figure 4b).

The bar charts in figure 5 shows the differences in terms of processing time for different configuration of the FFT block. As illustrated in the figure, the processing time grow impressively with the increase in the number of FFT-points, this means that the choice of the FFT configuration will affect the characteristics of the wireless node, such as processing time and power consumption.

On the other hand, the re-configurability of the FFT block gives more flexibility to the node in order to choose the appropriate parameters according to target application.

V. Conclusion

The main objective of this work was to design and realize a wireless sensor node based on a SoC FPGA architecture, which must meet certain requirements such as data acquisition at high sampling rate, reliable data transmission, and suitable for applications requiring intensive computing.

The Xilinx Zynq-7000 FPGA chip is chosen as a target for this implementation includes enough logical resources in its programmable logic part, and which are generally required in monitoring applications. In its processing system part, the FPGA is equipped with a hard-core ARM processor that manages the different tasks in the node. The results show that more than 95% of energy can be conserved by switching the node to its standby mode, and the lifetime of the node can be extended from 7 hours to 314 hours.

Several measurement tests have been done aiming to validate the effectiveness of the proposed node for high sampling rate and intensive computing. Experimental results illustrate a frequency relative error of 0.1 % in case of sinusoidal signal of 500 Hz where the node is set at a sampling rate of 50 kHz and 16384-point FFT.

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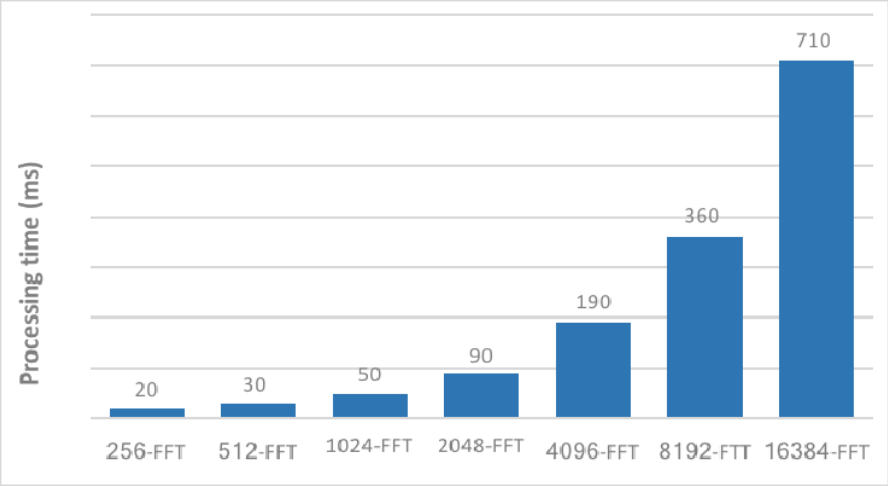

Fig. 5. Processing time in function of FFT points

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