RF Signal Generation for MRI System using PS-PL Communication in FPGA over Ethernet

Aditi S Deshpande
M. E. Electronics, Dept. of Electronics Engineering
Fr. Conceicao Rodrigues College of Engineering,
Bandra (W), Mumbai - 400050
Email: ylvjoshi@gmail.com

Imran Sheikh
Research Scientist, Technology Innovation Division
SAMEER IIT-B,
Powai, Mumbai - 400076
Email: imran.sheikh.vjti@gmail.com

Prof. Kranti Wagle
Assistant Professor, *Dept*. of Electronics Engineering
Fr. Conceicao Rodrigues College of Engineering,
Bandra (W), Mumbai - 400050
Email: kranti@fragnel.edu.in

Dharmesh Verma
Scientist – D, Technology Innovation Division
SAMEER IIT-B,
Powai, Mumbai – 400076
Email: dharmesh@sameer.gov.in

***Abstract*—FPGA (Field Programmable Gate Array) is an open-source framework consisting of a small hardware core and a host-software library. It provides a platform for extensible communications, allowing the specialized chips in the FPGAs to program and perform very specific functions in hardware. Implementation of a function in software can be done in the exact manner as in case of an FPGA and thus can be executed in hardware. This paper presents the designing and simulation of RF Signal Generation for MRI systemsusing the PS to PL communication over FPGA platform with the help of Ethernet communication protocol. The working of embedded processor inside FPGA is such that it can receive data via Ethernet in the form of packets. Further processing of the data is carried out on the received Ethernet packets from which actual data is extracted, processed and finally transmitted to the other required subsystems, as in this case to RF Transmit coils. The concept explained in this paper enables the host PC to transmit data to Xilinx-based FPGA board via Ethernet using a standard synchronous inter-networking protocol (TCP/IP). The implementation platform is an evaluation board which has an Arm processor on FPGA. Using the VIVADO tool, the processor is configured inside the Zynq SOC. SDK (Software Development Kit) helps in configuring the software part of the processor. The link between the PC and the evaluation board is well established using the Ethernet interface and the output is given to the AXI GPIO (General Purpose Input Output) pins. The output from GPIO is given to subsequent system like DUC (Digital-Up Converter) and from DUC it is further passed on to RF DAC.**

Keywords—ARM Processor, DUC, Ethernet packets, FPGA, GPIO, inter-networking protocol, RF transmit coils, RF DAC, SDK, SOC, VIVADO, Zynq.

I. INTRODUCTION

A basic MRI system includes an RF coil to which analog RF pulse signals are applied as an input, an RF signal generating circuitry which generates analog RF pulse signals and a dedicated MR signal receiving circuitry which receives analog magnetic resonance signals and further converts these signals into the baseband digital magnetic resonance signals. RF pulse generating circuit comprises of a carrier signal generator which generates a digital carrier signal having a predetermined frequency value, a digital modulator which modulates the digital carrier signal with a digital envelope signal thus generating digital RF pulse signal. A Digital to Analog Converter (DAC) is used which converts the digital RF pulse signal into analog RF pulse signal. It comprises of an inversion unit which generates a digital inverted carrier signal having two's complement relationship with original digital carrier signal and sends this inverted carrier signal to MR receiving circuitry. For successful RF signal Generation according to the required specifications, the Pulse Sequence Decode (PSD) file is required to know the exact RF signal point generated and its corresponding information. Thus after decoding the PSD file, the data is passed through the RF DAC to achieve digital analog RF signal.

II. HARDWARE SYSTEM

A. ZYNQ Architecture

The zynq-7000 series FPGAs come with an integrated ARM-Cortex processor. The Zynq architecture differs from the previously available programmable logics and embedded processors where there is a change observed from FPGA-centric platform to processor-centric subsystem. Prior to the invention of Zynq, processors were made available with a Field Programmable Gate Array (FPGA) which were designed in such a way that made the communication between the Programmable Logic (PL) and the Processing System (PS) tricky and complex. As the latest generation of SOCs (System-on-Chips) families manufactured by Xilinx's, the Zynq

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architecture combines dual-core ARM-Cortex A9 processor with traditional FPGA. Fig 1. shown below is the image of Xilinx's ZYNQ ZC702 FPGA Evaluation Board. Advanced eXtensible Interface (AXI) standard provides an interface between the various elements embedded within the Zynq architecture thus supporting for higher bandwidth operations and low latency connections. Xilinx's soft core processor such as Microblaze was initially used by the programmers which provided the main advantage of flexibility of processor within a design. On the other hand, further by implementing the ARM processor within the Zynq device, significant improvements in the performance was observed. Also, the overall cost and physical layout of the system was reduced by simplification of the system to single-chip system.

Fig. 1. ZC702 Evaluation Board

B. ZYNQ Design Flow

Zynq architecture has somecommon steps in designing as compared to the traditional FPGAs. The four major stages include Design Specification, System Design, Hardware and Software Development and Testing and System Integration. The design flow is as shown in Fig 2. as follows

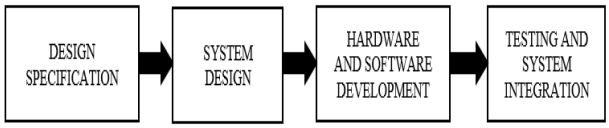

Fig. 2. ZYNQ Design Flow Model

The first stage defines the specifications and requirements of the system. During the second stage of system design, different tasks i.e., functions are allocated in either PL or PS for implementation called as task partitioning. This stage is the most important stage as the performance of the overall system depends on the way the tasks are assigned for implementation using the most appropriate technology with best hardware or software. Further the hardware and software development and testing is carried out. In case of Programmable Logic, the work is to identify the required functional blocks in order to achieve the required design characteristics and also to put together the IPs and make the appropriate connections among them. Likewise, developing the code to run on the Processing System comes under the head of software activity. Consequently, system integration and testing is done in order to finish up with the design.

C. DAC Evaluation Platform

The AD9122 is a dual data rate, 16-bit wide, digital-to-analog converter (DAC) which comes with high dynamic range that provides a sample rate of 1200 MSPS. The AD9122 TxDAC includes features optimized for direct conversion transmit applications, including complex digital modulation, and gain and offset compensation. The DAC outputs are optimized to interface smoothly and continuously with analog quadrature modulators, such as the ADL537x F-MOD series modulators.A 4-wire serial port interface available on-chip provides for programming of many internal system parameters. Full-scale output current can be programmed over a range of 8.7 mA to 31.7 mA.As compared to the other existing DACs, AD9122 works on double data rate allowing to transfer data on both the positive as well as the negative clock cycle. It has a dual digital signal path and dual DAC structure which allows for an easy interface with the quadrature modulators for designing single sideband transmitters. In comparison with the previously available DACs, the speed and performance of AD9122 allows for wider bandwidths and thus more carriers to be synthesized. In addition to this, AD9122 includes a low-power, 32-bit complex numerically controlled oscillator (NCO) that helps in increasing the ease of frequency placement anywhere in the given bandwidth.AD9122 offers features for simplified synchronization with incoming data and as well as with multiple devices. AD9122 evaluation board as shown in Fig 3. also comes with the facility of inbuilt auxiliary DACs provided on chip. The auxiliary DACs are used for providing output dc offset compensation and for gain matching. AD9122 communicates with other external devices via serial ports. The serial port is a flexible, synchronous serial communication port which is compatible with SPI protocols. The AD9122 contains 2-channel, 16-bit wide, 8 word deep FIFO designed to relax the timing relationship between the data arriving at the DAC input ports and the internal DAC rate clock.AD9122 follows the digital data-path process which includes a pre-modulation block, three half band interpolation filters, a quadrature modulator with fine resolution NCO, phase and offset adjustment blocks and an inverse sinc filter.

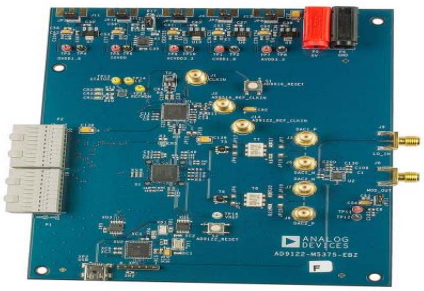

Fig. 3. DAC AD9122 Evaluation Board

III. SOFTWARE PLATFORM

FPGA configured soft core processors have become a priority for implementing various embedded systems. With the availability of these soft cores, application development can be split into executing certain portions of the applications as software programs and the remaining portions as customized hardware synthesis. The idea behind implementing this project completely revolves around performing the software based

tasks on majorly three important software like MATLAB, VIVADO and ACE (Analysis-Control-Evaluation). MATLAB is used for generating the sinc pulse by creating .COE file. In MATLAB, the filter specifications are set with the help of FDATOOL command option which allow for generation of coefficients necessary for acquiring the desired sinc pulse for RF Signal Modulation Technique. Further this .COE file is called in SDK (Software Development Kit) software where it is burnt in the targeted device, in this case Zynq XC7Z020 board. The XC7Z020 consists of processing system (PS) and programmable logic (PL). The design and configuration of the processing system (PS) and the programmable logic (PL) is done using VIVADO software. In VIVADO, the block design of the implementation is carried out using various IPs (Intellectual Property) cores. The software provides the option of re-customizing the IPs according to the required specifications and also has the facility of verifying the output on its in-built simulator window.

IV. PROPOSED BLOCK DIAGRAM

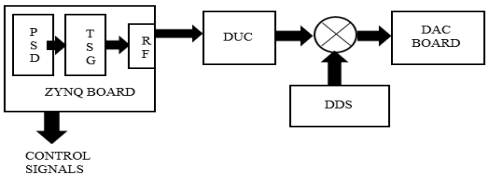

Fig. 4. RF Signal Generation Block Diagram

The proposed block diagram of RF Signal Generation for MRI Systems using PS to PL communication in FPGA over Ethernet is as shown in Fig 4. In FPGA approach, RF signal is generated using Zynq SOC ZC702 and RF DAC. This DAC works on double data rate and is pumped using both rising edge and falling edge of the clock. The differential system is coded using VHDL coding language for FPGA. The RF sample is up-converted and modulated inside the Processing System (PS) of an FPGA. The RF modulated signal is passed to other system through RF DAC. AXI GPIO interface is used in transferring the RF modulated signal to the RF DAC.

V. USED INTERFACING PLATFORM

A. Ethernet Interface

A data packet is transferred on the Ethernet link known as the Ethernet Packet, which carries the payload in the form of Ethernet Frame. At the physical layer, the Ethernet packet (payload) is preceded by preamble and start frame delimiter (SFD). Ethernet frame has an Ethernet header consisting of the destination and the source MAC address at its first two fields. The middle section of the frame contains the payload data and the frame ends with a frame check sequence (FCS) field. In case of RF signal generation, the payload is acquired from the Processing System (i.e., Zynq board) and is played out on the RF DAC. Thus, decoding of PSD is done in PS of FPGA and is transferred to the RF DAC. A successful Ethernet communication is achieved and displayed as shown in Fig 5.

```
-----Ethernet Communication------
DHCP Timeout
Configuring default IP of 192.168.1.10
Board IP: 192.168.1.10
Netmask : 255.255.255.0
Gateway : 192.168.1.1
TCP echo server started @ port 7
```

Fig. 5. Results of Ethernet Communication and PSD receiving data

B. MATLAB

For successful generation of modulated RF signal, the PSD file is decoded which contains the data for MRI scanning. In this paper, for verification and implementation purpose, decoding is done on the test signal. This test signal is generated through MATLAB software. In this paper, a sinc signal (test signal) is generated by creating a look-up table (LUT) and the sample points are then played out via FPGA through RF DAC to get the required RF modulated analog signal.

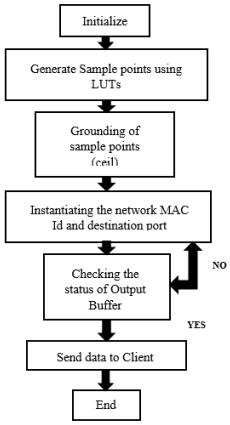

Fig. 6. MATLAB Server Code FlowChart

C. Processing System - Programmable Logic Interface

The generated data through MATLAB is sent to the Processing System on the FPGA wherein the SDK software comes into role. The software code is burnt into the FPGA Zynq board with the help of SDK software by targeting and connecting the device. Further, the processing of the acquired test signal, in this case, digital up-conversion and digital to analog conversion takes place in the Programmable Logic. Thus, in order to achieve a successful link between the generation of test signal and its advanced processing as per the required application, PS to PL interface plays a major role. In Xilinx's Zynq SOC ZC702, the PS comprises of ARM Cortex A9 processor, multiple peripherals and hard silicon core. PL of the ZC702 SOC is mainly made up of I/O banks. Heart of PS is the Application Processing Unit (APU). I/O peripherals, memory interfaces, on-chip memory, PS interconnects also bind up to form the Processing System. The Programmable Logic is configured after the PS boots. The task of configuring the PL is performed by application software accessing the hardware device configuration unit.

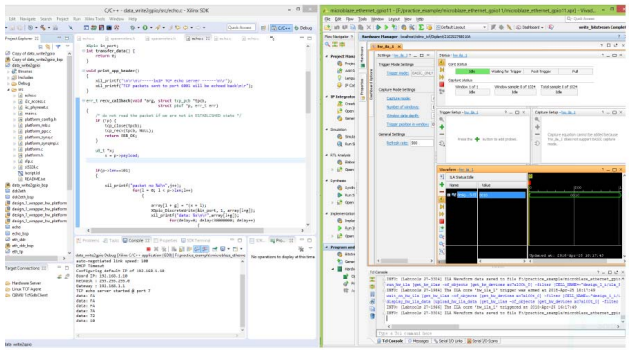

Fig. 7. Data transfer from MATLAB to SDK

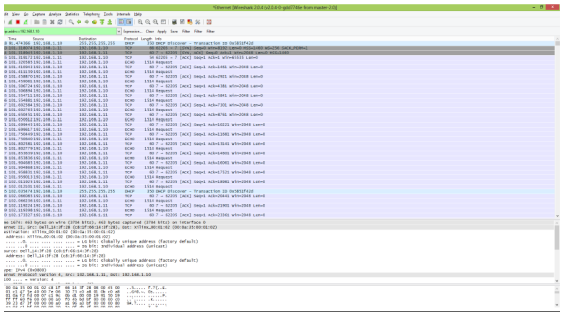

Fig. 8. Verification of data received on Wireshark window

Fig. 7 and Fig. 8 depicts the data transfer between the MATLAB and SDK software where the test signal is generated in MATLAB window and is targeted through the SDK software in order to configure the PL.

D. AXI GPIO Interface

Advanced eXtensible Interface or AXI is the most commonly used protocol by many SOC, which forms a part of the ARM Advanced Microcontroller Bus Architecture specification. Its widespread use is found in Xilinx's Zynq devices, providing an interface platform between the processing system and the programmable logic sections on chip. The protocol mainly discusses about the rules required for different modules resting on the chip to communicate with each other and also about the acknowledgement like procedure required before the transmission commences. The interface works by establishing a communication link between the server and the client device. There exists five different channels between these two devices like Read Address, Write Address, Read Data, Write Data and Write Response. Every channel possess is own unique signal and also there are certain common signals being shared between all five channels. Each channel has VALID and READY signal for acknowledgement process to occur for each channel. These signals are important for transmission of a signal over the channel. The source channel will provide an active VALID signal whereas the destination channel will provide active READY signal. Transmission may occur on that channel only when both the signals are made active. In AXI interface, transmission of control signals and data are done in separate phases. Thus for transferring data between two devices, an address must always be transferred between the devices before the handshake procedure occurs. Response channel indicates the completion of data transfer.

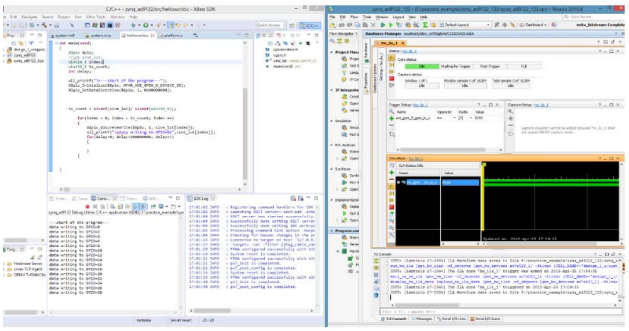

Fig. 9. PS – PL data transferred observed on ILA

VI. EXPERIMENTAL OBSERVATIONS AND RESULTS

To verify the working of the designed and proposed system, a laboratory setup is prepared and analyzed. The system here works on 400MHz system clock rate and an amplitude modulated sinc waveform is obtained which is of 64MHz peak frequency.Fig. 10 and Fig. 11 shows the modulated sinc waveform and the output of the frequency spectrum at 64MHz as observed on spectrum analyser.

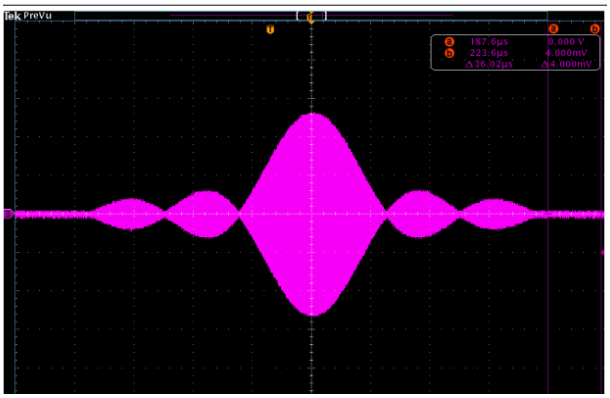

Fig. 10. Modulated RF Sinc Waveform

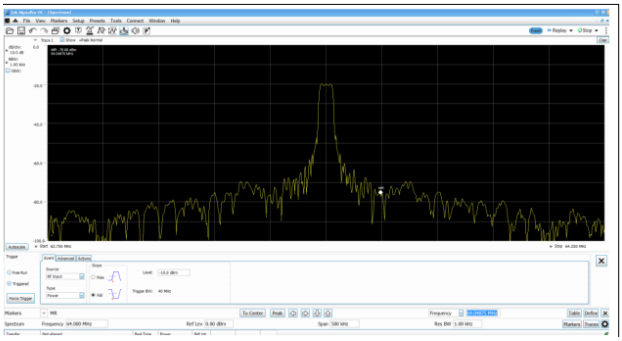

Fig. 11. Output observed on Spectrum Analyzer

The experimental setup for RF signal generation using FPGA and Digital to Analog Converter using Interposer Card is as shown in Fig. 12 and Fig. 13.

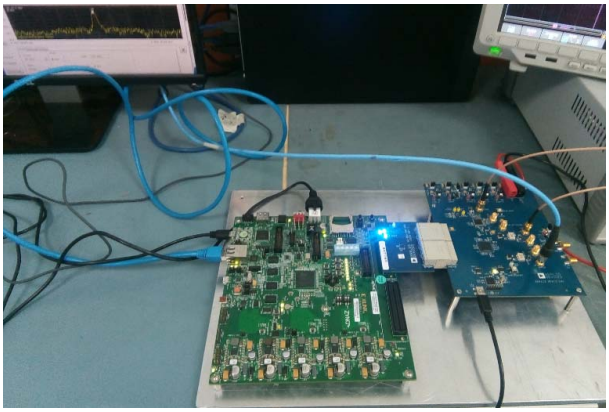

Fig. 12. Interfacing of FPGA Board and DAC Board through interposer card

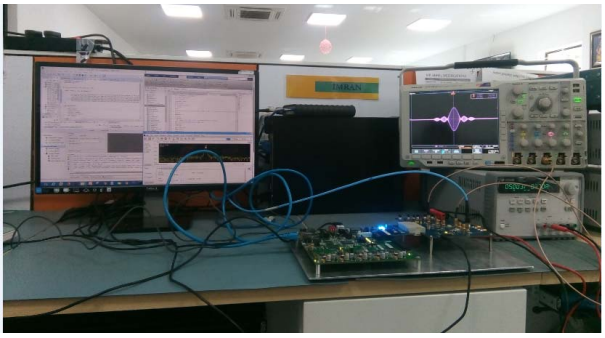

Fig. 13. Experimental Setup

VII. CONCLUSION

The generation of RF signal based on FPGA technology is achieved and presented successfully using software like VIVADO, ACE and MATLAB. The DAC used for RF generation verifies satisfactory results and performance. Also, efficient communication between Processing System (PS) and Programmable Logic (PL)is achieved and verified using software like Wire shark. Thus, it can be concluded that the results and output obtained from the above experimental procedure is modest and better than other previous work of others. The experimental results show effectiveness of system and functionality of algorithms followed throughout the procedure.

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