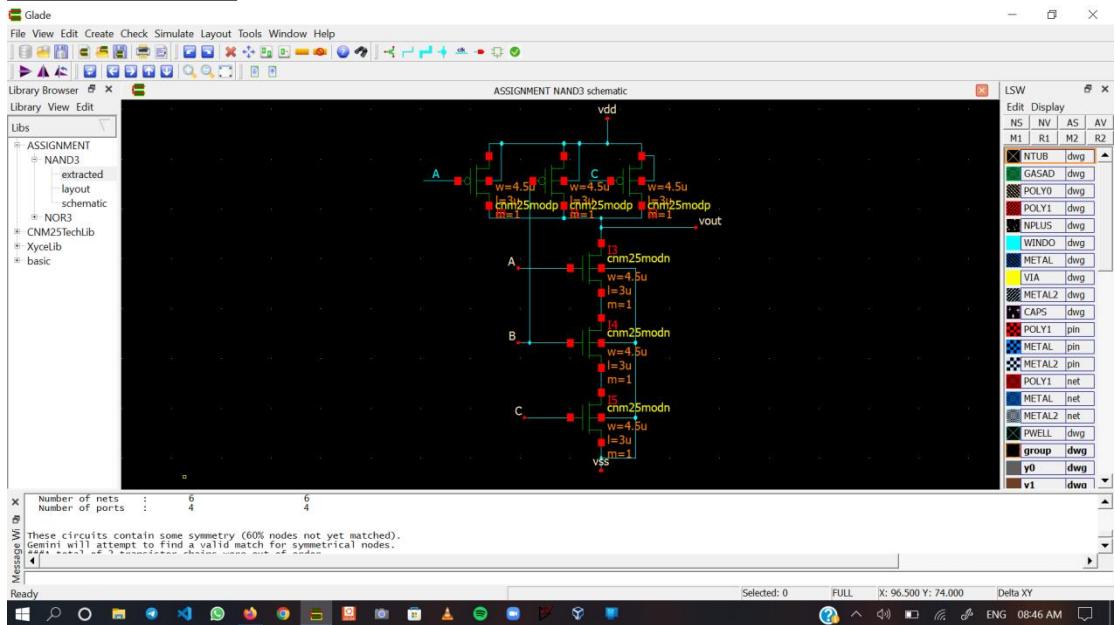


AYOUT DESIGN

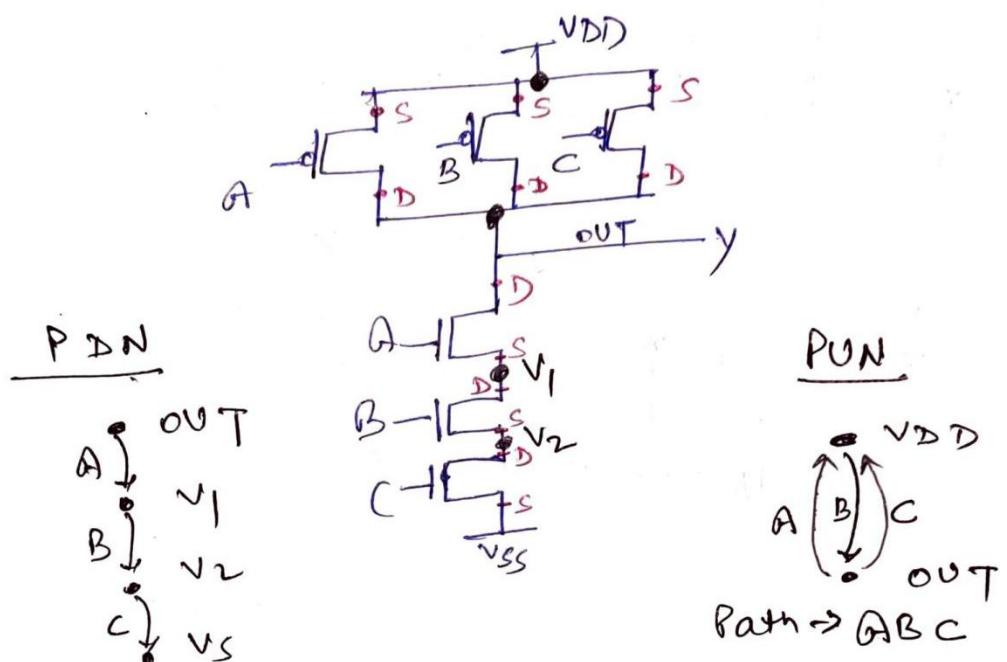
Q). Make Euler's Path, Stick Diagram and Layout for

A) 3 Input NAND SCHEMATIC

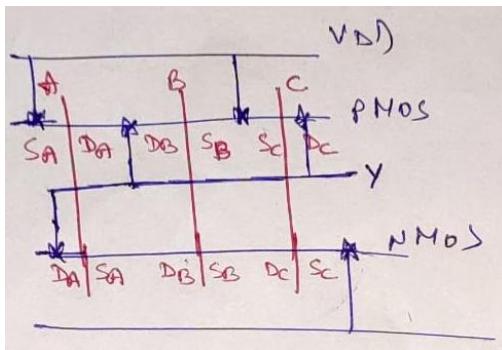


Euler's Path

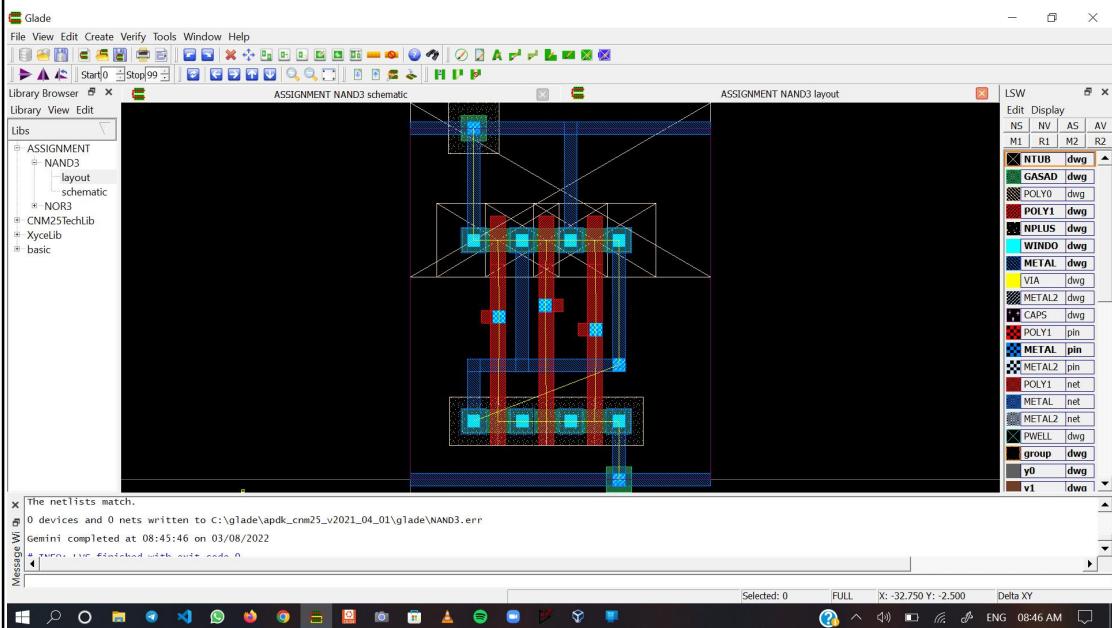
3 - input NAND



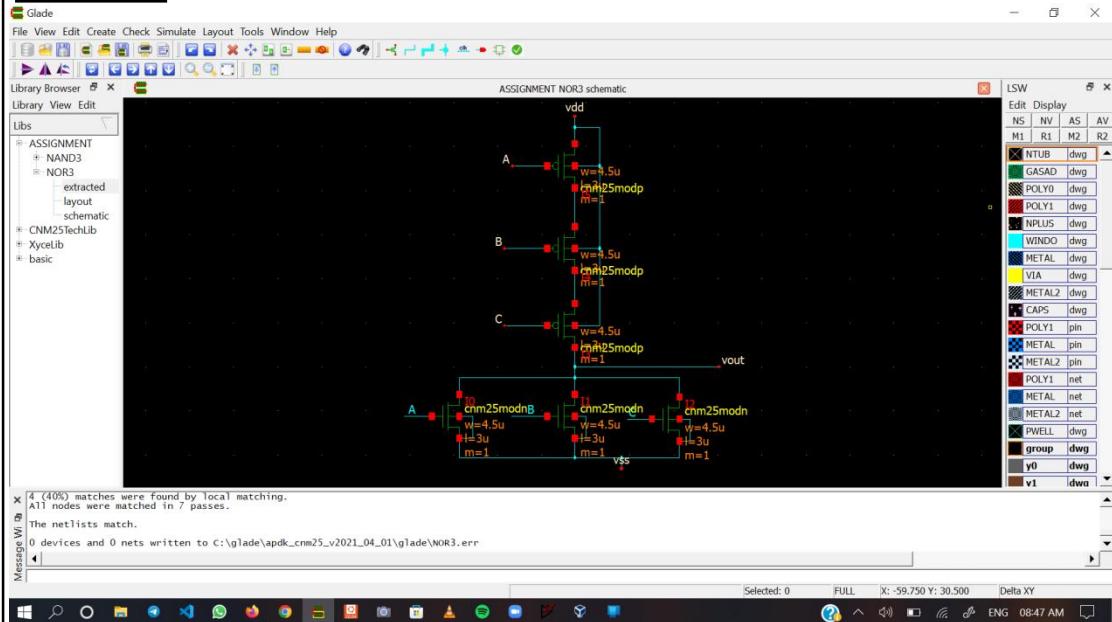
Stick Diagram



Layout

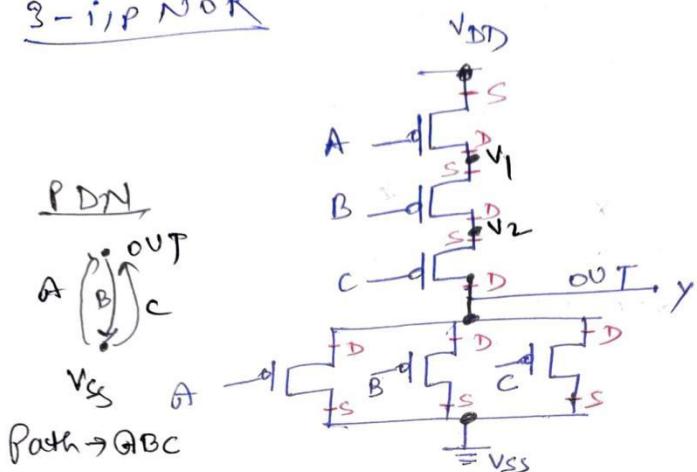


B) 3 Input NOR Schematic



Euler's Path

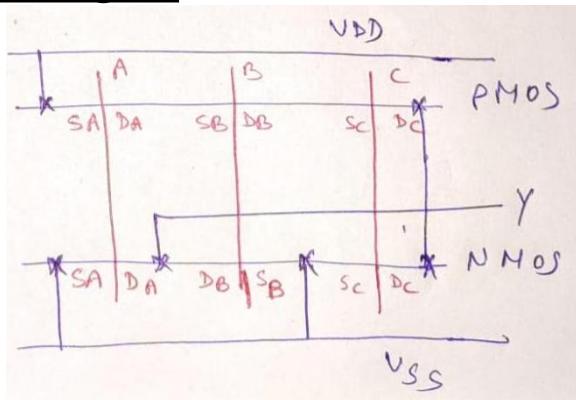
3-input NOR



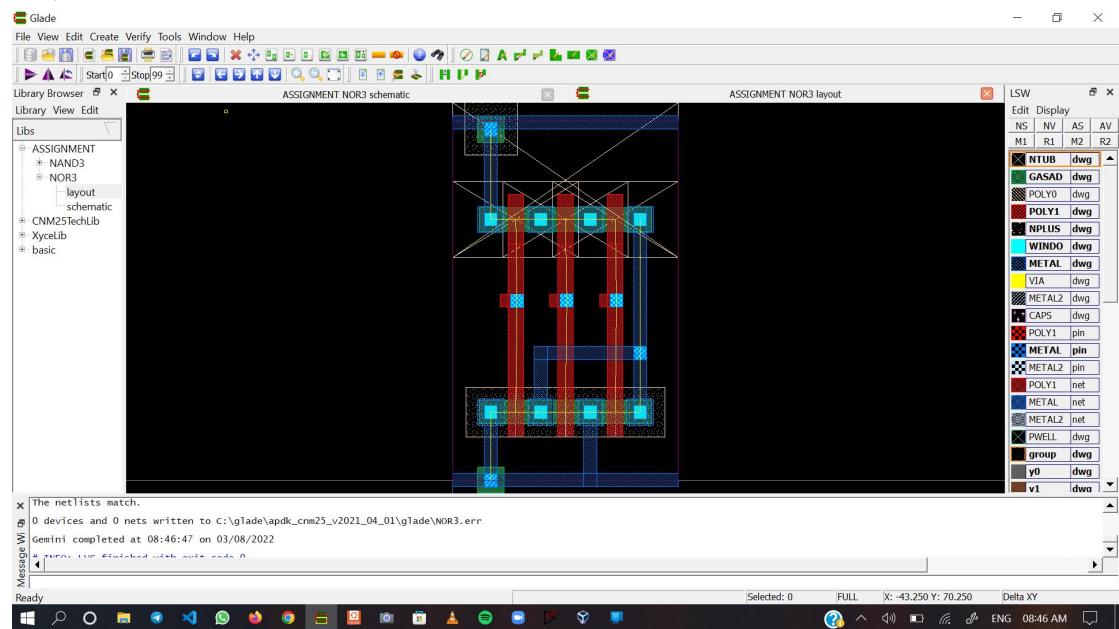
PUN



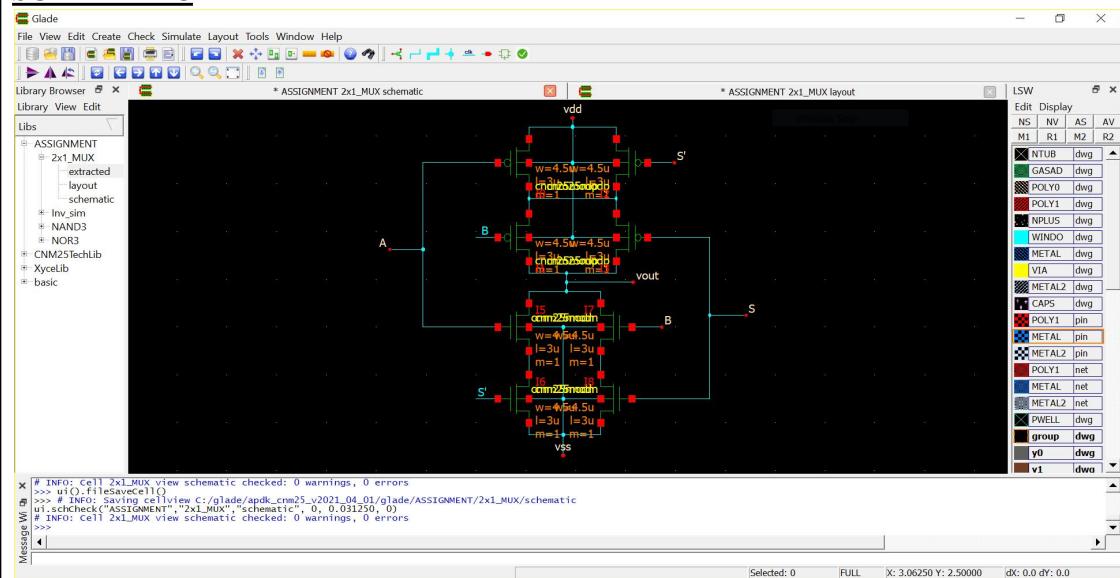
Stick Diagram



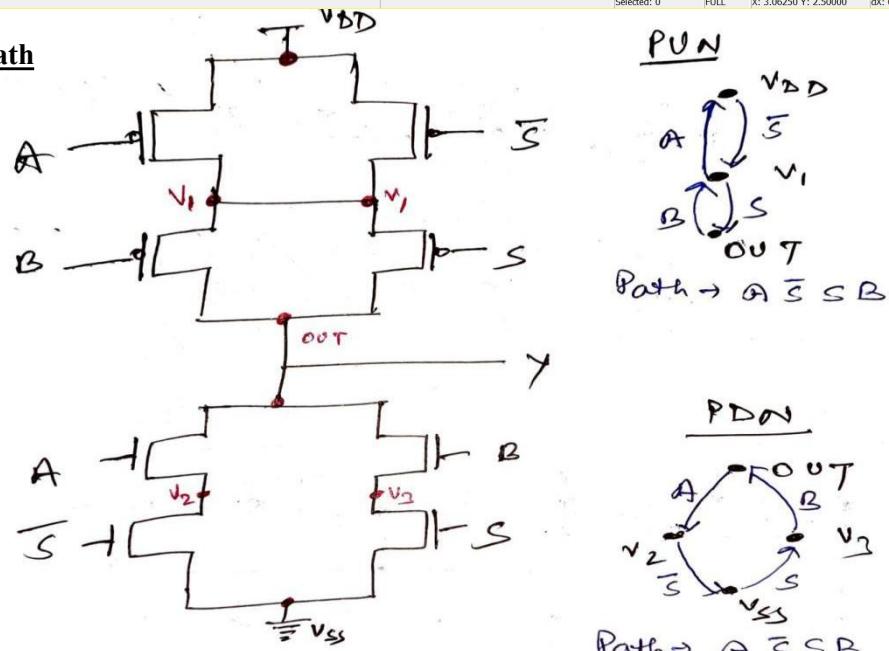
Layout



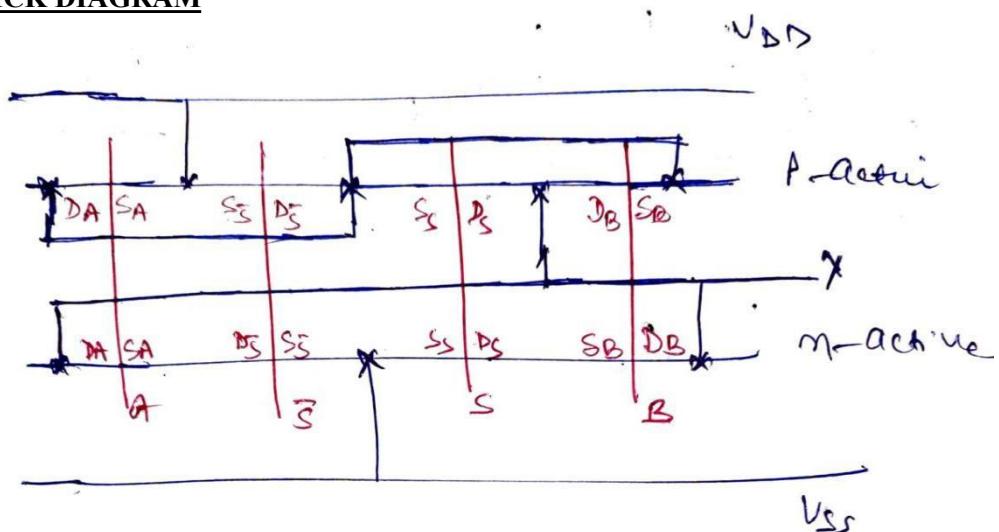
C) 2:1 MUX SCHEMATIC



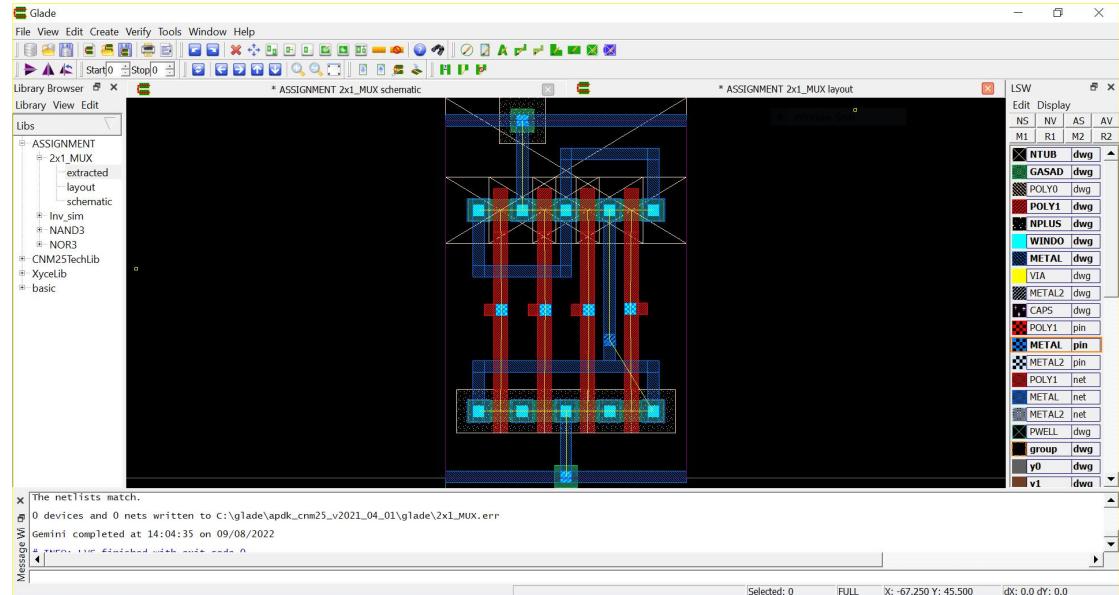
Euler's Path



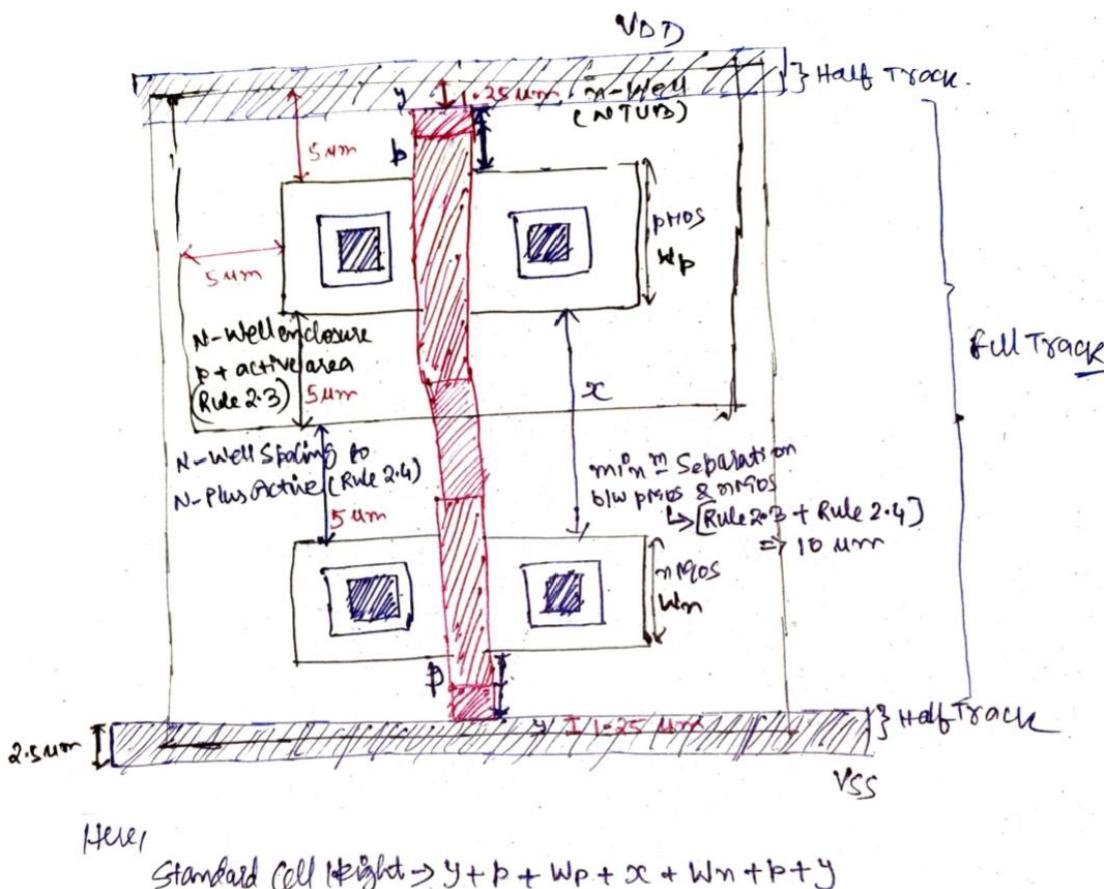
STICK DIAGRAM



LAYOUT



Q) Calculations for Pitch, Cell Height



Pitch (via-overhang)

$$= 2 \left\{ \frac{1}{2} (\text{Metal width}) + (\text{Via-overhang}) \right\} + \text{metal-to-metal spacing}$$

• Metal 1 spacing = 3 umm (Rule 7.2)

• Metal 2 spacing = 3.5 umm (Rule 9.2)

∴ metal-to-metal spacing should be maximum, $S = 3.5 \text{ umm}$

∴ via-overhang (Rule 8.3 & Rule 9.3)

$$\hookrightarrow 1.25 \text{ mm}$$

$$\therefore \text{Pitch} \rightarrow 2 \left\{ \frac{1}{2} (2.5) + 1.25 \right\} + 3.5$$

$$= 2 \{ 1.25 + 1.25 \} + 3.5$$

$$= 2.5 \times 2 + 3.5 = 5 + 3.5 = 8.5 \text{ umm}$$

Pitch = 8.5 umm

for 5T → with via,

$$\begin{aligned} \text{Std. Cell Height} &= \text{Pitch} * (N-1) \\ &= 8.5 * (4) \end{aligned}$$

$$\text{Std. Cell Height} = 34 \text{ umm}$$

for 7T → with via,

$$\text{Std. Cell Height} = 8.5 * (6) = 51 \text{ umm}$$

for 9T → with via,

$$\text{Std. Cell Height} = 8.5 * (8) = 68 \text{ umm}$$

for 11T → with via,

$$\text{Std. Cell Height} = 8.5 * (10) = 85 \text{ umm}$$

I have taken Beta ratio as 1, i.e., Beta = wp/wn = 1; wp=wn

5T	7T	9T	11T
Cell height = $P \cdot N \cdot h \cdot (N-1)$ = 8.5×4 = 34 μm	Cell height = 8.5×6 = 51 μm	Cell height = 8.5×8 = 68 μm	Cell height = 8.5×10 = 85 μm
$W_n = 8.25 \mu\text{m}$ $W_p = 8.25 \mu\text{m}$	$W_n = 16.75 \mu\text{m}$ $W_p = 16.75 \mu\text{m}$	$W_n = 25.25 \mu\text{m}$ $W_p = 25.25 \mu\text{m}$	$W_n = 33.75 \mu\text{m}$ $W_p = 33.75 \mu\text{m}$

for 5T

$$34 = 1.25 + 2.5 + 1w_n + 10 + 1w_p + 2.5 + 1.25$$

$$34 = 17.5 + 2w_n$$

$$2w_n = 16.5$$

$$\boxed{w_n = 8.25 \mu\text{m}} \\ w_p = 8.25 \mu\text{m}$$

$$l = 34 \mu\text{m}$$

for 7T

$$51 \mu\text{m} = 17.5 + 2w_n$$

$$2w_n = 33.5$$

$$\boxed{w_n = 16.75 \mu\text{m}} \\ w_p = 16.75 \mu\text{m}$$

$$l = 34 \mu\text{m}$$

for 9T

$$68 \mu\text{m} = 17.5 + 2w_n$$

$$2w_n = 50.5$$

$$\boxed{l = 34 \mu\text{m}} \\ \boxed{w_n = 25.25 \mu\text{m}} \\ w_p = 25.25 \mu\text{m}$$

for 11T

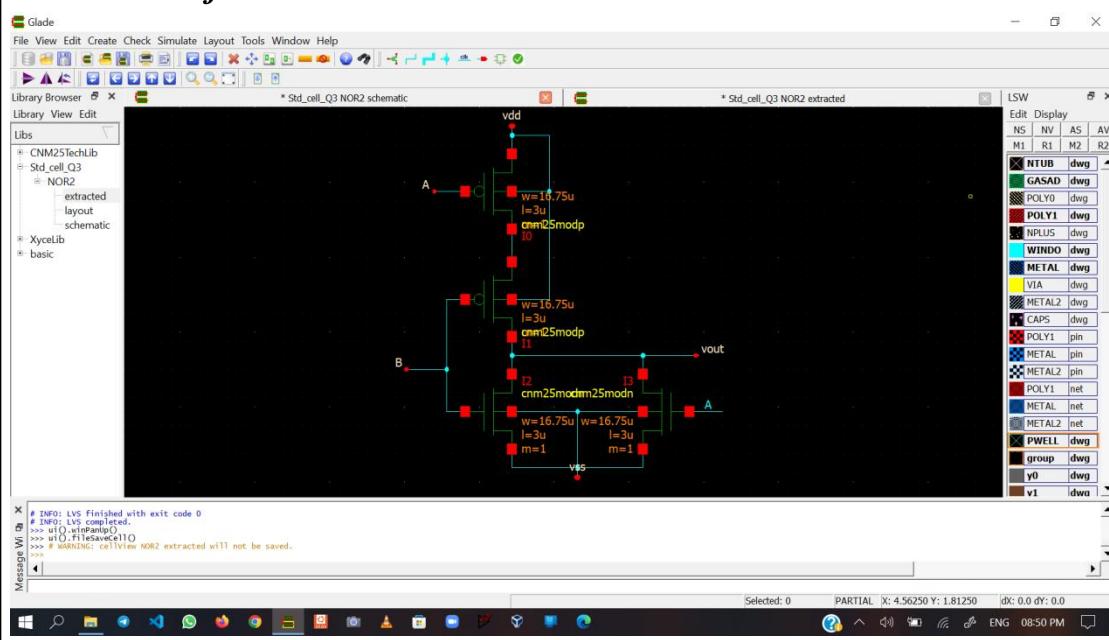
$$85 \mu\text{m} = 17.5 + 2w_n$$

$$2w_n = 67.5$$

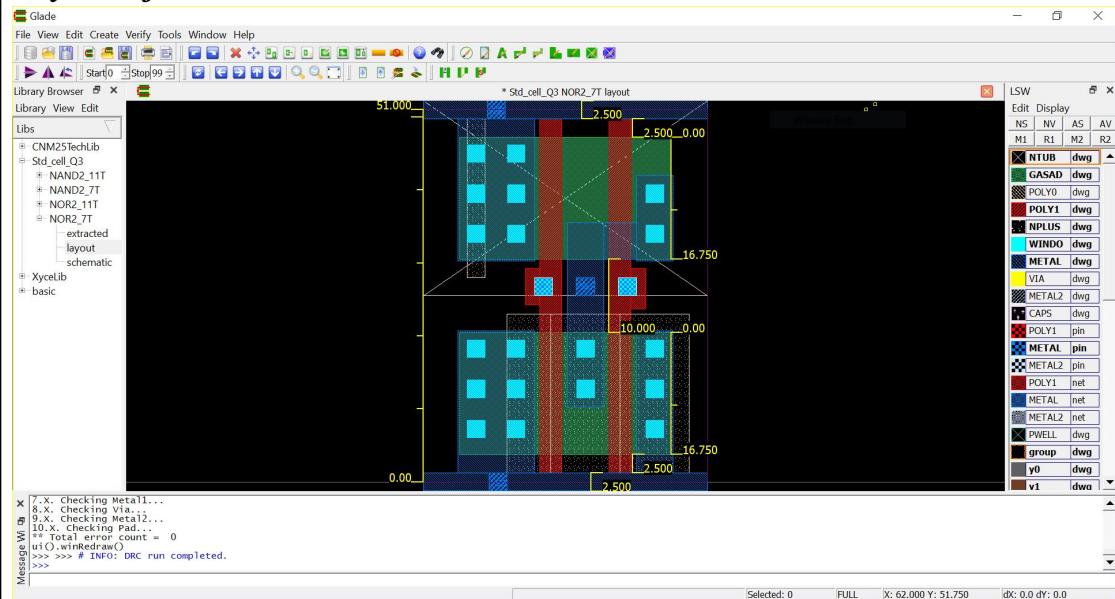
$$\boxed{l = 34 \mu\text{m}} \\ \boxed{w_n = 33.75 \mu\text{m}} \\ w_p = 33.75 \mu\text{m}$$

11T (Track) standard cell is taller than 7T standard cell, that means more metal1 routing space is available within the cell. Hence cells will be faster. Speed of 7T standard cell is less than 11T standard cell. 11T standard cell has more area than 7T standard cell.

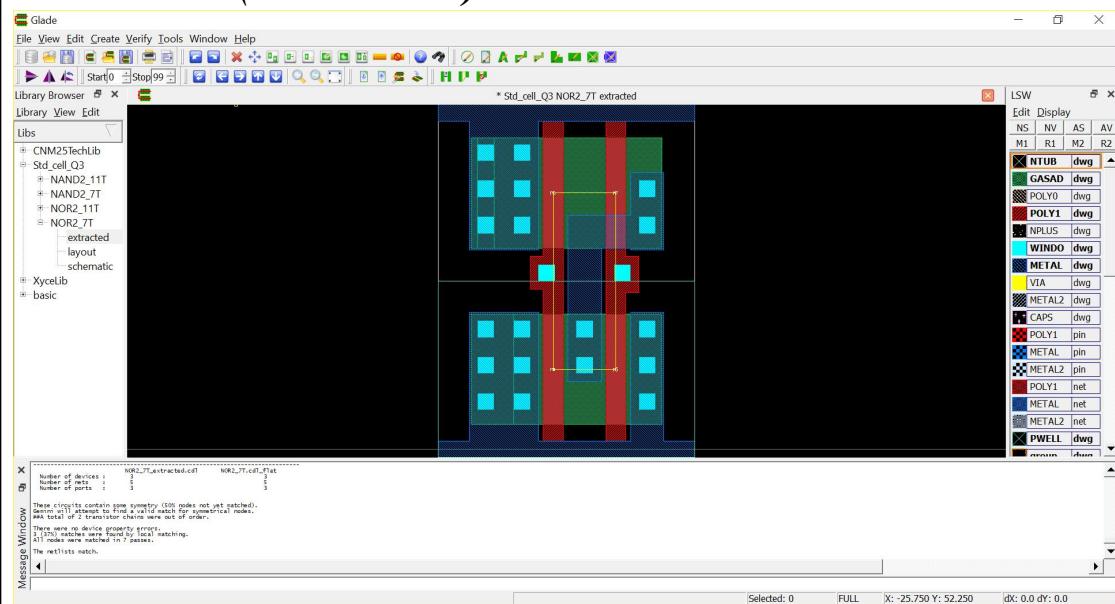
Schematic of NOR2 7T Standard Cell



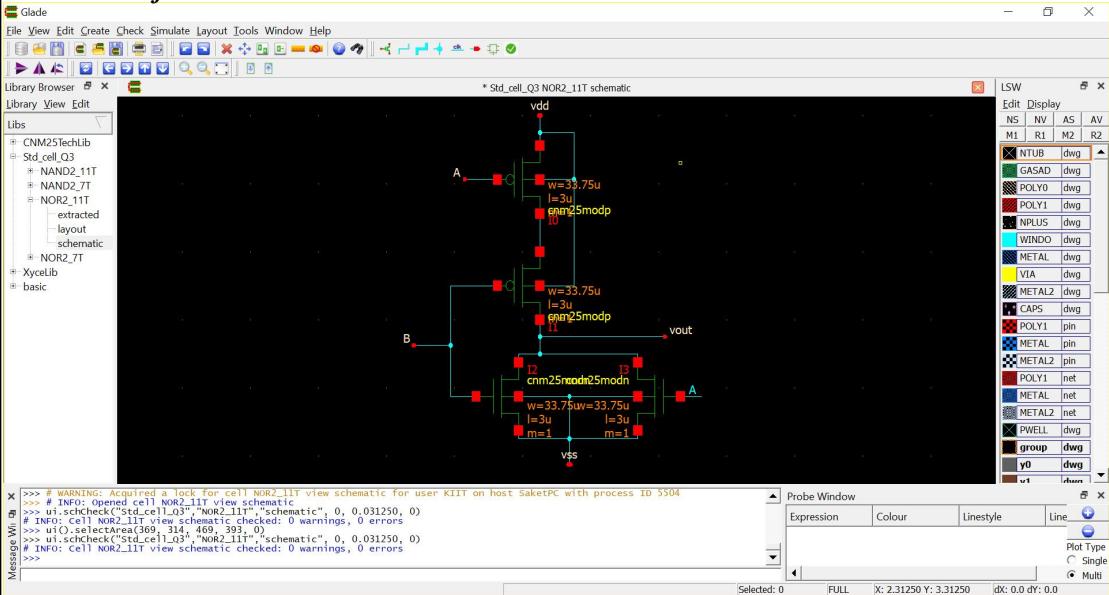
Layout of NOR2_7T Standard cell



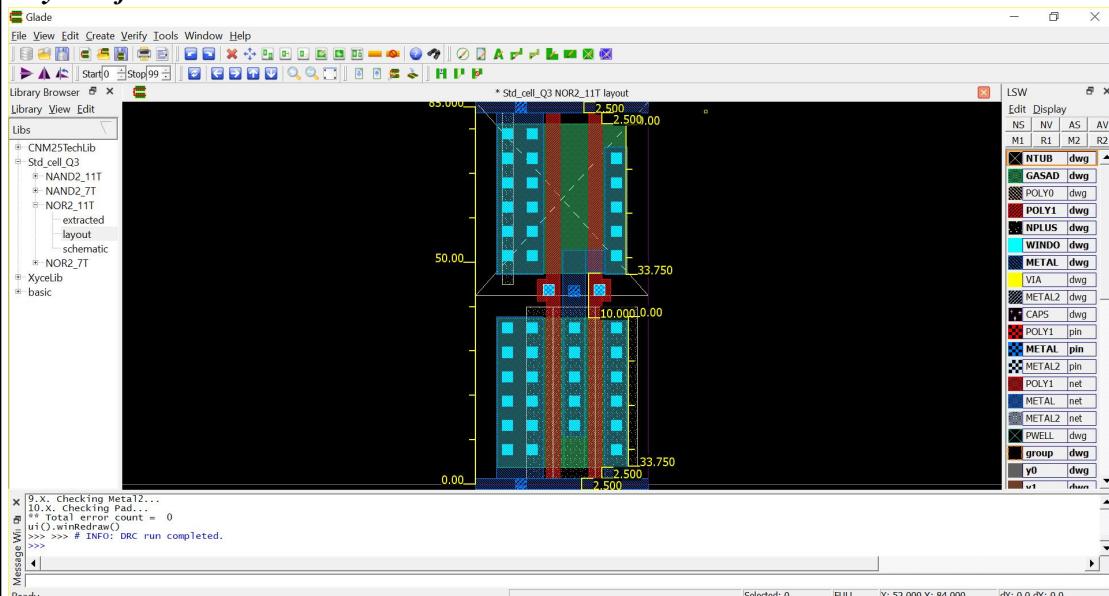
Extracted view(LVS Matched)



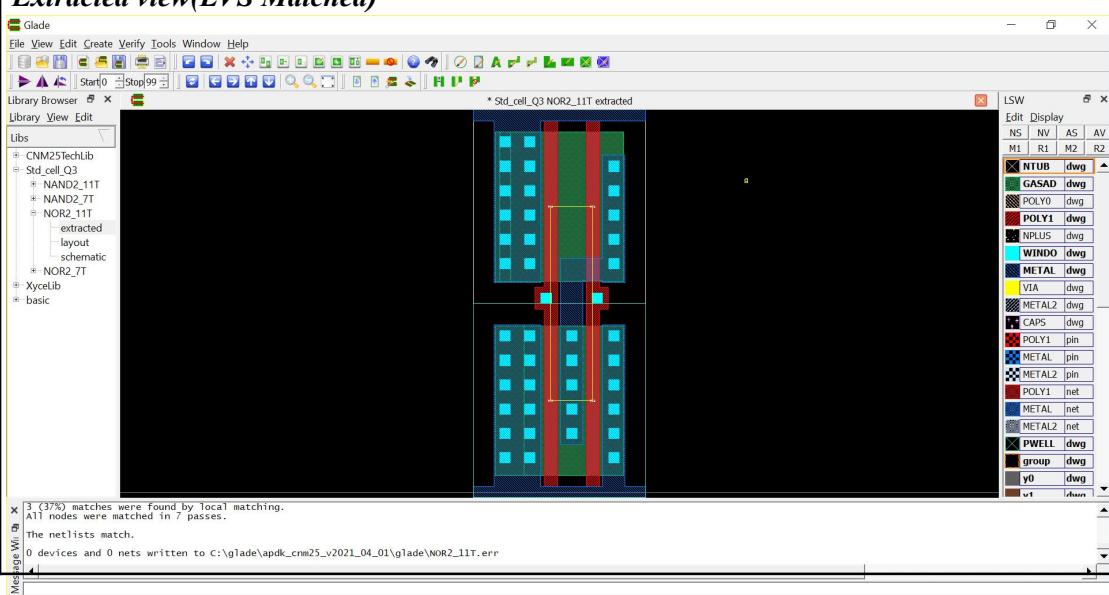
Schematic of NOR2_11T Standard Cell



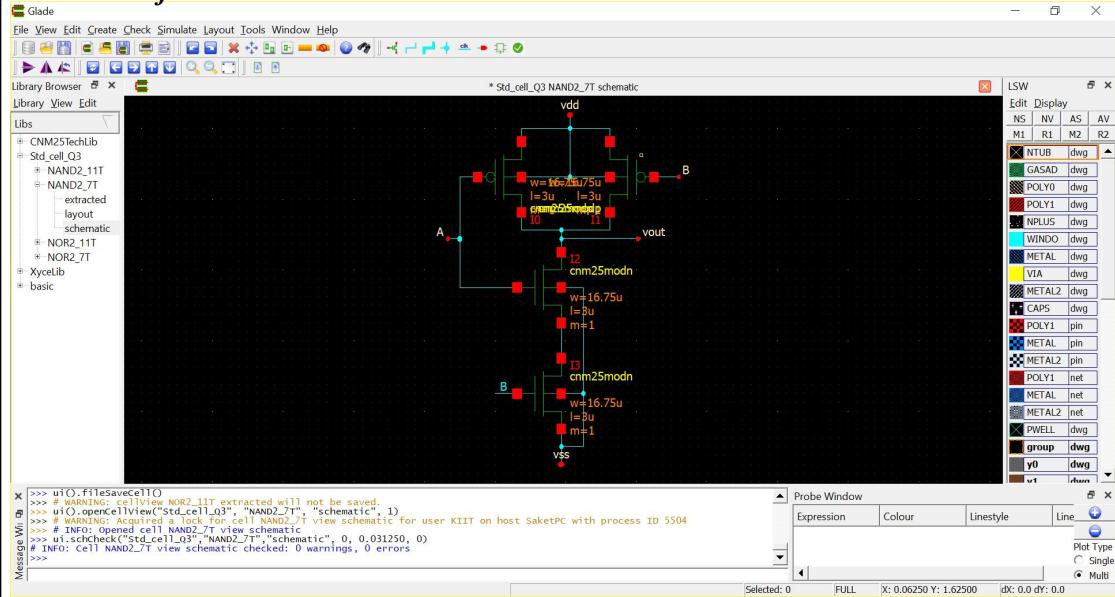
Layout of NOR2_11T Standard Cell



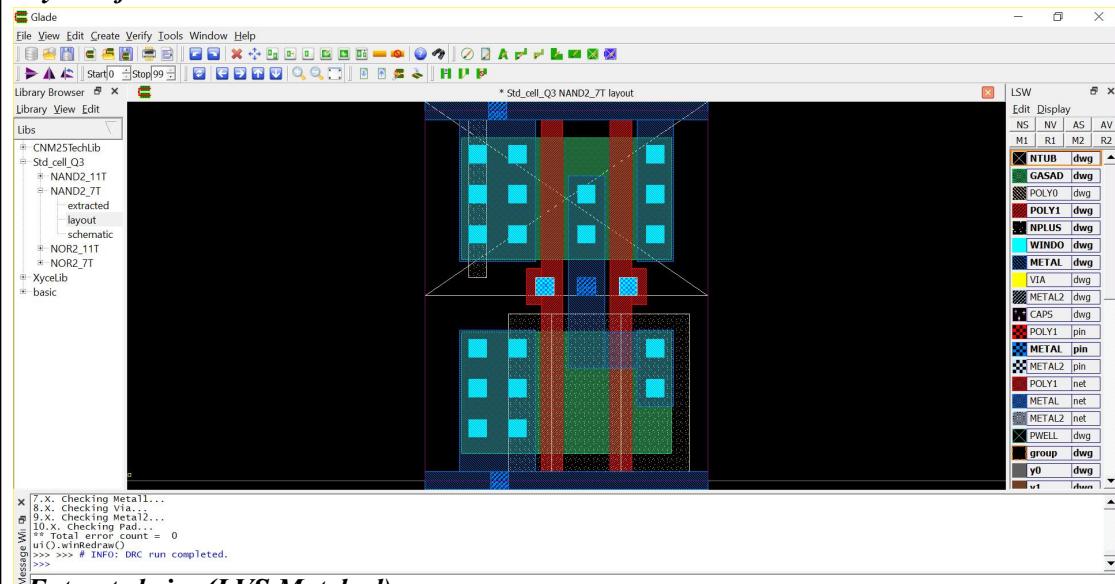
Extracted view(LVS Matched)



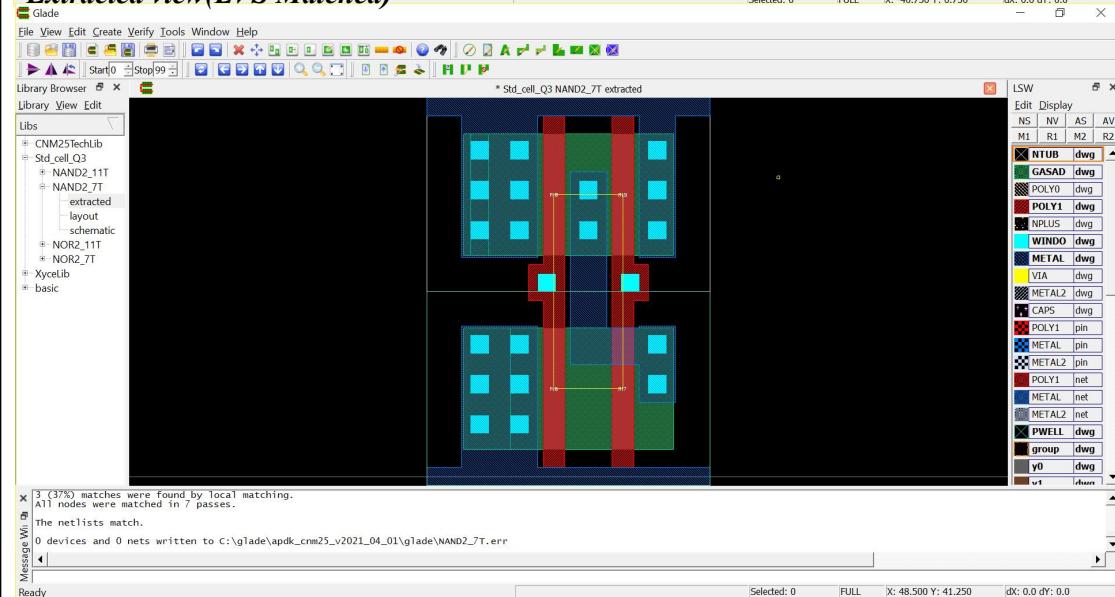
Schematic of NAND2 7T Standard Cell



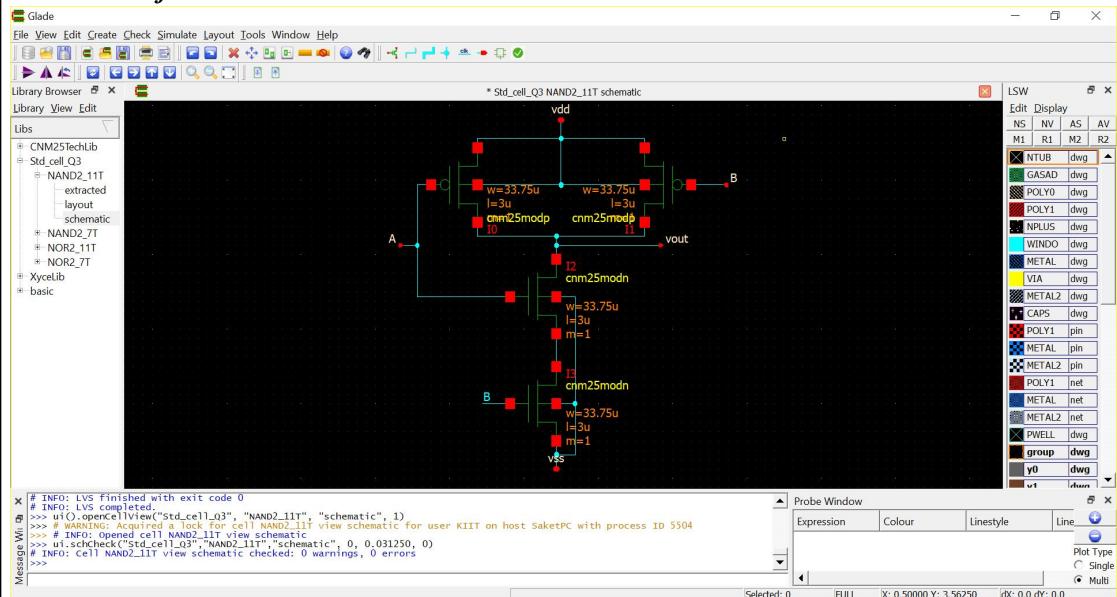
Layout of NAND2 7T Standard Cell



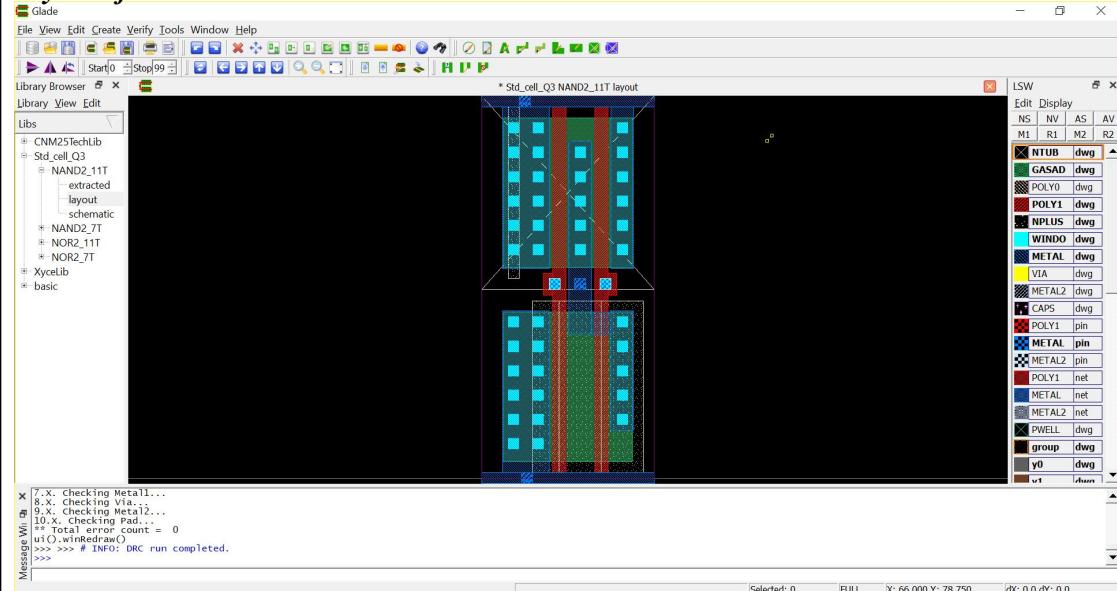
Extracted view(LVS Matched)



Schematic of NAND2 11T Standard Cell



Layout of NAND2 11T Standard Cell



Extracted View (LVS Matched)

