EE671: VLSI Design

Assignment 2

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Question 1

The load capacitance C_L is 154fF.

Part a

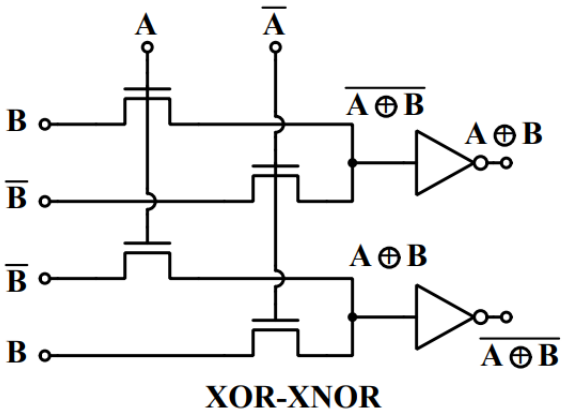

Figure 1: Circuit Diagram of CPL implementation of XOR-XNOR

- $I_{avg} = -52.76\mu A$ (-ve sign indicates current is being drawn from Vdd)
- The output swings between 0 and Vdd as per the XOR logic (the rise, and especially fall times are significant due to the load capacitance)
- The output of switch matrix only swings from 0 to approximately $Vdd - V_{tn}$ due to the NMOS
- We see sudden peaks in current - this is during switching when dynamic power is high. At other times, current is low, but still non zero since PMOS of inverter never fully turns off as input is $Vdd - V_{tn}$ at best.
- Fall time is high since NMOS has to pull down to 0 when PMOS isn't fully off.

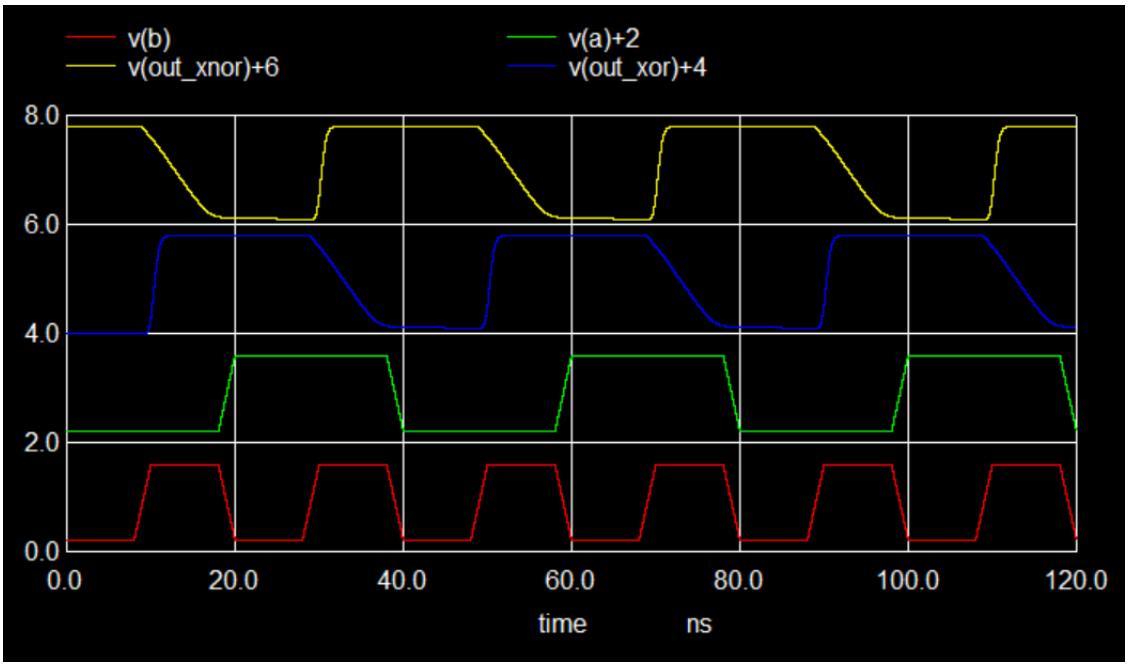

Figure 2: Input and output waveforms of CPL XOR gate

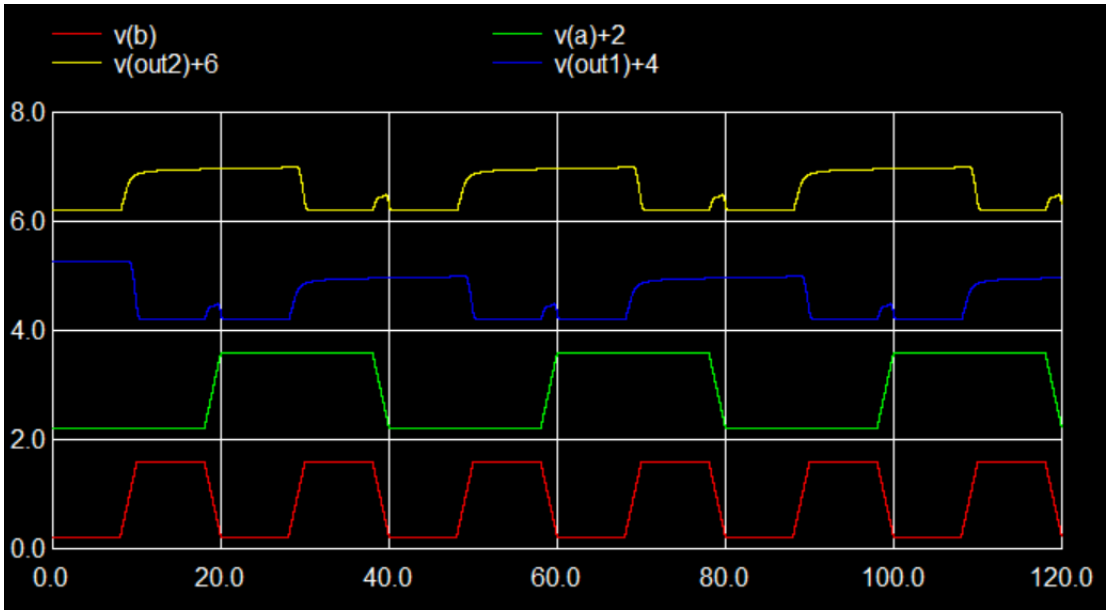

Figure 3: Voltages at output of switch matrix

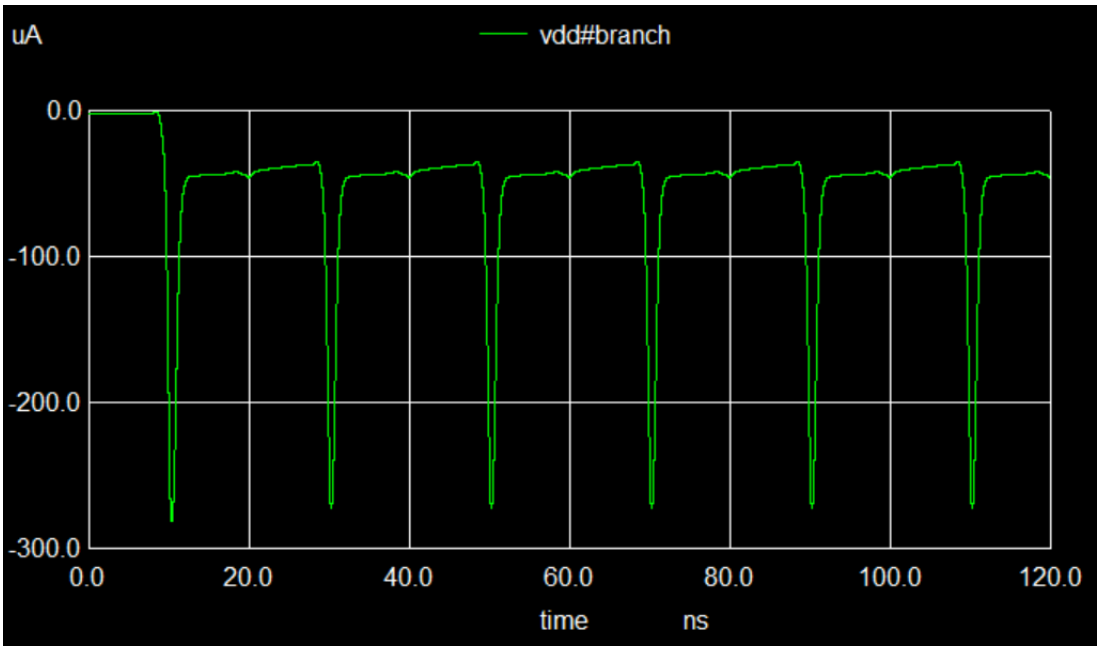

Figure 4: Current waveform

Part b

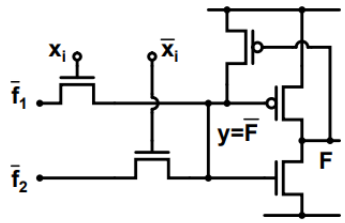

Figure 5: Pull-up PMOS connection

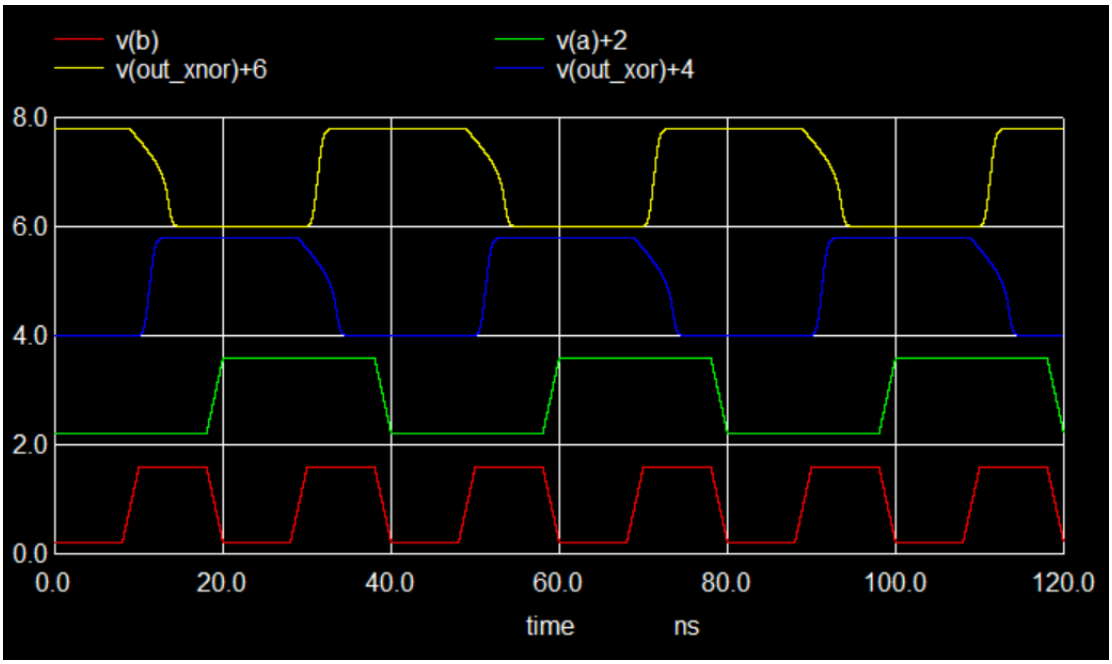

Figure 6: Input and output waveforms of CPL XOR gate after pull up PMOS

- $I_{avg} = -29.92\mu A$ (-ve sign indicates current is being drawn from Vdd)
- The output is now closer to the ideal XOR than previous case.
- The static power is now zero as the pull up transistor takes the input of inverter to Vdd, and the PMOS of inverter is therefore now fully off resulting in 0 static power.
- Outputs of switch matrix now swing rail to rail since PMOS fully brings input to Vdd (and also improves fall time).

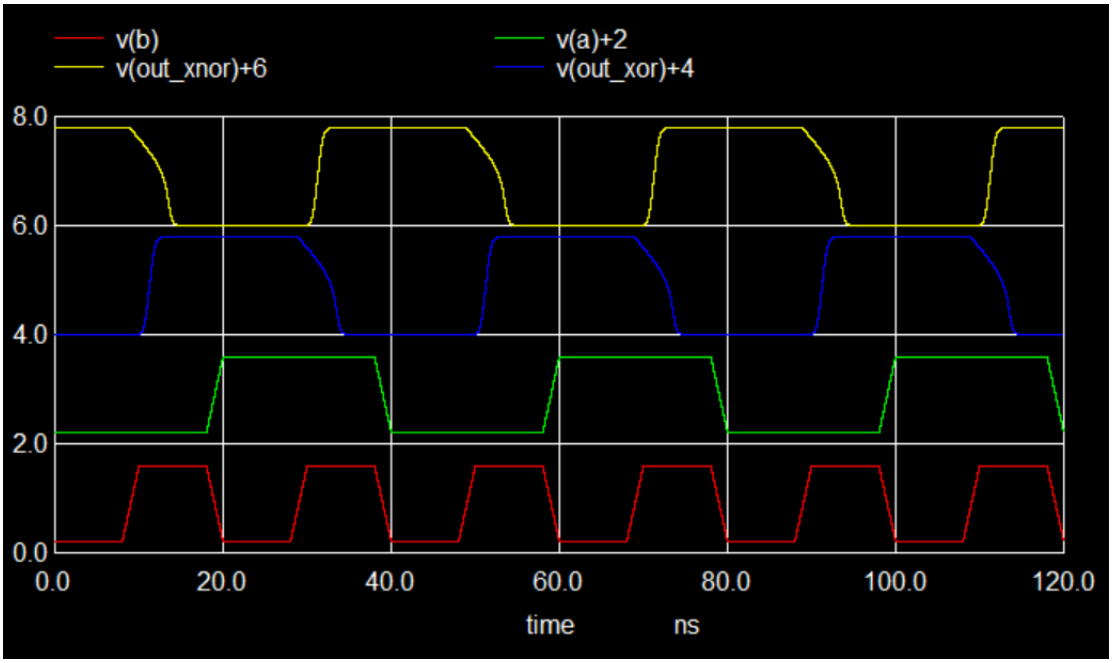

Figure 7: Voltages at output of switch matrix

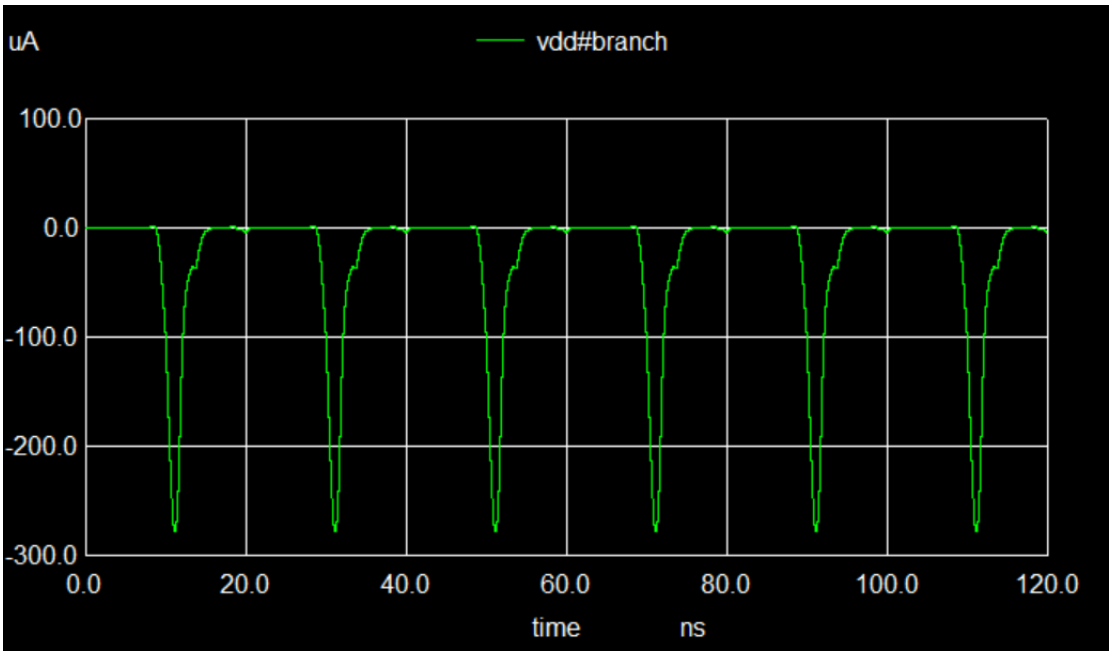

Figure 8: Current waveform

Part c

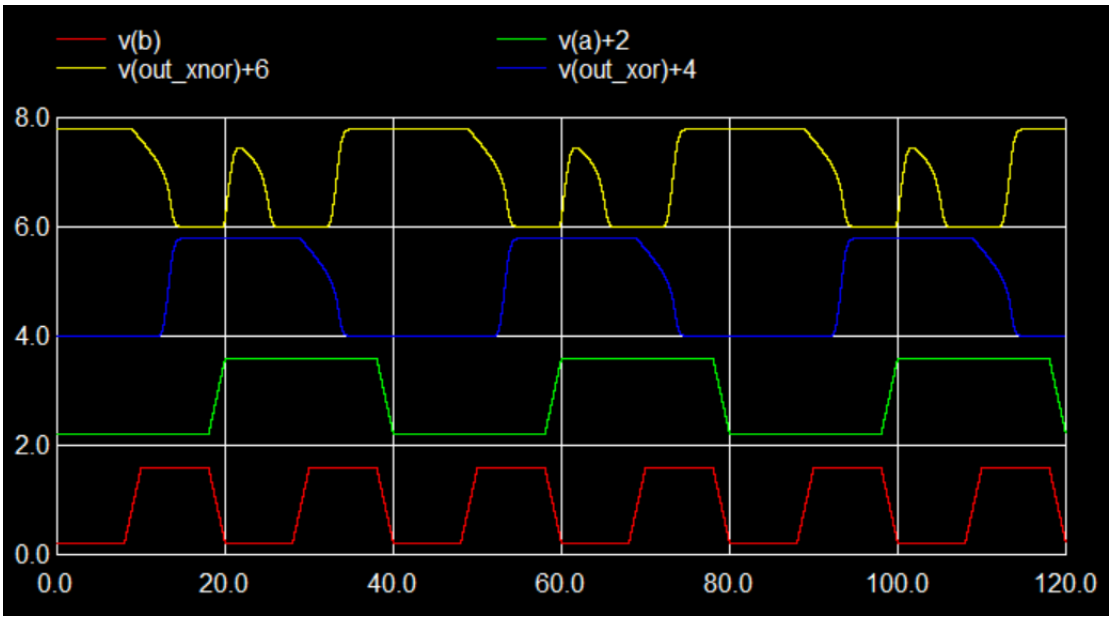

Figure 9: Input and output waveforms of CPL XOR gate after pull up PMOS and delayed complement inputs

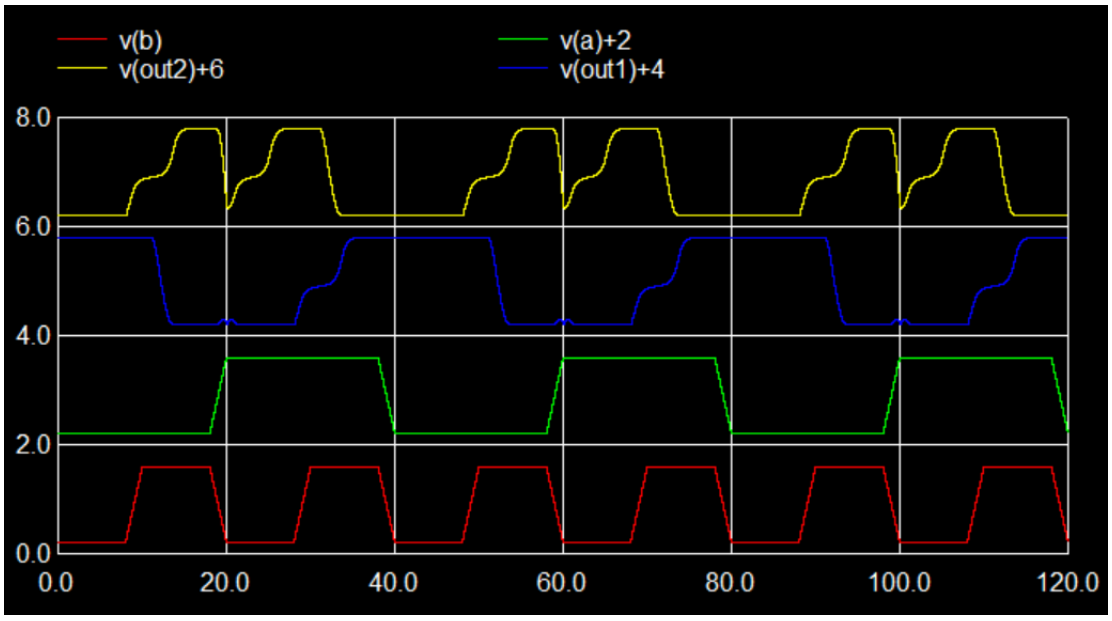

Figure 10: Voltages at output of switch matrix

- $I_{avg} = -42.66\mu A$ (-ve sign indicates current is being drawn from Vdd)
- The output has glitches– the delay in complement results in B and $\bar{B}$ being shorted at input of inverter, which results in an undefined output for the short duration they overlap.
- The current is non zero when the inputs are shorted, leading to higher power consumption.

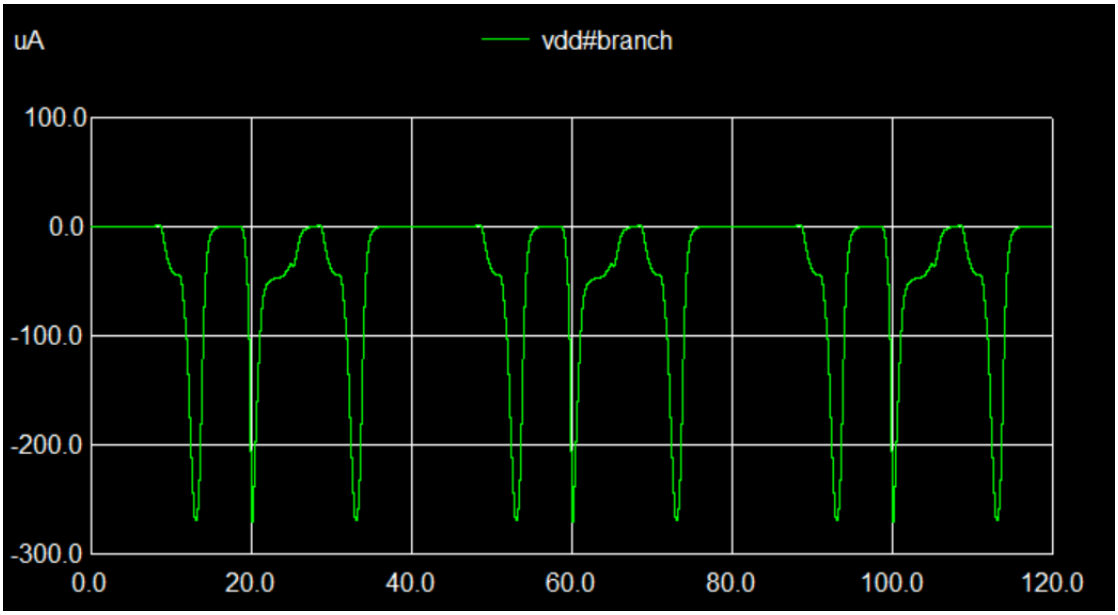

Figure 11: Current waveform

Part d

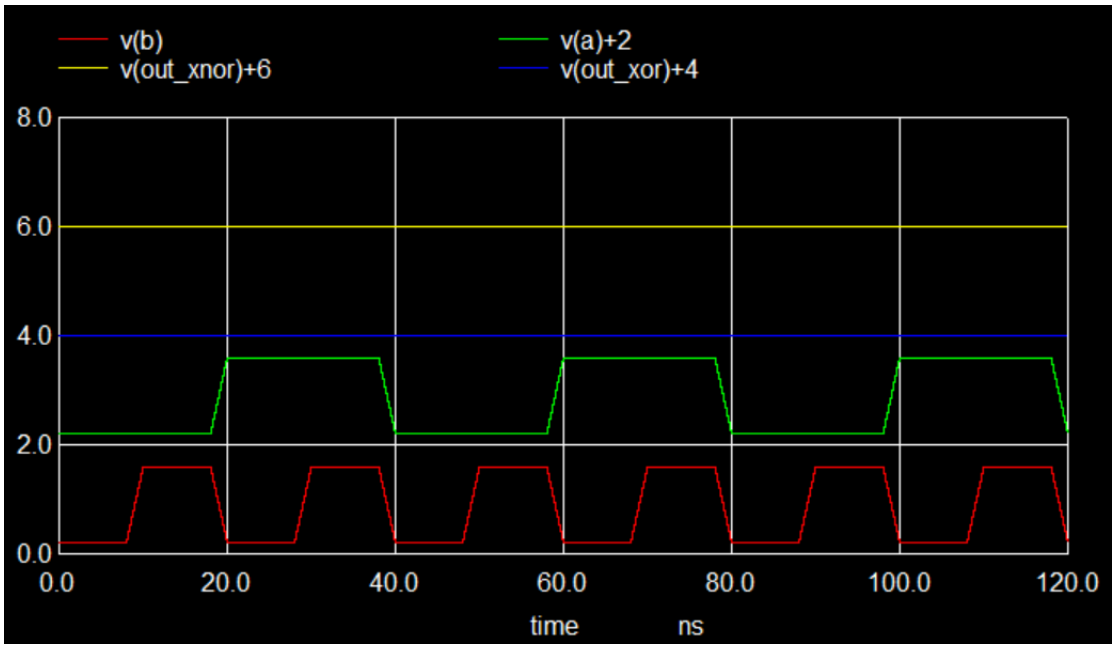

Figure 12: Input and output waveforms of CPL XOR gate after pull up PMOS with 4 times the minimum width

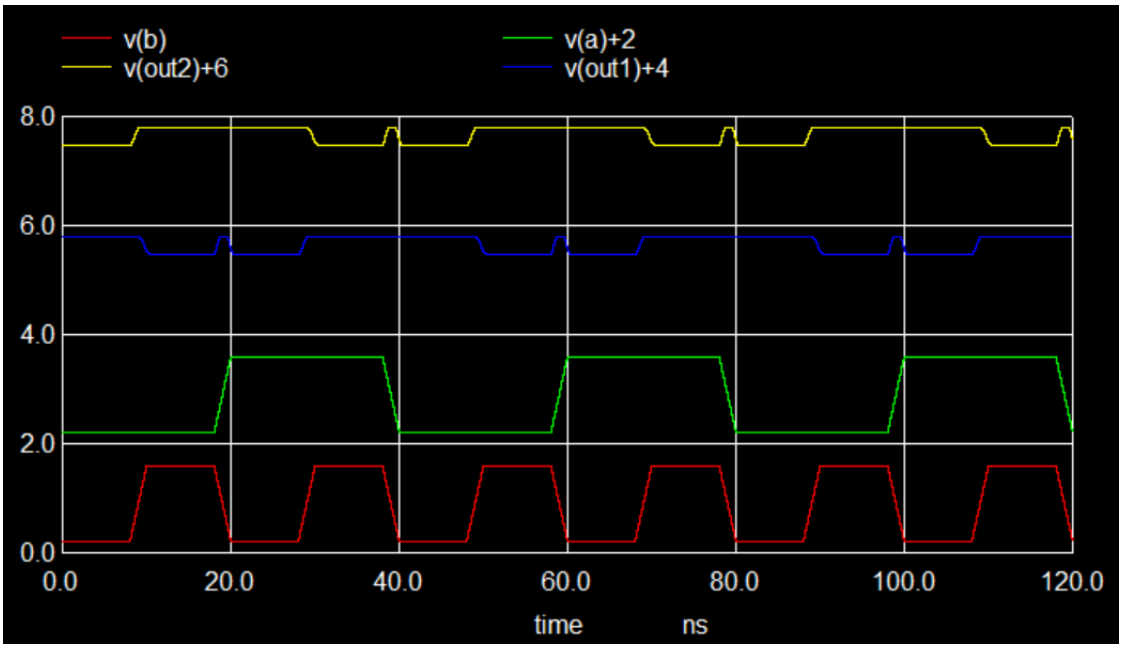

Figure 13: Voltages at output of switch matrix

- $I_{avg} = -111.565\mu A$ (-ve sign indicates current is being drawn from Vdd)
- The PMOS, being large, keeps the input of inverters permanently at almost Vdd, resulting in a constant 0 output at inverter.

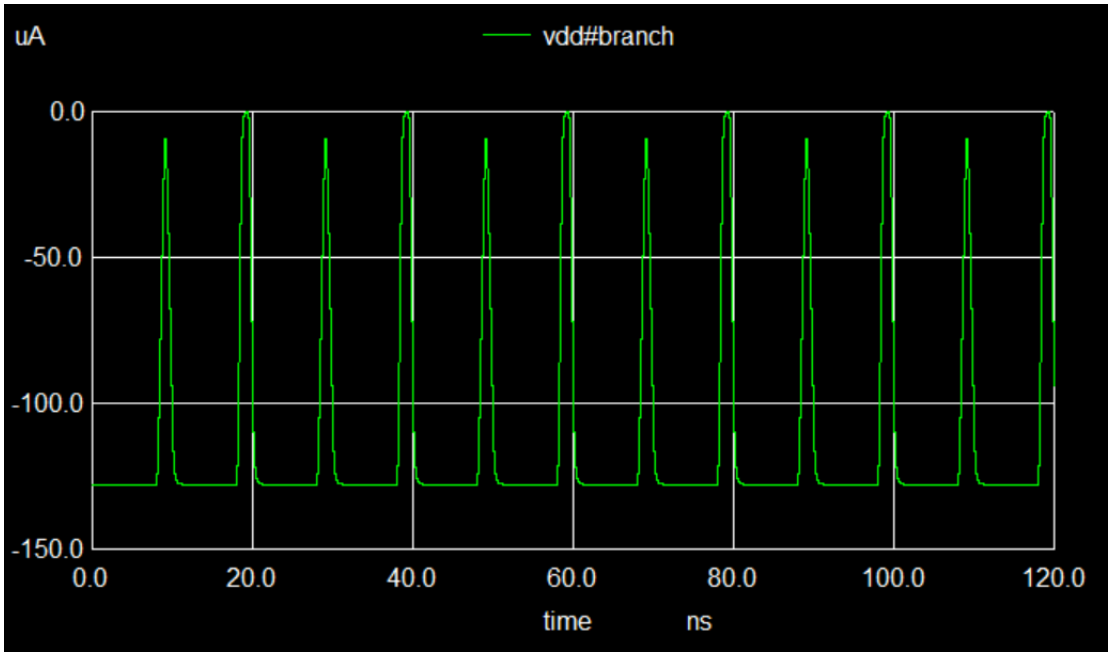

Figure 14: Current waveform

- The current is almost always high since it is essentially pseudo NMOS, and the pullup PMOS is always on along with the NMOS in switch matrix.

Question 2

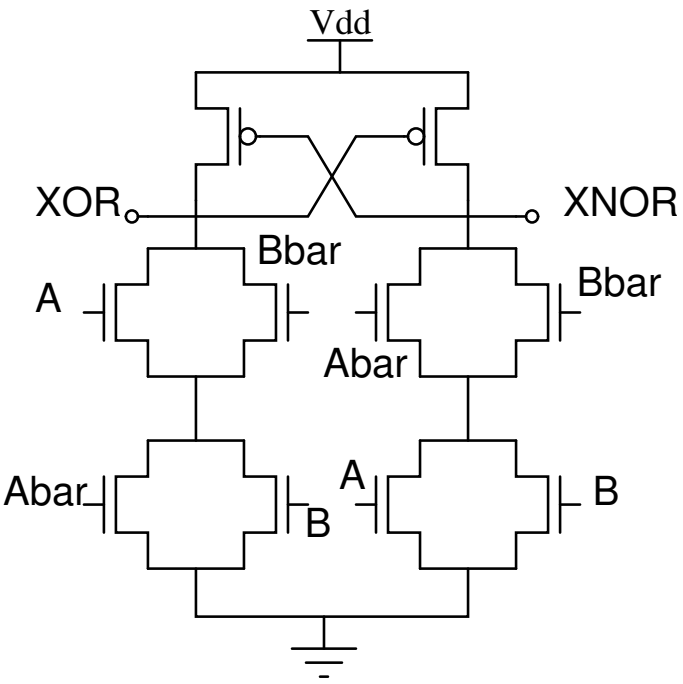

Figure 15: Circuit diagram

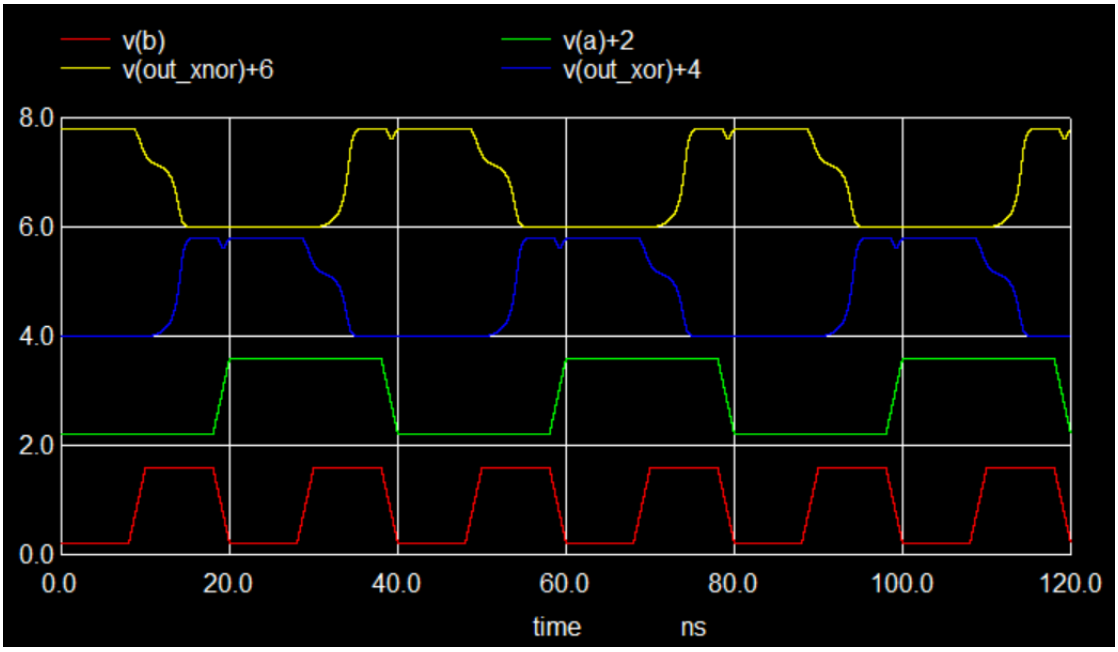

Figure 16: Input and output waveforms of CVSL XOR

- We see that the outputs are XOR and XNOR of inputs A and B.
- The NMOS transistors are all doubled in accordance to series parallel rules.

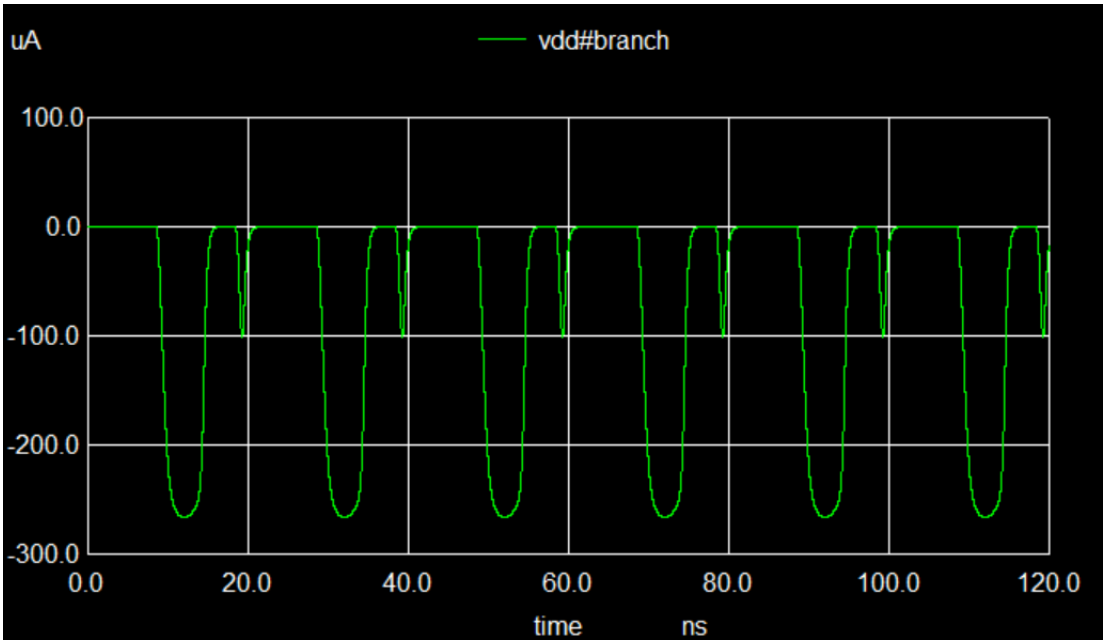

Figure 17: Current waveform

```
*CPL XOR
* Unit Inverter
.subckt inv supply Inp Output

.param Len = 0.18U
.param Wp = 1.275U Wn = 0.407U
.param Area_p = {2*Len*Wp} Area_n = {2*Len*Wn}
.param Per_p = {2*(Wp + 2*Len)} Per_n = {2*(Wn + 2*Len)}

MP1 Output Inp Supply Supply cmosp
+ L = Len W = Wp AD = Area_p AS = Area_p PD = Per_p PS = Per_p
MN1 Output Inp 0 0 cmosn
+ L = Len W = Wn AD = Area_n AS = Area_n PD = Per_n PS = Per_n
.ends


* Switch Matrix
.subckt swmat In1 In2 In3 In4 con conbar Out1 Out2
MN1 In1 con Out1 0 cmosn
+ L=0.18U W=0.24U AD = 86.4fF AS = 86.4fF PD = 1.2U PS = 1.2U
MN2 In2 conbar Out1 0 cmosn
+ L=0.18U W=0.24U AD = 86.4fF AS = 86.4fF PD = 1.2U PS = 1.2U
MN3 In3 con Out2 0 cmosn
+ L=0.18U W=0.24U AD = 86.4fF AS = 86.4fF PD = 1.2U PS = 1.2U
MN4 In4 conbar Out2 0 cmosn
+ L=0.18U W=0.24U AD = 86.4fF AS = 86.4fF PD = 1.2U PS = 1.2U
* Loads representing wiring capacitance
C1 Out1 0 50fF
C2 Out2 0 50fF
.ends

vdd supply 0 dc 1.8

* Device under test
```

```
x_swmat B Bbar Bbar B A Abar Out1 Out2 swmat
x_inv1 supply Out1 out_xor inv
x_inv2 supply Out2 out_xnor inv

* Load Capacitor
C3 out_xor 0 154f
C4 out_xnor 0 154f

.param Trep1= 40n
.param Trep2 = {Trep1/2.0}
.param Trf = {Trep1/20.0}
.param Tw1 = {Trep1/2.0 - Trf}
.param Tw2 = {Trep2/2.0 - Trf}
.param hival=1.6
.param loval=0.2
V1 A 0 DC 0 PULSE({loval} {hival} {Tw1} {Trf} {Trf} {Tw1} {Trep1})
V2 Abar 0 DC 0 PULSE({hival} {loval} {Tw1} {Trf} {Trf} {Tw1} {Trep1})
V3 B 0 DC 0 PULSE({loval} {hival} {Tw2} {Trf} {Trf} {Tw2} {Trep2})
V4 Bbar 0 DC 0 PULSE({hival} {loval} {Tw2} {Trf} {Trf} {Tw2} {Trep2})

.tran 1pS {3*Trep1} 0nS

.include models-180nm
.control
run
plot V(A)+2 V(B) V(out_xor)+4 V(out_xnor)+6
plot V(A)+2 V(B) V(out1)+4 V(out2)+6
plot vdd#branch
let i_vdd = vdd#branch
let t1 = 0ns
let t2 = 120ns
meas tran i_avg AVG i_vdd from = t1 to = t2
print i_avg
.endc
.options savecurrents
.end
```

```
* Unit Inverter
.subckt inv supply Inp Output

.param Len = 0.18U
.param Wp = 1.275U Wn = 0.407U
.param Area_p = {2*Len*Wp} Area_n = {2*Len*Wn}
.param Per_p = {2*(Wp + 2*Len)} Per_n = {2*(Wn + 2*Len)}

MP1 Output Inp Supply Supply cmosp
+ L = Len W = Wp AD = Area_p AS = Area_p PD = Per_p PS = Per_p
MN1 Output Inp 0 0 cmosn
+ L = Len W = Wn AD = Area_n AS = Area_n PD = Per_n PS = Per_n
.ends


* Switch Matrix
.subckt swmat In1 In2 In3 In4 con conbar Out1 Out2
MN1 In1 con Out1 0 cmosn
+ L=0.18U W=0.24U AD = 86.4fF AS = 86.4fF PD = 1.2U PS = 1.2U
MN2 In2 conbar Out1 0 cmosn
+ L=0.18U W=0.24U AD = 86.4fF AS = 86.4fF PD = 1.2U PS = 1.2U
```

```
MN3 In3 con Out2 0 cmosn
+ L=0.18U W=0.24U AD = 86.4fF AS = 86.4fF PD = 1.2U PS = 1.2U
MN4 In4 conbar Out2 0 cmosn
+ L=0.18U W=0.24U AD = 86.4fF AS = 86.4fF PD = 1.2U PS = 1.2U
* Loads representing wiring capacitance
C1 Out1 0 50fF
C2 Out2 0 50fF
.ends

vdd supply 0 dc 1.8

* Device under test
x_swmat B Bbar Bbar B A Abar Out1 Out2 swmat
x_inv1 supply Out1 out_xor inv
x_inv2 supply Out2 out_xnor inv

* Load Capacitor
C3 out_xor 0 154f
C4 out_xnor 0 154f

.param Len = 0.18U
.param Wp = 0.24U
.param Area_p = {2*Len*Wp}
.param Per_p = {2*(Wp + 2*Len)}

mp_out1 Out1 out_xor supply supply cmosp
+ L = Len W = Wp AD = Area_p AS = Area_p PD = Per_p PS = Per_p

mp_out2 Out2 out_xnor supply supply cmosp
+ L = Len W = Wp AD = Area_p AS = Area_p PD = Per_p PS = Per_p

.param Trep1= 40n
.param Trep2 = {Trep1/2.0}
.param Trf = {Trep1/20.0}
.param Tw1 = {Trep1/2.0 - Trf}
.param Tw2 = {Trep2/2.0 - Trf}
.param hival=1.6
.param loval=0.2
V1 A 0 DC 0 PULSE({loval} {hival} {Tw1} {Trf} {Trf} {Tw1} {Trep1})
V2 Abar 0 DC 0 PULSE({hival} {loval} {Tw1} {Trf} {Trf} {Tw1} {Trep1})
V3 B 0 DC 0 PULSE({loval} {hival} {Tw2} {Trf} {Trf} {Tw2} {Trep2})
V4 Bbar 0 DC 0 PULSE({hival} {loval} {Tw2} {Trf} {Trf} {Tw2} {Trep2})

.tran 1pS {3*Trep1} 0nS

.include models-180nm
.control
run
plot V(A)+2 V(B) V(out_xor)+4 V(out_xnor)+6
plot V(A)+2 V(B) V(out1)+4 V(out2)+6
plot vdd#branch
let i_vdd = vdd#branch
let t1 = 0ns
let t2 = 120ns
meas tran i_avg AVG i_vdd from = t1 to = t2
print i_avg
.endc
.options savecurrents
```

```
.end
```

```
* Unit Inverter
.subckt inv supply Inp Output

.param Len = 0.18U
.param Wp = 1.275U Wn = 0.407U
.param Area_p = {2*Len*Wp} Area_n = {2*Len*Wn}
.param Per_p = {2*(Wp + 2*Len)} Per_n = {2*(Wn + 2*Len)}

MP1 Output Inp Supply Supply cmosp
+ L = Len W = Wp AD = Area_p AS = Area_p PD = Per_p PS = Per_p
MN1 Output Inp 0 0 cmosn
+ L = Len W = Wn AD = Area_n AS = Area_n PD = Per_n PS = Per_n
.ends


* Switch Matrix
.subckt swmat In1 In2 In3 In4 con conbar Out1 Out2
MN1 In1 con Out1 0 cmosn
+ L=0.18U W=0.24U AD = 86.4fF AS = 86.4fF PD = 1.2U PS = 1.2U
MN2 In2 conbar Out1 0 cmosn
+ L=0.18U W=0.24U AD = 86.4fF AS = 86.4fF PD = 1.2U PS = 1.2U
MN3 In3 con Out2 0 cmosn
+ L=0.18U W=0.24U AD = 86.4fF AS = 86.4fF PD = 1.2U PS = 1.2U
MN4 In4 conbar Out2 0 cmosn
+ L=0.18U W=0.24U AD = 86.4fF AS = 86.4fF PD = 1.2U PS = 1.2U
* Loads representing wiring capacitance
C1 Out1 0 50fF
C2 Out2 0 50fF
.ends

vdd supply 0 dc 1.8

* Device under test
x_swmat B Bbar Bbar B A Abar Out1 Out2 swmat
x_inv1 supply Out1 out_xor inv
x_inv2 supply Out2 out_xnor inv

* Load Capacitor
C3 out_xor 0 154f
C4 out_xnor 0 154f

.param Len = 0.18U
.param Wp = 0.24U
.param Area_p = {2*Len*Wp}
.param Per_p = {2*(Wp + 2*Len)}

mp_out1 Out1 out_xor supply supply cmosp
+ L = Len W = Wp AD = Area_p AS = Area_p PD = Per_p PS = Per_p

mp_out2 Out2 out_xnor supply supply cmosp
+ L = Len W = Wp AD = Area_p AS = Area_p PD = Per_p PS = Per_p

.param Trep1= 40n
.param Trep2 = {Trep1/2.0}
.param Trf = {Trep1/20.0}
.param Tw1 = {Trep1/2.0 - Trf}
```

```
.param Tw2 = {Trep2/2.0 - Trf}
.param hival=1.6
.param loval=0.2
V1 A 0 DC 0 PULSE({loval} {hival} {Tw1} {Trf} {Trf} {Tw1} {Trep1})
V2 Abar 0 DC 0 PULSE({hival} {loval} {Tw1+2ns} {Trf} {Trf} {Tw1} {Trep1
   })
V3 B 0 DC 0 PULSE({loval} {hival} {Tw2} {Trf} {Trf} {Tw2} {Trep2})
V4 Bbar 0 DC 0 PULSE({hival} {loval} {Tw2+2ns} {Trf} {Trf} {Tw2} {Trep2
   })

.tran 1pS {3*Trep1} 0nS

.include models-180nm
.control
run
plot V(A)+2 V(B) V(out_xor)+4 V(out_xnor)+6
plot V(A)+2 V(B) V(out1)+4 V(out2)+6
plot vdd#branch
let i_vdd = vdd#branch
let t1 = 0ns
let t2 = 120ns
meas tran i_avg AVG i_vdd from = t1 to = t2
print i_avg
.endc
.options savecurrents
.end
```

```
* Unit Inverter
.subckt inv supply Inp Output

.param Len = 0.18U
.param Wp = 1.275U Wn = 0.407U
.param Area_p = {2*Len*Wp} Area_n = {2*Len*Wn}
.param Per_p = {2*(Wp + 2*Len)} Per_n = {2*(Wn + 2*Len)}

MP1 Output Inp Supply Supply cmosp
+ L = Len W = Wp AD = Area_p AS = Area_p PD = Per_p PS = Per_p
MN1 Output Inp 0 0 cmosn
+ L = Len W = Wn AD = Area_n AS = Area_n PD = Per_n PS = Per_n
.ends


* Switch Matrix
.subckt swmat In1 In2 In3 In4 con conbar Out1 Out2
MN1 In1 con Out1 0 cmosn
+ L=0.18U W=0.24U AD = 86.4fF AS = 86.4fF PD = 1.2U PS = 1.2U
MN2 In2 conbar Out1 0 cmosn
+ L=0.18U W=0.24U AD = 86.4fF AS = 86.4fF PD = 1.2U PS = 1.2U
MN3 In3 con Out2 0 cmosn
+ L=0.18U W=0.24U AD = 86.4fF AS = 86.4fF PD = 1.2U PS = 1.2U
MN4 In4 conbar Out2 0 cmosn
+ L=0.18U W=0.24U AD = 86.4fF AS = 86.4fF PD = 1.2U PS = 1.2U
* Loads representing wiring capacitance
C1 Out1 0 50fF
C2 Out2 0 50fF
.ends

vdd supply 0 dc 1.8
```

```

* Device under test
x_swmat B Bbar Bbar B A Abar Out1 Out2 swmat
x_inv1 supply Out1 out_xor inv
x_inv2 supply Out2 out_xnor inv

* Load Capacitor
C3 out_xor 0 154f
C4 out_xnor 0 154f

.param Len = 0.18U
.param Wp = 0.96U
.param Area_p = {2*Len*Wp}
.param Per_p = {2*(Wp + 2*Len)}

mp_out1 Out1 out_xor supply supply cmosp
+ L = Len W = Wp AD = Area_p AS = Area_p PD = Per_p PS = Per_p

mp_out2 Out2 out_xnor supply supply cmosp
+ L = Len W = Wp AD = Area_p AS = Area_p PD = Per_p PS = Per_p

.param Trep1= 40n
.param Trep2 = {Trep1/2.0}
.param Trf = {Trep1/20.0}
.param Tw1 = {Trep1/2.0 - Trf}
.param Tw2 = {Trep2/2.0 - Trf}
.param hival=1.6
.param loval=0.2
V1 A 0 DC 0 PULSE({loval} {hival} {Tw1} {Trf} {Trf} {Tw1} {Trep1})
V2 Abar 0 DC 0 PULSE({hival} {loval} {Tw1} {Trf} {Trf} {Tw1} {Trep1})
V3 B 0 DC 0 PULSE({loval} {hival} {Tw2} {Trf} {Trf} {Tw2} {Trep2})
V4 Bbar 0 DC 0 PULSE({hival} {loval} {Tw2} {Trf} {Trf} {Tw2} {Trep2})

.tran 1pS {3*Trep1} 0nS

.include models-180nm
.control
run
plot V(A)+2 V(B) V(out_xor)+4 V(out_xnor)+6
plot V(A)+2 V(B) V(out1)+4 V(out2)+6
plot vdd#branch
let i_vdd = vdd#branch
let t1 = 0ns
let t2 = 120ns
meas tran i_avg AVG i_vdd from = t1 to = t2
print i_avg
.endc
.options savecurrents
.end
```

```
*CVSL Half Ckt
.subckt halfckt g x y z w Supply out

.param Len = 0.18U
.param Wp = 1.275U Wn = 0.814U
.param Area_p = {2*Len*Wp} Area_n = {2*Len*Wn}
.param Per_p = {2*(Wp + 2*Len)} Per_n = {2*(Wn + 2*Len)}

```

```
MP1 out g Supply Supply cmosp
+ L = Len W = Wp AD = Area_p AS = Area_p PD = Per_p PS = Per_p
MNx out x out1 0 cmosn
+ L = Len W = Wn AD = Area_n AS = Area_n PD = Per_n PS = Per_n
MNy out y out1 0 cmosn
+ L = Len W = Wn AD = Area_n AS = Area_n PD = Per_n PS = Per_n
MNz out1 z 0 0 cmosn
+ L = Len W = Wn AD = Area_n AS = Area_n PD = Per_n PS = Per_n
MNw out1 w 0 0 cmosn
+ L = Len W = Wn AD = Area_n AS = Area_n PD = Per_n PS = Per_n
.ends

vdd supply 0 dc 1.8
x1 out_xnor A Bbar Abar B Supply out_xor halfckt
x2 out_xor Abar Bbar A B Supply out_xnor halfckt

* Load Capacitor
C3 out_xor 0 154f
C4 out_xnor 0 154f

.param Len = 0.18U
.param Wp = 0.96U
.param Area_p = {2*Len*Wp}
.param Per_p = {2*(Wp + 2*Len)}

.param Trep1= 40n
.param Trep2 = {Trep1/2.0}
.param Trf = {Trep1/20.0}
.param Tw1 = {Trep1/2.0 - Trf}
.param Tw2 = {Trep2/2.0 - Trf}
.param hival=1.6
.param loval=0.2
V1 A 0 DC 0 PULSE({loval} {hival} {Tw1} {Trf} {Trf} {Tw1} {Trep1})
V2 Abar 0 DC 0 PULSE({hival} {loval} {Tw1} {Trf} {Trf} {Tw1} {Trep1})
V3 B 0 DC 0 PULSE({loval} {hival} {Tw2} {Trf} {Trf} {Tw2} {Trep2})
V4 Bbar 0 DC 0 PULSE({hival} {loval} {Tw2} {Trf} {Trf} {Tw2} {Trep2})

.tran 1pS {3*Trep1} 0nS

.include models-180nm
.control
run
plot V(A)+2 V(B) V(out_xor)+4 V(out_xnor)+6
plot vdd#branch
let i_vdd = vdd#branch
let t1 = 0ns
let t2 = 120ns
meas tran i_avg AVG i_vdd from = t1 to = t2
print i_avg
.endc
.options savecurrents
.end
```