EE671: VLSI Design

Assignment 5

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The following delays are used for the logic gates required.

Function	**Delay (in ps)**
AND	44
A + B.C	58
XOR	68
A.B + C.(A + B)	68

Design

- Initially, the maximum number of partial product bits in any column is 9.
- We need 4 stages of reduction ($9 \longrightarrow 6 \longrightarrow 4 \longrightarrow 3 \longrightarrow 2$)
- For each stage of reduction, as per the Dadda algorithm, we choose the least number of smallest adders required so that the capacity of the next stage is not exceeded.
- From the dot diagram below, we see that 48 (8 + 16 + 11 + 13) Full Adders and 8 (4 + 2 + 1 + 1) Half Adders are needed.
- Once we reduce it to 2 vectors, we use a 16-bit logarithmic Brent Kung adder to obtain the final MAC sum and carry results

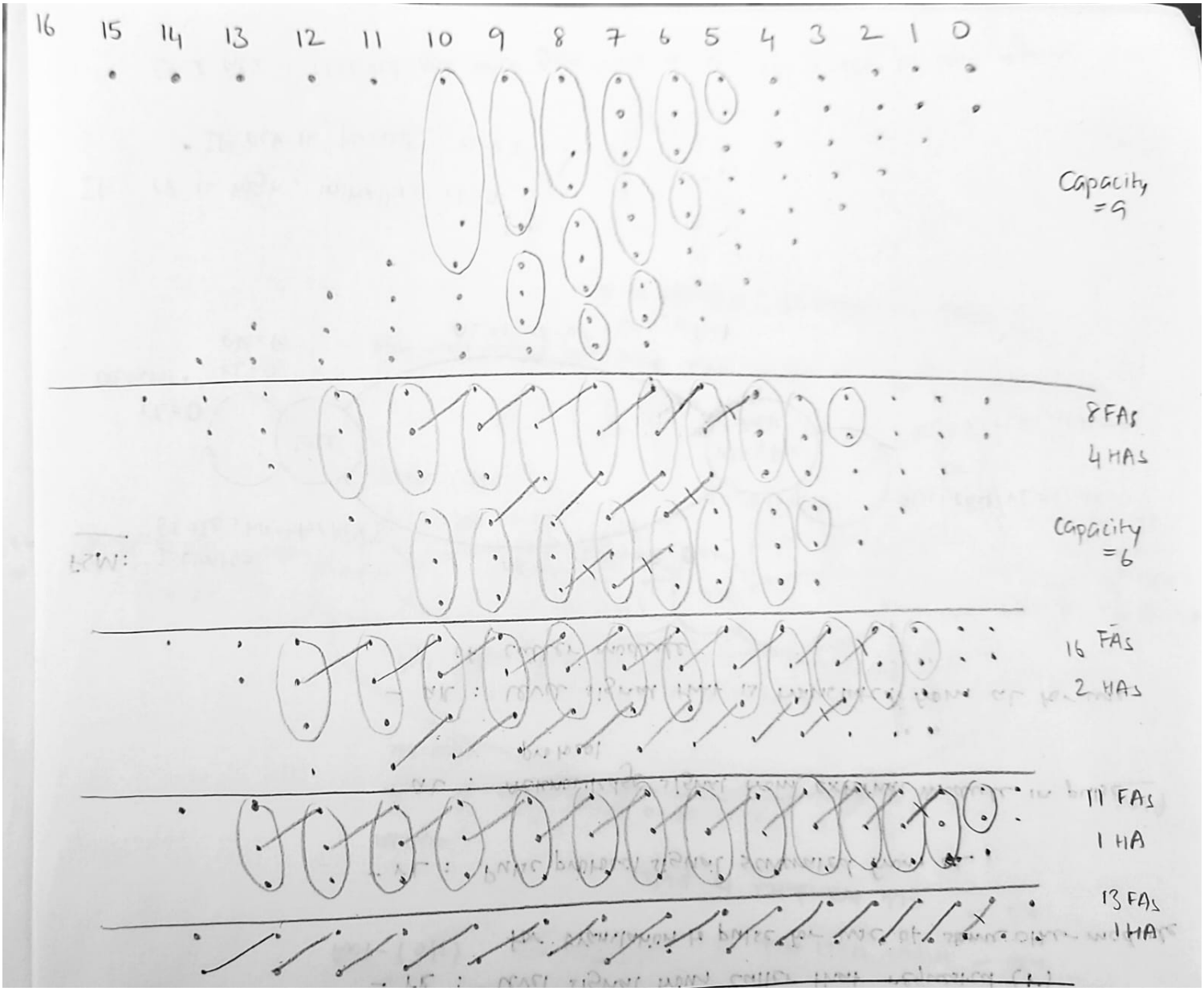

Figure 1: Dot Diagram for Dadda MAC

Testbench

The trace file has two vectors, one with appended inputs (A and B are 8-bit inputs to be multiplied, and C is a 16-bit number to be added to this product) and the other with carry-out and sum appended.

- Vector 1: A B C (32 bits)
- Vector 2: Cout Sum (17 bits)

This appending is done by DUT, which instantiates a MAC component.

The testbench py file generates 'TRACEFILE.txt', which contains 10 randomized test-cases (including corners cases where all have minimum, maximum and complementary values).

Results

- Delay in RTL simulation $\approx 800ps$
- Delay in Gate Level simulation $\approx 23ns$

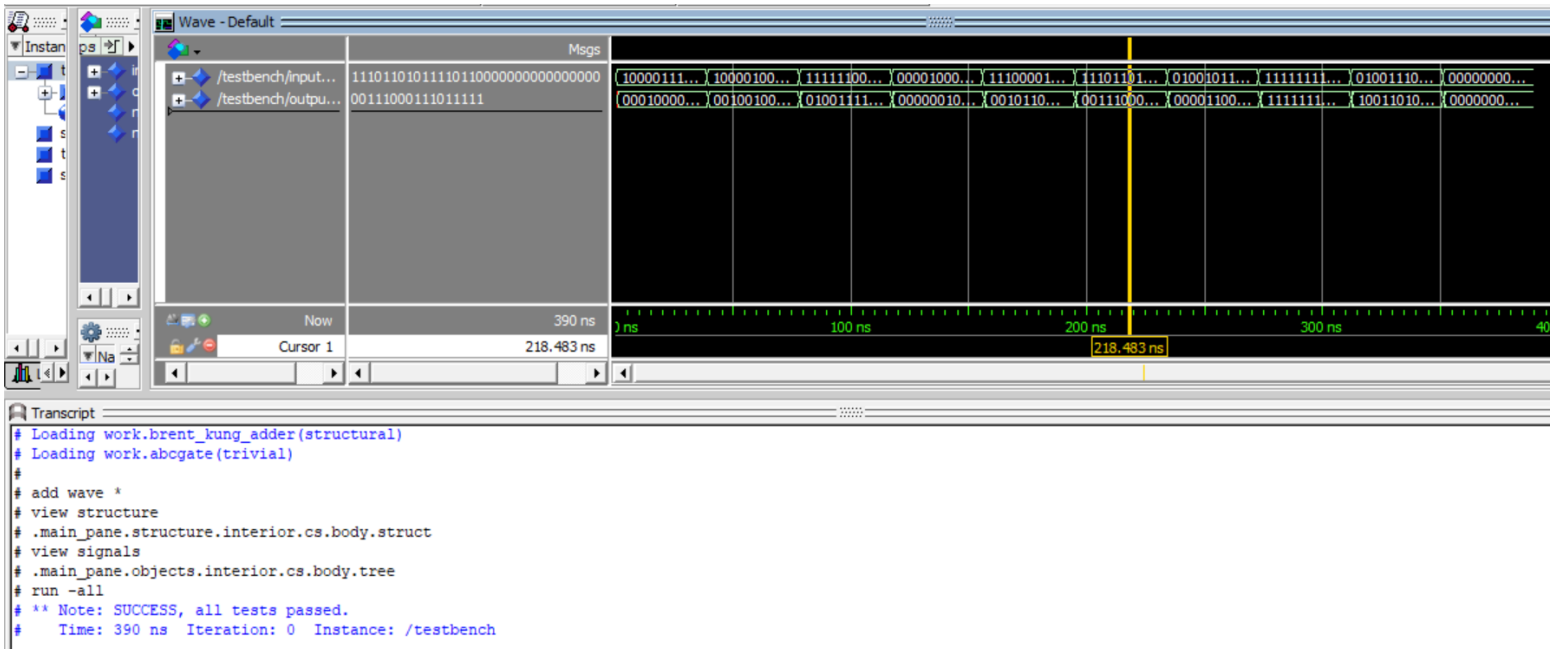

Figure 2: RTL Simulation

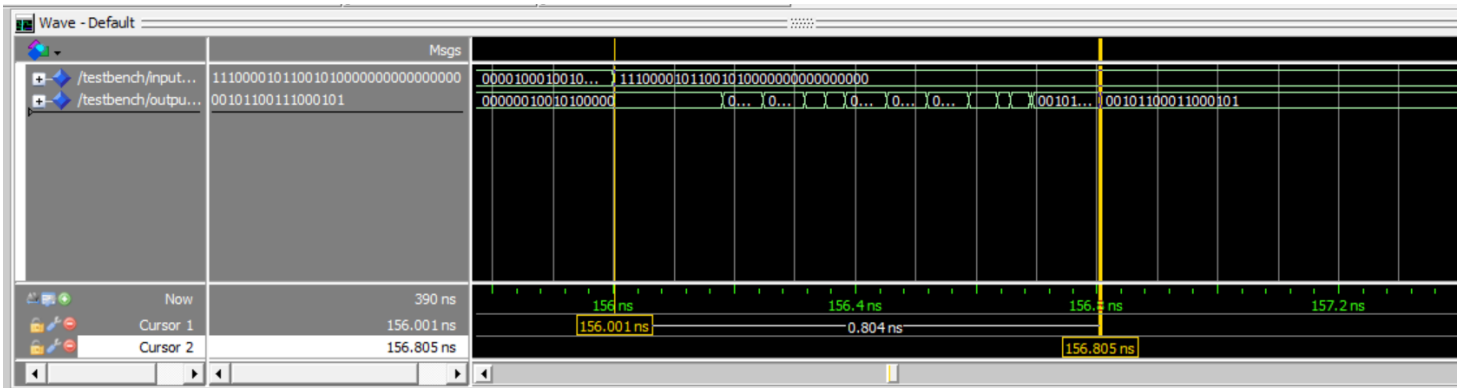

Figure 3: Delay in RTL Simulation

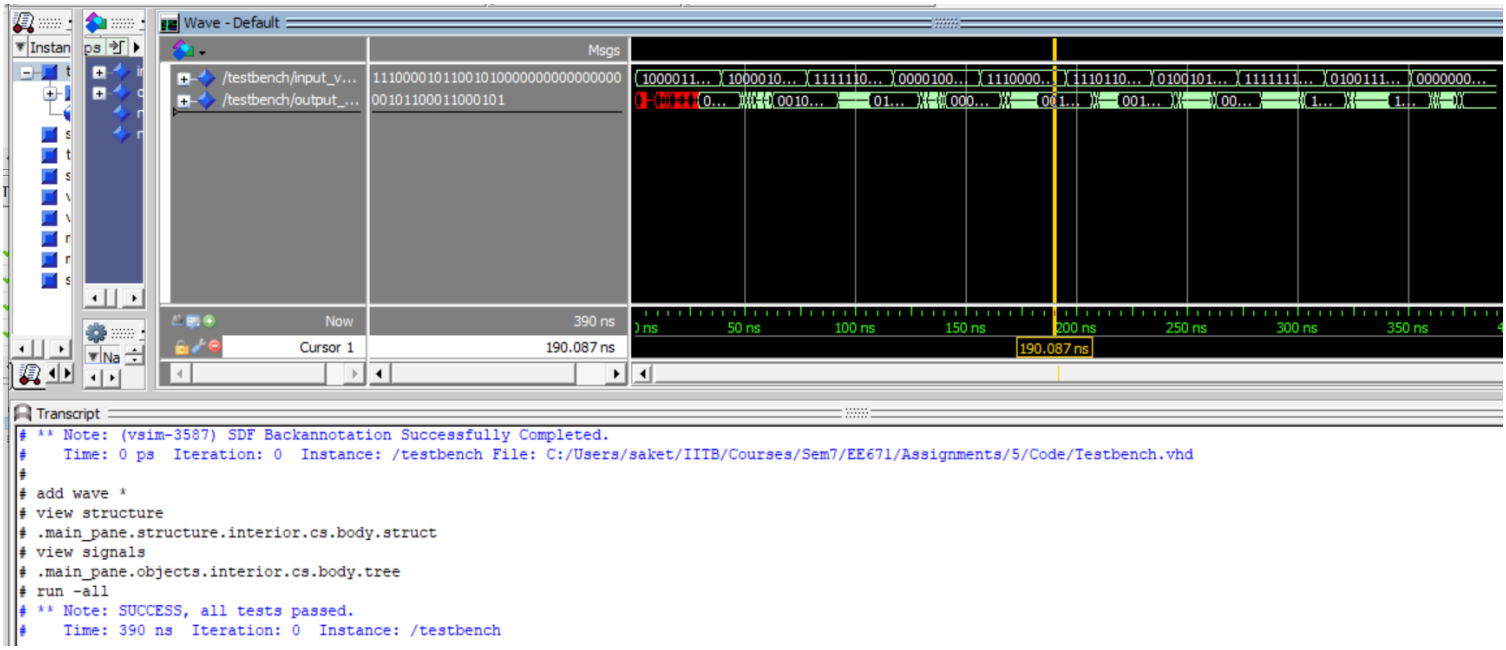

Figure 4: Gate Level Simulation

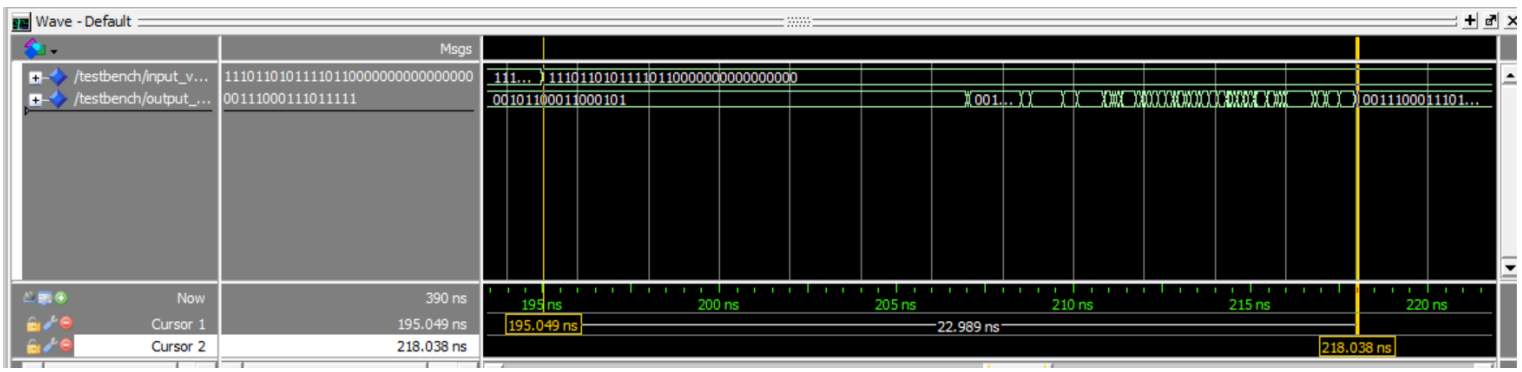

Figure 5: Delay in Gate Level Simulation