EE671: VLSI Design

Assignment 3

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Question 1

The circuit used to measure the required delays is shown below.

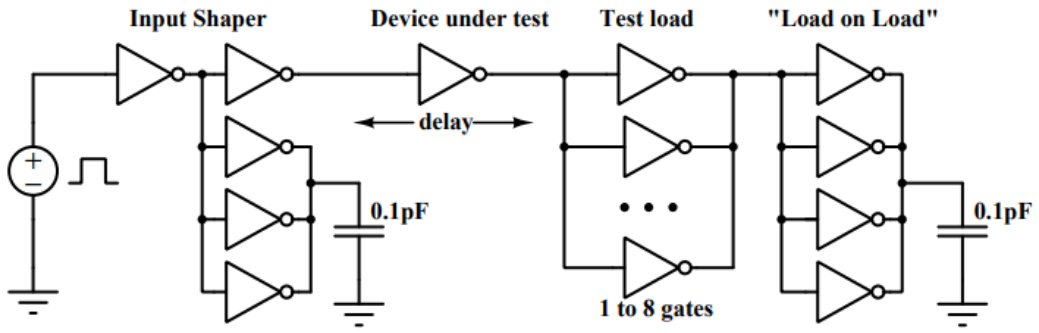
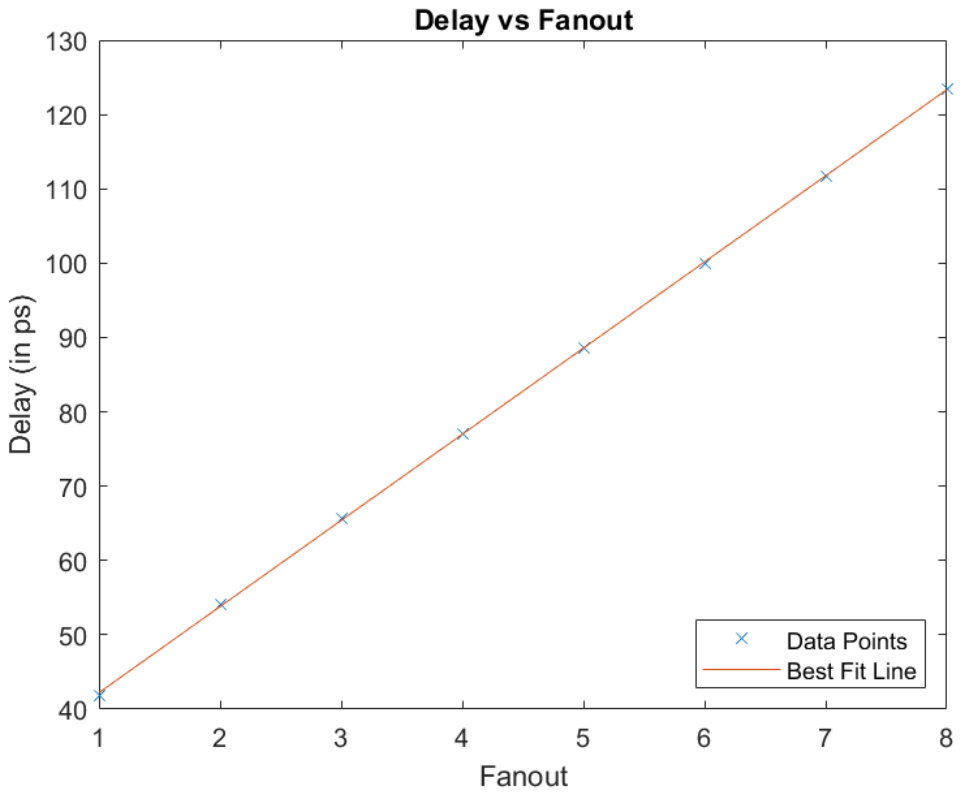


Figure 1: Circuit Diagram of testing circuit

The rise and fall delays are summarized in this table. All delays are in units of ps. Rise delay is the delay when input is rising (and output is falling), while fall delay is when input is falling (and output is rising).

# Load Inverters	Rise Delay (in ps)	Fall Delay (in ps)	Average Delay (in ps)
1	41.291	42.451	41.871
2	53.917	54.202	54.059
3	65.827	65.443	65.635
4	77.491	76.623	77.075
5	89.102	87.909	88.505
6	100.737	99.323	100.030
7	112.417	110.918	111.668
8	124.157	122.694	123.425

Slope of line $= 1.15899 \times 10^{-11}$
Intercept of line $= 3.06271 \times 10^{-11}$



From this, we know that τ = slope, and p_{inv} = intercept/slope (in units of τ)

$\boxed{\tau = 11.5899 \text{ ps}}$

$\boxed{\text{p}_{inv} = 2.6426\tau = 30.6271 \text{ ps}}$

From Assignment 1, $W_p = 1.275\mu m$ and $W_n = 0.407\mu m$ so $\boxed{\gamma = 3.133}$

```
Parastic delay of inverter
* Unit Inverter
.subckt inv supply Inp Output

.param Len = 0.18U
.param Wp = 1.275U Wn = 0.407U
.param Area_p = {2*Len*Wp} Area_n = {2*Len*Wn}
.param Per_p = {2*(Wp + 2*Len)} Per_n = {2*(Wn + 2*Len)}

MP1 Output Inp Supply Supply cmosp
+ L = Len W = Wp AD = Area_p AS = Area_p PD = Per_p PS = Per_p
MN1 Output Inp 0 0 cmosn
+ L = Len W = Wn AD = Area_n AS = Area_n PD = Per_n PS = Per_n
.ends

* pulse with time period of Trep, rise and fall times = Trep/20
.param Trep= 5n
.param Trf = {Trep/20.0}
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```
.param Tw = {Trep/2.0 - Trf}
.param hival=1.8
.param loval=0.0
Vpulse pgen 0 DC 0 PULSE({loval} {hival} {Tw} {Trf} {Trf} {Tw} {Trep})

vdd supply 0 dc 1.8

*input shaper invs
x_i1 supply pgen a inv
x_i2 supply a dutin inv
x_i3 supply a b inv
x_i4 supply a b inv
x_i5 supply a b inv
c_i c 0 0.1p


* Device under test
x_dut supply dutin dutout inv

* Load Capacitor
x_l1 supply dutout c inv
x_l2 supply dutout c inv
x_l3 supply dutout c inv
x_l4 supply dutout c inv
x_l5 supply dutout c inv
x_l6 supply dutout c inv
x_l7 supply dutout c inv
x_l8 supply dutout c inv

*Load on Load
x_ll1 supply c d inv
x_ll2 supply c d inv
x_ll3 supply c d inv
x_ll4 supply c d inv
c_l d 0 0.1p

.include models-180nm
*TRANSIENT ANALYSIS with pulse inputs
.tran 0.5pS {3*Trep} 0nS
.control

run
* plot v(dutin) v(dutout)
meas tran invdelay1 TRIG v(dutin) VAL=0.9 RISE=2 TARG v(dutout) VAL=0.9
    FALL=2
meas tran invdelay2 TRIG v(dutin) VAL=0.9 FALL=2 TARG v(dutout) VAL=0.9
    RISE=2

let invdelay = (invdelay1 + invdelay2)/2
print invdelay

.endc
.options savecurrents
.end
```