A 10-bit Segmented CMOS DAC

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Overview

- "The world we live in is analog." [1]
- All data processing happens digitally.
- Interfaces are needed to convert between analog and digital domains.
- We will focus on Digital-to-Analog Converters (DACs).

[1] Source: Peter Kinget, https://www.ee.columbia.edu/~kinget/WhyAnalog/circuitcellar_The_World_Is_Analog_201410.pdf

Background

- A DAC converts a digital input to an analog output.
- Many different topologies of DAC are available; we will look at current-steering DACs.
- Current-steering DACs are the superior choice out of all topologies for high-frequency applications and driving resistive loads without needing buffers.

Ideal DAC

- The increase in output current is the same for every LSB increase in the digital code.

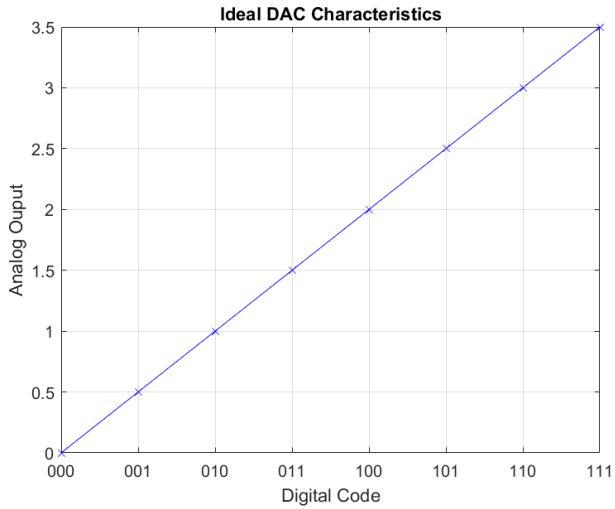


Figure 1: Ideal DAC Characteristics

- As input increases, the output always increases. Hence it is monotonic.

Realistic DACs

- As we increment the digital code by 1 LSB, the change in the output current may not always be equal.
- Further, the output might fall from its previous value as input is incremented. That is, the DAC might be non-monotonic.

Examples of Realistic DACs

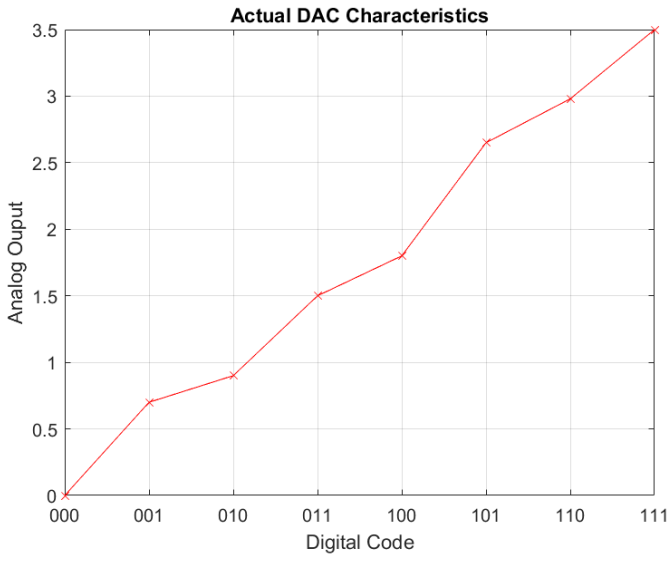


Figure 2: Example of a monotonic non-ideal DAC

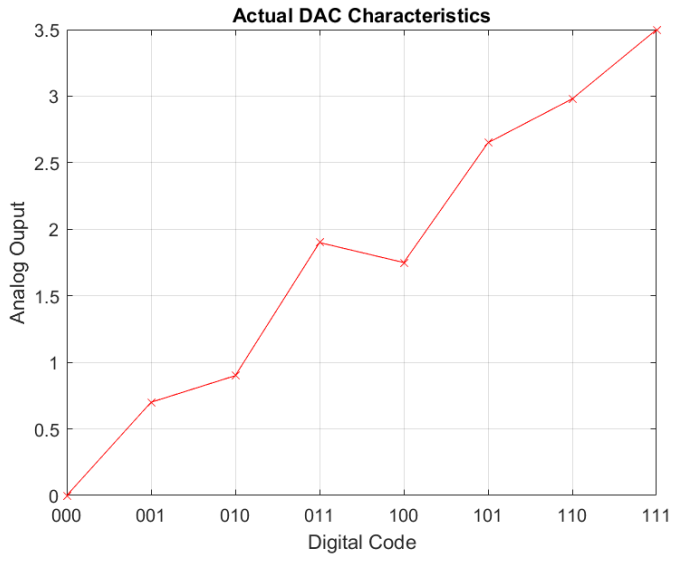


Figure 3: Example of a non-monotonic non-ideal DAC

Static Errors

Definition (Integral Non-Linearity (INL))

The difference between the actual and ideal analog output values for a particular digital code.[2]

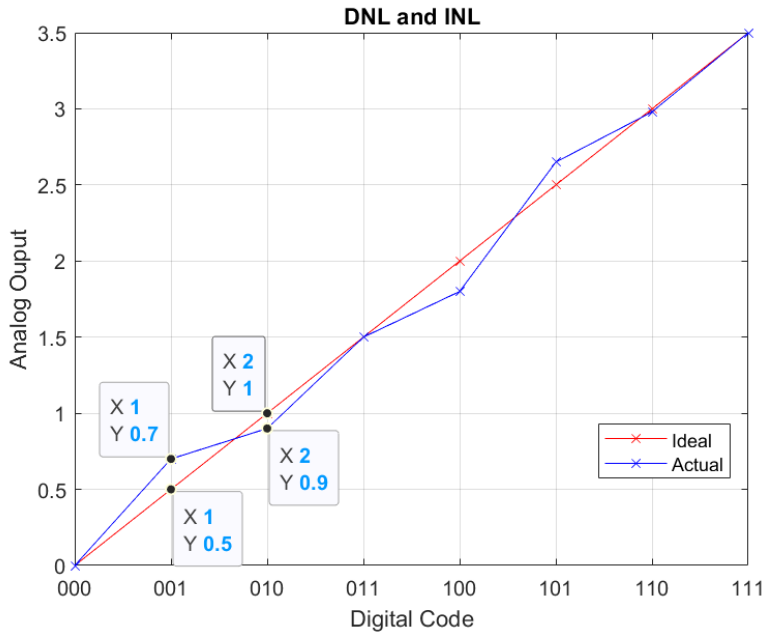
Definition (Differential Non-Linearity (DNL))

The deviation in analog output step sizes away from 1 LSB.[2]

[2]Source: Carusone, Tony Chan, David Johns, Kenneth W. Martin, and David Johns. Analog Integrated Circuit Design.

Example

- For the example given below, 1 LSB = 0.5



- INL for 001 is $(0.7 - 0.5)/0.5 = 0.4$ LSB
- DNL for the segment considered is $((0.9 - 0.7)/0.5) - 1 = -0.6$ LSB

Problem Statement

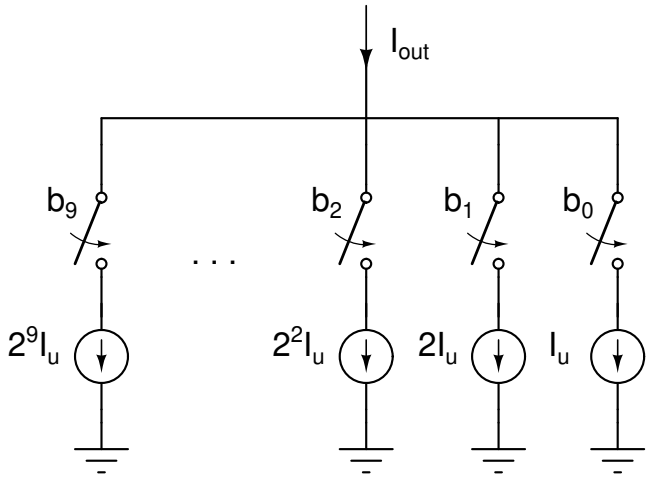
We want to design a 10-bit current-steering DAC with:

- $\mathrm{INL}_{\mathrm{max}} = 1$ LSB
- $\mathrm{DNL}_{\mathrm{max}} = 0.5$ LSB
- Optimal chip area and digital complexity

Binary-Weighted DAC

- Each digital bit controls a switch carrying a current of a different binary weight.
- If the unit cell carries current I_u, and if the bits are labeled b_0 to b_9, with b_0 representing the LSB, the output is

$$I_{out} = b_9(2^9 I_u) + b_8(2^8 I_u) + \ldots + b_0(I_u) \qquad (1)$$



Advantages

- Digital bits directly control the switches; there is no need for decoding logic.
- Complexity is relatively low.

Disadvantages

- In reality, all the current sources are not perfectly matched. Each current source has a random variation, and hence the current through each unit cell is $I + \Delta I_u$.
- All switches toggle at the same time at the mid-code transition (01 1111 1111 $\rightarrow$ 10 0000 0000) leading to a glitch.
- The current before the transition is $(2^{N-1} - 1)(I + \Delta I_u)$, and after would be $2^N(I + \Delta I_u)$. Mismatches might even cause the output to be non-monotonic.

Disadvantages

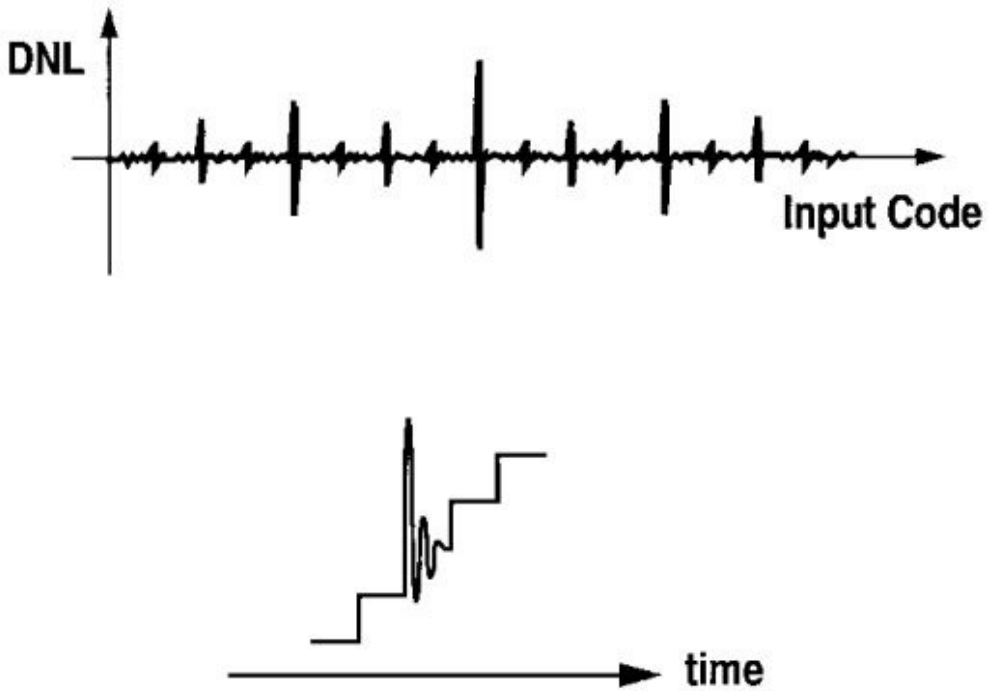
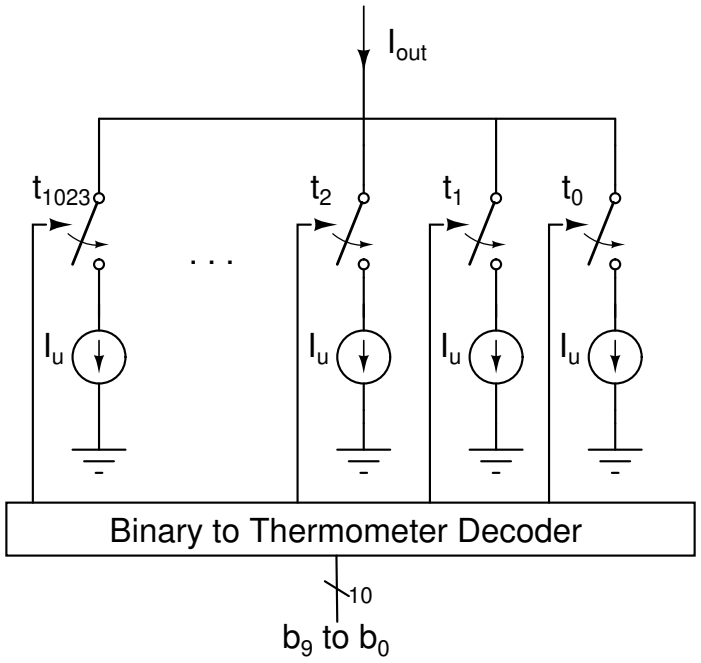


Figure 4: Example of a glitch [3]

[3] Source: Chi-Hung Lin and K. Bult, "A 10-b, 500-MSample/s CMOS DAC in 0.6 mm^2," in IEEE Journal of Solid-State Circuits

Thermometer-Coded DAC

- $(2^{10} - 1)$ unit current sources are used in place of the 10 binary-weighted current sources.
- Only one new current source is switched on when the digital input is incremented by 1 LSB.



Advantages

- Mid-code transition no longer causes a significant glitch since just one new current source switches on.
- The glitch amplitude is directly proportional to the change in digital code since exactly those many unit cells switch, in contrast to the unpredictable glitch amplitude in the previous architecture.
- DNL error of a thermometer-coded DAC is much lower than that of a binary-weighted DAC.

Disadvantages

- An additional binary-to-thermometer decoder is needed.
- Each of the 1023 unit cells needs a decoder to determine whether they turn on or not, depending on the thermometer bit input.
- Therefore, digital complexity is very high.

Need for Segmentation

We want to leverage the benefits of both architectures:

- The high accuracy of thermometer-coded DACs
- The low digital complexity of binary-weighted DACs

For simplicity, a fully binary-weighted DAC is regarded as 0% segmented and a thermometer-coded DAC as 100% segmented.

Maximum INL and DNL errors

- The expression for maximum INL of a DAC (regardless of % segmentation), for a random change of σ in the current I_u, is given by [4]

$$\text{INL}_{\text{max}} = \frac{\sigma}{2I_u}\sqrt{2^N} \tag{2}$$

- For B_b binary bits and $B_t = N - B_b$ thermometer bits, the maximum DNL is approximately

$$\text{DNL}_{\text{max}} = \frac{\sigma}{2I_u}\sqrt{2^{B_b+1}} \tag{3}$$

[4] Source: B. Razavi, "The Current-Steering DAC [A Circuit for All Seasons]," in IEEE Solid-State Circuits Magazine

Varying % segmentation

Table 1: Trade-Offs With Variation in % Segmentation

Architecture	**INL**	**DNL**	**No. of decoding units**
Fully Binary	16σ	32σ	0
Segmented ($B_t = 2$)	16σ	22.63σ	3
Segmented ($B_t = 5$)	16σ	8σ	31
Segmented ($B_t = 8$)	16σ	2.83σ	255
Fully Thermometer	16σ	σ	1023

Area Requirements

- Let $\sigma = 0.5$ LSB represent the DNL_{max}.
- The dependence of area on σ is given by [5]

$$\text{Area} \propto \frac{1}{\sigma^2} \tag{4}$$

[5] Source: M. J. M. Pelgrom, A. C. J. Duinmaijer and A. P. G. Welbers, "Matching properties of MOS transistors," in IEEE Journal of Solid-State Circuits

Area Requirements

Let A_{unit} represents the minimum analog area of a thermometer-coded architecture to have a $\text{DNL}_{\text{max}} = \sigma$

Table 2: Area and Static Error Conditions for Binary-Weighted and Thermometer-Coded DAC

Specification	**Binary-Weighted**	**Thermometer-Coded**
DNL	32σ	σ
INL	16σ	16σ
Area for DNL = 0.5 LSB	$1024A_{\text{unit}}$	A_{unit}
Area for INL = 1 LSB	$64A_{\text{unit}}$	$64A_{\text{unit}}$

Optimal Segmentation

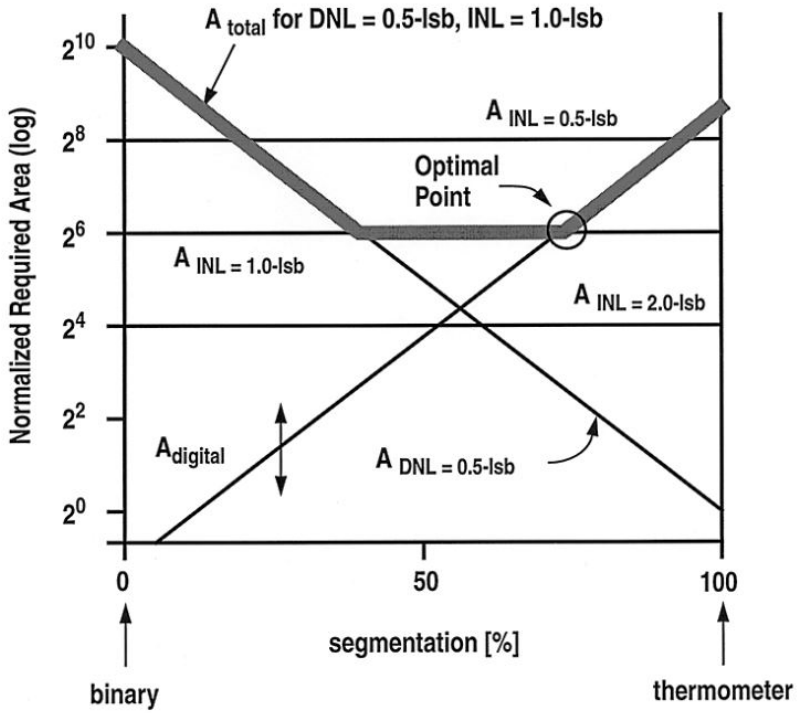


Figure 5: Normalized chip area versus percentage segmentation [6]

[6] Source: Chi-Hung Lin and K. Bult, "A 10-b, 500-MSample/s CMOS DAC in 0.6 mm^2," in IEEE Journal of Solid-State Circuits

Optimal Segmentation

- All points on the highlighted portion of the horizontal line would meet the maximum INL and DNL targets in the same area.
- Using the maximal segmentation possible would result in the least DNL error and give the best total harmonic distortion performance, and hence is considered the optimal point.
- The optimal point corresponds to 8 thermometer bits and 2 binary bits for the specifications we considered.

Conclusion

- Thermometer-coded DACs have fewer spurious frequency components compared to binary-weighted DACs owing to smaller glitches.
- Digital complexity can be reduced by choosing an optimal percentage of segmentation while meeting the INL and DNL specifications and maintaining the minimum possible area.

References


Chi-Hung Lin and K. Bult, "A 10-b, 500-MSample/s CMOS DAC in 0.6 mm^2," in IEEE Journal of Solid-State Circuits, vol. 33, no. 12, pp. 1948-1958, Dec. 1998, doi: 10.1109/4.735535.


B. Razavi, "The Current-Steering DAC [A Circuit for All Seasons]," in IEEE Solid-State Circuits Magazine, vol. 10, no. 1, pp. 11-15, Winter 2018, doi: 10.1109/MSSC.2017.2771102.


M. J. M. Pelgrom, A. C. J. Duinmaijer and A. P. G. Welbers, "Matching properties of MOS transistors," in IEEE Journal of Solid-State Circuits, vol. 24, no. 5, pp. 1433-1439, Oct. 1989, doi: 10.1109/JSSC.1989.572629.


Carusone, Tony Chan, David Johns, Kenneth W. Martin, and David Johns. Analog Integrated Circuit Design. Hoboken, NJ: John Wiley & Sons, 2012.