Indian Institute of Technology Bombay

Department of Electrical Engineering

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Course Project Report

Course: EE 344: Electronic Design Lab

Project Group No: TUE-JJ-8-2

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Project Title: 20 MHz Receiver Frontend for POF Data Communications

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Abstract:

POF links have the potential to provide a higher data rate (DR) and a longer channel length, together with considerably easier handling as compared to coaxial cables. They are much lighter in weight, robust to bending, and more compact, making them easier to install and adjust. Additionally, POF cables provide immunity from noisy electromagnetic interference (EMI) and have a lower fabrication cost due to their plastic nature. This project aims to create a receiver circuit suitable for interfacing with POF applications at high frequencies.

The optical signal from the POF link is incident on a PIN photodiode that produces a current proportional to the intensity of the incident light. Typically, the current produced by the photodiode is in the range of a few μA; we need a Trans-Impedance Amplifier (TIA) to convert the input current signal to line level voltage, that can be used as the input to a comparator. In addition to low noise amplification, we need to make sure that the TIA is capable of operating at frequencies up to the order of tens of MHz.

Contents

1 Introduction

This project presents a 3-stage closed-loop TIA: comprising a JFET input stage, followed by two cascaded BJT common emitter stages. We tested the circuit using a Pseudo-Random Bit Sequence (PRBS) generated using a shift register and an XOR gate. The following sections present a detailed explanation of the transmitter and receiver circuits and the results we achieved at different frequencies up to 2.5 MHz.

1.1 Block Diagram

Figure 1 shows the block diagram for the overall system.

1.2 Project Goal

To build a receiver frontend for POF Data Communications capable of communicating at up to 20 MHz, with the majority of the focus being on designing a competent Trans-impedance Amplifier to suitably amplify the current emitted from the photodiode receiver and output a voltage waveform that can later be fed to a comparator to obtain digital output.

2 System Overview

Our project can be broadly divided into the following subsections:

2.1 Transmitter

This subsystem is responsible for the generation and optical transmission of a pseudo-random bit-sequence. It consists of a PRBS Generator and an LED driving circuit. Input is a clock signal generated from an AFG, and output is the light emitted by the LED.

2.2 Transmitting Medium

The transmitter and receiver are linked through air as a medium for initial testing. A POF (Plastic Optical Fiber) can be used to enhance transmission and reduces noise and losses.

2.3 Receiver

This subsystem is responsible for reception, conversion of the optical signal to a voltage signal, and amplification to rail-to-rail levels for further digital processing. The receiver consists of a photodiode that converts the optical signal to a current signal and a TIA circuit made of discrete devices for amplification. The input to this subsystem is the optical signal, and the output is a rail-to-rail voltage signal representing the information bits.

Our TIA consists of 3 stages in cascade, with the input JFET CS (Common-Source) stage to deal with the low input current without introducing much noise. The following 2 BJT stages are CE (Common-Emitter) with Collector-Base-Feedback and Emitter degeneration, as shown in Figure 2. The emitter resistance is chosen to set the DC bias points. This configuration results in very stable biasing. For instance after biasing, say the collector current I_C *increases* slightly. Then, assuming $I_B << I_C \sim I_E$, $V_C = V_{CC} - I_C \cdot R_C$ decreases, and $V_E = I_E \cdot R_E$ increases slightly. Hence $I_B = \frac{V_C - V_B}{R_B} = \frac{V_C - (V_E + 0.7)}{R_B}$ decreases, and consequently $I_C = \beta \cdot I_B$ will also decrease, pulling us back to our stable operating point. We feed the output back to the input through a resistor and a capacitor.

3 Project Implementation

3.1 Transmitter Circuit

The circuit is made as shown in Figure 3 using a +5/0 V power supply. A PRBS is generated using a 4-bit shift register (74LS195), a 2-input XOR gate (SN74ALS86N), and a 4-input NAND gate (SN7440N). The input to the first flipflop is the XOR of the outputs of any two other flipflops. This ensures that the 4-bit binary number formed by the outputs of all the flipflops cycles through all non-zero 4-bit binary

numbers. Consequently, a sequence of eight zeroes and seven ones is generated at the output of each flipflop, which repeats. The clock input to this circuit is a square signal generated by an AFG. Table 1 demonstrates the generation of a PRBS signal using the circuit shown in Figure 3.

The PRBS output is then interfaced with the LED through a NOT gate (SN74LS04) to ensure that the diode is appropriately biased. The LED is finally coupled with a POF (obtained from WEL) for data transmission.

3.2 Receiver Circuit

3.2.1 Version 1

The preliminary receiver circuit is made as in Figure 4. We test our transmitter circuit using an off-the-shelf OPAMP (TL082) in inverting configuration to understand the challenges faced while making our own receiver circuit. To get a high gain, we were required to choose a very high feedback resistance value. Thus we could only obtain good results for frequencies $\sim$ 100 kHz. Hence the gain-bandwidth trade-off was apparent.

3.2.2 Version 2

We next build our custom TIA circuit as shown in Figure 5. Our receiver circuit consists of a trans-impedance amplifier to amplify the low current generated by the photodetector to line level. We work with a single power supply of +5 V for the photodetector and +12 V for the rest of the receiver.

The circuit consists of a PIN photodiode receiver that produces a current proportional to the intensity of light that falls on it, followed by three single-transistor stages connected in feedback to generate high gain with high bandwidth.

The light emitted by the LED falls onto the photodiode, which generates a current of about a few μA. This current passes through a 1 MΩ resistor to create a voltage input to stage 1 of our amplifier.

Taking inspiration from the circuit diagram for TL082, we also use an input JFET stage in our custom design due to the very low input current. Stage 1 consists of an N-JFET in the common-source configuration in self-biasing mode. The source resistance is chosen to bias the transistor in the saturation region properly. It is shunted with a 0.33 μF capacitor to achieve a reasonable gain at a high frequency. We choose the drain resistance to achieve a target gain of 10. The calculations are shown below:

Let I_D = 2 mA, V_{GS} = -1.5 V and V_G = 0 V. Designing for a gain of 10,

$$R_S = \frac{1.5\ V}{2\ mA} = 750\ \Omega \tag{1}$$

$$Gain = g_m \cdot R_D = 10 \tag{2}$$

$$\frac{2 \times 6.6}{2.5} \cdot \left(1 - \frac{1.5}{2.5}\right) \times R_D = 10 \tag{3}$$

$$\implies R_D = 4.7\ k\Omega \tag{4}$$

Bias Points obtained after Stage 1 -

- $V_{D,1}$ = 4.49 V
- $V_{G,1}$ = 0 V
- $V_{S,1}$ = 1.56 V

Stage 2 consists of an NPN-BJT in the common-emitter configuration connected in cascade with the previous JFET stage. We have a resistor shunted across its base and collector terminals that trades-off gain for better bandwidth and ensures that the BJT always operates in the linear region of operation. The base of stage 2 is biased at the voltage of the drain of stage 1. The emitter is degenerated by a resistor for self-biasing. It is split into two individual resistances R_{E1} and R_{E2} and the lower one (R_{E2}) is shunted with a 0.33 μF capacitor for achieving a reasonable gain at a high frequency. The collector resistance is chosen to achieve a stand-alone target gain of 17. The calculations are shown below:

Given $V_{B,2} = V_{D,1} = 4.49$ V. Hence $V_{E,2} = 4.49$ - $0.7 = 3.79$ V. Assuming a current ~ 1 mA:

$$R_{E,1} + R_{E,2} = \frac{3.79\ V}{1\ mA} \sim 3.79\ k\Omega \tag{5}$$

Choosing standard values of resistances we take R_{E1} =270 Ω and $R_{E2} = 3.3\ k\Omega$

$$Gain = \frac{R_D}{R_{E1}} = 17 \tag{6}$$

$$R_D \sim 4.7\ k\Omega \tag{7}$$

Bias Points obtained after Stage 2 -

- $V_{C,2} = 6.8$ V
- $V_{B,2} = 4.49$ V
- $V_{E,2} = 3.79$ V

Stage 3 consists of another NPN-BJT in the common-emitter configuration connected in cascade with the previous BJT stage. The design specifications and considerations are the same as that for the second stage, with the only change being the base bias points.

Given $V_{B,3} = V_{C,2} = 6.8\ V$. Hence $V_{E,3} = 6.8 - 0.7 = 6.1\ V$. Assuming a current $\sim 1\ mA$:

$$R_{E,1} + R_{E,2} = \frac{6.1\ V}{1\ mA} \sim 6.1\ k\Omega \tag{8}$$

Choosing standard values of resistances we take $R_{E1} = 270\ \Omega$ and $R_{E2} = 5.6\ k\Omega$

$$Gain = \frac{R_D}{R_{E1}} = 17 \tag{9}$$

$$R_D \sim 4.7\ k\Omega \tag{10}$$

Bias Points obtained after Stage 3 -

- $V_{C,3} = 7.6$ V
- $V_{B,3} = 6.8$ V
- $V_{E,3} = 6.1$ V

Finally in feedback we have a 1 MΩ resistor and a 0.33 μF capacitance in series, so that the feedback and the biasing of the JFET is de-coupled with the bias of the last BJT stage.

We first made the transmitter circuit for generating a PRBS signal on a breadboard. Using a +5 V power supply, we made the circuit as in Figure 3, using GD74LS195A IC for the 4-bit shift register, SN74ALS86N IC for the 2-input XOR gate, SN74LS04 IC for the inverter, and a 5-mm red LED as the load.

4 Testing and Evaluation

We first assembled the transmitter circuit of Section 3.1 on a breadboard, which we then tested using a DSO to verify that the input to the LED was indeed a PRBS signal.

We then constructed the receiver circuit of Section 3.2.1 on a breadboard. We observed the output of the TIA on DSO to see if the received signal was of the same pattern as the transmitted signal and if it had been sufficiently amplified to rail-to-rail level. We realized that we had taken a very high value of feedback resistance for a high value of gain, which resulted in our setup working well only up to 100 kHz.

We then proceeded to build the circuit of Section 3.2.2 stage-by-stage on a breadboard. We looked up the datasheet of JFET to figure out its DC parameters and then designed it appropriately. Once made, we tested it with an input sinusoidal signal to test for amplification. We proceeded similarly for the remaining two BJT stages, first checking the working of the particular stage in isolation and then checking the working of the stage in cascade with the previous one.

Having achieved a reasonable gain with a 3-stage cascade, we introduced a feedback resistor and capacitor and tested the entire transmitter-receiver circuit at once. After finalizing our breadboard circuit, we proceeded to solder our circuit on a PCB of dimension 160 mm $\times$ 60.7 mm. However, while the transmitter circuit worked perfectly fine, the receiver circuit did not work on PCB, with the voltage at all terminals of the JFET being about 2.3 V.

After many hours of debugging, we decided to manually solder only the entire receiver circuit on a Perforated Circuit Board of dimension 67 mm $\times$ 50 mm, which worked. The total bill of materials is appended in Table 2.

5 Experiments and Results

We tested the working of our TIA circuit at different clock frequencies — 100 kHz (Figure 6), 500 kHz (Figure 7), and 2.5 MHz (Figure 8) — and observed the output waveforms (the yellow channel is the output of the TIA and the blue channel is the PRBS signal input to the LED).

6 Conclusions

We have been able to achieve good performance at 2.5 MHz using a 5-mm LED and BPW-46 photodiode. The bandwidth of our circuit has predominantly been limited by the presence of discrete components in our analog TIA circuit, our photodiode (we have used BPW46, which has a large radiant sensitive area $\implies$ large capacitance $\implies$ lower speed), and the low f_T ($\sim$ 300 MHz) of BJT transistors (BC547). Future work can aim at improving the same.

Acknowledgements

We would like to thank:

- Professor Joseph John for having been an excellent faculty mentor. Without his detailed and systematic guidance, we would have been lost
- Maheshwar sir for his invaluable inputs throughout, especially while soldering
- The entire WEL team for their tireless assistance

Appendices

References

[1] John Senior, Optical Fiber Communications Principles, Fig 9.13 Pg 532

Tables

Table 1: Table for PRBS - assuming initial state is 1000

Clock	$Q_0 = Q_2 \oplus Q_3$	Q_1	Q_2	Q_3
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	1	0	0	1
5	1	1	0	0
6	0	1	1	0
7	1	0	1	1
8	0	1	0	1
9	1	0	1	0
10	1	1	0	1
11	1	1	1	0
12	1	1	1	1
13	0	1	1	1
14	0	1	1	1
15	0	0	0	1
16	1	0	0	0

Table 2: Bill Of Materials

Component	Model	Purpose	Total Cost (Rs)
LED	5mm Red	Transmitter	2
4-bit Shift Register	GD74LS195A	PRBS generation	20
2-input XOR gate	SN74ALS86N	PRBS generation	51
NOT gate	SN74LS04	PRBS generation	72.20
1mm POF	-	POF link	-
Photodiode	BPW46	Receiver	60
JFET	BFW11	Final Receiver	88
NPN BJT	BC547	Receiver	2×20
Opamp	TL082	Testing	25

Figures

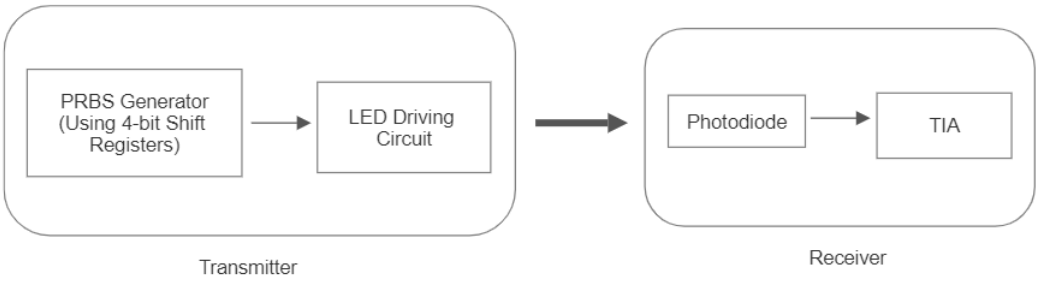

Figure 1: Overall System Block Diagram

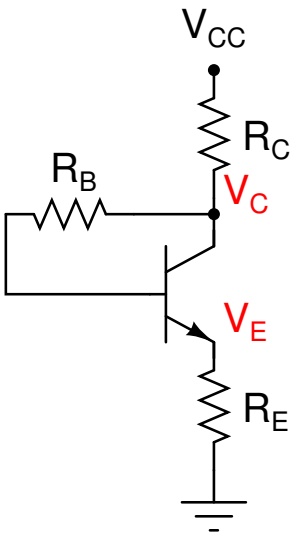

Figure 2: BJT CE Collector-Base Feedback configuration

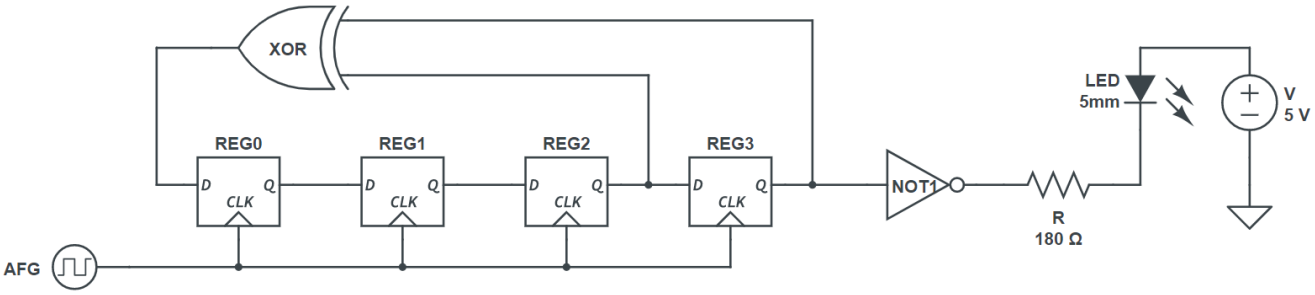

Figure 3: Circuit Diagram of Transmitter

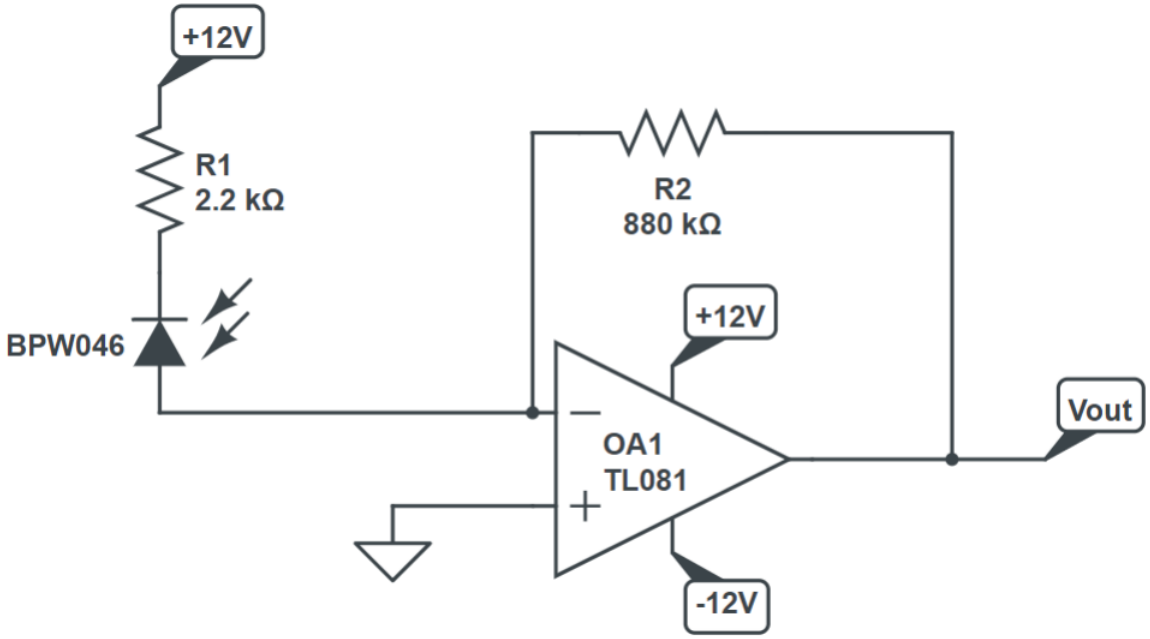

Figure 4: Circuit Diagram of Receiver with off-the-shelf TIA

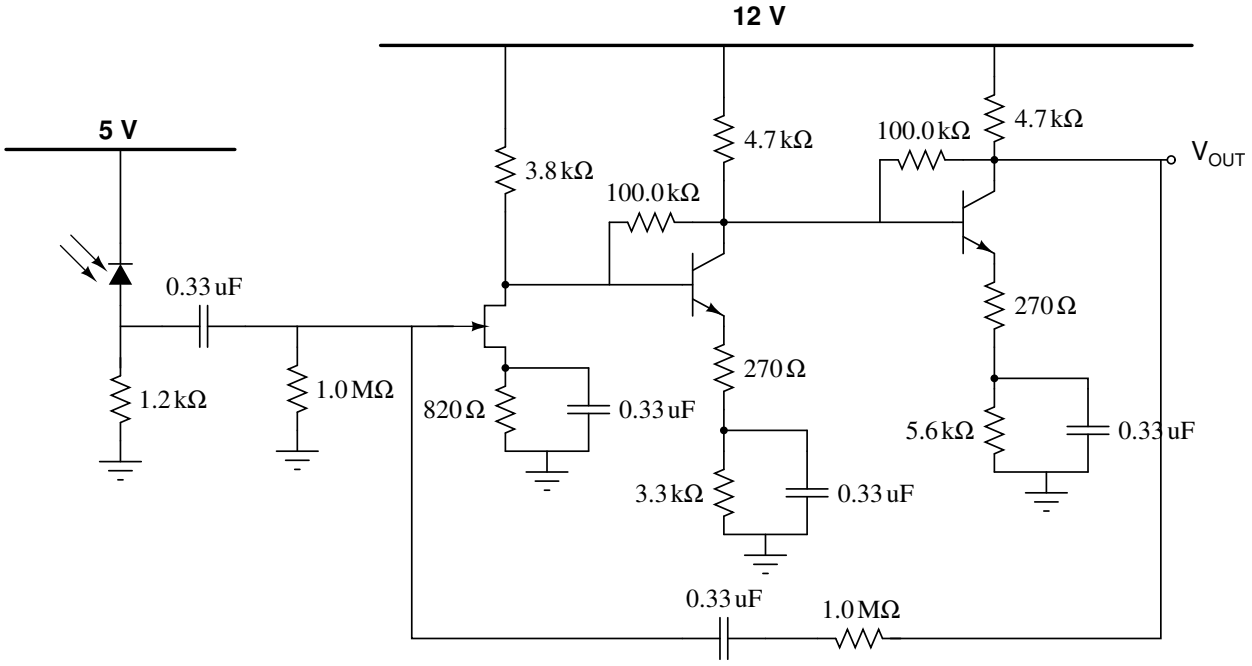

Figure 5: Circuit Diagram of Receiver with custom TIA

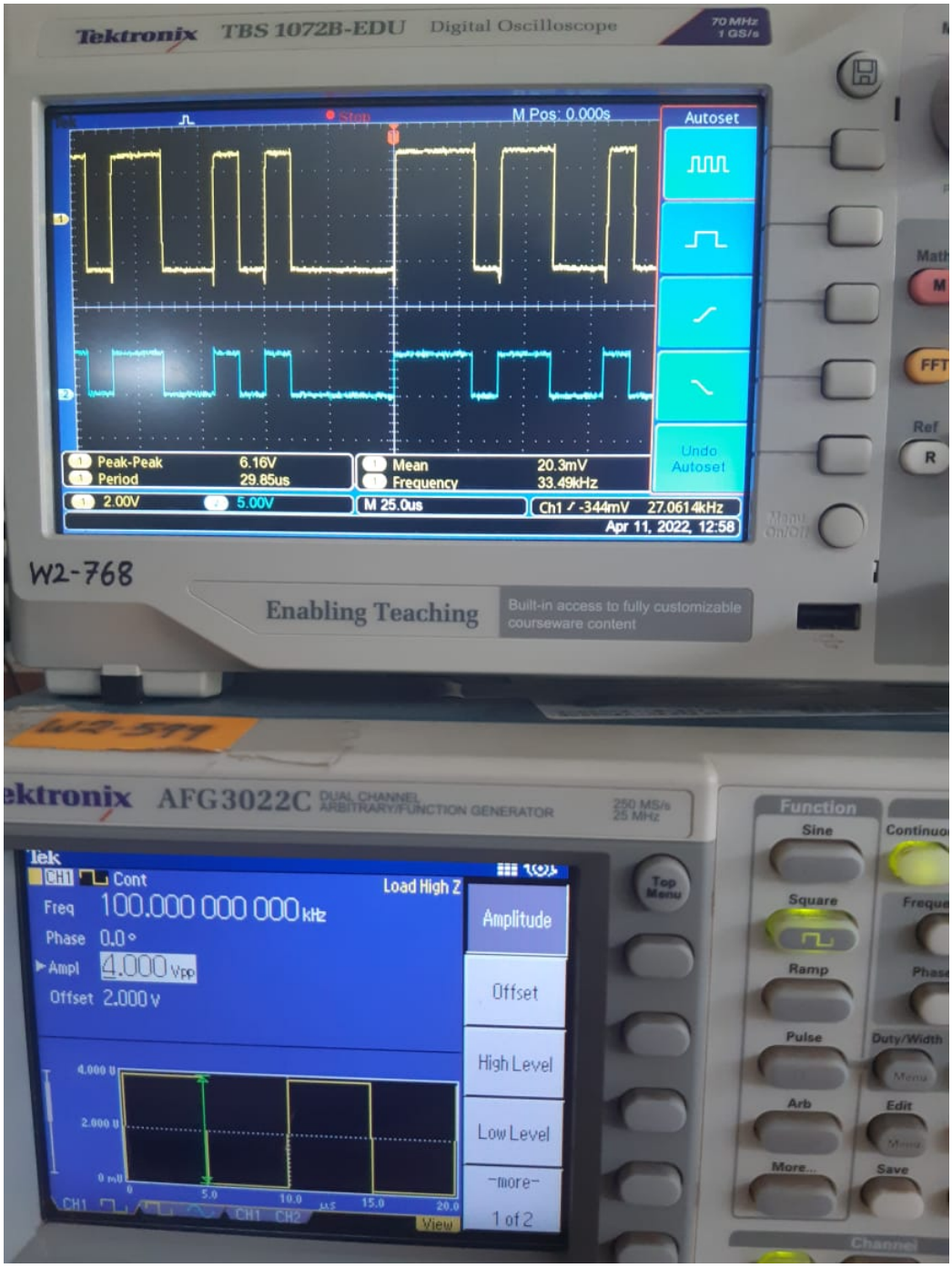

Figure 6: Input Output waveforms at 100 kHz (Ch1-Yellow is the output)

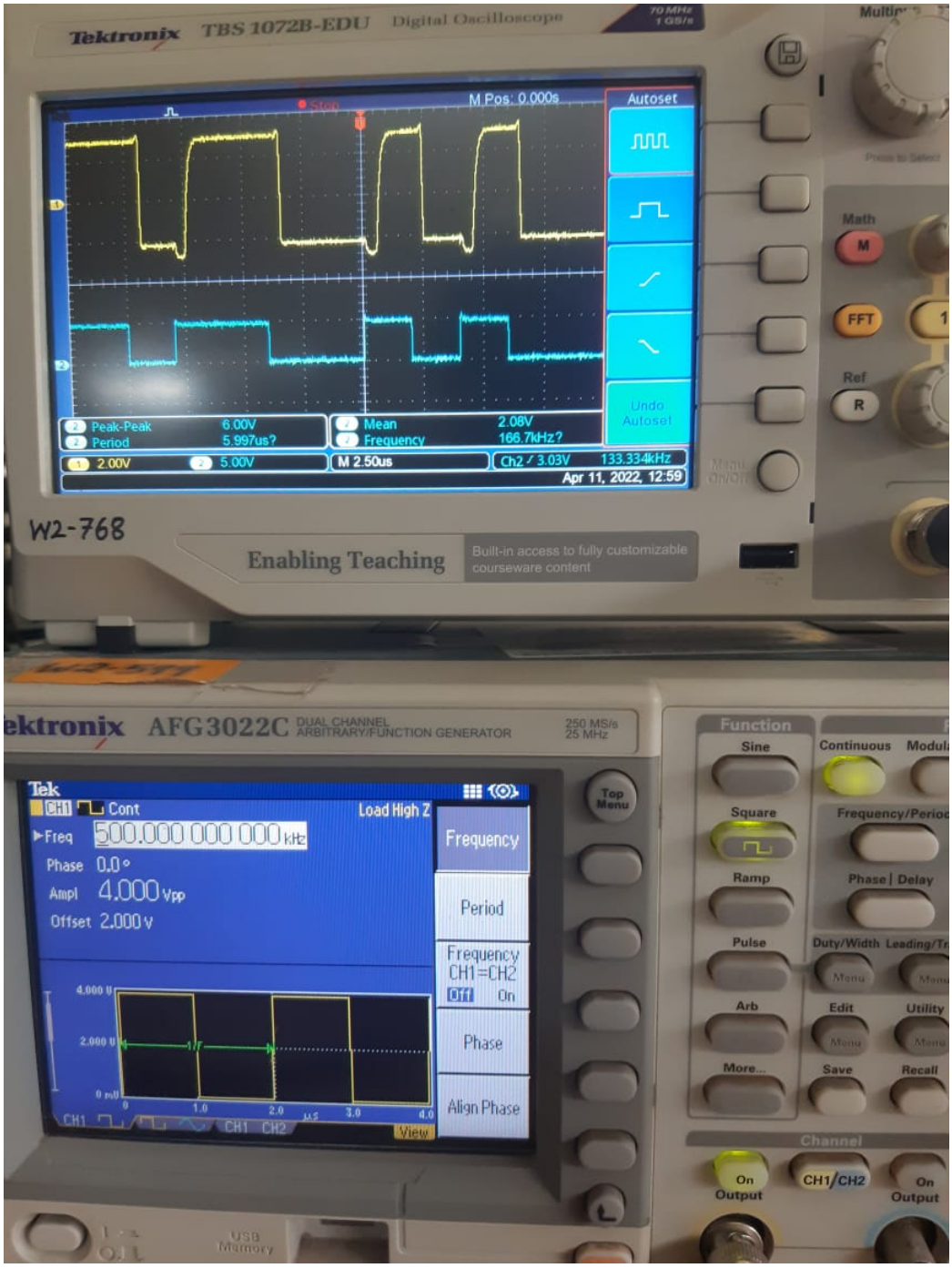

Figure 7: Input Output waveforms at 500 kHz (Ch1-Yellow is the output)

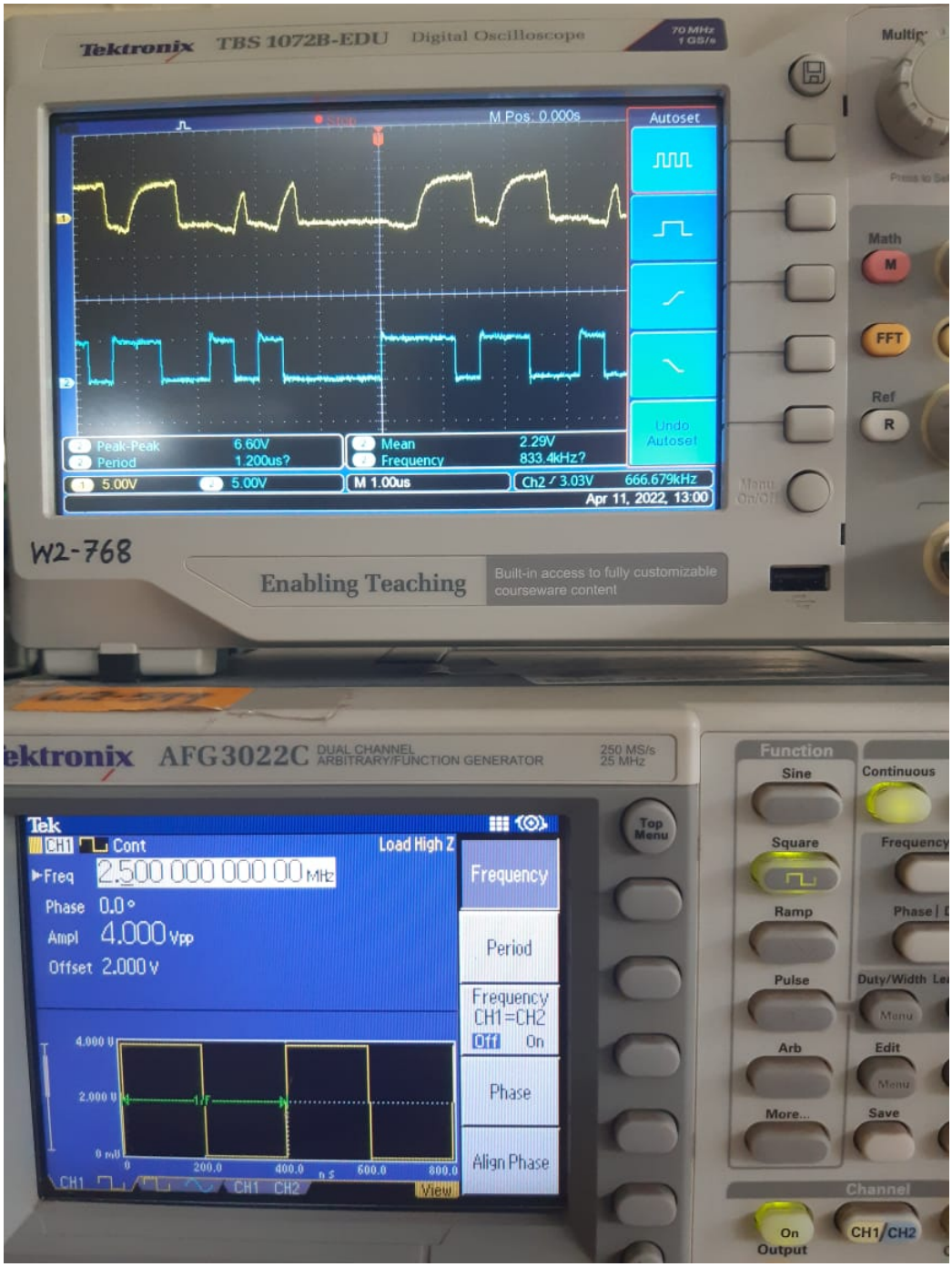

Figure 8: Input Output waveforms at 2.5 MHz (Ch1-Yellow is the output)