EE671: VLSI Design

Assignment 1

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Question 1

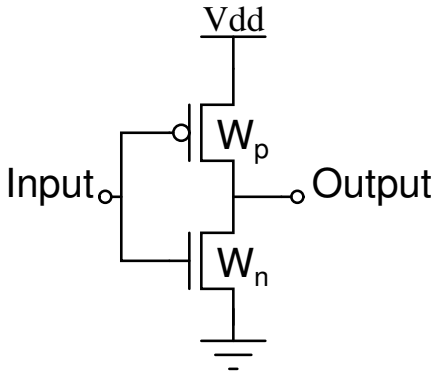

Figure 1: Circuit Diagram of Inverter

To get a rise and fall time of 20ps for the square wave, the rise and fall time parameters of pulse input should be 25ns (since 10 to 90 % used for rise/fall time calculation).

We have,

$$\tau_r \propto \frac{C}{k_p}$$

$$\tau_f \propto \frac{C}{k_n}$$

Where C includes load and parasitic capacitance. For our calculations however, we take $C \approx C_L$ and therefore $\tau \times k =$ constant.
We keep the lengths at the minimum value of 180 nm, so this simplifies to $\tau \times W =$ constant.

For the default widths given (240nm for both NMOS and PMOS), the rise time is 1200ps and fall time is 424ps.

The desired rise and fall time is $200 + 2 \times 54 = \boxed{308ps}$.

$$1200 \times 0.24 = 308 \times W_p$$

$$424 \times 0.24 = 308 \times W_n$$

These relations give rough estimates of $W_p = 0.935\mu m$ and $W_n = 0.330\mu m$. We iterate further by updating values on simulations, and get the final values as:

$$\boxed{W_p = 1.275\mu m}$$

$$\boxed{W_n = 0.407\mu m}$$

These values give the following rise and fall times:

```
inrise = 2.000000e-11
infall = 2.000000e-11
drise = 3.084630e-10
dfall = 3.087791e-10
```

The differences between calculation and simulation is since we don't account for parasitic capacitances, which themselves depend on W and L, while calculating widths of transistors.

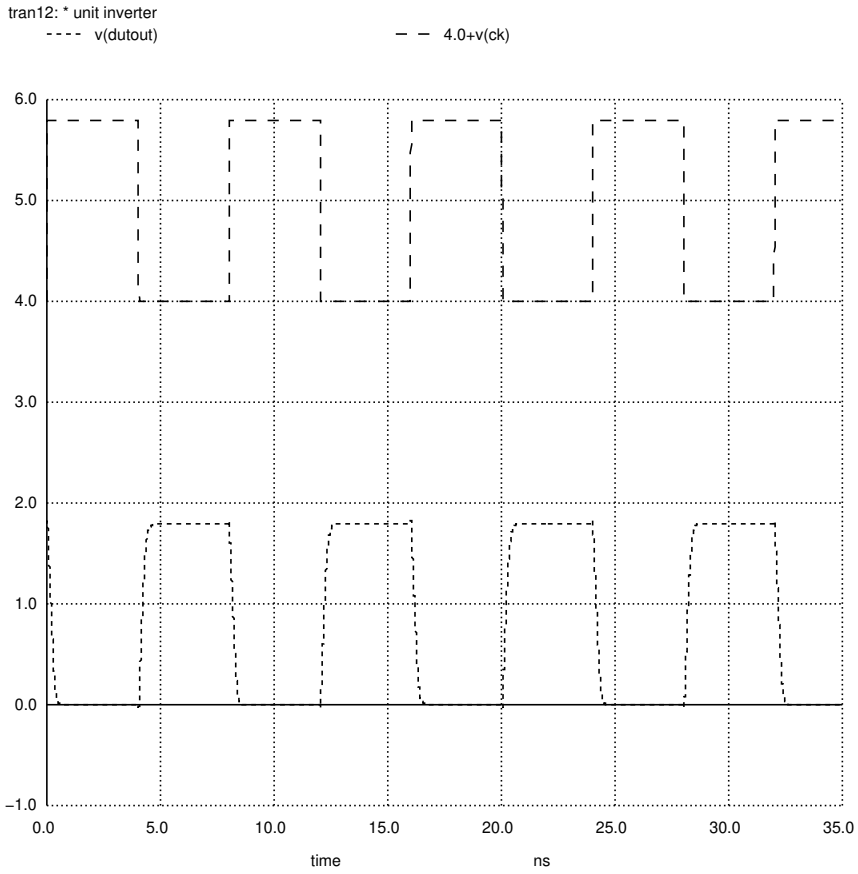

Figure 2: Input and Output Waveforms

```
* Unit Inverter
.subckt inv supply Inp Output

.param Len = 0.18U

.param Wp = 1.275U Wn = 0.407U

.param Area_p = {2*Len*Wp} Area_n = {2*Len*Wn}
.param Per_p = {2*(Wp + 2*Len)} Per_n = {2*(Wn + 2*Len)}

MP1 Output Inp Supply Supply cmosp
+ L = Len W = Wp AD = Area_p AS = Area_p PD = Per_p PS = Per_p
MN1 Output Inp 0 0 cmosn
+ L = Len W = Wn AD = Area_n AS = Area_n PD = Per_n PS = Per_n
.ends

vdd supply 0 dc 1.8

* Device under test
x3 supply Ck dutout inv

* Load Capacitor
C3 dutout 0 0.05pF

.include models-180nm
*TRANSIENT ANALYSIS with pulse inputs
VCk Ck 0 DC 0 PULSE(0 1.8 0nS 25pS 25pS 4nS 8.0nS)
.tran 1pS 35nS 0nS
.control

run
hardcopy 1.ps 4.0+V(Ck) V(dutout)
meas tran inrise TRIG v(ck) VAL=0.18 RISE=2 TARG v(Ck) VAL=1.62 RISE=2
meas tran infall TRIG v(ck) VAL=1.62 FALL=2 TARG v(Ck) VAL=0.18 FALL=2
meas tran drise TRIG v(dutout) VAL=0.18 RISE=2 TARG v(dutout) VAL=1.62
    RISE=2
meas tran dfall TRIG v(dutout) VAL=1.62 FALL=2 TARG v(dutout) VAL=0.18
    FALL=2

let targ_time = 308e-12

print inrise infall drise dfall targ_time

.endc
.options savecurrents
.end
```

Question 2

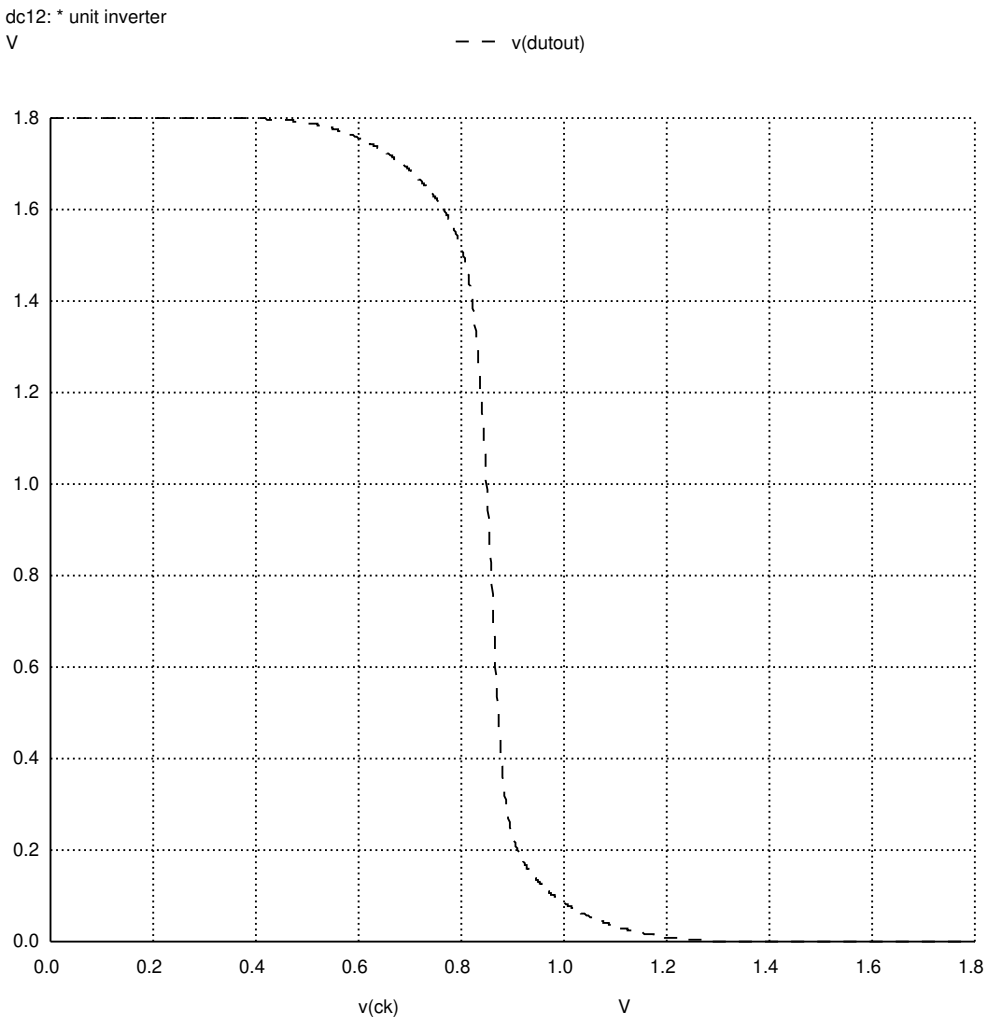

Figure 3: Static Voltage Transfer Characteristics

The *deriv* function has been used to find the coordinates at which the gain is -1, and these coordinates have been used to calculate noise margins ($\mathrm{NM}_H = V_{OH} - V_{IH}$ and $\mathrm{NM}_L = V_{IL} - V_{OL}$)

```
vout_l              =  1.136777e-01
vin_h               =  9.657371e-01
vout_h              =  1.681751e+00
vin_l               =  7.040975e-01

nm_h = 7.160139e-01
nm_l = 5.904198e-01
```

```
1 * Unit Inverter
2 .subckt inv supply Inp Output
3
```

```
.param Len = 0.18U

.param Wp = 1.275U Wn = 0.407U

.param Area_p = {2*Len*Wp} Area_n = {2*Len*Wn}
.param Per_p = {2*(Wp + 2*Len)} Per_n = {2*(Wn + 2*Len)}

MP1 Output Inp Supply Supply cmosp
+ L = Len W = Wp AD = Area_p AS = Area_p PD = Per_p PS = Per_p
MN1 Output Inp 0 0 cmosn
+ L = Len W = Wn AD = Area_n AS = Area_n PD = Per_n PS = Per_n
.ends

vdd supply 0 dc 1.8

* Device under test
x3 supply Ck dutout inv

* Load Capacitor
C3 dutout 0 0.05pF

.include models-180nm

*DC sweep
VCk Ck 0

.dc VCk 0 1.8 0.001
.control

run

hardcopy 2.eps V(dutout) vs V(Ck)

let deriv_vout = deriv(V(dutout))
meas dc vout_l find V(dutout) when deriv_vout = -1 rise = 1
meas dc vin_h find V(Ck) when deriv_vout = -1 rise = 1

meas dc vout_h find V(dutout) when deriv_vout = -1 fall = 1
meas dc vin_l find V(Ck) when deriv_vout = -1 fall = 1

let NM_H = vout_h - vin_h
let NM_L = vin_l - vout_l

print NM_H NM_L
.endc
.options savecurrents
.end
```

Question 3

Using the series parallel rules, the circuit diagram of the custom logic gate is as follows:

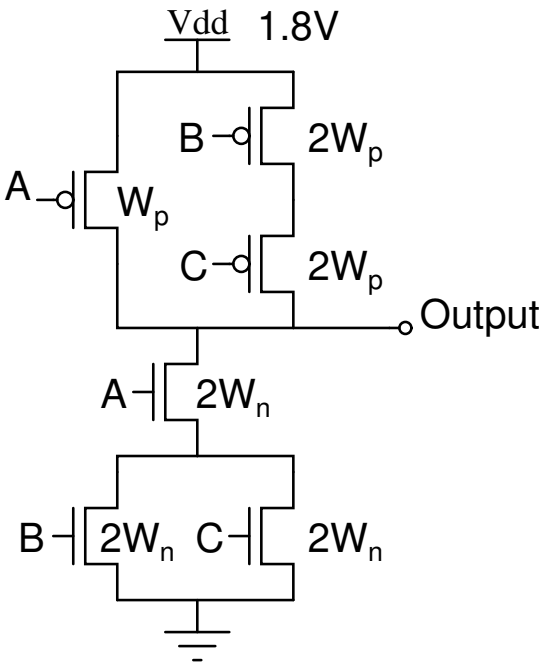

Figure 4: Logic Gate Design

The scaling is as shown in diagram to account for worst case (B and C's PMOS scaled by 2 since in series, and all NMOS scaled by 2 since 2 in series at a time in the worst case), where W_p and W_n are the lengths of transistors of the inverter in Q1.

Keeping the rise and fall times of input fixed at 20ps, we vary the values of inputs.

A	B	C	Rise Time (in ps)	Fall Time (in ps)
$0 \longleftrightarrow 1$	1	1	335.40	245.83
$0 \longleftrightarrow 1$	0	1	335.40	311.72
$0 \longleftrightarrow 1$	1	0	385.16	343.63
1	$0 \longleftrightarrow 1$	0	359.74	343.63
1	0	$0 \longleftrightarrow 1$	359.74	311.72

```
* Unit Inverter
.subckt logic_gate supply Inp_A Inp_B Inp_C Output

.param Len = 0.18U

.param Wp = 1.275U Wn = 0.407U
.param Wp_A = Wp Wp_B = 2*Wp Wp_C = 2*Wp
.param Wn_A = 2*Wn Wn_B = 2*Wn Wn_C = 2*Wn

.param Area_p_A = {2*Len*Wp_A} Area_n_A = {2*Len*Wn_A}
.param Area_p_B = {2*Len*Wp_B} Area_n_B = {2*Len*Wn_B}
.param Area_p_C = {2*Len*Wp_C} Area_n_C = {2*Len*Wn_C}

.param Per_p_A = {2*(Wp_A + 2*Len)} Per_n_A = {2*(Wn_A + 2*Len)}
```

```
.param Per_p_B = {2*(Wp_B + 2*Len)} Per_n_B = {2*(Wn_B + 2*Len)}
.param Per_p_C = {2*(Wp_C + 2*Len)} Per_n_C = {2*(Wn_C + 2*Len)}

MP_A Output Inp_A Supply Supply cmosp
+ L = Len W = Wp_A AD = Area_p_A AS = Area_p_A PD = Per_p_A PS =
    Per_p_A

MP_B o1 Inp_B Supply Supply cmosp
+ L = Len W = Wp_B AD = Area_p_B AS = Area_p_B PD = Per_p_B PS =
    Per_p_B

MP_C Output Inp_C o1 Supply cmosp
+ L = Len W = Wp_C AD = Area_p_C AS = Area_p_C PD = Per_p_C PS =
    Per_p_C

MN_A Output Inp_A o2 0 cmosn
+ L = Len W = Wn_A AD = Area_n_A AS = Area_n_A PD = Per_n_A PS =
    Per_n_A

MN_B o2 Inp_B 0 0 cmosn
+ L = Len W = Wn_B AD = Area_n_B AS = Area_n_B PD = Per_n_B PS =
    Per_n_B

MN_C o2 Inp_C 0 0 cmosn
+ L = Len W = Wn_C AD = Area_n_C AS = Area_n_C PD = Per_n_C PS =
    Per_n_C
.ends

vdd supply 0 dc 1.8

* Device under test
x1 supply Inp_A Inp_B Inp_C dutout logic_gate

* Load Capacitor
C3 dutout 0 0.05pF

.include models-180nm

VA Inp_C 0 DC 0 PULSE(0 1.8 0nS 25pS 25pS 4nS 8.0nS)
VB Inp_A 0 1.8
VC Inp_B 0 0

.tran 1pS 35nS 0nS
.control
run
let Ck = V(Inp_C)
meas tran inrise TRIG v(Ck) VAL=0.18 RISE=2 TARG v(Ck) VAL=1.62 RISE=2
meas tran infall TRIG v(Ck) VAL=1.62 FALL=2 TARG v(Ck) VAL=0.18 FALL=2
meas tran drise TRIG v(dutout) VAL=0.18 RISE=2 TARG v(dutout) VAL=1.62
    RISE=2
meas tran dfall TRIG v(dutout) VAL=1.62 FALL=2 TARG v(dutout) VAL=0.18
    FALL=2

print inrise infall drise dfall

.endc
.options savecurrents
.end
```