EE719
Course Project

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Contents

1 Target Specifications

In the following design of the unit cell, these specifications have been considered:

Parameter	Value
Total number of bits ($B = B_b + B_t$)	8
Number of binary bits (B_b)	2
Number of thermometer bits (B_t)	6
Supply Voltage (V_{DD})	1.2 V
Output Voltage Swing (Differential Peak-Peak) V_{FS}	> 0.8 V_{pp}
σ_{INL}	< 1 LSB
σ_{DNL}	< 0.5 LSB
SFDR	> 50 dB
Sampling Frequency (f_s)	1GSps

2 Design of Unit Cell

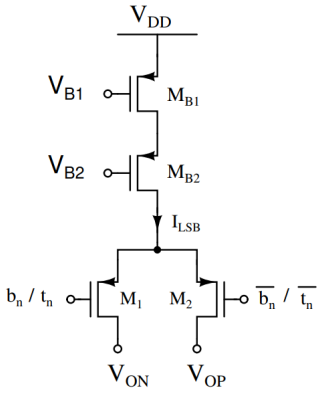


Figure 1: Circuit for DAC Unit Cell

Parameter	Value Used
R	29 Ω
$\mu_p C_{ox}$	140 $\mu A/V^2$
A_β	4% μm
$A_{V_{TH}}$	$4.6mV \cdot \mu m$

Things to incorporate in design as per Razavi's paper:

- $V_{SD,Sat} \approx 200mV$ for M_{B1} and M_{B2} and $V_{SD,Sat} \approx 100mV$ for M_1 and M_2
- Value of L for M_{B1} and M_{B2} should be large to minimize effect of output resistance
- For fast switching and minimal capacitance at the tail node, the switching transistors should have minimum channel length, i.e. 45 nm in our design

2.1 Calculating I_{LSB} and V_{FS} values

For proper operation of M_{B1} and M_{B2} as part of cascode current source, they should always stay in saturation.

The following assumptions are made for these two transistors, to be able to decide biasing voltages:

$$V_{THp} = 0.5V$$
$$V_{SD,Sat,M_{B1}} = V_{SD,Sat,M_{B2}} = 200mV$$
$$V_{SD,M_{B1}} = V_{SD,M_{B2}} = 300mV$$

Therefore, $V_{SG,M_{B1}} = V_{SG,M_{B2}} = V_{THp} + V_{DS,Sat} = 0.5 + 0.2 = 0.7$

$$V_{B1} = V_{DD} - V_{SG,M_{B1}} = 1.2 - 0.7 = 0.5V$$
$$V_{B2} = V_{DD} - V_{SD,M_{B1}} - V_{SG,M_{B2}} = 1.2 - 0.3 - 0.7 = 0.2V$$
$$V_{D,M_{B2}} = V_{DD} - V_{SD,M_{B1}} - V_{SD,M_{B2}} = 1.2 - 0.3 - 0.3 = 0.6V$$

When either of M_1 or M_2 turns on, it should also be in saturation. Say, $b_n = 0$. For M_1 to turn on:

$$V_{SG,M1} > V_{THp} \implies 0.6 > 0.5$$

This relation automatically holds, so our assumption that $V_{SD} = 300mV$ for M_{B1} and M_{B2} and therefore our choices for bias voltages are justified.
Also, $V_{SD,Sat,M_1/M_2} = V_{D,M_{B2}} - V_{THp} = 0.6 - 0.5 = 0.1V$, so it adheres to the what is recommended in Razavi's paper.

For the given 8-bit DAC architecture given, the maximum value of $V_{ON} = 255I_{LSB}R$. If the saturation condition is satisfied for this, M_1 will be in saturation for all input values when $b_n = 0$ (Taking $b_n = 1$ and requiring M_2 to be in saturation gives same result)
For M_1 to be in saturation, we need

$$V_{SD,M_1} > V_{SG,M_1} - V_{THp}$$
$$V_S - 255I_{LSB} \cdot R > V_S - 0 - 0.5$$
$$I_{LSB} < \frac{0.5}{255 \times 29}$$
$$I_{LSB} < 67.61\mu A \tag{1}$$

$$V_{out,max} = (V_{OP} - V_{ON})_{max} = V_{OP,max} = 255I_{LSB} \cdot R$$
$$V_{out,min} = (V_{OP} - V_{ON})_{min} = -V_{ON,max} = -255I_{LSB} \cdot R$$

$$V_{FS} = V_{out,max} - V_{out,min} = 2 \times 255I_{LSB} \cdot R$$

As per the specification given,

$$V_{FS} > 0.8V$$
$$2 \times 255I_{LSB} \times 29 > 0.8$$
$$I_{LSB} > 54.09\mu A \tag{2}$$

Using equations 4 and 2, I'm choosing:

$$\boxed{I_{LSB} = 60\mu A}$$

This results in full scale voltage to be

$$V_{FS} = 2 \times 255 \times 60 \times 10^{-6} \times 29$$
$$\boxed{V_{FS} = 0.8874V}$$

2.2 Calculating W and L values

Ignoring channel length modulation,

$$I_D = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}{V_{SD,Sat}}^2$$

Substituting the values for M_{B1} and M_{B2},

$$60 \times 10^{-6} = \frac{1}{2} \times 140 \times 10^{-6} \times \left(\frac{W}{L}\right)_{M_B} \times 0.2^2$$

This gives $(W/L)_{M_{B1}} = (W/L)_{M_{B2}} = 150/7$

Similarly, substituting $V_{SD,Sat} = 0.1V$ for M_1 and M_2, we get $(W/L)_{M_1} = (W/L)_{M_2} = 600/7$

We have,

$$\sigma_{INL} = \frac{\sigma_{I_{LSB}}}{2I_{LSB}}\sqrt{2^8} < 1 \text{ LSB} \tag{3}$$

From Pelgrom's paper,

$$\frac{{\sigma_{I_{LSB}}}^2}{{I_{LSB}}^2} = \frac{4{\sigma_{V_{TH}}}^2}{{V_{SD,Sat}}^2} + \frac{{\sigma_\beta}^2}{\beta^2}$$

From the above equation, substituting the following into equation 3,

$$\sigma^2_{V_{TH}} = \frac{{A_{V_{TH}}}^2}{WL}$$

$$\frac{{\sigma_\beta}^2}{\beta^2} = \frac{{A_\beta}^2}{WL}$$

We get:

$$\sqrt{\frac{1}{WL}\left(\frac{4{A_{V_{TH}}}^2}{{V_{SD,Sat}}^2} + {A_\beta}^2\right)} < \frac{1}{8}$$

$$WL > 64 \times \left(\frac{4 \times 4.6^2}{200^2} + 0.04^2\right)\mu m^2$$

$$WL > 0.2378\mu m^2$$

Since INL is caused due to mismatches in current sources, this relation is applicable to M_{B1} and M_{B2}. Since (W/L) for these transistors is 150/7,

$$\frac{150}{7}L^2 > 0.2378\mu m^2$$

$$\implies L > 105.35nm$$

Since a larger L means larger output resistance, I'm choosing $L_{M_{B1}} = L_{M_{B2}} = 7 \times 45 = 315nm$ Therefore, $W_{M_{B1}} = W_{M_{B2}} = 150 \times 45 = 6.75\mu m$ using the (W/L) ratios calculated.

For the differential transistors at the tail node, $L_{M_1} = L_{M_2} = 45nm$ since we require minimum length for fast switching. We get, $W_{M_1} = W_{M_2} = \frac{600}{7} \times 45nm \approx 3.85\mu m$

For the segmented DAC architecture given, ${\sigma_{DNL}}^2 = \frac{8{\sigma_{I_{LSB}}}^2}{{I_{LSB}}^2}$
This gives

$$\frac{\sigma_{I_{LSB}}}{I_{LSB}} < 0.125 \text{ LSB}$$

which is a less stringent condition than what was obtained for INL requirements, so DNL specification is automatically met.

Parameter	M_{B1}	M_{B2}	M_1	M_2	V_{FS}	I_{LSB}
Width	6.75 μm	6.75 μm	3.85 μm	3.85 μm	0.8874 V	60 μA
Length	315 nm	315 nm	45 nm	45nm	-	-

2.3 Designing Cascode Current Source

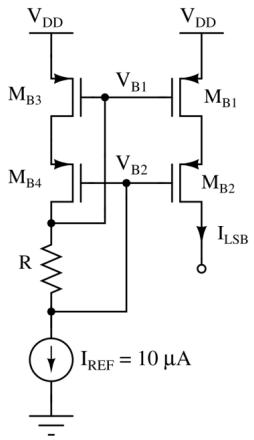


Figure 2: Circuit for Cascode Current Source

For good matching, $L_{M_{B1}} = L_{M_{B2}} = L_{M_{B1}} = L_{M_{B2}} = 315nm$

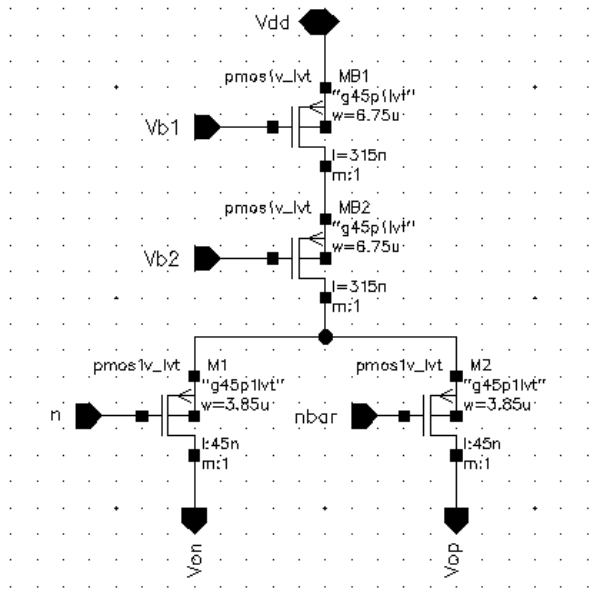
Also,

$$\frac{I_{LSB}}{I_{REF}} = \frac{(W/L)_{M_{B1/2}}}{(W/L)_{M_{B3/4}}} = \frac{W_{M_{B1/2}}}{W_{M_{B3/4}}} = 6$$

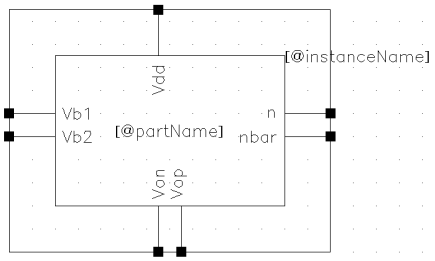
We get $W_{M_{B3}} = W_{M_{B4}} = 6.75/6 = 1.125\mu m$
Since we calculated the bias voltages before,

$$R = \frac{V_{B1} - V_{B2}}{10\mu A} = \frac{0.5 - 0.2}{10\mu A} = 30k\Omega$$

Parameter	M_{B3}	M_{B4}	R
Width	1.125 μm	1.125 μm	30 $k\Omega$
Length	315 nm	315 nm	-



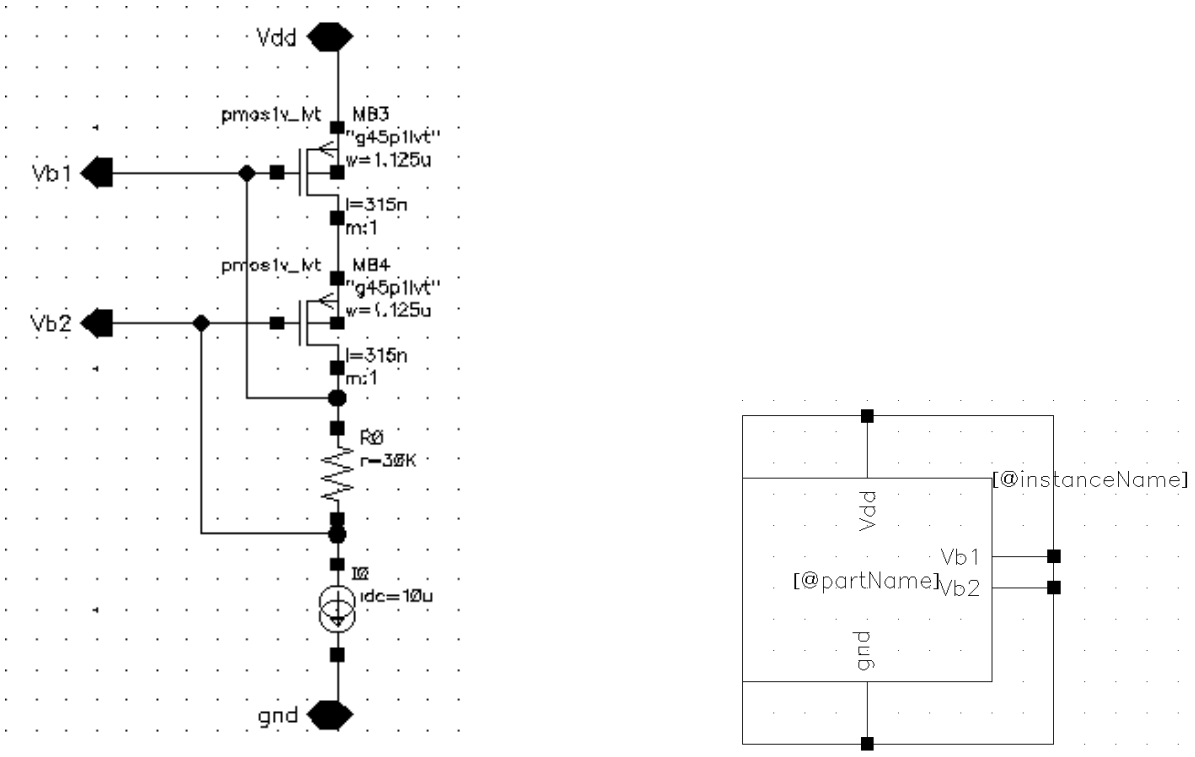
(a) Schematic



(b) Symbol

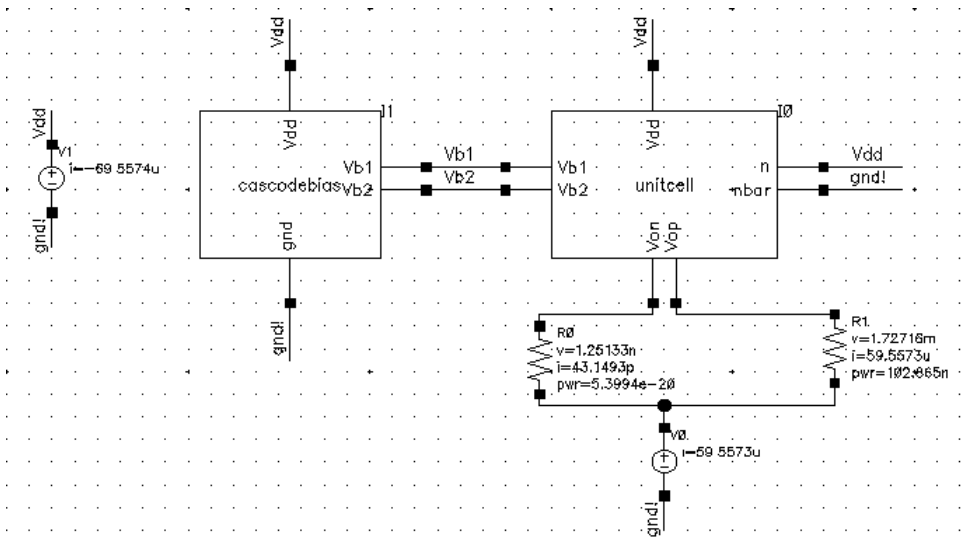
Figure 3: DAC unit cell (fig 2 in project pdf)

3 Schematic and operating points of unit cell

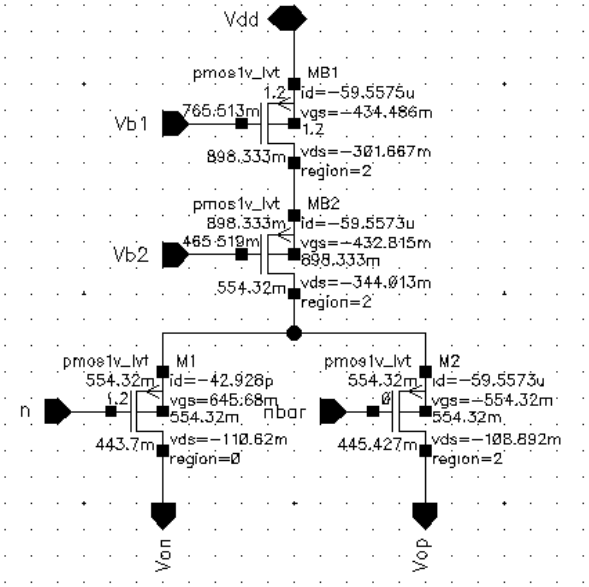


(a) Schematic (b) Symbol

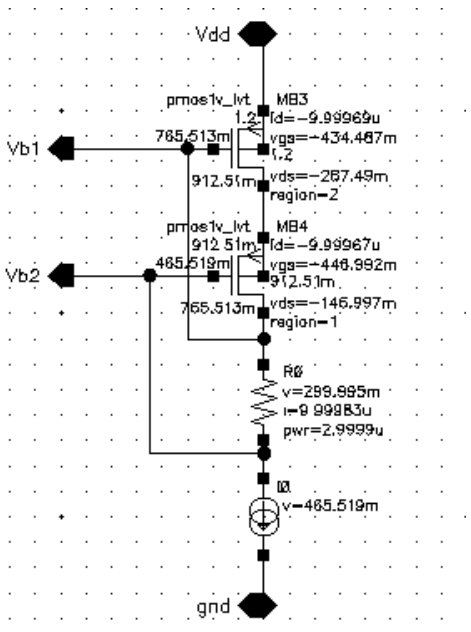
Figure 4: Cascode biasing (fig 3 in project pdf)



(a) Testbench

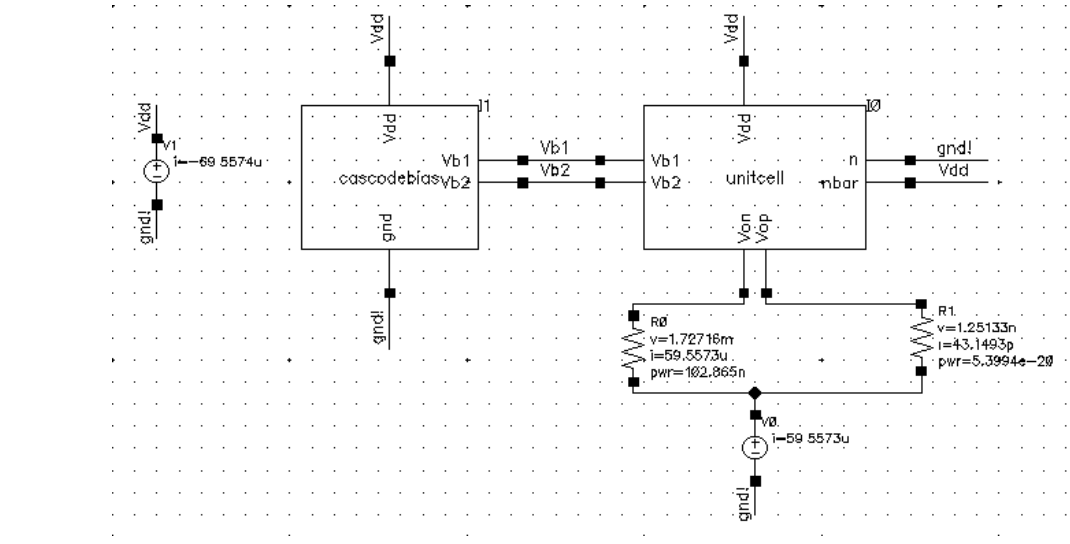


(b) Unit cell

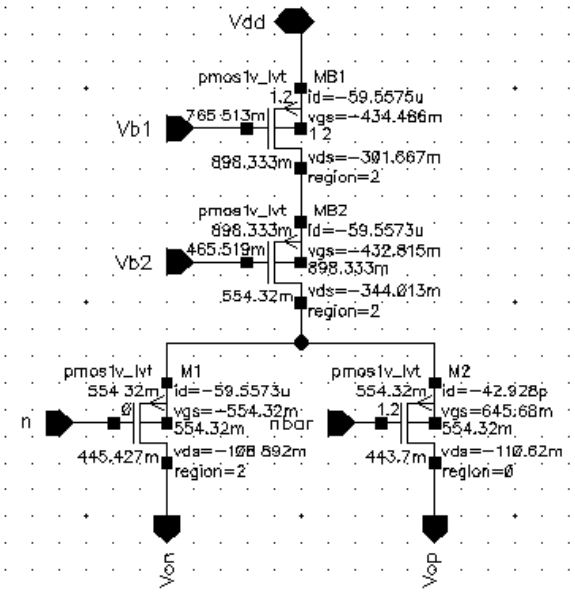


(c) Cascode biasing

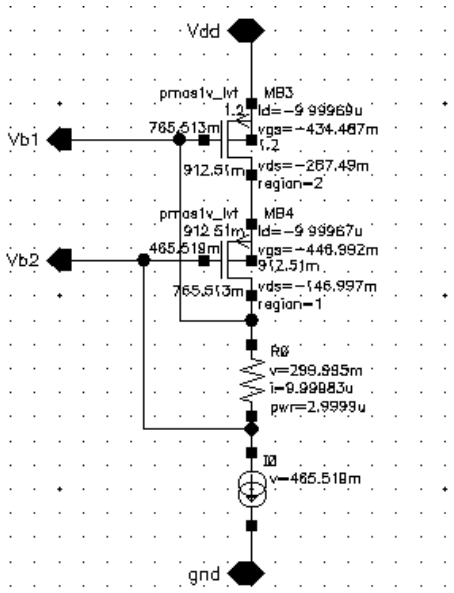
Figure 5: DC operating points for $b_n = 1$



(a) Testbench

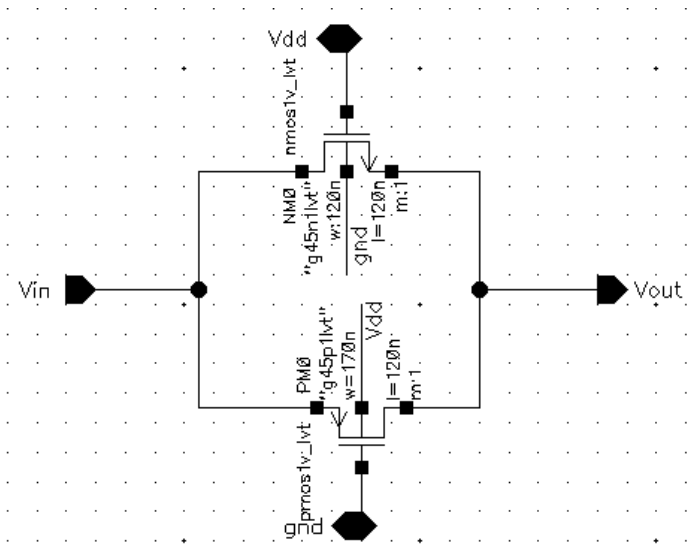


(b) Unit cell

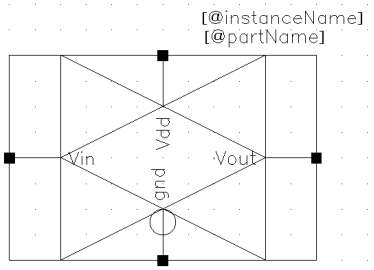


(c) Cascode biasing

Figure 6: DC operating points for $b_n = 0$



(a) Schematic



(b) Symbol

Figure 7: Pass transistor

4 Pass transistor and inverter

Parameter	NM0	PM0
Width	135 nm	225 nm
Length	45 nm	45 nm

Table 1: Parameters for inverter

Parameter	NM0	PM0
Width	120 nm	170 nm
Length	120 nm	120 nm

Table 2: Parameters for pass transistor

Parameter	Inverter	Pass transistor	Difference
Falling edge of input	114.350 ps	115.893 ps	1.543 ps
Rising edge of input	118.128 ps	115.782 ps	2.346 ps

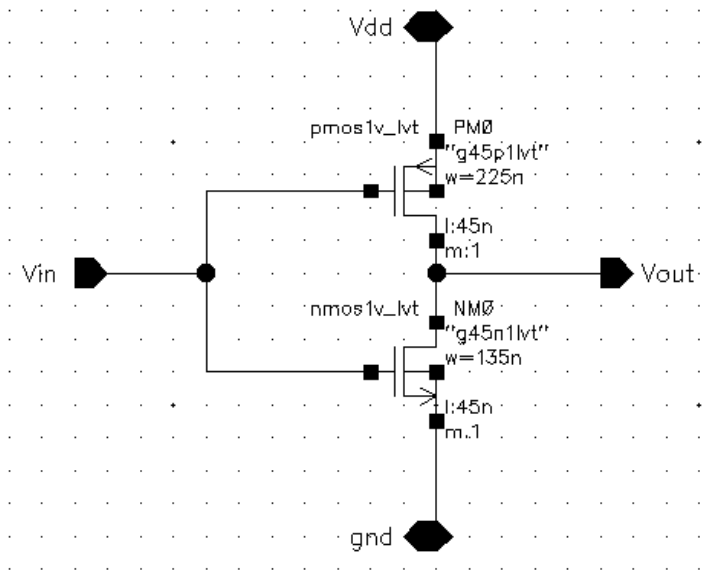
Table 3: Delays of pass transistor and inverter

5 Buffer Design

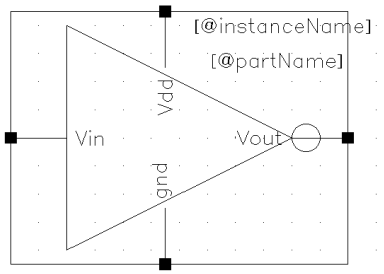
According to the buffer design paper,

$$n = \frac{ln\,(C_L/C_i)}{ln(\beta)}$$

Since we have $\beta = e$, the denominator reduces to 1. For the value of C_L, a DC operating point analysis of the testbench circuit (5a) has been performed to find C_{gg}. When $b_n = 1$, $C_{gg,M1} = 2.45835fF$ and $C_{gg,M2} = 2.99401fF$ and these values are swapped when $b_n = 0$.



(a) Schematic



(b) Symbol

Figure 8: Inverter

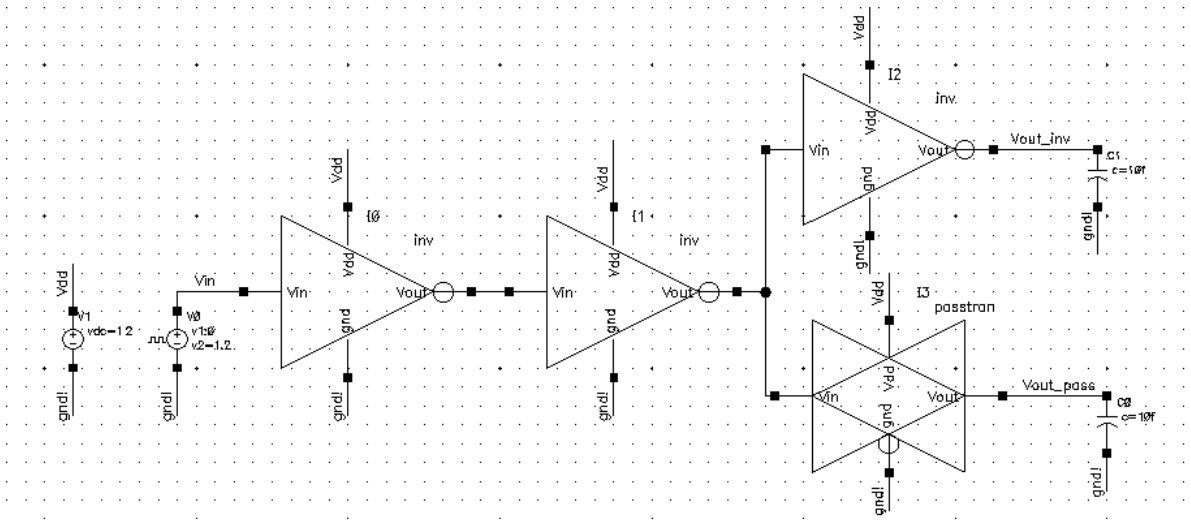


Figure 9: Pass transistor and inverter testbench

Since we're interested in the max capacitive loading, C_L is taken as $2.99401fF$ for the calculations (in the testbench circuit, this is approximately taken as $3fF$).
For the inverter, the capacitance of PMOS and NMOS are in parallel, so they add up. Therefore, $C_i = C_{gg,NM0} + C_{gg,PM0} = 52.2064 + 220.092aF = 272.2984aF$

Substituting these values,

$$n = ln\left(2.99401 \times 10^{-15}/272.2984 \times 10^{-18}\right) = 2.39 \approx 2$$

Here, the number of stages, n has been rounded off to 2, the closest integer.

In the first stage, $(W/L)_{NM0} = 135/45$, so in the second stage, $(W/L)_{NM1} = 135/45 \times 2.72 = 367.2/45 \approx 365/45$

Also, in the first stage, $(W/L)_{PM0} = 225/45$, so in the second stage, $(W/L)_{PM1} = 225/45 \times$

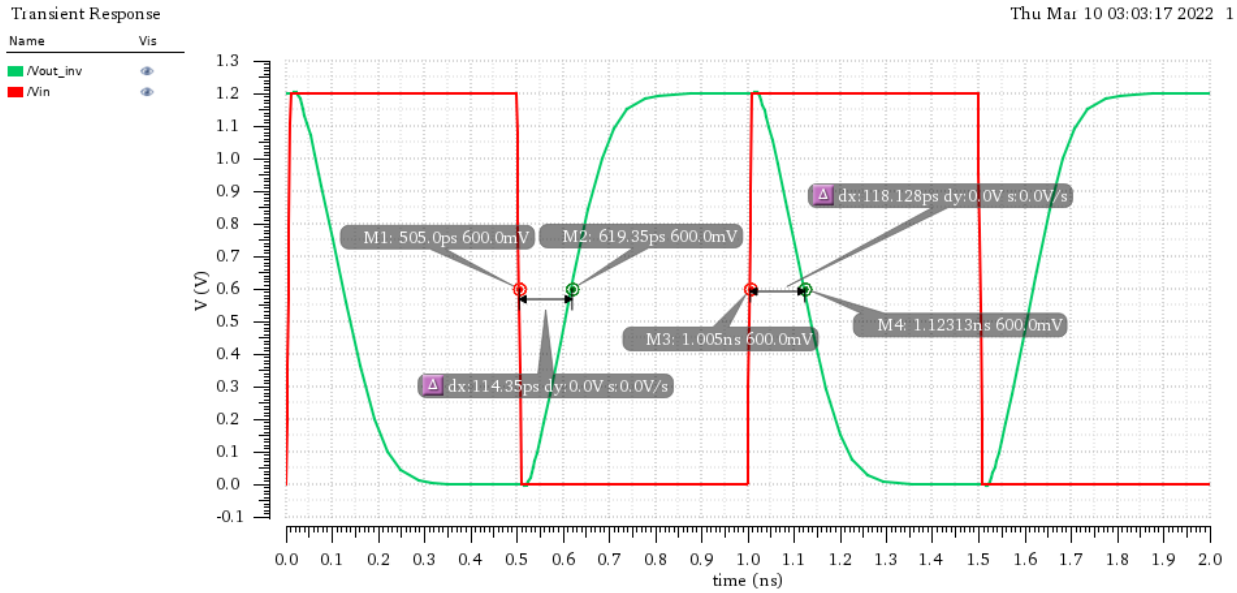


Figure 10: Delay of inverter

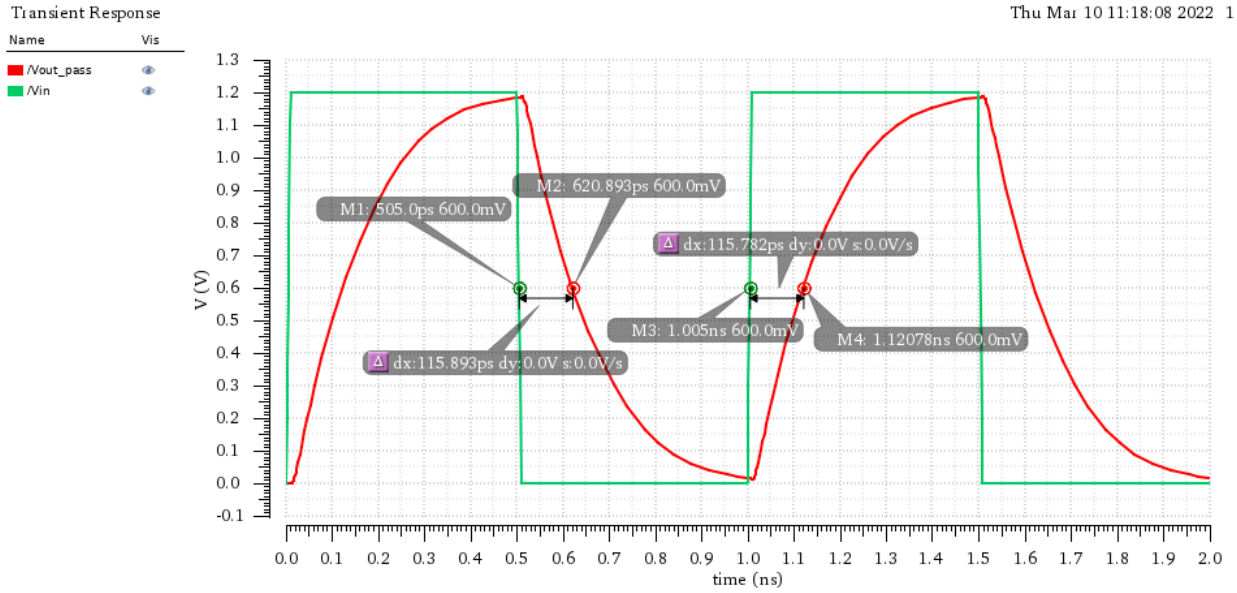
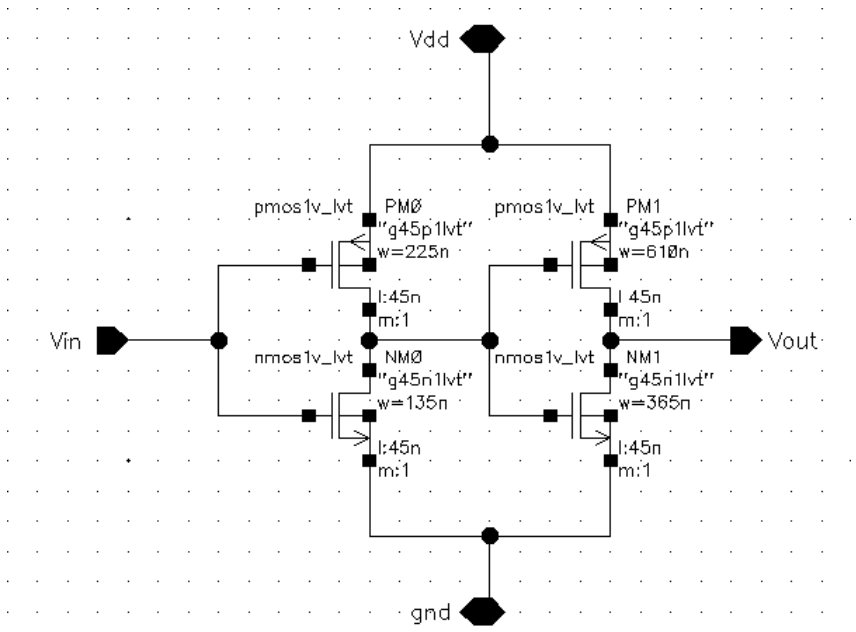


Figure 11: Delay of pass transistor

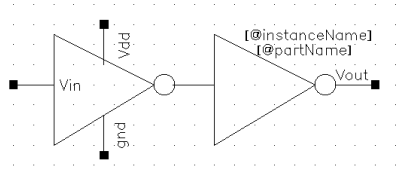
$2.72 = 612/45 \approx 610/45$

Parameter	NM0	PM0	NM1	PM1
Width	135 nm	225 nm	365 nm	610 nm
Length	45 nm	45 nm	45 nm	45 nm

Table 4: Parameters of buffer transistors



(a) Schematic



(b) Symbol

Figure 12: Buffer

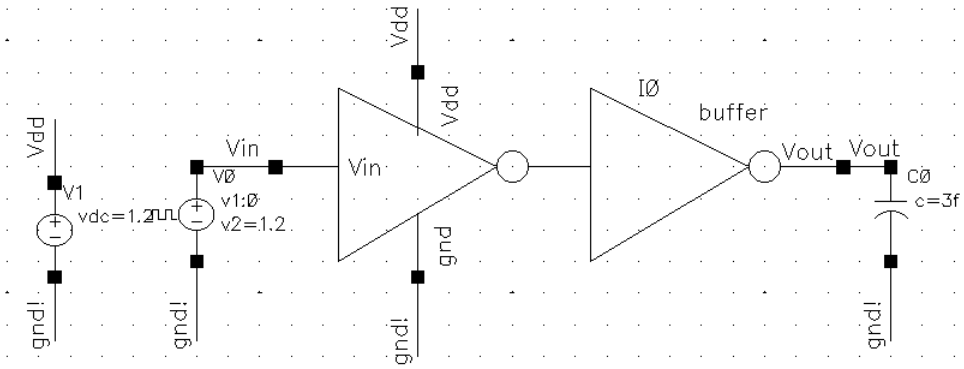


Figure 13: Buffer testbench

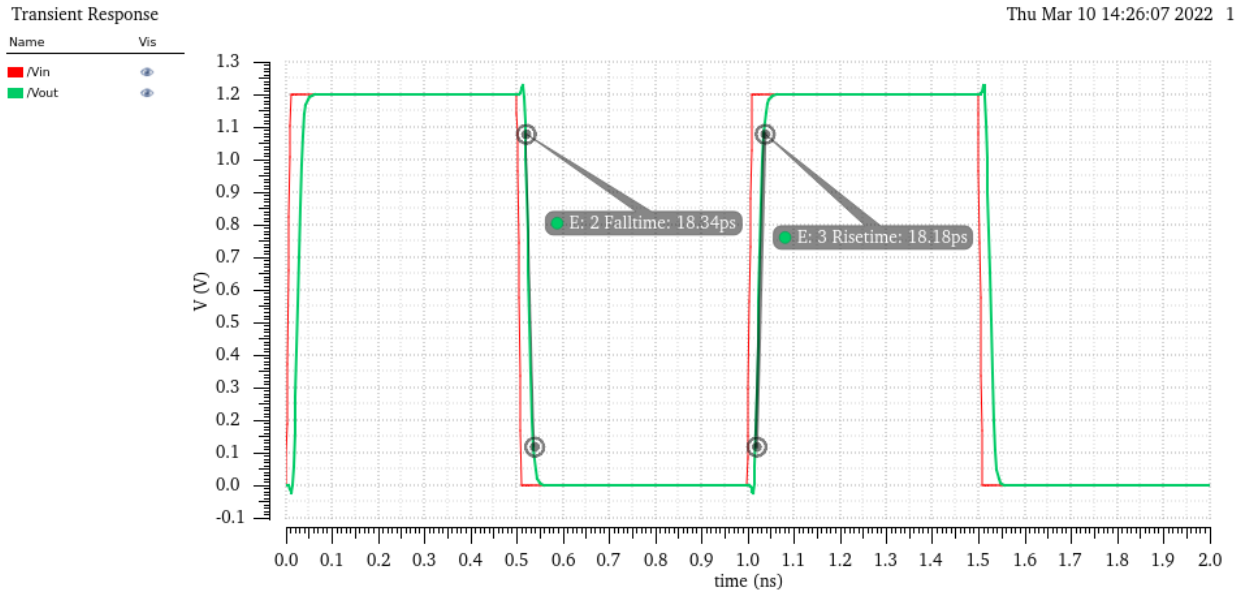


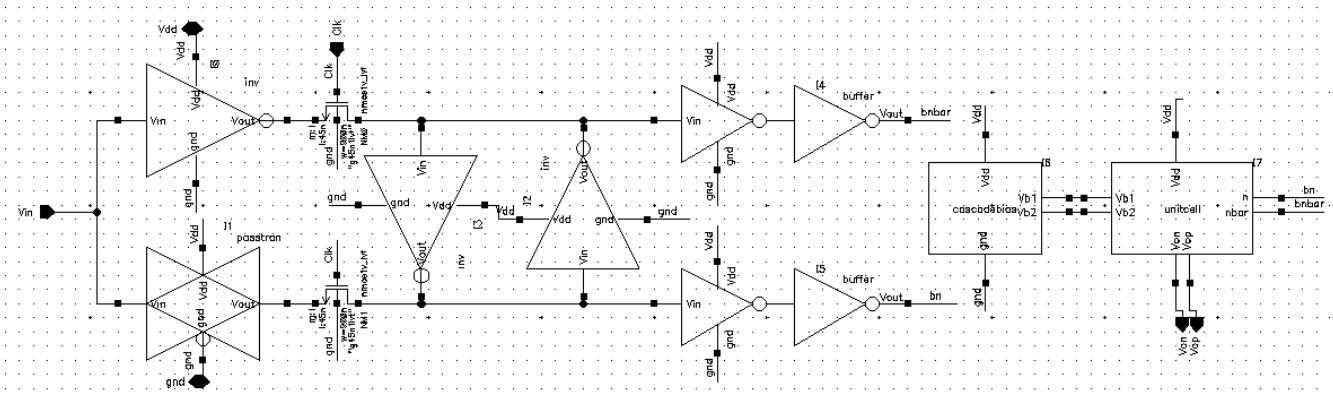
Figure 14: Transient simulation of buffer testbench at 1GHz

6 Unit cell

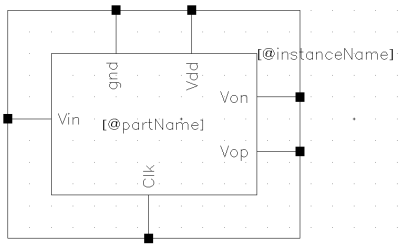
As suggested, the aspect ratio of NMOS sampling switch is taken as 20 ($W = 900nm$, $L = 45nm$).

The plots show that b_n follows B_n and $\bar{b_n}$ is the inverted version of B_n, albeit with a slight delay.

We see that when B_n, and therefore b_n is high, M1 is off (in cutoff, region 0) so $V_{ON} = V_{FS}/2 = 887.4/2 = 443.7mV$. When b_n is high, M2 is on (in saturation, region 2), so $V_{OP} = I_{LSB} \cdot R + V_{FS}/2 = 60 \times 10^{-3} \times 29 + 887.4/2 = 444.44mV$. The values are interchanged when b_n is low.



(a) Schematic



(b) Symbol

Figure 15: Entire unit cell

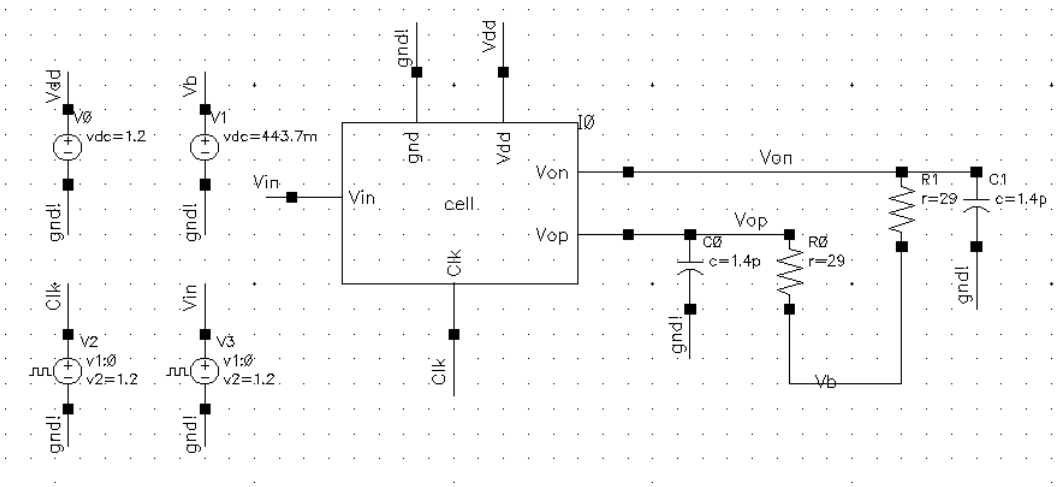
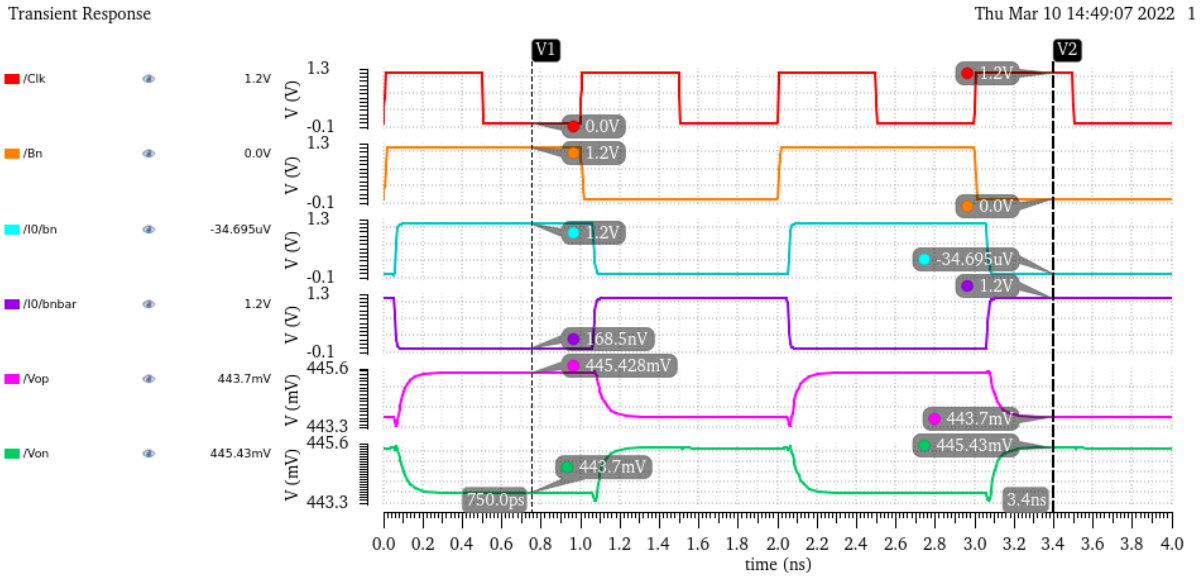
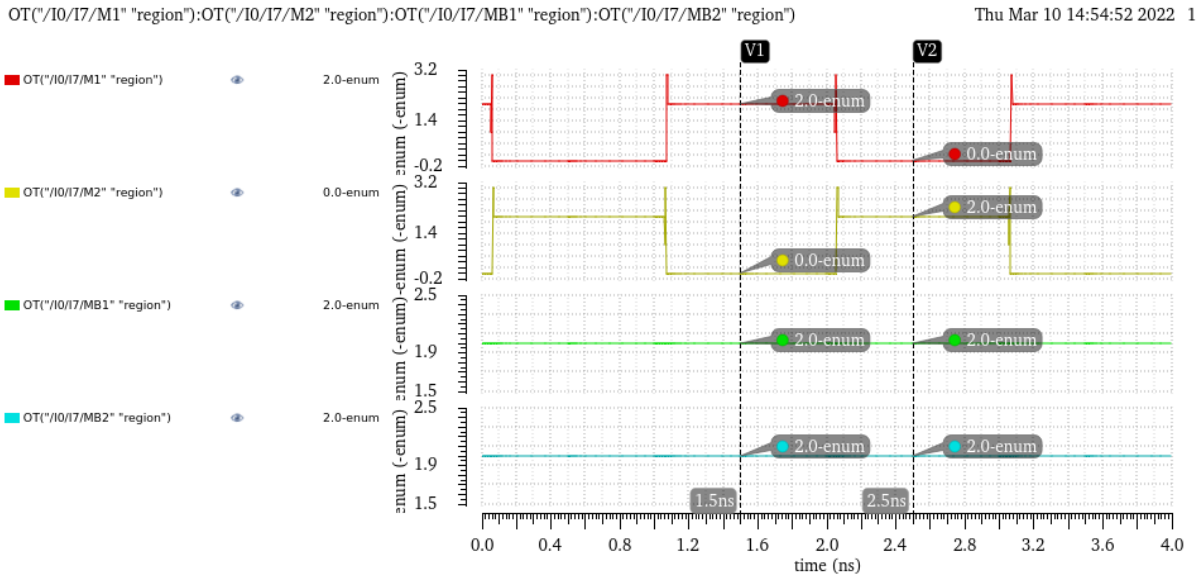


Figure 16: Unit cell testbench



(a) Plots



(b) Region of operation of the current source and current switch transistors

Figure 17: Entire unit cell

"01010100"	Value	1	1	1	0	0	0	0	0
Value		C0	C1	C2	C3	C4	C5	C6	C7
1	R0								
1	R1								
1	R2								
1	R3								
1	R4								
0	R5								
0	R6								
0	R7								

(a) Cells contributing for 01010100

"01110100"	Value	1	1	1	1	0	0	0	0
Value		C0	C1	C2	C3	C4	C5	C6	C7
1	R0								
1	R1								
1	R2								
1	R3								
1	R4								
0	R5								
0	R6								
0	R7								

(b) Cells contributing for 01110100

Figure 18: Cells contributing to I_{OP}

7 Working of row-column decoder

In the figures shown, the colored cells (blue+yellow) correspond to thermometer cells contributing to I_{OP}. The blue cells are those that are active due to C_n AND R_n, and the yellow cells are active due to C_{n+1}

8 Reiteration of Design

To achieve the SFDR specification, I had to re-iterate my design and increase the length of M_{B1} and M_{B2} (and therefore also M_{B3},M_{B4}). All the schematics and operating point/transient analyses done in part 2 have been repeated below.

For proper operation of M_{B1} and M_{B2} as part of cascode current source, they should always stay in saturation.
The following new assumptions are made for these two transistors:

$$V_{THp} = 0.5V$$

$$V_{SD,Sat,M_{B1}} = V_{SD,Sat,M_{B2}} = 250mV$$

$$V_{SD,M_{B1}} = V_{SD,M_{B2}} = 300mV$$

Therefore, $V_{SG,M_{B1}} = V_{SG,M_{B2}} = V_{THp} + V_{DS,Sat} = 0.5 + 0.25 = 0.75$

$$V_{B1} = V_{DD} - V_{SG,M_{B1}} = 1.2 - 0.75 = 0.45V$$

$$V_{B2} = V_{DD} - V_{SD,M_{B1}} - V_{SG,M_{B2}} = 1.2 - 0.3 - 0.75 = 0.15V$$

$$V_{D,M_{B2}} = V_{DD} - V_{SD,M_{B1}} - V_{SD,M_{B2}} = 1.2 - 0.3 - 0.3 = 0.6V$$

When either of M_1 or M_2 turns on, it should also be in saturation. Say, $b_n = 0$. For M_1 to turn on:

$$V_{SG,M1} > V_{THp} \implies 0.6 > 0.5$$

This relation automatically holds, so our assumption that $V_{SD} = 300mV$ for M_{B1} and M_{B2} and therefore our choices for bias voltages are justified.

The I_{LSB}, V_{FS} relations are still relevant, so

$$\boxed{I_{LSB} = 60\mu A}$$

$$\boxed{V_{FS} = 0.8874V}$$

W and L values

Ignoring channel length modulation,

$$I_D = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}{V_{SD,Sat}}^2$$

Substituting the values for M_{B1} and M_{B2},

$$60 \times 10^{-6} = \frac{1}{2} \times 140 \times 10^{-6} \times \left(\frac{W}{L}\right)_{M_B} \times 0.25^2$$

This gives $(W/L)_{M_{B1}} = (W/L)_{M_{B2}} = 96/7$

Similarly, substituting $V_{SD,Sat} = 0.1V$ for M_1 and M_2, we get $(W/L)_{M_1} = (W/L)_{M_2} = 600/7$

We have

$$\sigma_{INL} = \frac{\sigma_{I_{LSB}}}{2I_{LSB}}\sqrt{2^8} < 1LSB \tag{4}$$

From Pelgrom's paper,

$$\frac{{\sigma_{I_{LSB}}}^2}{{I_{LSB}}^2} = \frac{4{\sigma_{V_{TH}}}^2}{{V_{SD,Sat}}^2} + \frac{{\sigma_\beta}^2}{\beta^2}$$

From the above equation, substituting the following into equation 4,

$$\sigma^2_{V_{TH}} = \frac{{A_{V_{TH}}}^2}{WL}$$

$$\frac{{\sigma_\beta}^2}{\beta^2} = \frac{{A_\beta}^2}{WL}$$

We get:

$$\sqrt{\frac{1}{WL}\left(\frac{4{A_{V_{TH}}}^2}{{V_{SD,Sat}}^2} + {A_\beta}^2\right)} < \frac{1}{8}$$

$$WL > 64 \times \left(\frac{4 \times 4.6^2}{250^2} + 0.04^2\right)\mu m^2$$

$$WL > 0.1891 \mu m^2$$

Since INL is caused due to mismatches in current sources, this relation is applicable to M_{B1} and M_{B2}. Since (W/L) for these transistors is 150/7,

$$\frac{96}{7}L^2 > 0.1891 \mu m^2$$

$$\implies L > 117.415nm$$

Since a larger L means larger output resistance, I'm choosing $L_{M_{B1}} = L_{M_{B2}} = 14 \times 45 = 630nm$ Therefore, $W_{M_{B1}} = W_{M_{B2}} = 150 \times 45 = 8.64\mu m$ using the (W/L) ratios calculated.

For the differential transistors at the tail node, $L_{M_1} = L_{M_2} = 45nm$ since we require minimum length for fast switching. We get, $W_{M_1} = W_{M_2} = \frac{600}{7} \times 45nm \approx 3.85\mu m$

For the cascode current source, since $V_{B1} - V_{B2}$ value is still 0.3, $R = 30k\Omega$.

For good matching, $L_{M_{B1}} = L_{M_{B2}} = L_{M_{B1}} = L_{M_{B2}} = 630nm$, and $W_{M_{B3}} = W_{M_{B4}} = 8.64/6 = 1.440\mu m$

Parameter	M_{B1}	M_{B2}	M_{B3}	M_{B4}	M_1	M_2	V_{FS}	I_{LSB}	R
Width	8.64 μm	8.64 μm	1.44 μm	1.44 μm	3.85 μm	3.85 μm	0.8874 V	60 μA	30 $k\Omega$
Length	630 nm	630 nm	630 nm	630 nm	45 nm	45nm	-	-	-

9 8-bit Segmented DAC

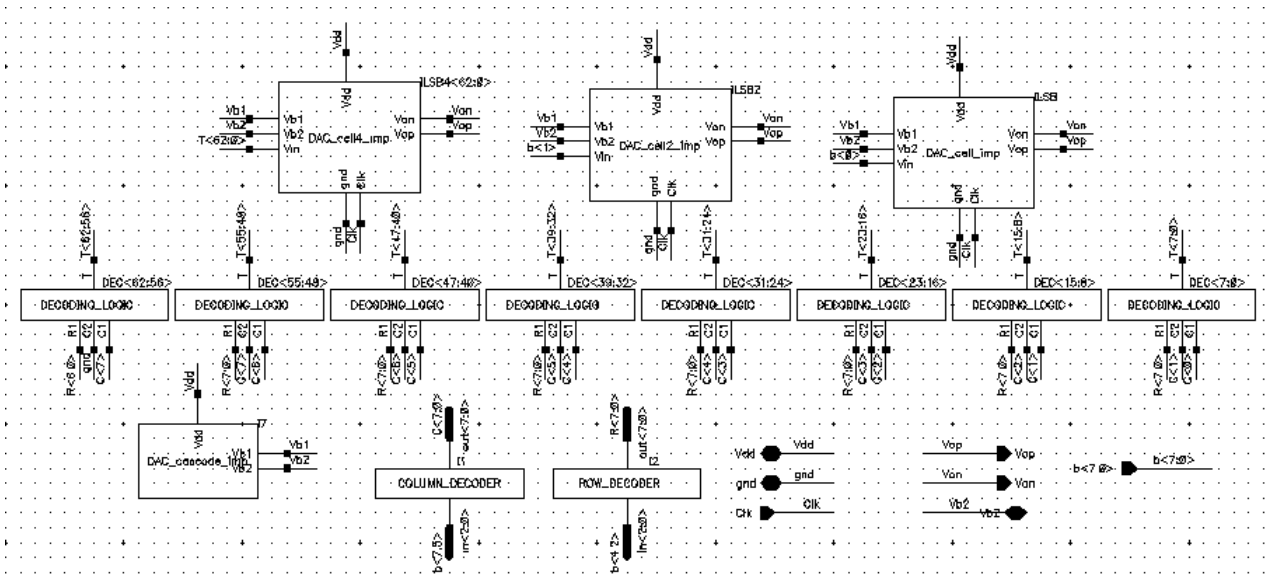


Figure 19: Schematic for DAC

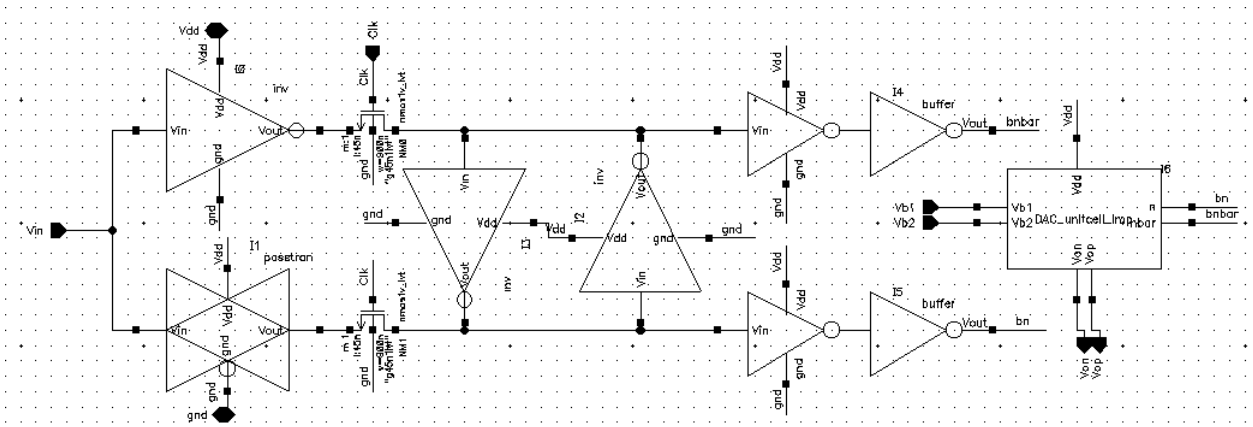


Figure 20: Schematic for DAC I_{LSB} cell

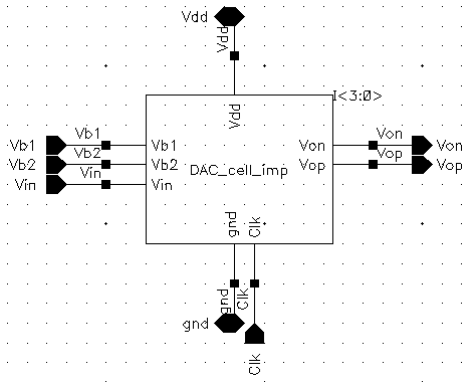


Figure 21: Schematic for DAC $4I_{LSB}$ cell

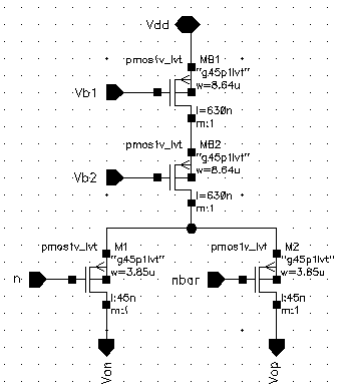


Figure 22: Schematic for DAC unit cell

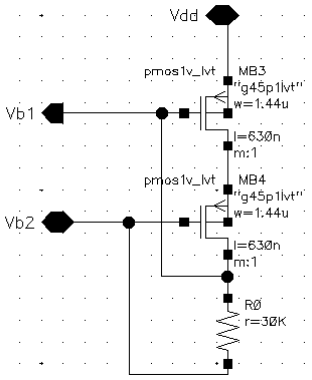
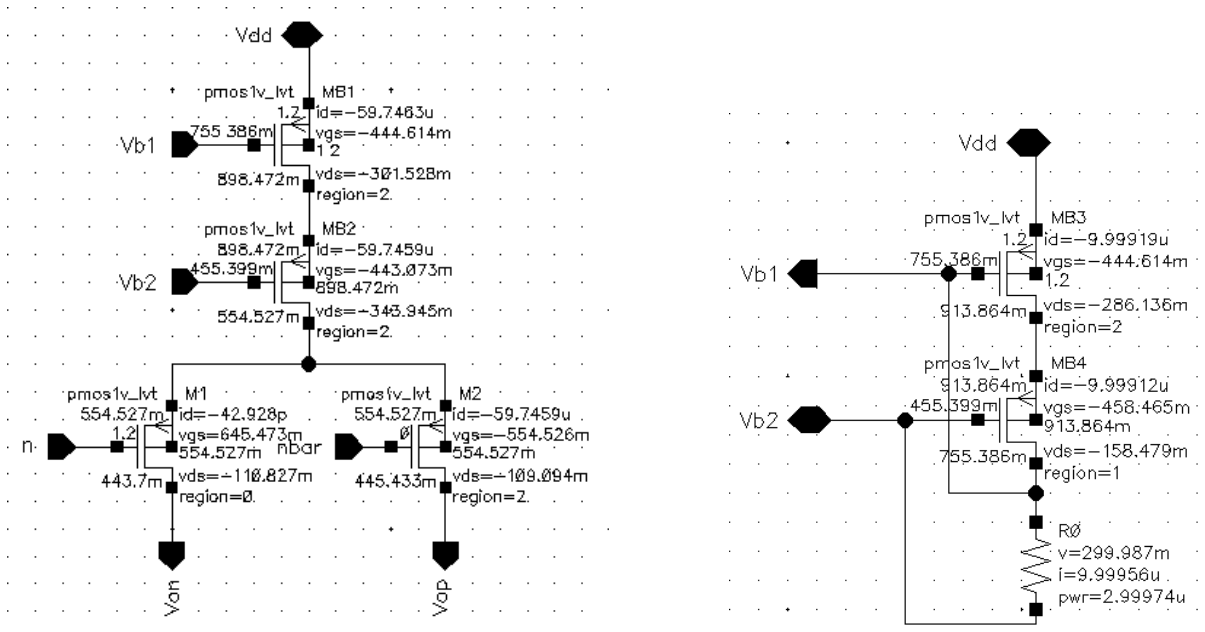
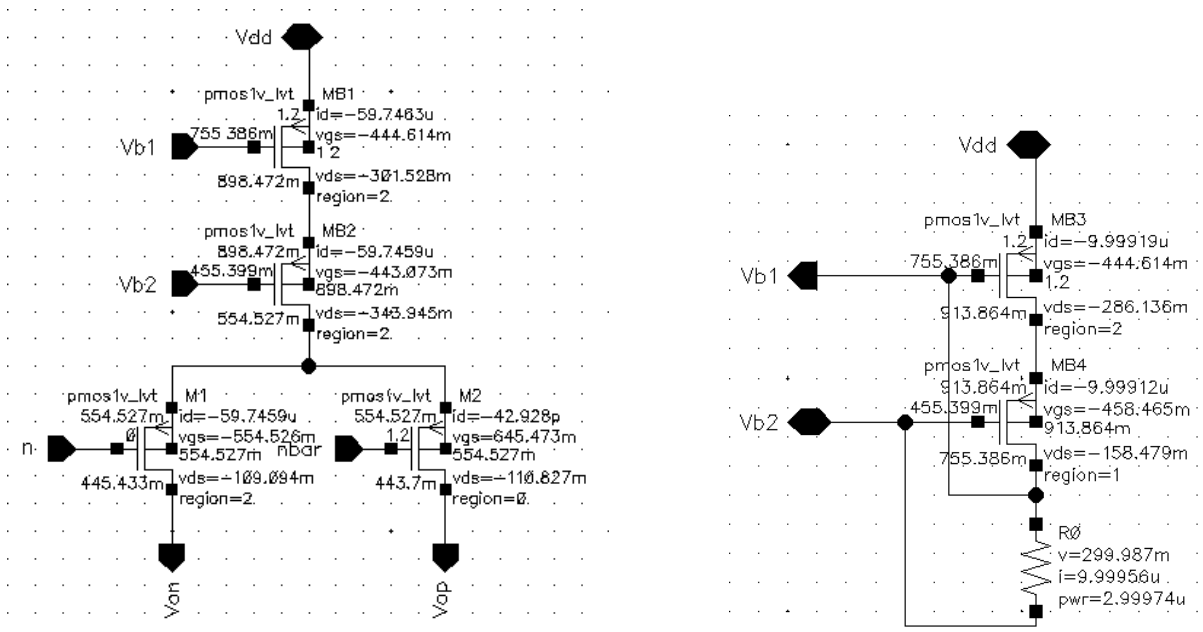


Figure 23: Schematic for DAC cascode bias cell



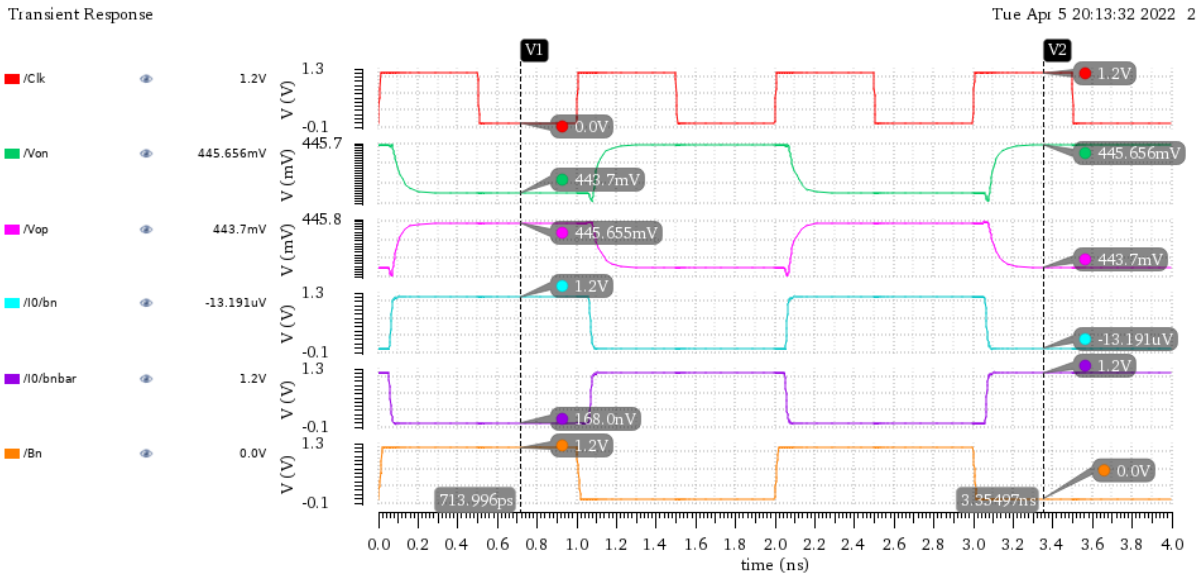
(a) Unit cell (b) Cascode biasing

Figure 24: DC operating points for $b_n = 1$

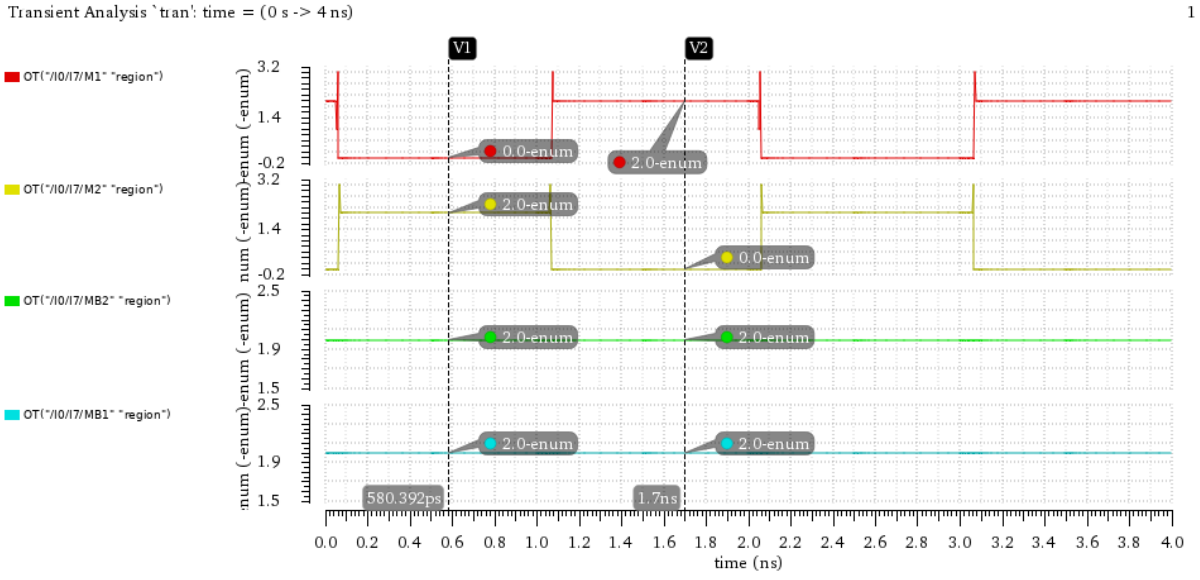


(a) Unit cell (b) Cascode biasing

Figure 25: DC operating points for $b_n = 0$



(a) Plots



(b) Region of operation of the current source and current switch transistors

Figure 26: Entire unit cell

10 DC Analysis

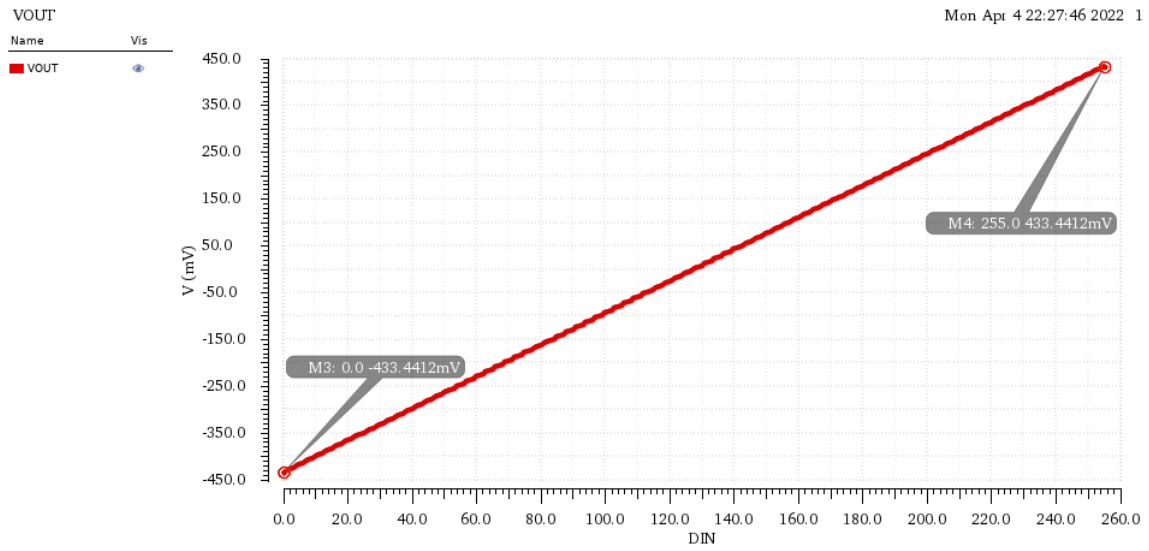


Figure 27: Different voltage output

Parameter	Value
Min Voltage	-443.4412 mV
Max Voltage	443.4412 mV
Offset error	6.9 mV
Full-scale error	-6.9 mV
Gain error	1.0160

Table 5: Parameters found during DC analysis

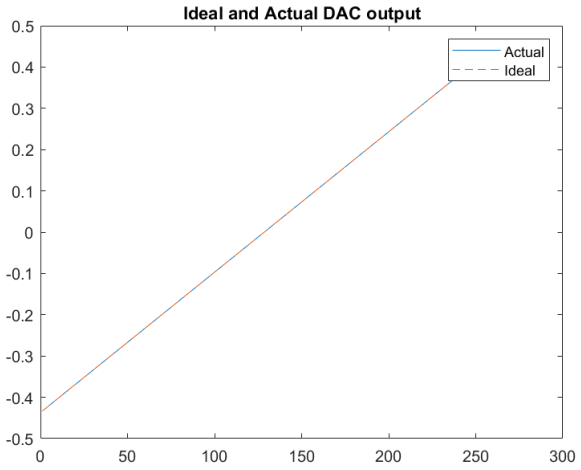


Figure 28: Ideal and output characteristics in MATLAB

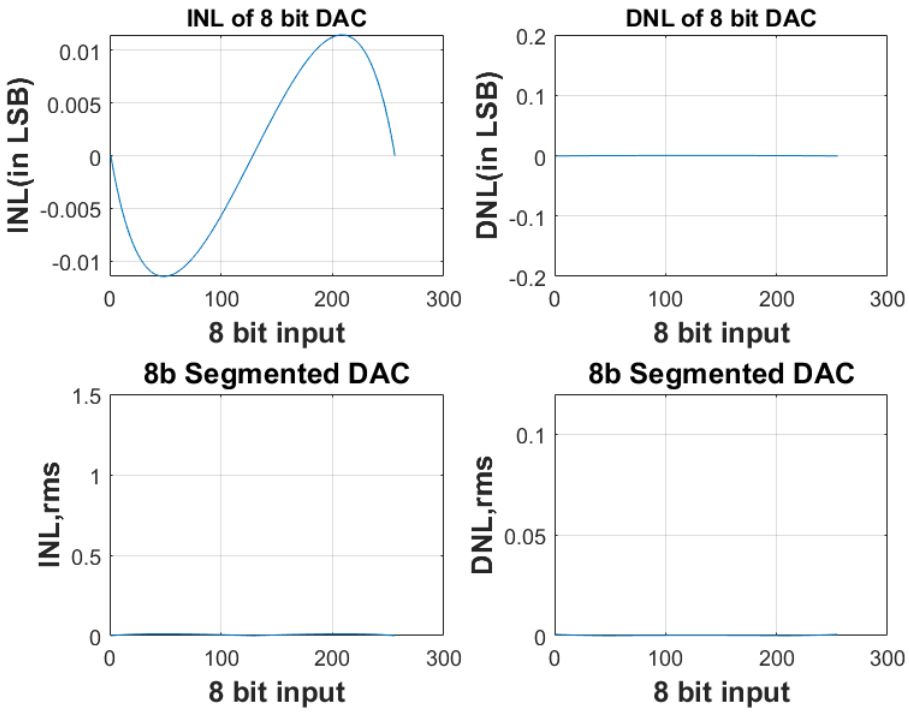


Figure 29: DNL and INL values as calculated in MATLAB

11 Monte Carlo Analysis

20 Monte Carlo simulations were performed, and the results are illustrated below.

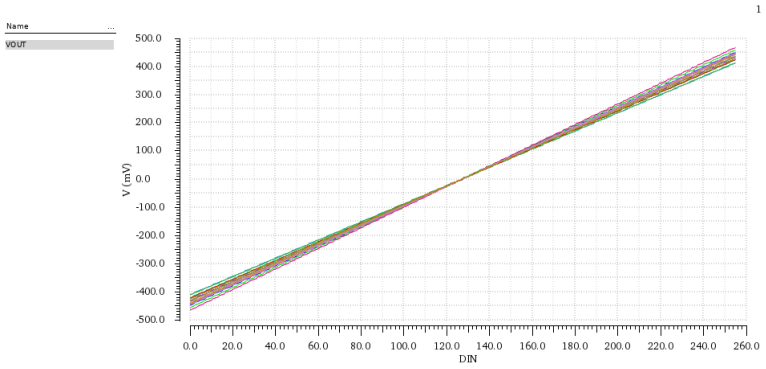


Figure 30: Differential output voltage in Cadence

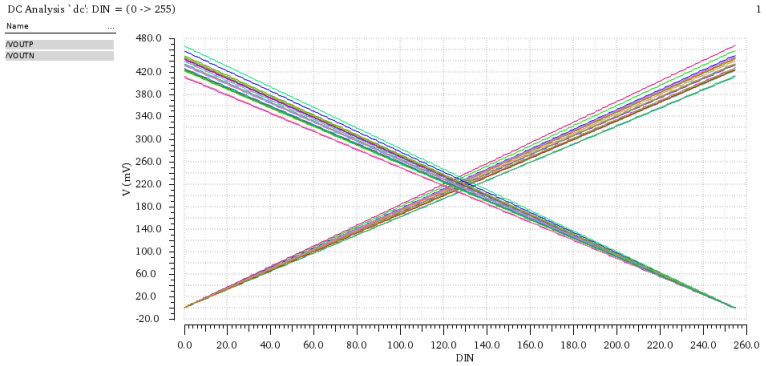


Figure 31: V_{op} and V_{on} as plotted on Cadence

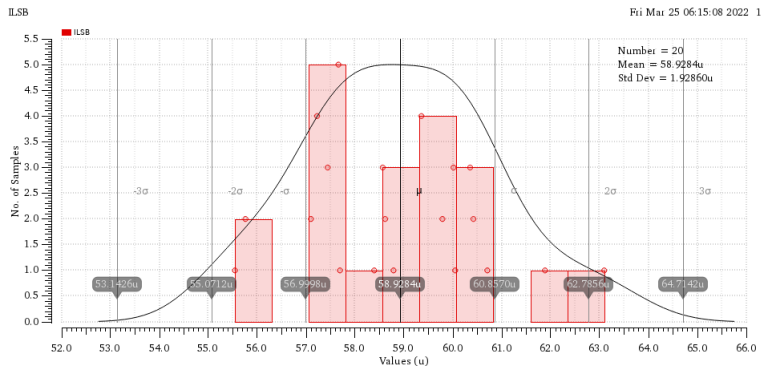


Figure 32: Distribution of current for the 20 runs

From the simulations:

- Mean $I_{LSB} = 58.9284\mu A$
- $\sigma_{I_{LSB}} = 1.9296\mu A$
- $\text{INL}_{\text{rms,max}} = 0.1261$ LSB
- $\text{DNL}_{\text{rms,max}} = 0.0473$ LSB

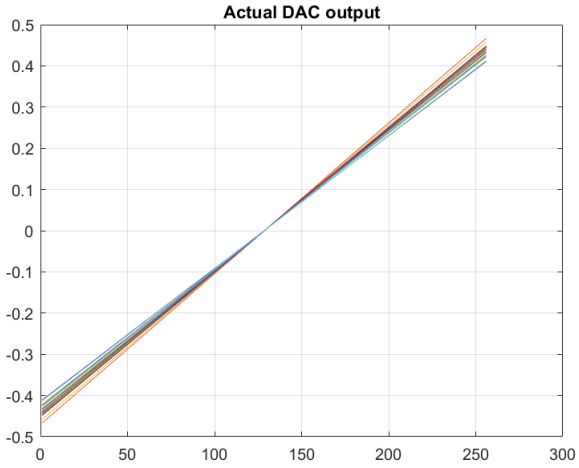


Figure 33: Ideal and output characteristics in MATLAB

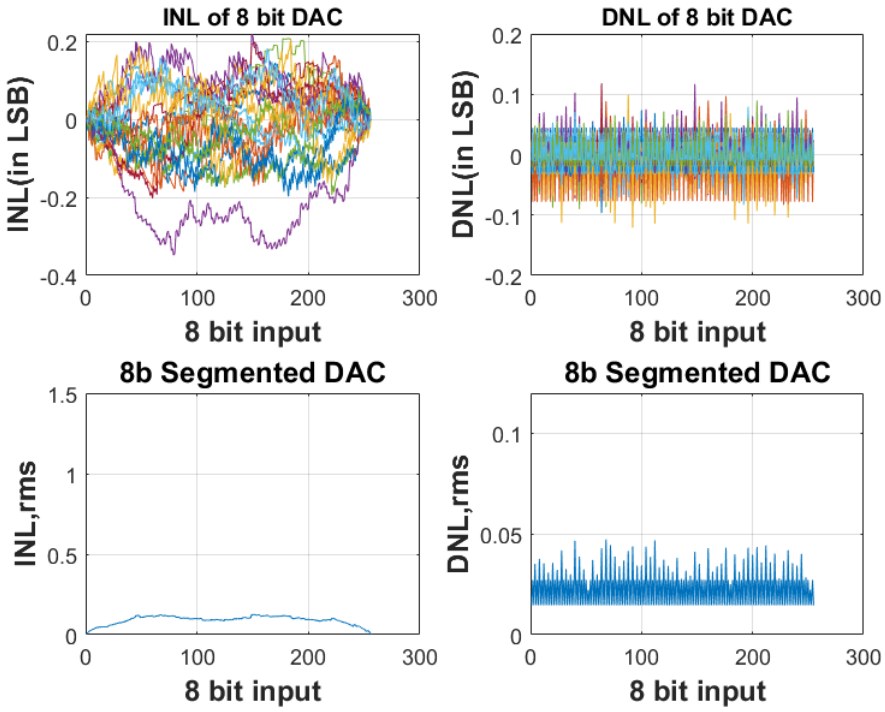


Figure 34: DNL and INL values as calculated in MATLAB

Thereotical calculations of INL and DNL

From 4, we get:

$$\begin{aligned}\sigma_{INL} &= \frac{\sigma_{I_{LSB}}}{2I_{LSB}}\sqrt{2^8} \\ &= 8\sqrt{\frac{1}{WL}\left(\frac{4{A_{V_{TH}}}^2}{{V_{SD,Sat}}^2} + {A_\beta}^2\right)} \\ &= 8\sqrt{\frac{1}{0.630 \times 8.64}\left(\frac{4(4.6)^2}{(250)^2} + (0.04)^2\right)} \\ &= \boxed{0.1864 \text{ LSB}}\end{aligned}$$

$$\begin{aligned}\sigma_{DNL} &= \frac{\sigma_{I_{LSB}}}{I_{LSB}}\sqrt{2^3} \\ &= \sqrt{\frac{8}{WL}\left(\frac{4{A_{V_{TH}}}^2}{{V_{SD,Sat}}^2} + {A_\beta}^2\right)} \\ &= \sqrt{\frac{8}{0.630 \times 8.64}\left(\frac{4(4.6)^2}{(250)^2} + (0.04)^2\right)} \\ &= \boxed{0.6489 \text{ LSB}}\end{aligned}$$

These theoretical values deviate slightly from the calculated values, due to differences in V_{SD} and the estimations of $A_{V_{TH}}$, A_β, and other varying parameters during Monte Carlo simulation.

12 Transient Analysis

12.1 At Low Frequency

The value of m chosen for coherent sampling is 127.

$$f = \frac{m}{n} f_{sample} = \frac{127}{2048} \times 1GHz = 62.0117MHz$$

The harmonics arise due to coupling of the tail nodes to the bias line through the gate-drain capacitance of the current sources, causing distortions during transitions and hence, non-linearities. Since the signal frequency (f) is much lesser than the Nyquist frequency (500 MHz), we see harmonics at frequencies $3f$ (= 186.035 MHz), $5f$ (= 310.058 MHz), $7f$ (= 434.0819 MHz, peaks at $5f$ and $7f$ are almost indistinguishable in the spectrum) etc.

Also, we only see odd harmonics here, since the even harmonics are cancelled out by using a differential output.

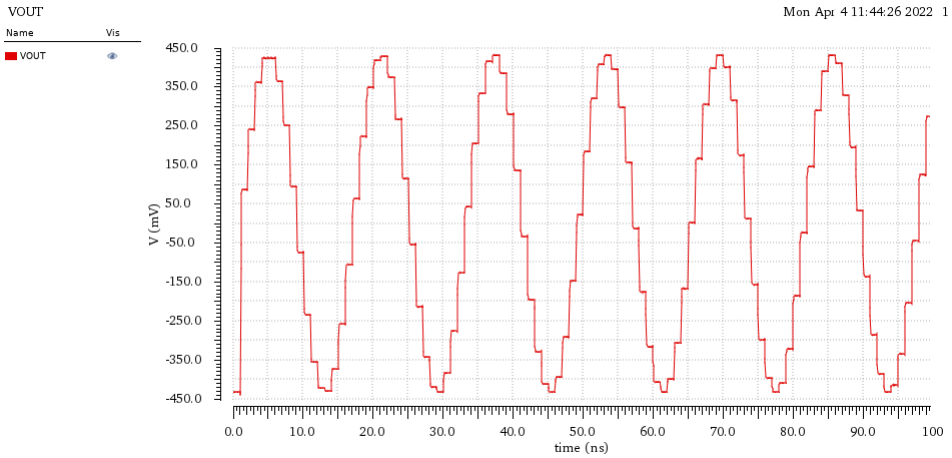


Figure 35: V_{out} at $f = 62.0117MHz$

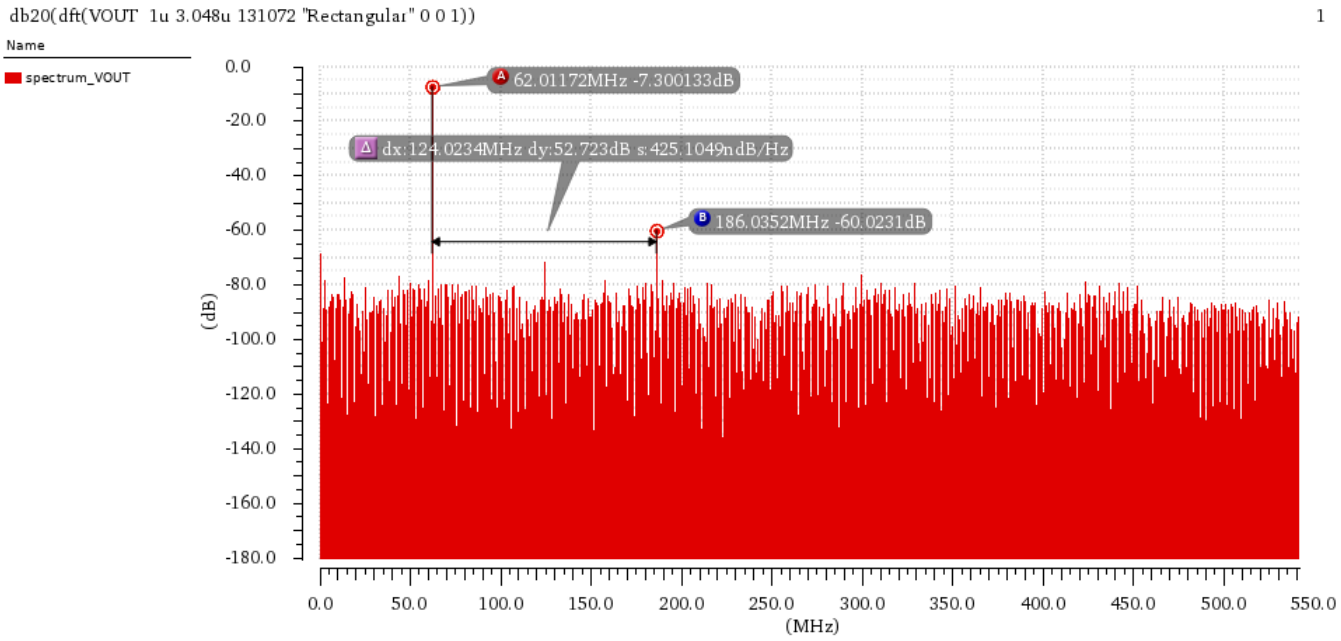


Figure 36: FFT spectrum at $f = 62.0117MHz$ (only two harmonics above noise floor)

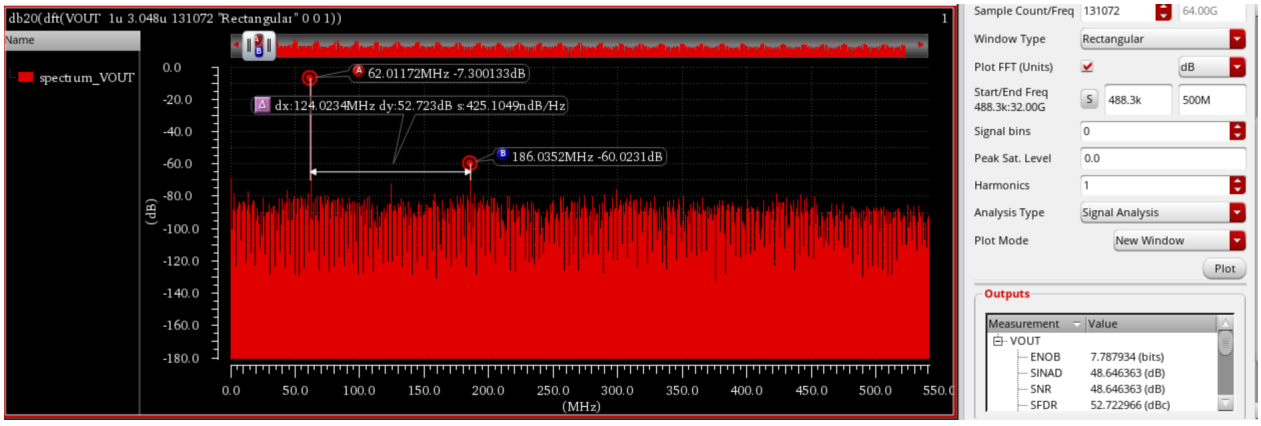


Figure 37: Results at $f = 62.0117MHz$

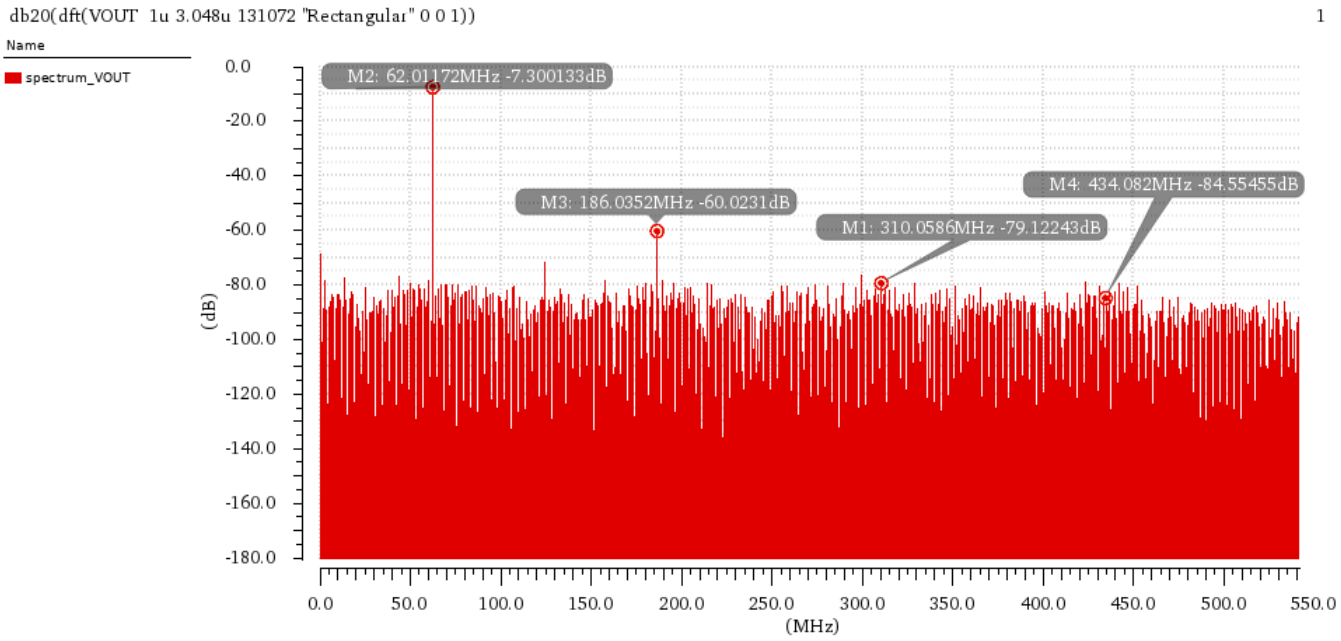


Figure 38: Harmonics at $f = 62.0117MHz$ (the later ones are indistinguishable due to noise)

12.2 At High Frequency

The value of m chosen for coherent sampling is 1009.

$$f = \frac{m}{n} f_{sample} = \frac{1009}{2048} \times 1GHz = 492.6758MHz$$

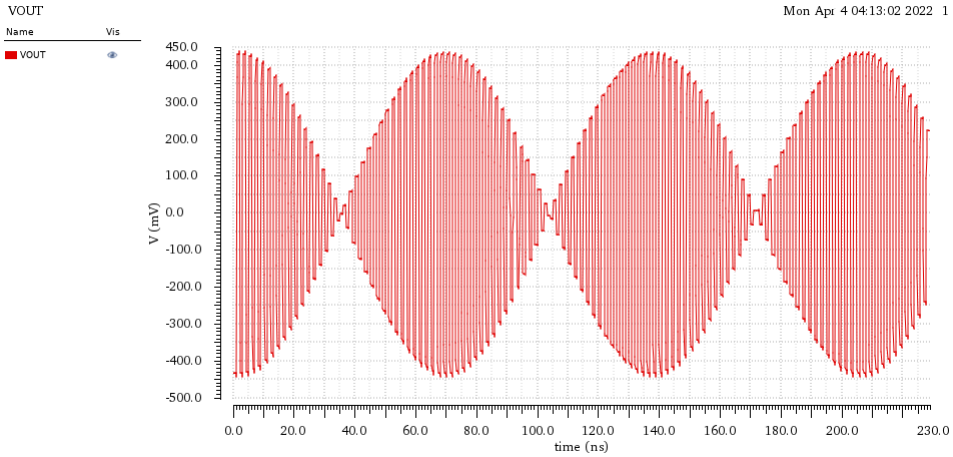


Figure 39: V_{out} at $f = 492.6758MHz$

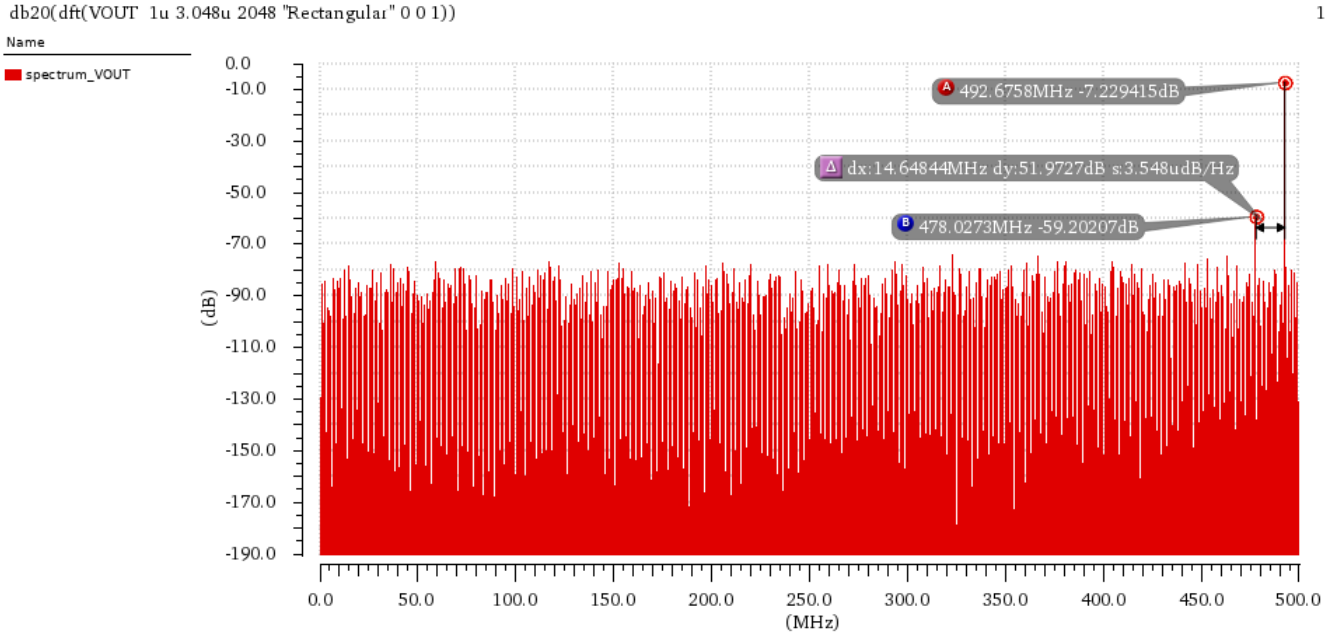


Figure 40: FFT spectrum at $f = 492.6758MHz$ (the two marked peaks are the only harmonics above noise floor)

Since the frequency is already close to Nyquist frequency, the harmonics are folded back into the Nyquist band due to aliasing during sampling. Therefore, we have a peak at $3f - f_s = 3 \times 492.6758 - 1000MHz = 478.027MHz$.

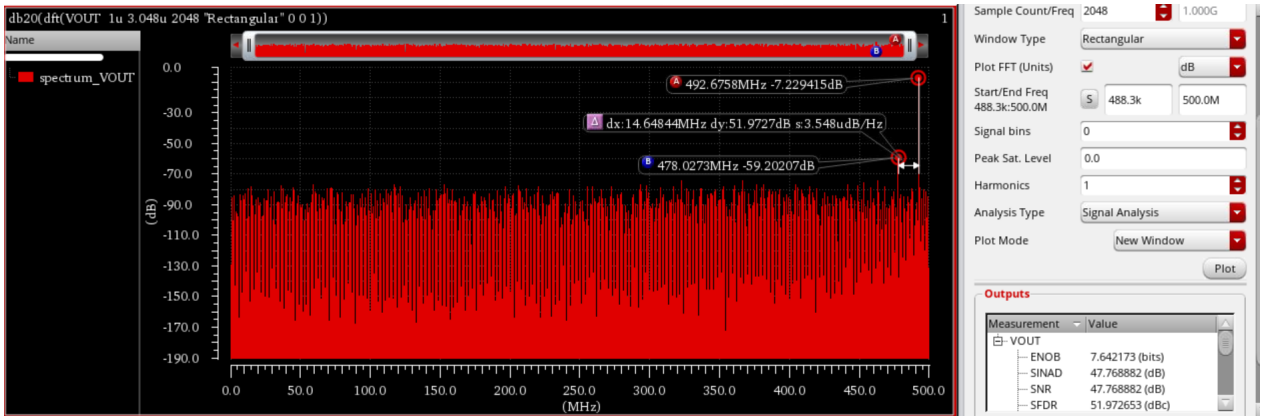


Figure 41: Results at $f = 492.6758MHz$

13 Dynamic Performance Characteristics

	SNDR (in dB)	SFDR (in dB)	ENOB (in bits)
f = 62.0117 MHz	48.646	52.723	7.788
f = 492.6758 MHz	47.769	51.973	7.642

Table 6: Dynamic performance characteristics of DAC

14 Power Consumption

The theoretical power consumed is $P \approx V_{DD} \times 255 I_{LSB} = 1.2 \times 255 \times 60\mu A =$ **18.36mW**

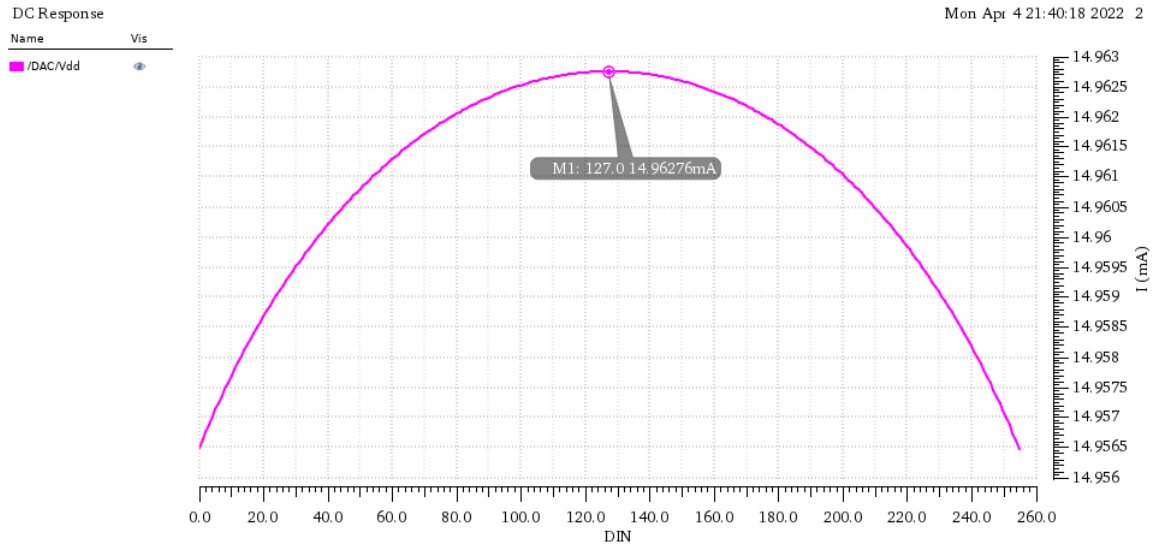


Figure 42: Total current drawn from V_{DD} source

Using the test bench for DC analysis, and plotting the current, we see that the current slightly varies with the digital input. The peak current is for an input of around 127, and the max total power = $1.2V \times 14.9628$ mA = **17.955 mW**

Of this, the analog power is $= 1.2 \cdot (63 \times 234.556 + 117.278 + 58.639)\mu W = 17.943mW$ (the different terms are currents of the 63 $4I_{LSB}$,$2I_{LSB}$ and I_{LSB} units respectively. Therefore, power consumed by digital circuitry is $12\mu W$.

15 Layout

The number of fingers and multipliers had to be changed, to ensure good matching during layout. The new schematic is shown below.

Additional layout images are included at the end of report.
The SFDR after layout is (surprisingly) higher than earlier for both high and low frequencies of input.

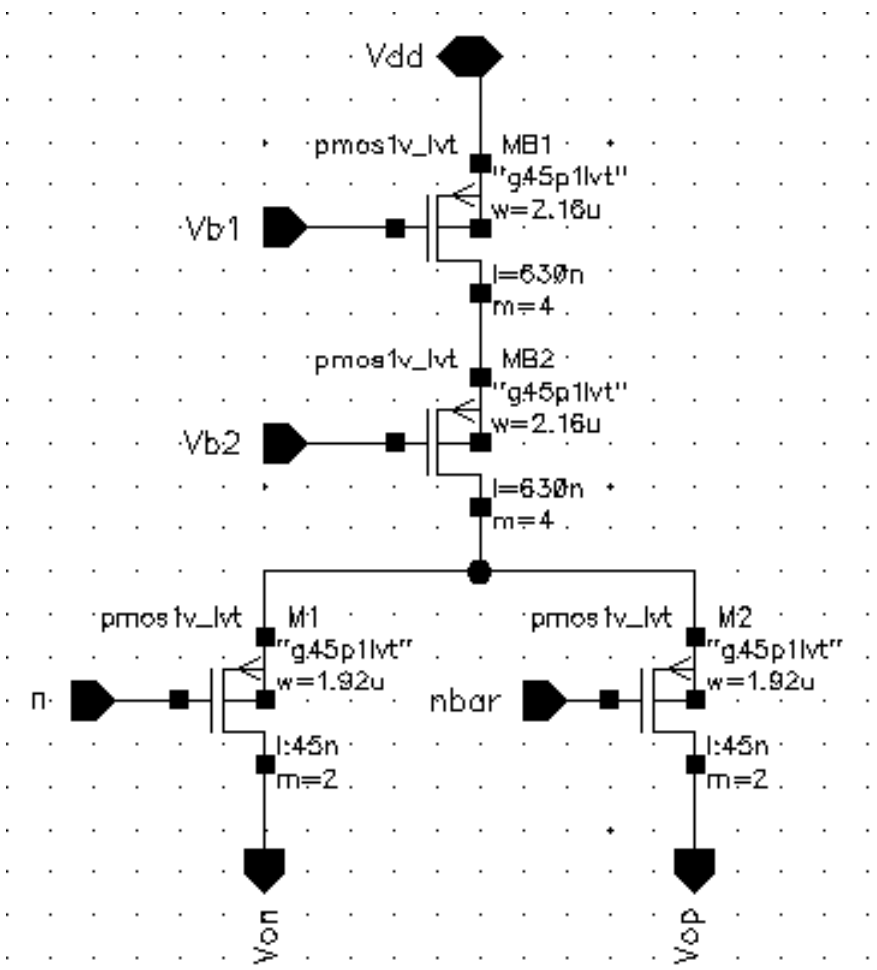


Figure 43: Schematic of analog component of unit cell

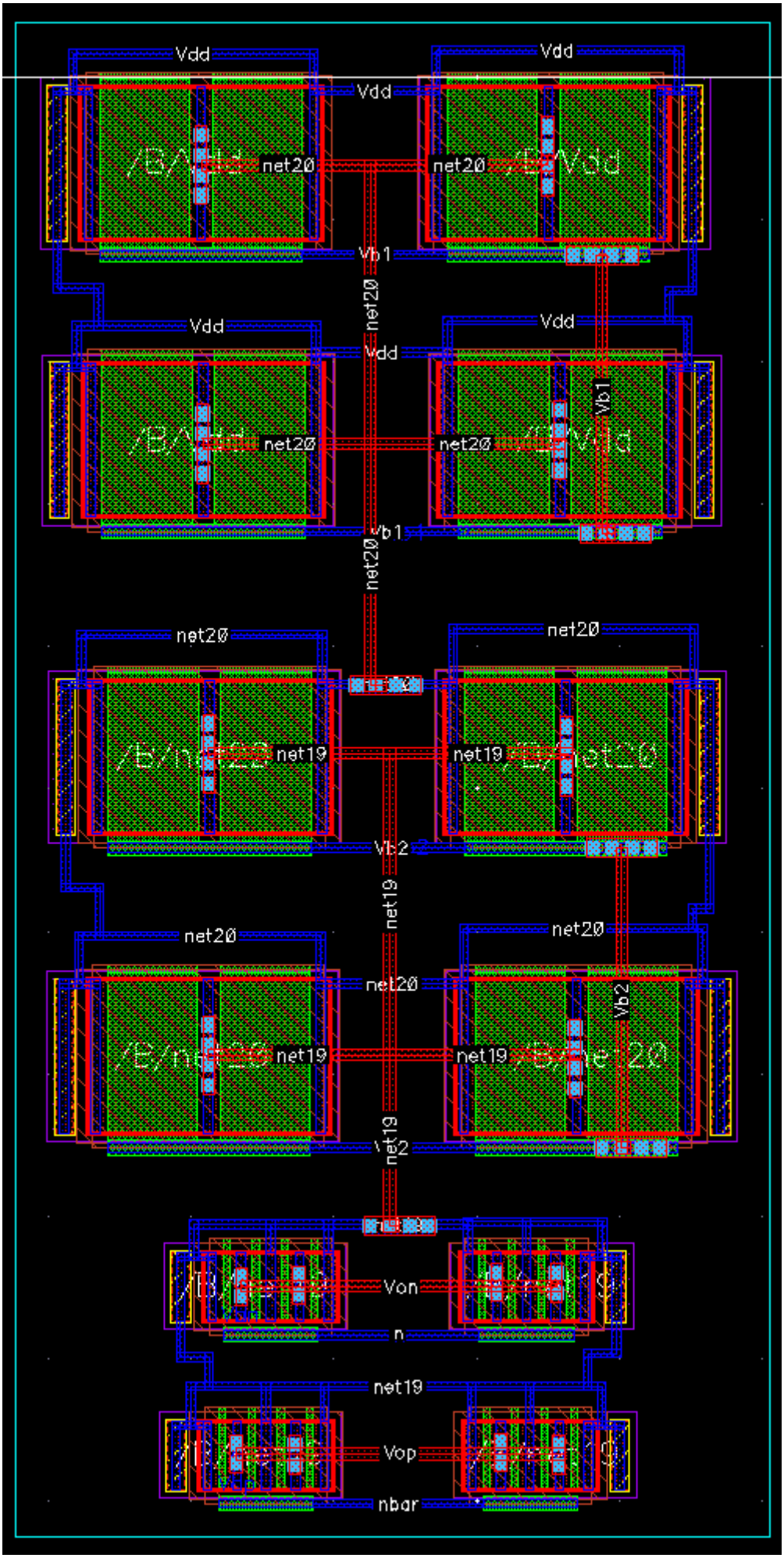


Figure 44: Layout of entire cell

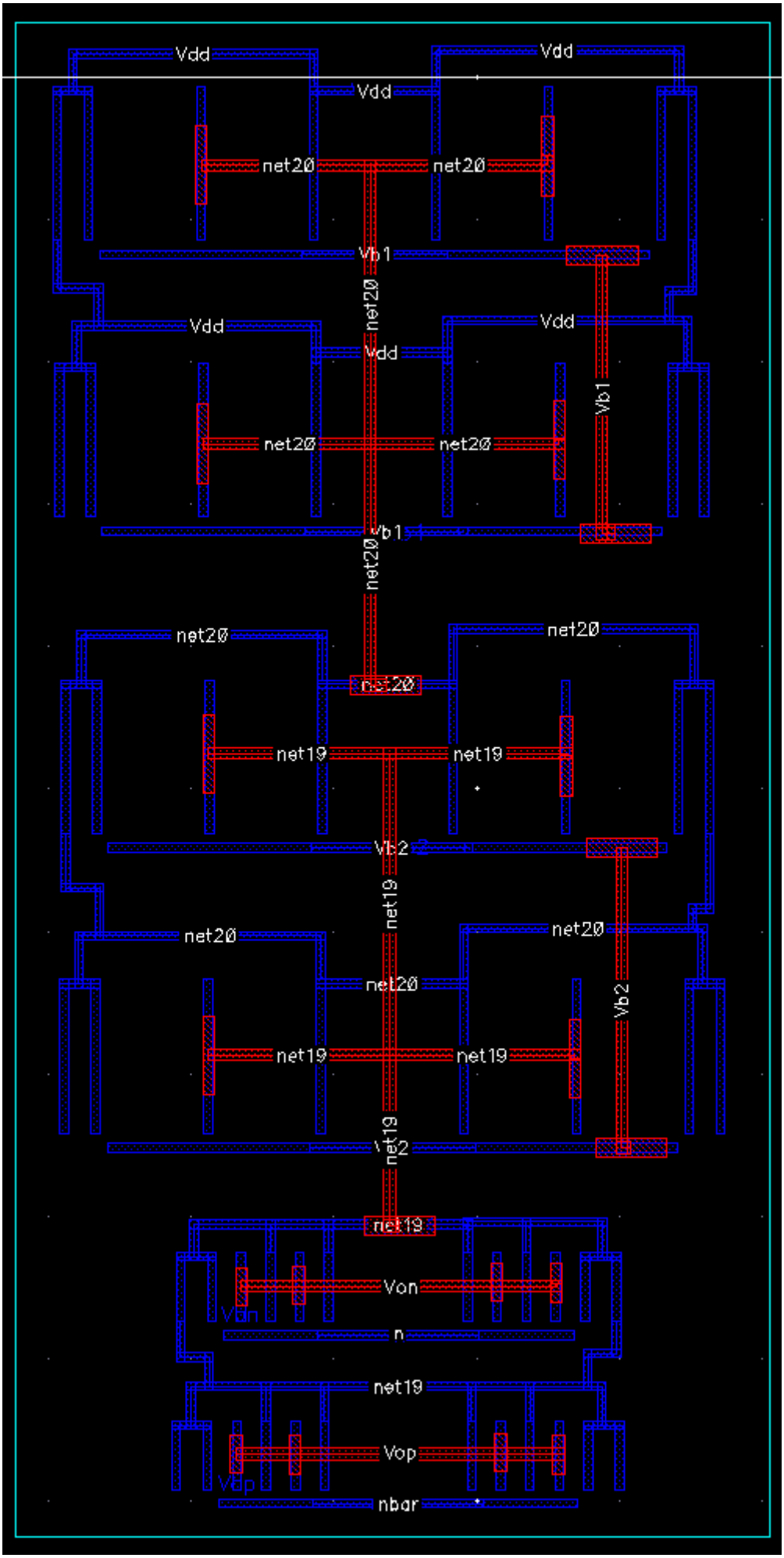


Figure 45: Metal 1 and Metal 2 layers of cell

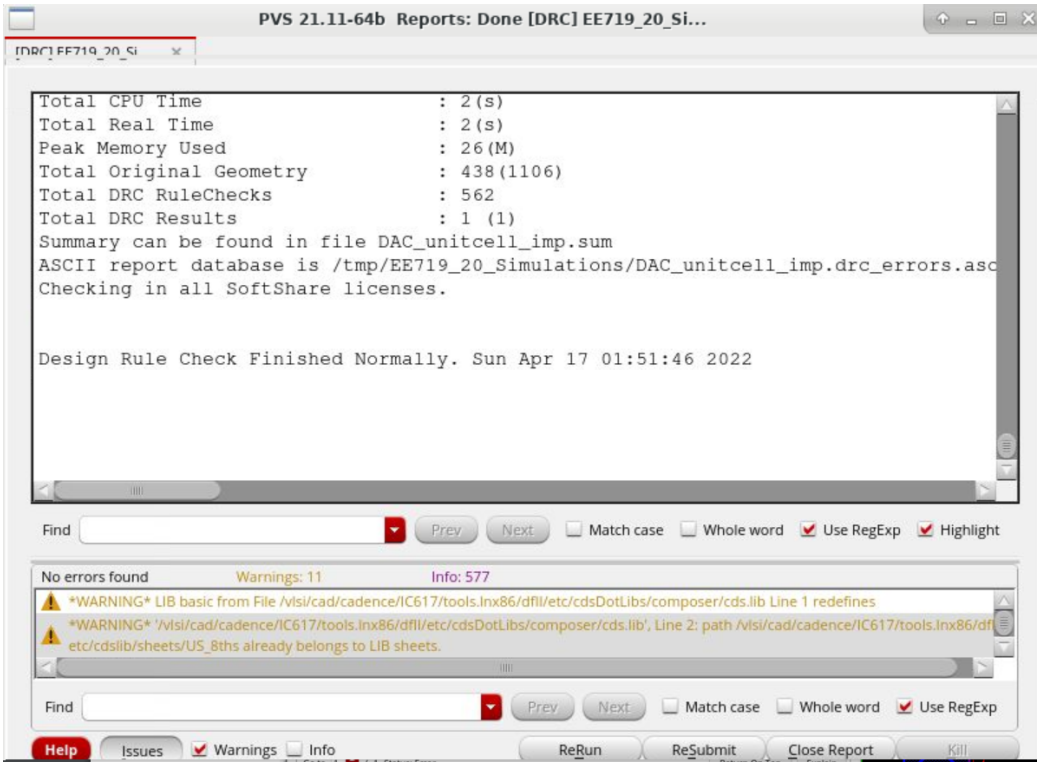


Figure 46: DRC check

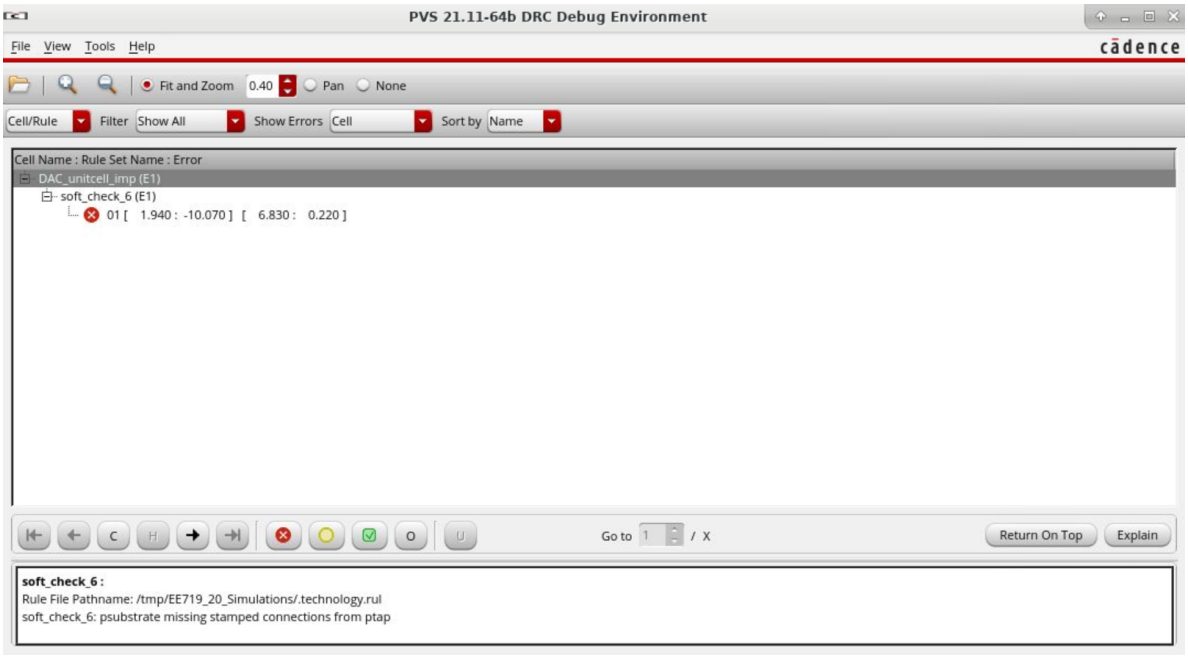


Figure 47: DRC check

Figure 48: LVS check

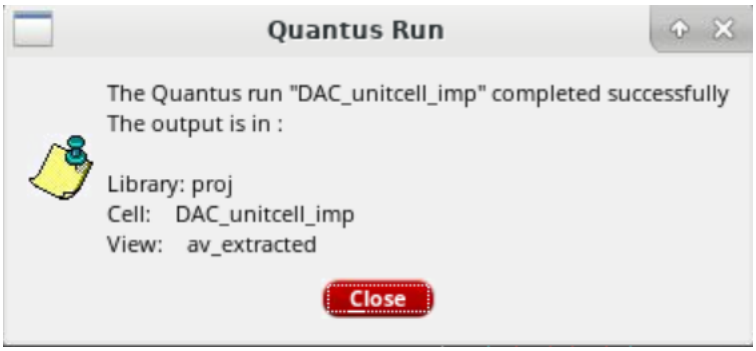


Figure 49: Parasitic extraction

	SNDR (in dB)	SFDR (in dB)	ENOB (in bits)
f = 62.0117 MHz	49.248	54.212	7.888
f = 492.6758 MHz	48.125	53.150	7.701

Table 7: Dynamic performance characteristics of DAC after post-layout extraction

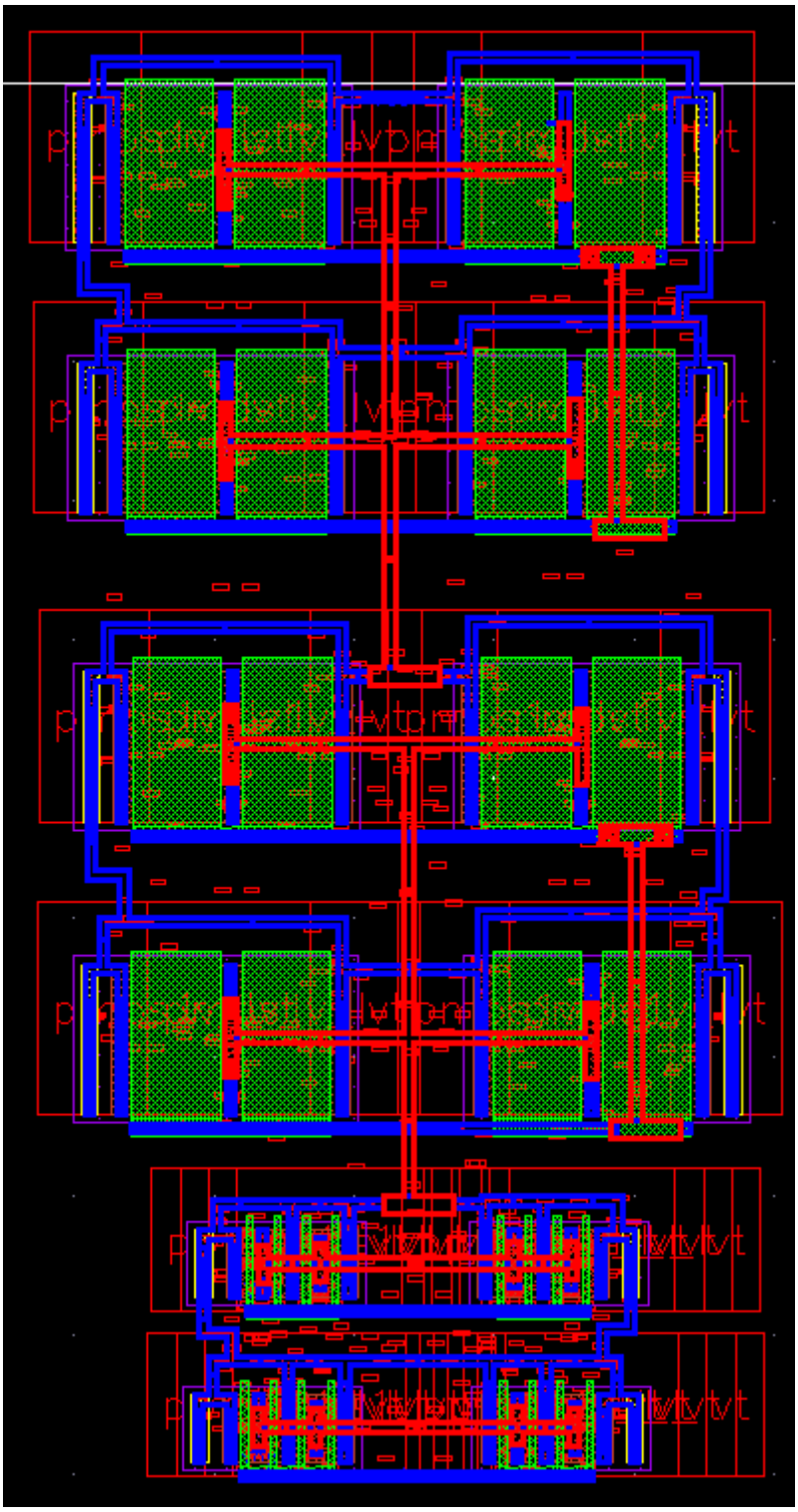


Figure 50: av extracted figure (RC)

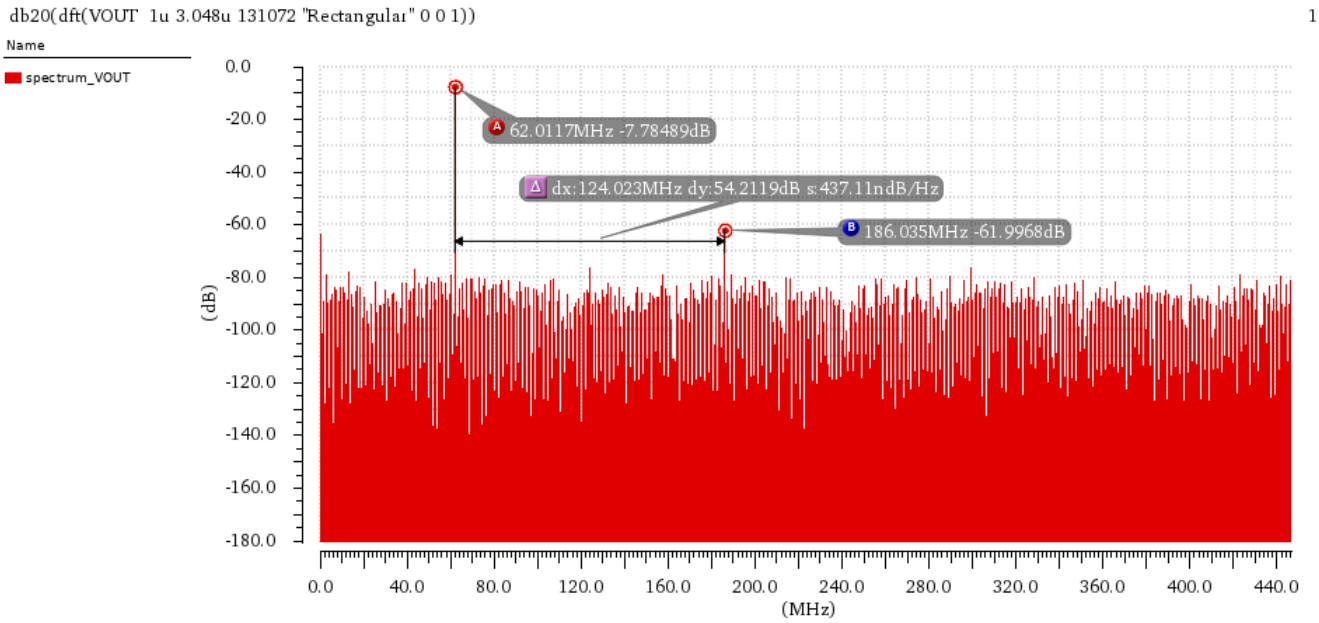


Figure 51: FFT spectrum at $f = 62.0117MHz$ after post-layout extraction

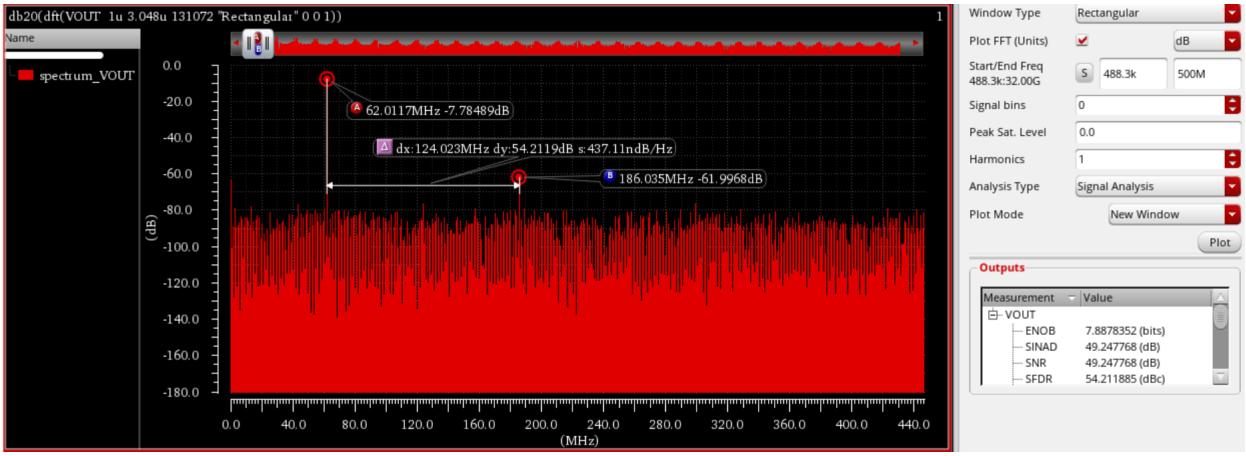


Figure 52: Results at $f = 62.0117MHz$

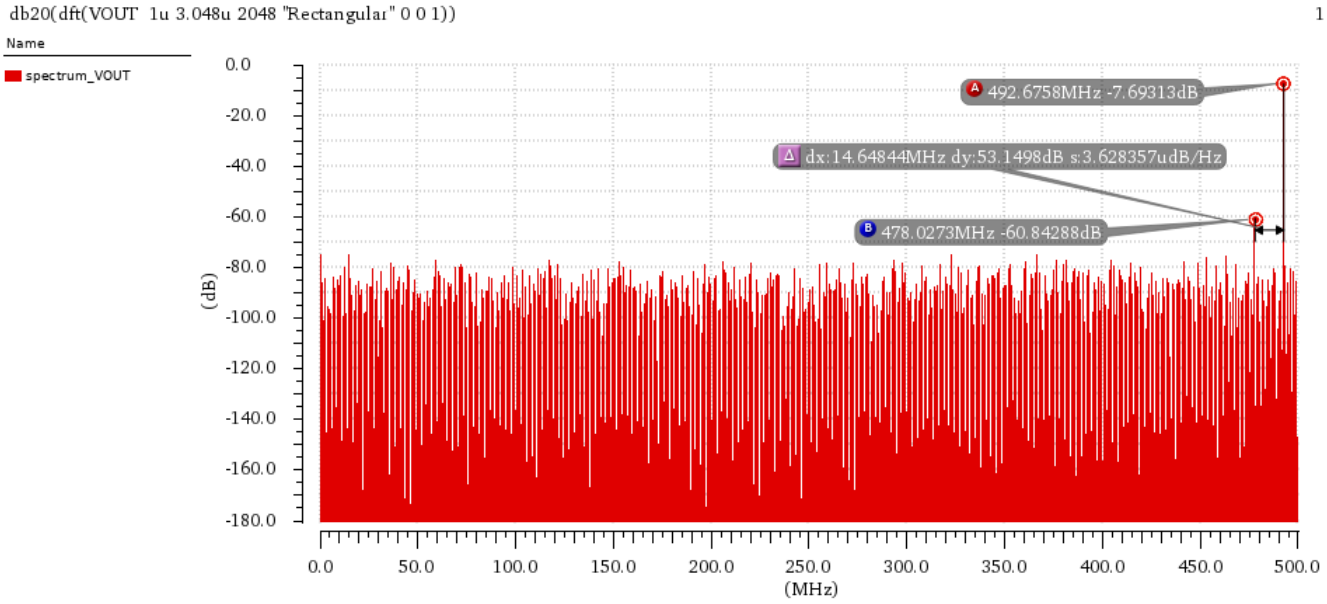


Figure 53: FFT spectrum at $f = 492.6758MHz$ after post-layout extraction

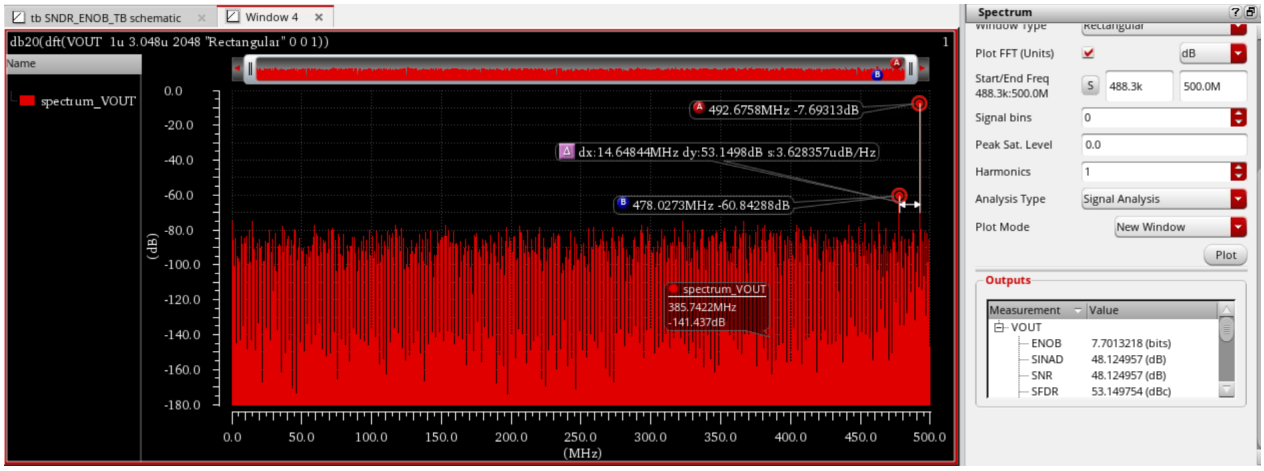


Figure 54: Results at $f = 492.6758MHz$

16 Additional Layout Images

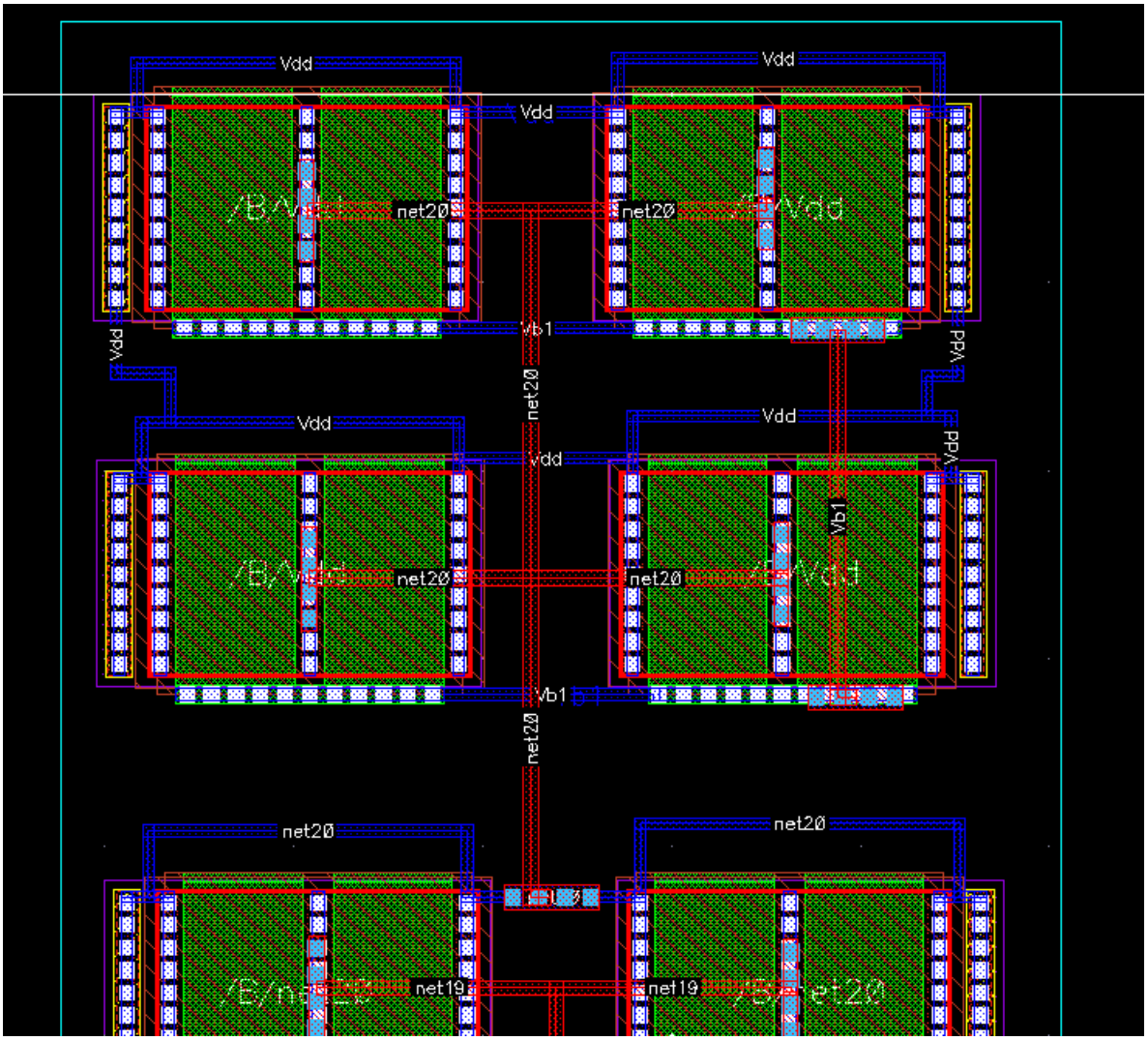


Figure 55: All layers of MOSFET MB1

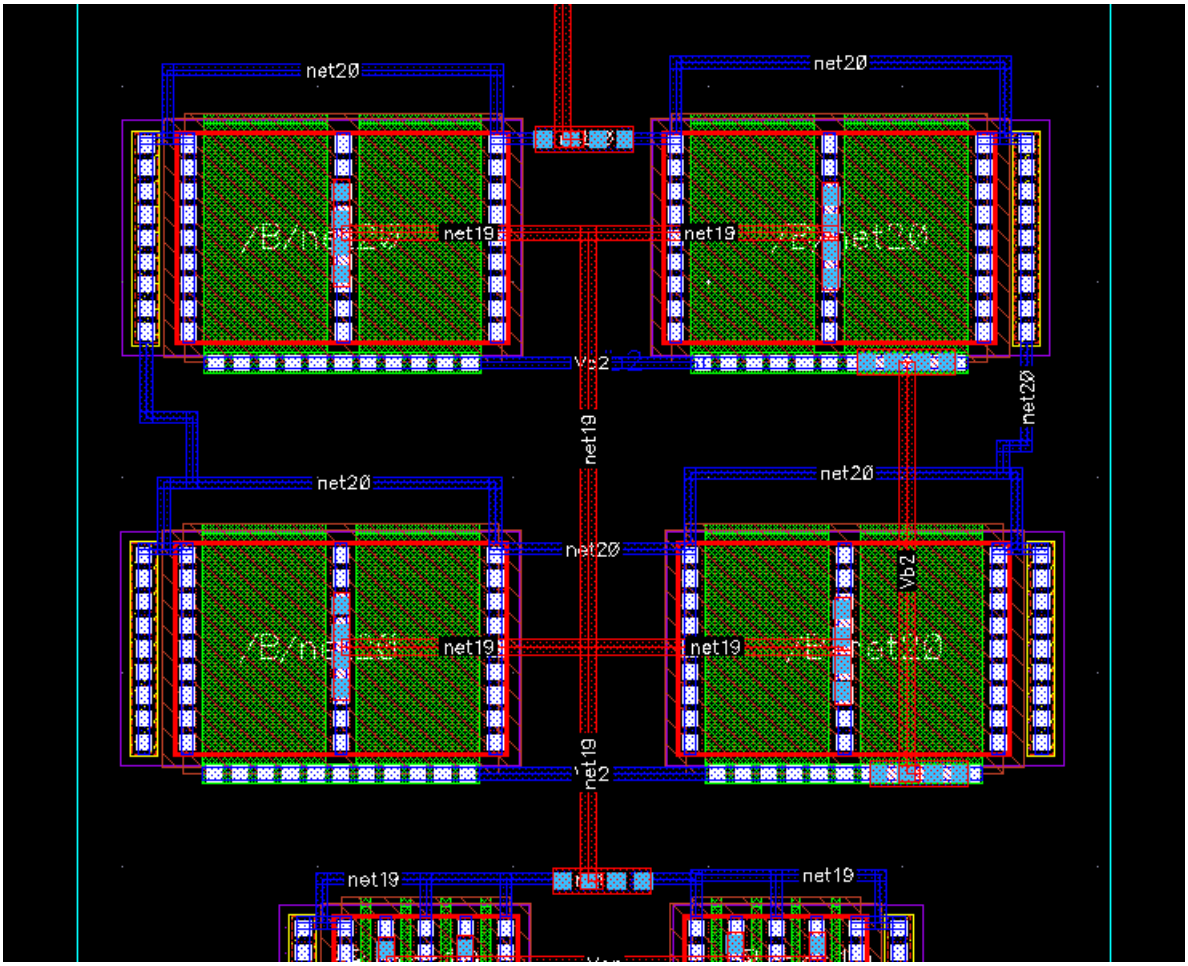


Figure 56: All layers of MOSFET MB2

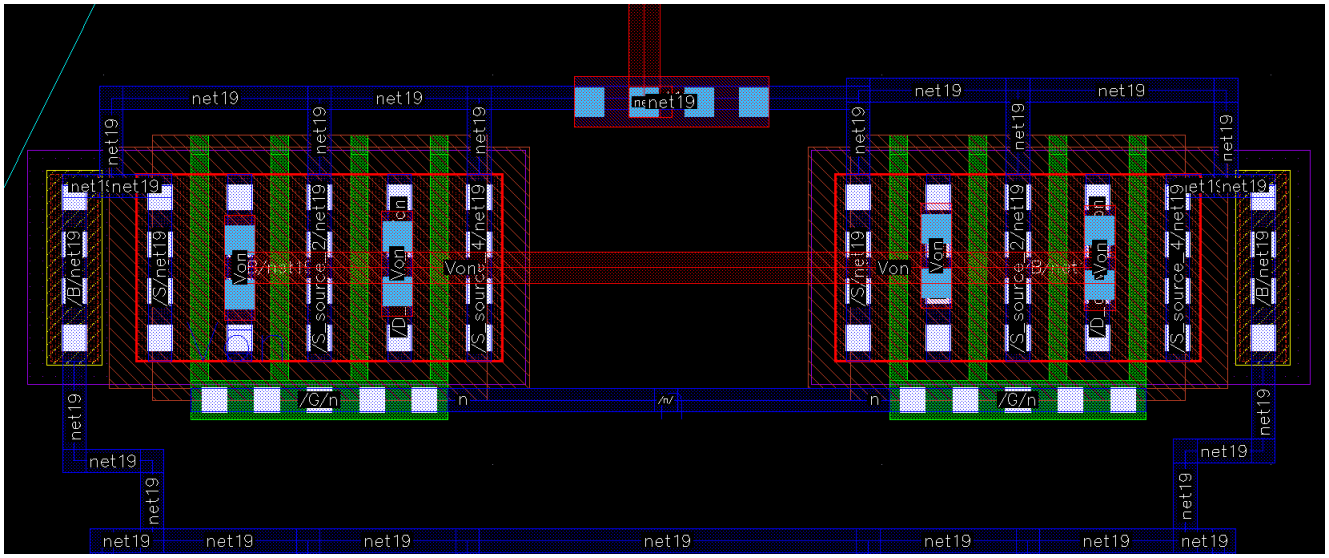


Figure 57: All layers of MOSFET M1

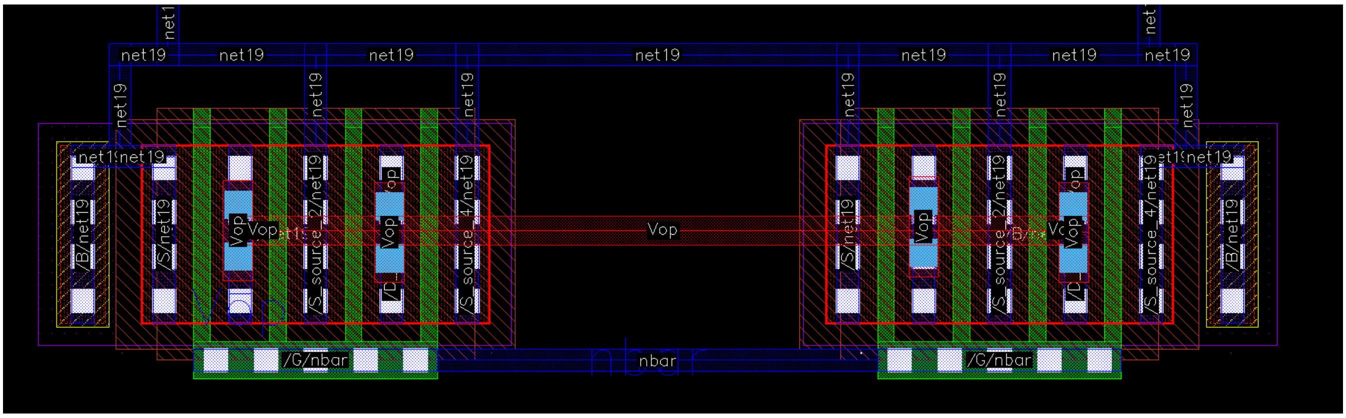


Figure 58: All layers of MOSFET M2