A 10-bit Segmented CMOS DAC

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***Abstract*—A 10-bit segmented current-steering digital-to-analog converter (DAC) with optimal performance for high-frequency applications is detailed. The advantages and disadvantages of a fully binary and fully thermometer-coded DAC are illustrated, along with the need for segmentation to maintain the requisite spectral purity for high-frequency applications. The requirements to be met are INL_{max} = 1 LSB and DNL_{max} = 0.5 LSB, while also optimizing chip area and digital circuitry complexity.**

***Index Terms*—Digital-to-analog converter (DAC), mixed signal integrated circuits, segmentation**

I. Introduction

The world is analog, whereas all the data processing is digital, necessitating interfaces to seamlessly translate the information between the two domains. These interfaces have diverse applications in many systems, ranging from communication systems to audio and television applications. One such converter, a digital-to-analog converter (DAC), is discussed, especially its current steering topology, which is the superior choice for high-frequency applications and driving resistive loads without buffers.

There is an increasing demand to improve the linearity of a DAC while also minimizing the area and maximizing the speed of operation. The accuracy of a DAC is expressed in terms of its integral non-linearity (INL) and differential non-linearity (DNL) errors. Each digital input's INL error is defined as the difference between the actual and ideal analog output values. In an ideal DAC, the adjacent outputs are exactly one least significant bit (LSB) apart, and the value of the deviation from 1 LSB in an actual DAC is termed the DNL error. We want the converter to be monotonic, i.e., the output should always increase as the input increases. Glitches, which occur due to differential delays during switching of current sources, also degrade the performance of a DAC by contributing to non-linearity.

II. Binary-Weighted DAC

We have a 10-bit digital input, which we wish to convert to an analog output. Fig. 1. shows a high-level circuit of a binary-weighted DAC, where each digital bit controls a switch carrying a current of a different binary weight. If the unit cell carries current I_u, and if the bits are labeled b_0 to b_9, with b_0 representing the LSB, the output is

$$I_{out} = b_9(2^9 I_u) + b_8(2^8 I_u) + \ldots + b_0(I_u) \qquad (1)$$

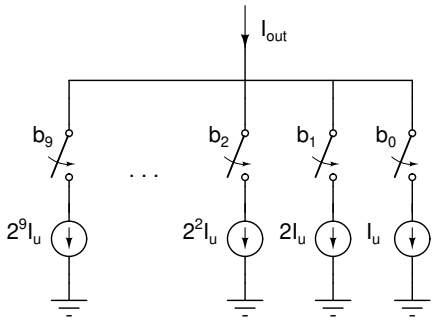

Fig. 1. Binary-weighted DAC

Since the digital bits directly control the switches, there is no need for any decoding logic, and the implementation of such a DAC is simple. In reality, all the current sources are not perfectly matched, and hence this particular topology is not inherently monotonic. The glitch magnitude is highest at the mid-code transition (01 1111 1111 $\rightarrow$ 10 0000 0000) when all the switches toggle at the same time. Let ΔI_u be the tolerance of each current source, representing a random variable with a different value for each current source. The current before the transition is $(2^{N-1} - 1)(I_u + \Delta I_u)$, and after would be $2^N(I_u + \Delta I_u)$. Due to the mismatches, we can see that the difference in currents deviates from the ideal value of I_u (assuming perfect matching), and in the worst case, the output might even be non-monotonic.

III. Thermometer-Coded DAC

The glitches arising due to simultaneous switching of current sources are undesirable as they contain non-linear components of the signal and result in spurious frequencies, reducing the SFDR of the system. Larger glitches also mean a larger DNL, making it harder to meet the specifications. This problem is mitigated by using thermometer coding, where $(2^{10} - 1)$ unit current sources are used in place of binary-weighted current sources such that only one new current source is switched on when the digital input is incremented by 1 LSB. For a binary code of 01 1111 1111, 511 unit current sources are activated, and for 10 0000 0000, 512 unit current sources are active (511 unit cells of the previous input are still active, and just one new unit cell is switched on). Therefore, this architecture is monotonic by design.

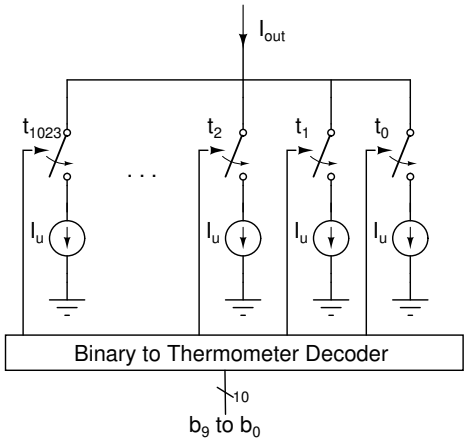

Fig. 2. Thermometer-coded DAC

In binary-weighted DACs, there is no definite relation between the glitch amplitude and the magnitude of input since the switching of a group of unit cells can take place even by one LSB increase in input, like the mid-code glitch. However, in thermometer-coded DACs, the glitch is directly proportional to the change in digital code since exactly those many unit cells switch. Thus, the DNL error of a thermometer-coded DAC is much lower than that of a binary-weighted DAC.

The main drawback of this architecture is that a decoding circuit for every current source and a digital binary-to-thermometer decoder are needed, which makes it significantly more complex compared to a binary-weighted DAC.

IV. Partial Segmentation

A hybrid topology with thermometer coding for the MSBs (since high accuracy is needed) and binary-weighted coding for the LSBs (to cut down on the digital complexity from a fully thermometer coded DAC) is used to take advantage of the features of both topologies. For simplicity, a fully binary-weighted DAC is regarded as 0% segmented and a thermometer-coded DAC as 100% segmented. We wish to find the optimal chip area while meeting the DNL and INL specifications.

The expression for INL of a DAC (regardless of % segmentation), for a random change of σ in the current I_u, is given by [2]

$$\text{INL}_{\text{max}} = \frac{\sigma}{2I_u}\sqrt{2^N} \tag{2}$$

The real advantage of segmentation (for B_b binary bits and $B_t = N - B_b$ thermometer bits) is seen in the expression of DNL, which is approximately

$$\text{DNL}_{\text{max}} = \frac{\sigma}{2I_u}\sqrt{2^{B_b+1}} \tag{3}$$

This expression is obtained by considering that in the worst case, only the binary-weighted unit cells and exactly one thermometer unit cell can switch at a time. As the number of binary bits decreases, the DNL drops exponentially.

TABLE I
Trade-Offs With Variation in % Segmentation

Architecture	INL	DNL	Number of digital decoding units
Fully Binary	16σ	32σ	0
Segmented ($B_t = 2$)	16σ	22.63σ	3
Segmented ($B_t = 5$)	16σ	8σ	31
Segmented ($B_t = 8$)	16σ	2.83σ	255
Fully Thermometer	16σ	σ	1023

V. Area Requirement

The target specifications for the 10-bit DAC are INL_{max} = 1 LSB and DNL_{max} = 0.5 LSB.

Let σ = 0.5 LSB represent the maximum DNL. The dependence of area on σ is given by [3]

$$\text{Area} \propto \frac{1}{\sigma^2} \tag{4}$$

If A_{unit} represents the minimum analog area of a thermometer-coded architecture to have a DNL of σ, then a binary-weighted DAC that has the same DNL would require an analog area of $1024\text{A}_{\text{unit}}$. Since the INL is the same regardless of the architecture, a DNL of σ leads to an INL of 16σ. The area would have to be increased 64 times for each architecture to reduce its INL to 2σ (= 1 LSB). These results are summarized in Table II.

TABLE II
Area and Static Error Conditions for Binary-Weighted and Thermometer-Coded DAC

Specification	Binary-Weighted	Thermometer-Coded
DNL	32σ	σ
INL	16σ	16σ
Area for DNL = 0.5 LSB	$1024A_{\text{unit}}$	A_{unit}
Area for INL = 1 LSB	$64A_{\text{unit}}$	$64A_{\text{unit}}$

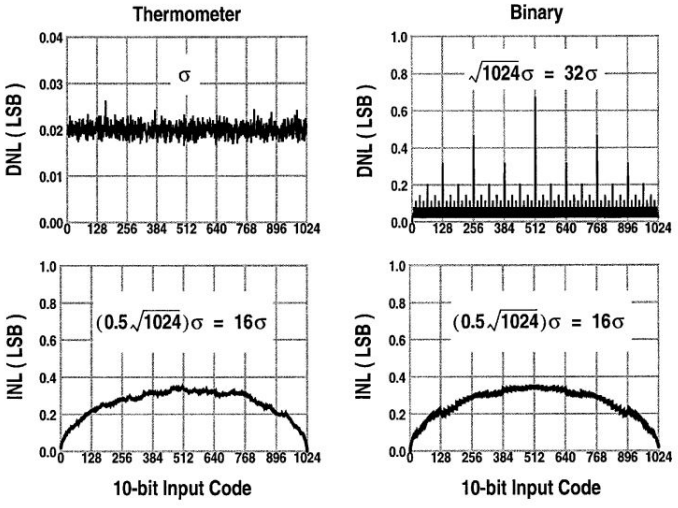

Fig. 3. RMS of 100 MATLAB simulations for thermometer-coded versus binary-weighted DAC. The INL performance of both DACs is similar, but the DNL error of binary-weighted is much higher, reaching the peak during the mid-code transition. Source: Reproduced from [1]

Fig. 4. shows the normalized area (in logarithmic scale) versus the percentage segmentation. As expected, the analog area (denoted by A_{total}) reduces as the segmentation increases. However, the area required for the digital circuitry (represented by $A_{digital}$) of thermometer cells should also be considered, which increases linearly in the logarithmic scale with segmentation. Since the area to meet the INL target is the same regardless of the degree of segmentation, it is represented as a horizontal line.

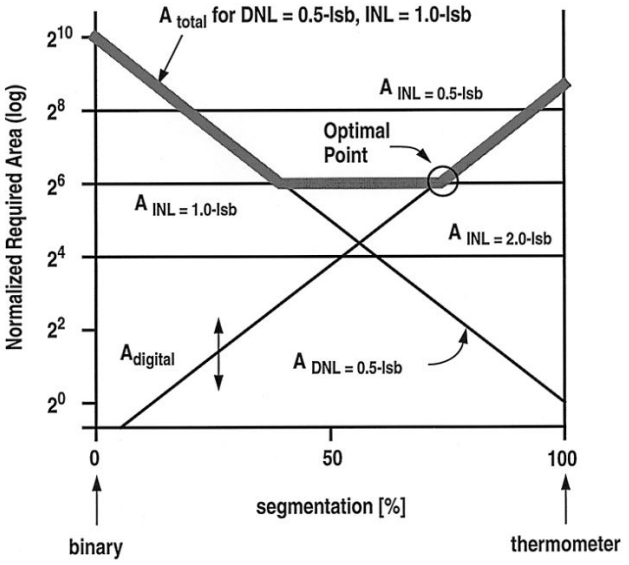

Fig. 4. Normalized chip area versus percentage segmentation. Source: Reproduced from [1]

All points on the highlighted portion of the horizontal line would meet the maximum INL and DNL targets in the same area. However, using the maximal segmentation possible would result in the least DNL error and give the best total harmonic distortion performance, and hence is considered the optimal point.

The optimal point corresponds to 8 thermometer bits and 2 binary bits for the specifications considered, which is implemented as shown in Fig. 5. The exact unit cell along with digital decoding and the block diagram of all the connections are shown in Fig. 6. and Fig. 7. respectively.

VI. Conclusion

Thermometer-coded DACs have fewer spurious frequency components compared to binary-weighted DACs owing to smaller glitches. The digital complexity can be reduced by choosing an optimal percentage of segmentation while meeting the INL and DNL specifications and maintaining the minimum possible area. For the 10-bit designed reviewed, the optimal split was 8 bits for the thermometer-coded MSB segment and 2 bits for the binary-weighted LSB segment. Using this segmentation split, instead of a fully thermometer-coded design reduces the digital decoding complexity approximately by an order of 4, as outlined in Table I.

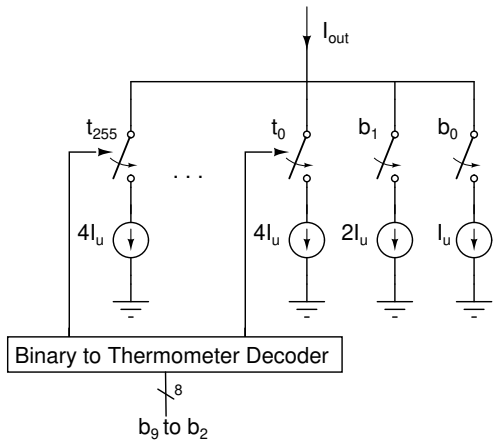

Fig. 5. Segmented DAC implementation. The 2 LSB current sources form the binary-weighted segment, and the 8 MSBs of the binary input are decoded and fed to the thermometer-coded segment.

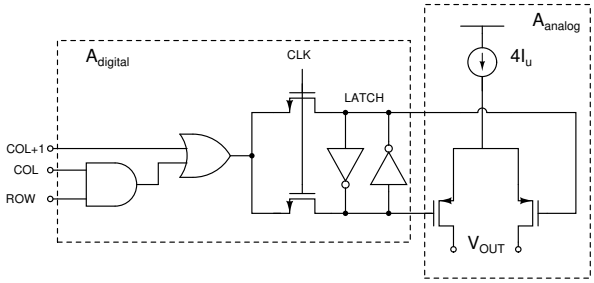

Fig. 6. Breakdown of analog and digital components of each unit cell, along with decoding.

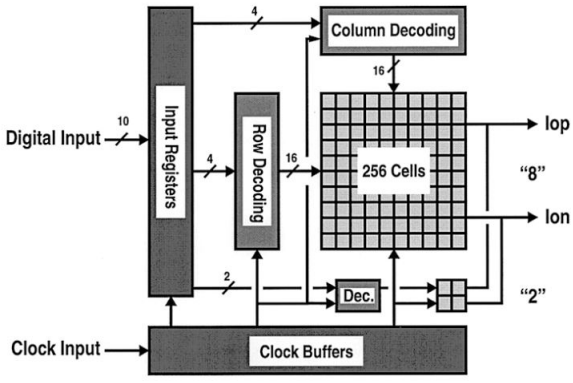

Fig. 7. Block diagram of decoding for segmentation. Row and column binary-to-thermometer decoders are additionally needed, and each of the 256 grey cells represents a unit cell shown in Fig. 6. Source: Reproduced from [1]

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