IIT BOMBAY

EE618
COURSE PROJECT

OPERATIONAL AMPLIFIER DESIGN

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Team 7

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Contents

1 Pseudo class AB design

We start by using the model parameters of 130 nm CMOS process for hand-analysis:

Parameter	NMOS	PMOS
Low field mobility (μ)	140 cm^2/Vs	60 cm^2/Vs
Channel-length modulation parameter (λ)	0.1 V^{-1}	0.2 V^{-1}
Gate-oxide thickness (t_{ox})	3.3 nm	3.3 nm
Threshold voltage ($\|V_{th}\|$)	0.3782V	0.321V

Table 1: Approximate Model Parameters

We calculate the following constants for ease:

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.9 \times 8.85 \times 10^{-12}}{3.3 \times 10^{-9}} = 10.46 \times 10^{-3} F/A^2$$
$$k_n = \mu_n \cdot C_{ox} = 140 \times 10^{-4} \times 10.46 \times 10^{-3} = 1.464 \times 10^{-4} A/V^2$$
$$k_p = \mu_p \cdot C_{ox} = 60 \times 10^{-4} \times 10.46 \times 10^{-3} = 6.275 \times 10^{-5} A/V^2$$

PTM 130nm CMOS technology model with $V_DD = 1.5V$ and $V_SS = 0V$ has been used. Bulk of NMOS transistors have been connected to V_{SS} and bulk of PMOS transistors have been connected to its source.

1.1 Iteration 1

Our aim is to meet the specifications given below:

- Slew Rate $> 400V/\mu s$
- DC gain $> 70dB$
- Phase Margin $> 60°$
- Unity gain frequency $F_{UGF} > 1GHz$

1.1.1 Slew Rate

Let I_{B1} be the current through MSS3. As a first order guess, we take $C_Z = 0.5pF$, which is in the same order as C_L. We have:

$$SR = \frac{I_{B1}}{C_Z} > 4 \times 10^8$$
$$\implies I_{B1} > 0.2mA$$

For a safe slew rate margin, we take $I_{B1} \approx 0.4mA$.

We know that

$$I_{10} = I_{B1}\left(1 + \frac{C_L}{C_Z}\right) = 2I_{B1} = 0.8mA$$

1.1.2 Unity Gain Frequency

As the name suggests, at $f = F_{UGF}$ (or $\omega = \omega_u$), the loop gain is 1. Assuming a contribution from the dominant pole only, we can write:

$$|H(j\omega_u)| = \left| \frac{H^0}{\frac{j\omega_u}{\omega_1}} \right| = 1$$
$$\implies \omega_u = |H^0| \cdot \omega_1$$

Substituting for the low frequency gain and the dominant pole ω_1, we get:

$$\omega_u = (g_{m1} \cdot R_{Out1} \cdot |A_{v2}|) \cdot (\frac{1}{C_Z R_{Out1} |A_{v2}|})$$
$$\implies \omega_u = \frac{g_{m1}}{C_Z}$$
$$F_{UGF} = \frac{g_{m1}}{2\pi C_Z}$$

Therefore, $g_{m1} \geq 3.14 \times 10^{-3}$

Using this value of g_{m1}, and taking $I_1 = I_{B1}/2$,

$$g_{m1} = \sqrt{2 \cdot I_1 \cdot k_n \cdot \left(\frac{W}{L}\right)_1} \geq 3.14 \times 10^{-3} \text{℧}$$
$$\implies \left(\frac{W}{L}\right)_1 \geq 169$$

We take $\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 \approx 200$, which would mean $g_{m1} = g_{m2}$

1.1.3 Phase Margin

We need PM $\geq 60°$. We calculate the first non-dominant pole to be

$$p_2 = \frac{g_{m10}}{2\pi C_L}$$

Assuming $F_{UGF} >> p_1$ ($p_1 = \frac{\omega_1}{2\pi}$) and considering only poles, we compute the phase margin at F_{UGF} to be

$$PM = 180 + (-90° - tan^{-1}(\frac{F_{UGF}}{p_2})) > 60$$
$$\implies p_2 > 1.73 F_{UGF}$$
$$g_{m10} \geq 5.92 \times 10^{-3}$$

Since we expect the gain margin to be better than this value due to zero by R_Z, we take $\boxed{g_{m10} = 5.92 \times 10^{-3}}$

To improve the phase margin, we choose the value of R_Z such that the left half plane zero cancels the first non-dominant pole to yield a phase margin of about 90° (excluding the effect of the other non-dominant poles).

The location of zero due to R_Z is at

$$s = \frac{g_{m10}}{C_Z(1 - g_{m10}R_Z)}$$

We want to cancel out the first non dominant pole, which lies in the left half plane with this zero. Therefore,

$$\frac{g_{m10}}{C_Z(1 - g_{m10}R_Z)} = -\frac{g_{m10}}{C_L}$$

Which yields:

$$R_Z = \frac{1}{g_{m10}}\left(1 + \frac{C_L}{C_Z}\right)$$

Substituting the values, we get $\boxed{R_Z \approx 338\Omega}$.

1.1.4 Gain

We need a gain of 70 dB, or 3162 V/V. The expression for low frequency gain A_v of the circuit is

$$A_V = A_{v1} \cdot A_{v2}$$

Where A_{v1} and A_{v2} are as follows:

$$A_{v1} = g_{m1} \cdot (g_{m4}r_{o4}r_{o2}||g_{m6}r_{o6}r_{o8}||R_2) \tag{1}$$
$$A_{v2} = g_{m10} \cdot (r_{10}||r_{12}) \tag{2}$$

We take $R_1 = R_2 = 10M\Omega$ to avoid it interfering in the gain expression.

The values of various g_m and r_o are calculated below. We have $I = 0.2mA$ for transistors M1-8 and $I_{10} = 0.8mA$

$$r_{o2} = r_{o4} = \frac{1}{\lambda_n I} = 50000$$
$$r_{o6} = r_{o8} = \frac{1}{\lambda_p I} = 25000$$
$$r_{o12} = \frac{1}{\lambda_n I_{10}} = 12500$$
$$r_{o10} = \frac{1}{\lambda_p I_{10}} = 6250$$
$$A_{v2} = 5.92 \times 10^{-3} \times (12500||6250) = 24.67$$

We would need $A_{v1} = 128.18$. Let's assume $g_{m6} = g_{m4}$. We have:

$$g_{m1} = \sqrt{2 \cdot I \cdot k_n \cdot \left(\frac{W}{L}\right)_1} = 3.42 \times 10^{-3} \mho$$
$$g_{m4} = \sqrt{2 \cdot I \cdot k_n \cdot \left(\frac{W}{L}\right)_4}$$

Therefore,

$$\begin{aligned} A_{v1} &= g_{m1} g_{m4} \cdot (r_{o4} r_{o2} || r_{o6} r_{o8}) \\ &= 3.43 \times 10^{-3} \times g_{m4} \times (50000^2 || 25000^2) \approx 128 \end{aligned}$$

We get $g_{m4} = 7.46 \times 10^{-5} \mho$ to get the minimum required gain. Choosing a value much higher than this for a good gain margin, we get $g_{m4} = g_{m6} = 2 \times 10^{-3}$.

Using the g_m values for W/L ratios, we end up with $\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = 68$, and $\left(\frac{W}{L}\right)_5 = \left(\frac{W}{L}\right)_6 = 160$.

For the remaining transistors whose W/L ratios don't have a direct impact on gain, we chose V_{GST} values such that they stay well out of subthreshold region and in saturation.

1.1.5 Results

Gain	71.4 dB
Phase Margin	38°
UGF	0.3 GHz

Table 2: Iteration 1 Results

1.2 Iteration 2

We missed out on UGF and Phase margin in iteration 1, which was not able to be met at our chosen bias current values. Hence we decided to increase the current through the tail current source (MSS3) to roughly three times the previous value to 1.26 mA. The currents through MSS1 and MSS2 are chosen to be 0.45 mA.

Dimensions of M1-M10 were scaled by $0.18\mu m$ and M11-M14 by $0.75\mu m$ for meeting UGF and PM specifications.

We then increased C_Z to 1pF and choose an appropriate value of $R_Z = 210\Omega$ for maximum Phase Margin (pole zero cancellation).

Using the inequalities of iteration 1 we adjust the $\left(\frac{W}{L}\right)$ values suitably for the new current value after NgSpice simulations to get the transistor sizes. The bias values are set to keep all transistors in saturation.

Finally, the CMFB resistor was chosen to be $R3 = R4 = 0.01M\Omega$ to satisfy the slew rate criterion.

1.2.1 Power

The total static power dissipated in the circuit is given as follows:

$$\begin{aligned}
P_{AB} &= V_{DD} \times (I_{SS3} + I_{SS1} + I_{SS2}) \\
&= 1.5 \times (1.26 + 0.45 + 0.45) mW \\
&= 3.24 mW \\
P_{bias} &= V_{DD} \times (I_1 + I_2 + I_7 + I_9 + I_{11} + I_{13} + I_{15}) \\
&\approx 1.5 \times (50 + 50 + 50 + 50 + 85 + 266 + 76) \mu W \\
&= 0.94 mW \\
P_{SR} &\approx V_{DD} \times I_{MSS4} = 1.5 \times 75 = 1.125 mW \\
P_{AB+bias} &= 4.18 mW \\
P_{AB+bias+SR} &= 5.3 mW
\end{aligned}$$

1.2.2 Results

Gain	71.69 dB
Phase Margin	83°
UGF	1.07 GHz
Slew Rate	404.44 $V/\mu s$

Table 3: Iteration 2 Results

1.3 Schematic

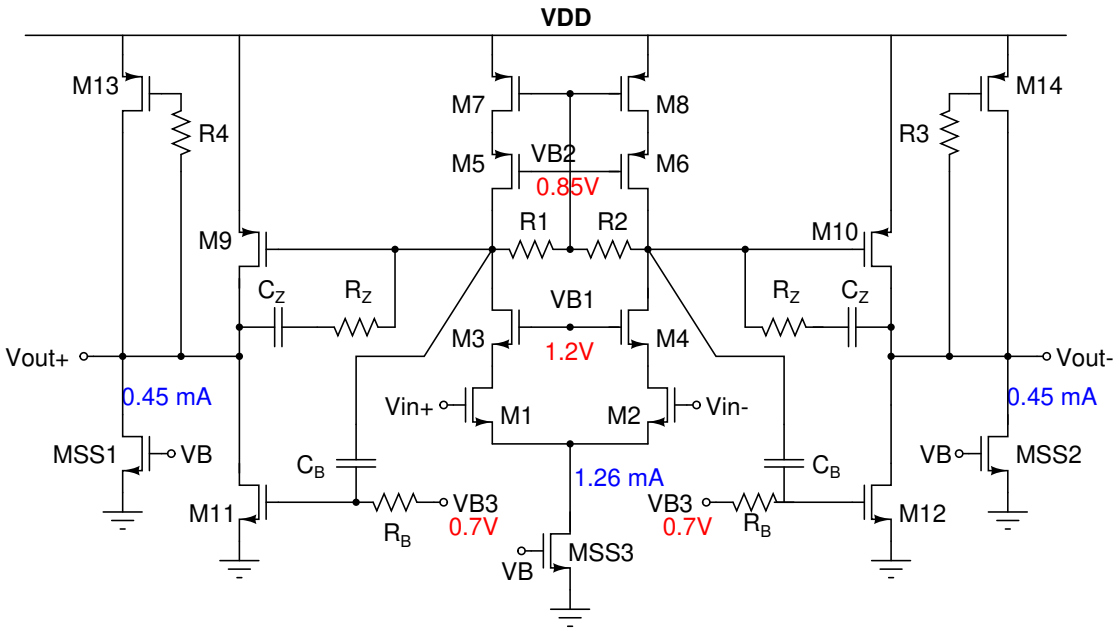

Figure 1: Main Circuit

1.4 Component Values

Transistors	W/L ($\mu m/\mu m$)
M1-M4	9.9/0.18
M5-M8	64.8/0.18
M9-M10	102.6/0.18
M11-M12	12/0.75
M13-M14	11.25/0.75
MSS3	126/1
MSS1-MSS2	45/1
Component	Value
C_B	0.5 pF
R_B	3.5kΩ
C_Z	1 pF
C_L	0.5 pF

Table 4: Pseudo class AB amplifier component values

2 Auxiliary circuit design

2.1 Design Flow

The tail current has been chosen as $I_B = 0.75$ mA. For a common mode bias of 0.75V, we will have a V_{GST} of about 0.35V. Setting that the current through M1 and M2 should be 0.375 mA in saturation, taking into account channel length modulation as well we get

$$0.375mA = 0.5 \cdot k_n \cdot 0.35^2 \cdot (1 + 0.1 \cdot 1) \cdot \left(\frac{W}{L}\right)_1$$

Giving $\left(\frac{W}{L}\right)_{M1,2} = 38$. After NgSpice simulations, this value was set to 30 for optimality. Setting the drain voltage to 1.1V such that M1 and M2 are comfortably in saturation we get and R_1 and R_2 to $\frac{1.5-1.1}{0.375mA} = 1.066k\Omega$.

VBP and VBN are set to 1.13V and 0.423V such that MP1, MP2, MN1, MN2 are in sub-threshold. The stage 1 output current was set as 0.45mA. We need that the combination of MP1-MN1 and MP2-MN2 must be able to supply a current that is a few times the above current. From simulations in NgSpice, we settle on the values of $\left(\frac{W}{L}\right)_{MP1,2} = 800$ and $\left(\frac{W}{L}\right)_{MN1,2} = 100$.

2.2 Iteration 2

As suggested in the reference paper, the dominant pole of this stage is given by $\omega_{p1} = \frac{1}{R_B \cdot C_B}$. For a settling time of $3ns$ using the dominant pole approximation we get that the dominant pole must be $\approx 0.212GHz$. Hence for $C_B = 0.5pF$ we get $R_B = 1.5k\Omega$. In simulation these values are tweaked further for best settling time.

Since R_1 is also involved in the non-dominant pole of the system and hence the speed of the system, we also needed to change its value to 900Ω to meet settling time and slew rate.

Dimensions of M1-M2 and MP1,2-MN1,2 are scaled by 0.18 and 0.3 respectively as they are also in the direct signal path.

2.3 Schematic

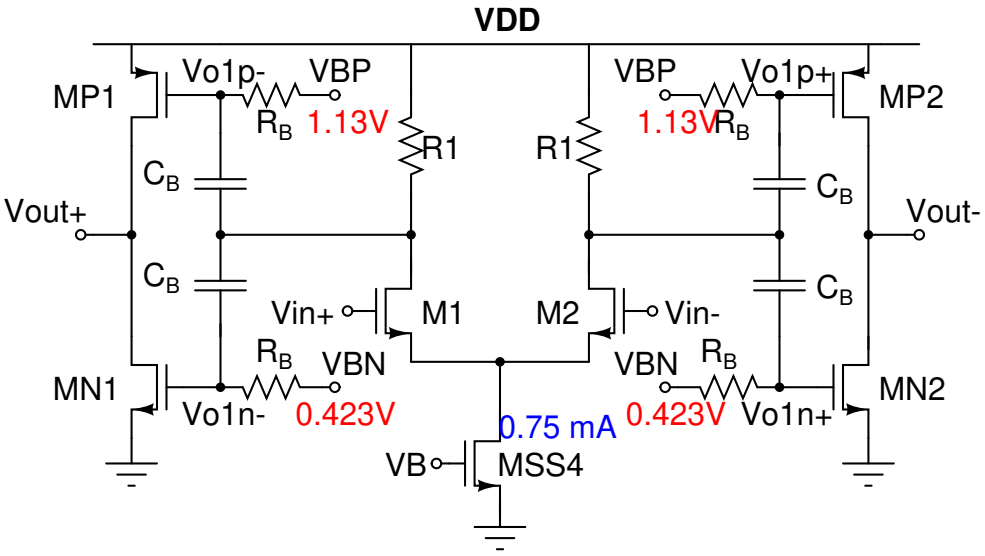

Figure 2: Auxiliary Circuit

2.4 Component Values

Transistors	W/L ($\mu m/\mu m$)
M1-M2	5.4/0.18
MP1-MP2	240/0.3
MN1-MN2	30/0.3
MSS4	75/1
Component	Value
R_1	900Ω
C_B	0.5 pF
R_B	2kΩ

Table 5: Auxiliary Circuit component values

3 Current Reference Generator Circuit Design

3.1 Design Flow

Transistors M1-M5 constitute a circuit that is capable of establishing a supply independent current, with a value $I_{out} = 50\mu A$. M5 is used as a start up device.

Here, R_S value can be changed to adjust the value of current.

Let W/L ratios for M1,M3, M4 as 5 (a small value chosen such that we can increase if the need arises). Choosing $K = 5$, gives $\left(\frac{W}{L}\right)_2 = 25$.

$$I_{out} = \frac{2}{k_n \times (W/L)_1} \cdot \frac{1}{R_s^2} \left(1 - \frac{1}{\sqrt{K}}\right)^2$$

Substituting values, we get $R_S = 4086\Omega$. However, during actual simulation, we got the best results for $R_S = 1973\Omega$, which could be attributed to body effect and the error in the assumed values of C_{ox} and μ_n for the model file considered.

The current is mirrored through M6 and M7 and is used to generate V_{b3}, which is needed in the main amplifier stage. We choose $\left(\frac{W}{L}\right)_6 = 5$ for mirroring, and find an appropriate value (via NgSpice simulations) of $\left(\frac{W}{L}\right)_7$ to get $V_{b3} = 0.7$.

Similarly, mirroring the currents, and finding the needed W/L ratios for the required bias voltages for the auxiliary and main amplifiers, we get the ratios as summarized in the following table.

3.2 Schematic

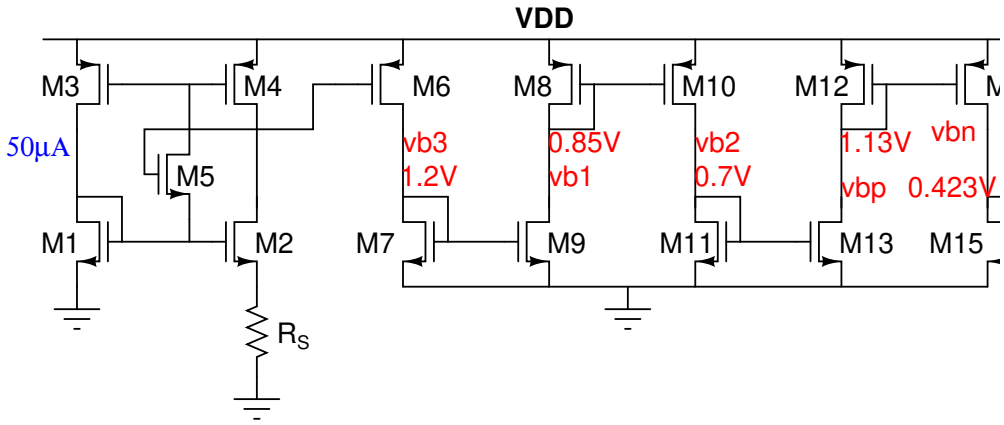

Figure 3: Current reference Circuit

3.3 Component Values

Transistors	W/L ($\mu m/\mu m$)
M1,M3,M4,M5,M6	5/1
M2	25/1
M7,M9	1.4/1
M8	600/1
M10	1000/1
M11	1.33/1
M12	900/1
M13	4.1/1
M14	250/1
M15	30/1

Table 6: Current Reference Circuit component values

4 DC Operating point simulations

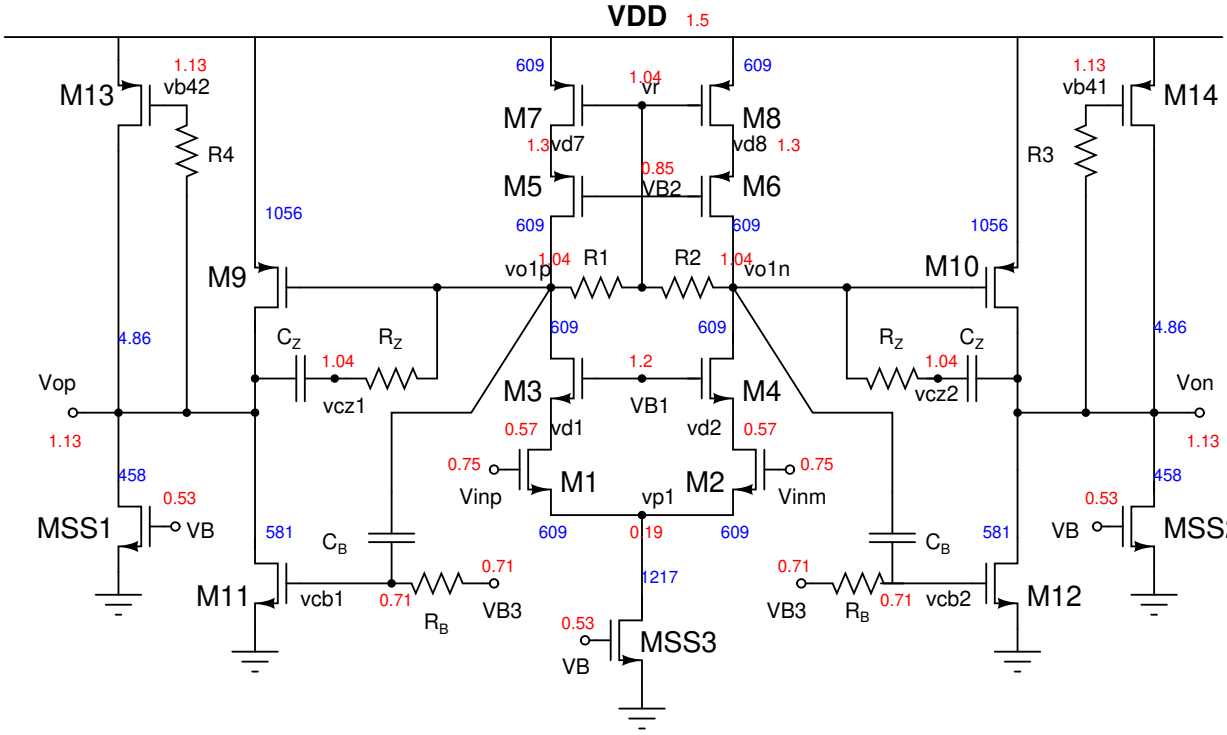

Figure 4: Pseudo Class AB Circuit Operating Points - Node voltages in red (V) and Currents in blue (μA)

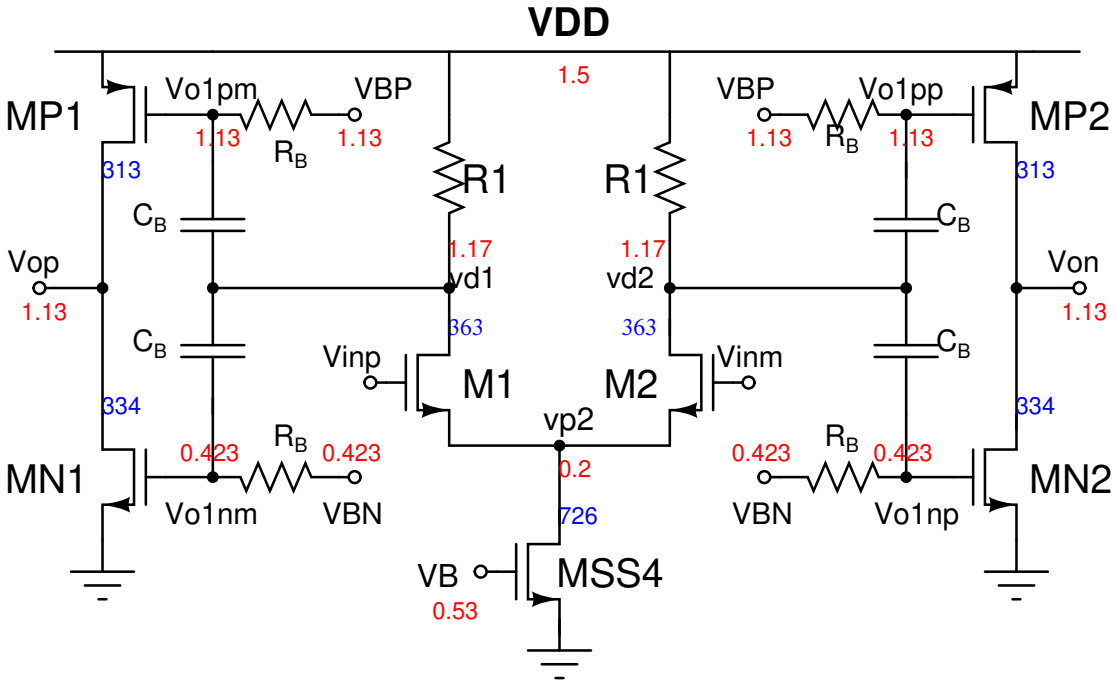

Figure 5: Auxiliary Circuit Operating Points - Node voltages in red (V) and Currents in blue (μA)

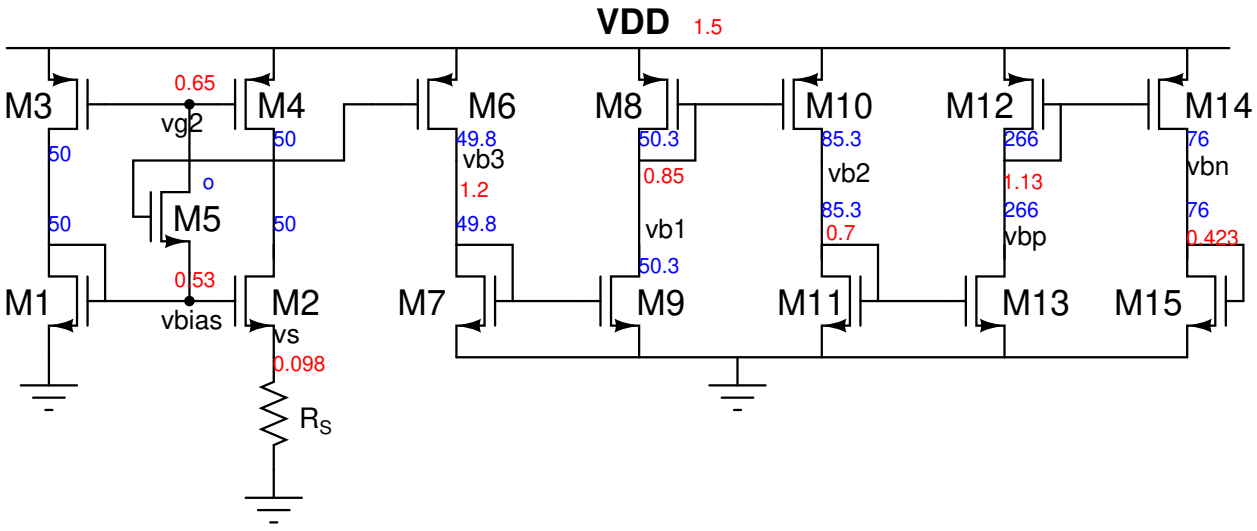

Figure 6: Current reference Circuit Operating Points - Node voltages in red (V) and Currents in blue (μA)

5 AC simulations

5.1 Pseudo Class AB amplifier

The results of the simulation are as follows (GBW and unity gain frequency have the same value):

Open Loop DC Gain	71.69 dB
Phase Margin	83°
Small signal GBW	1.07 GHz

Table 7: AC simulation results

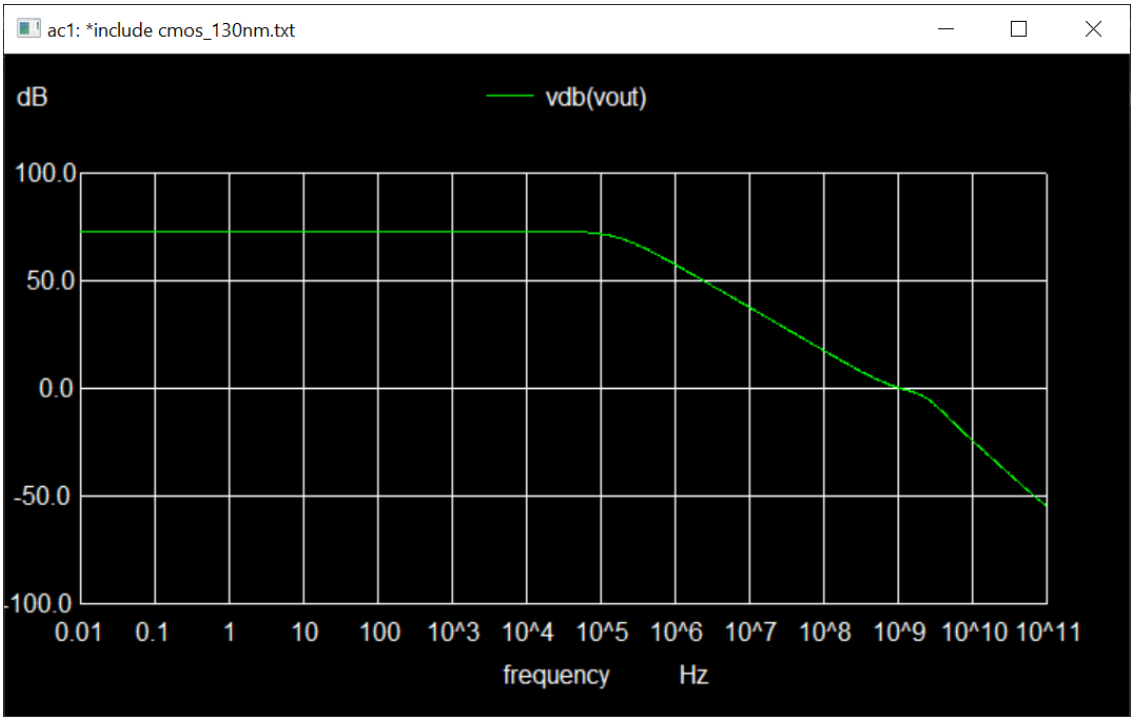

Figure 7: Bode magnitude plot for Pseudo class AB amplifier

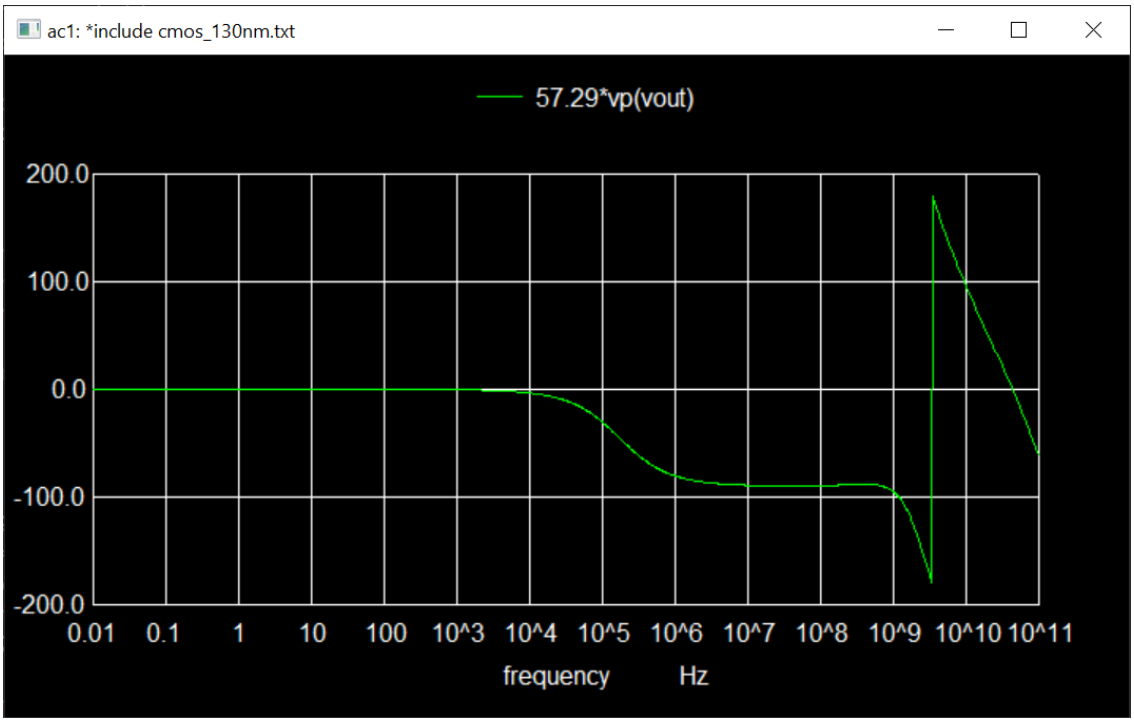

Figure 8: Bode phase plot for Pseudo class AB amplifier

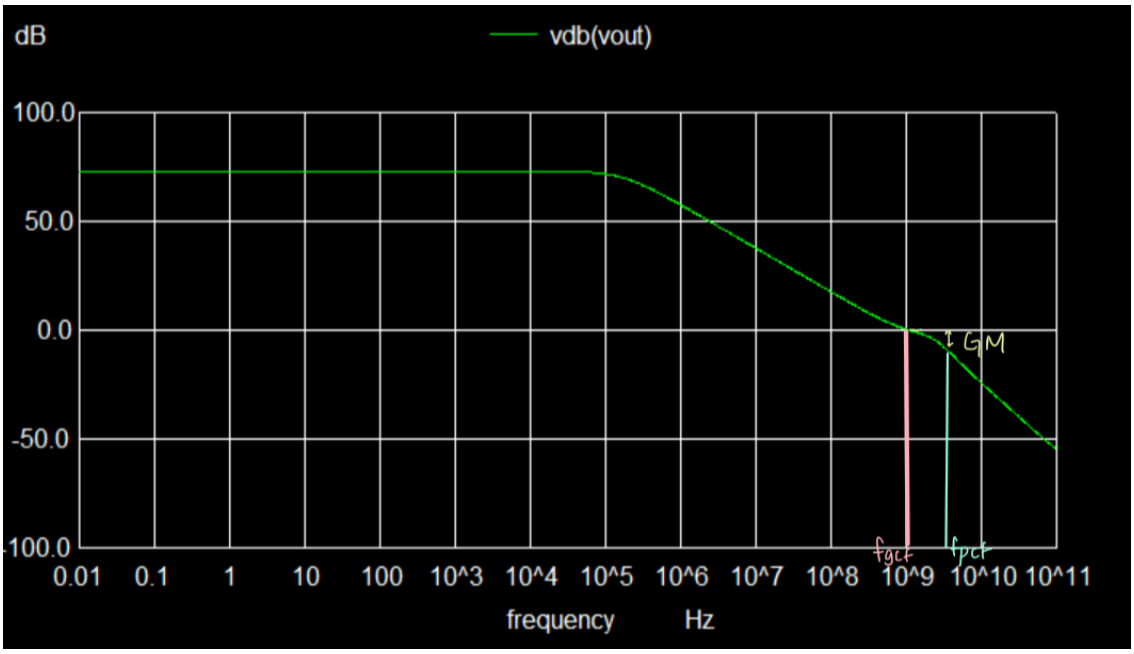

Figure 9: Bode magnitude plot with phase and gain crossover frequencies

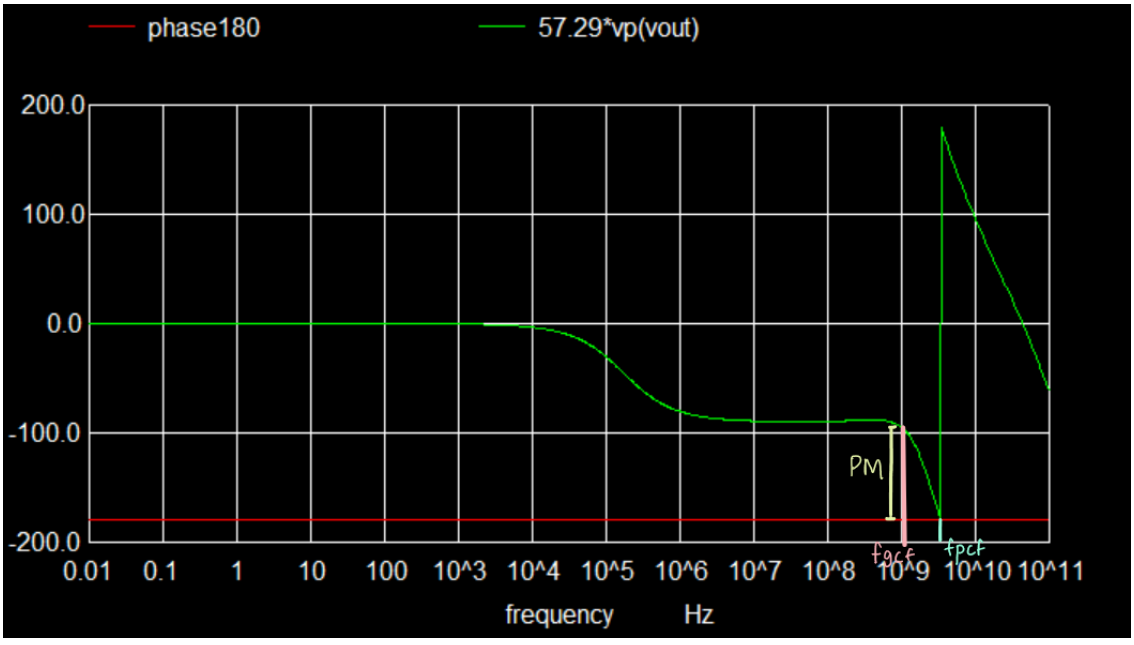

Figure 10: Bode phase plot with phase and gain crossover frequencies

5.2 Pseudo class AB amplifier with auxiliary circuit

The results of the simulation are as follows (GBW and unity gain frequency have the same value):

Open Loop DC Gain	71.7dB
Phase Margin	66.17°
Small signal GBW	1.61 GHz

Table 8: AC simulation results

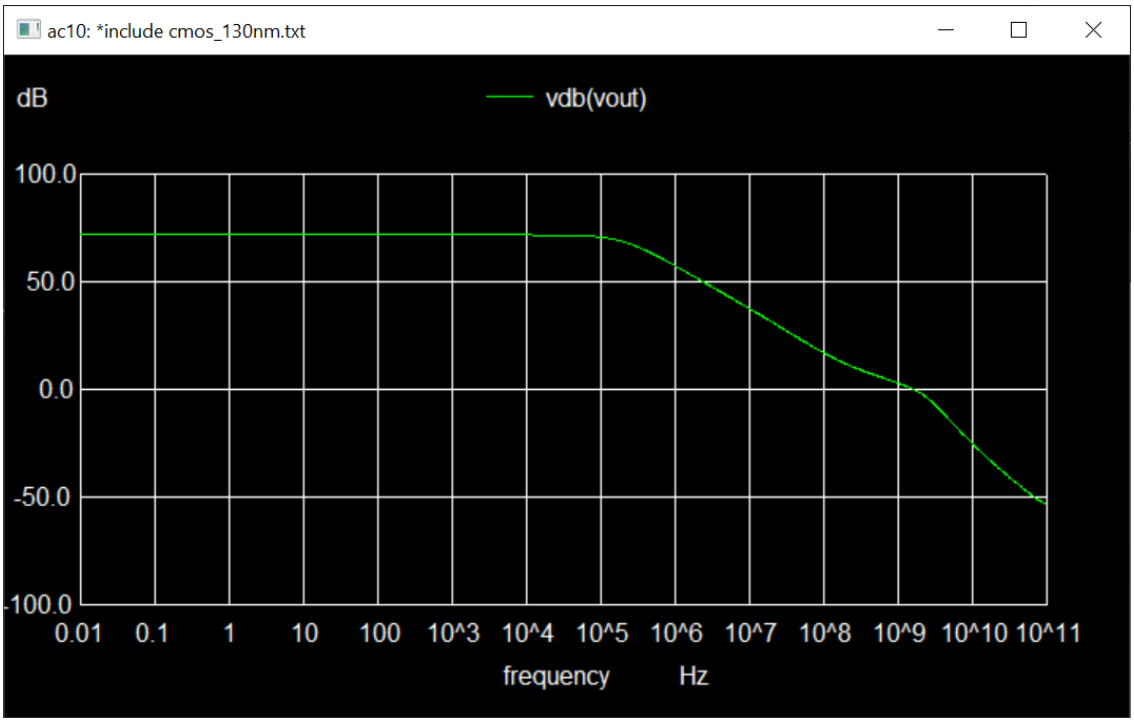

Figure 11: Bode magnitude plot for Pseudo class AB amplifier with auxiliary circuit

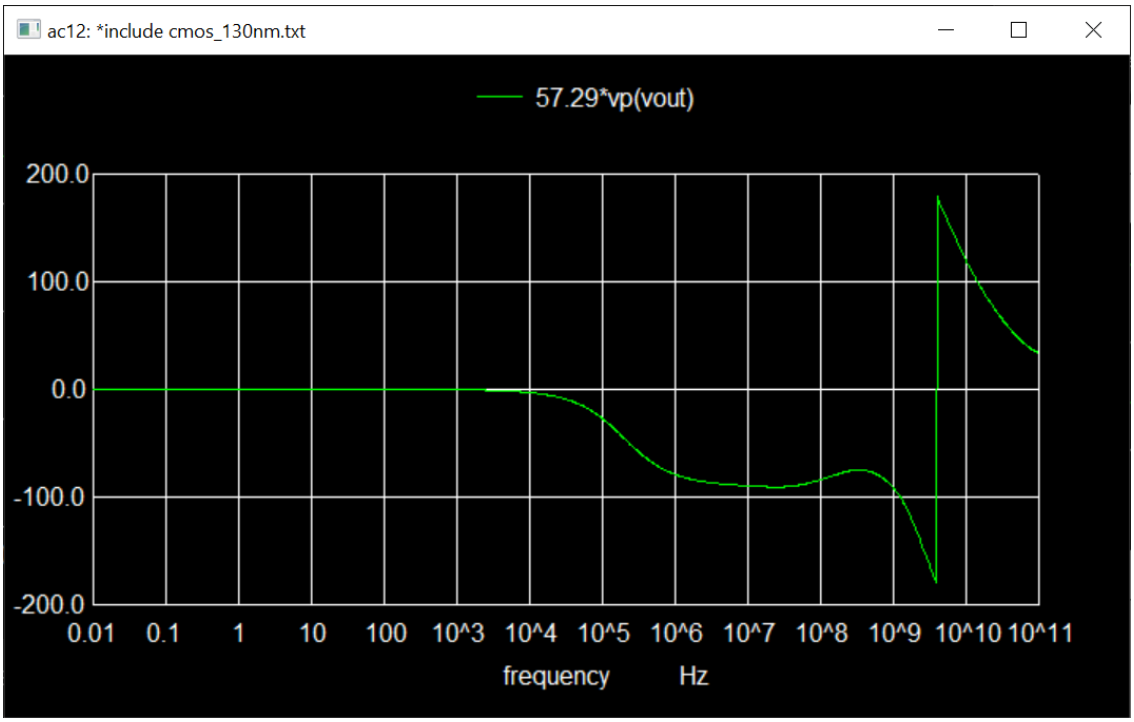

Figure 12: Bode phase plot for Pseudo class AB amplifier with auxiliary circuit

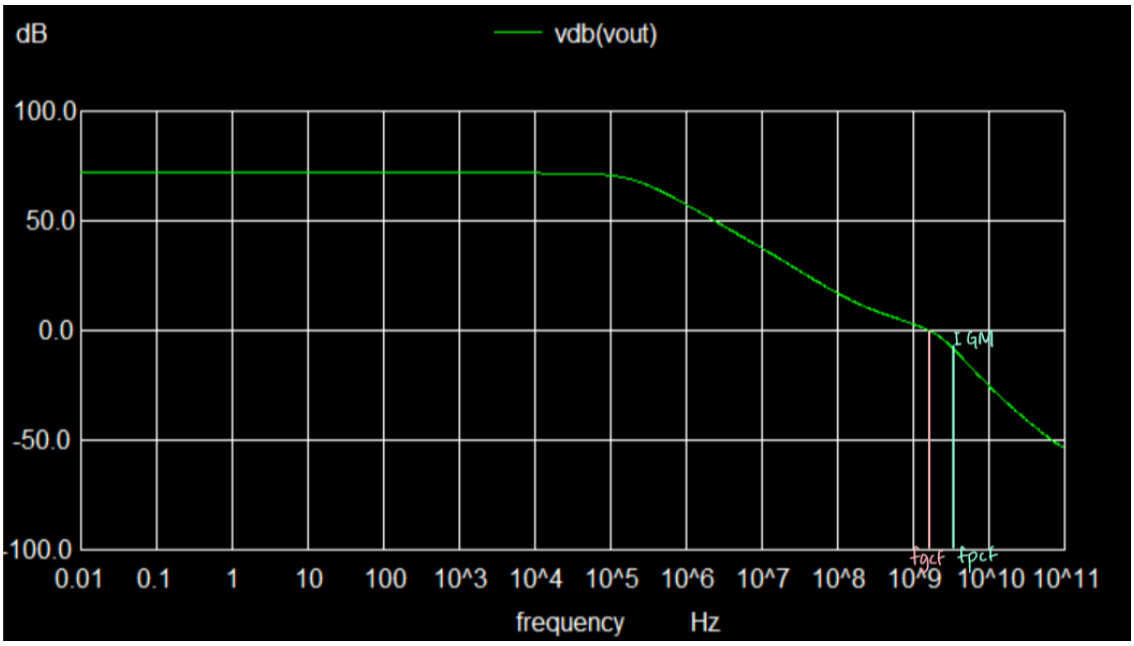

Figure 13: Bode magnitude plot with phase and gain crossover frequencies

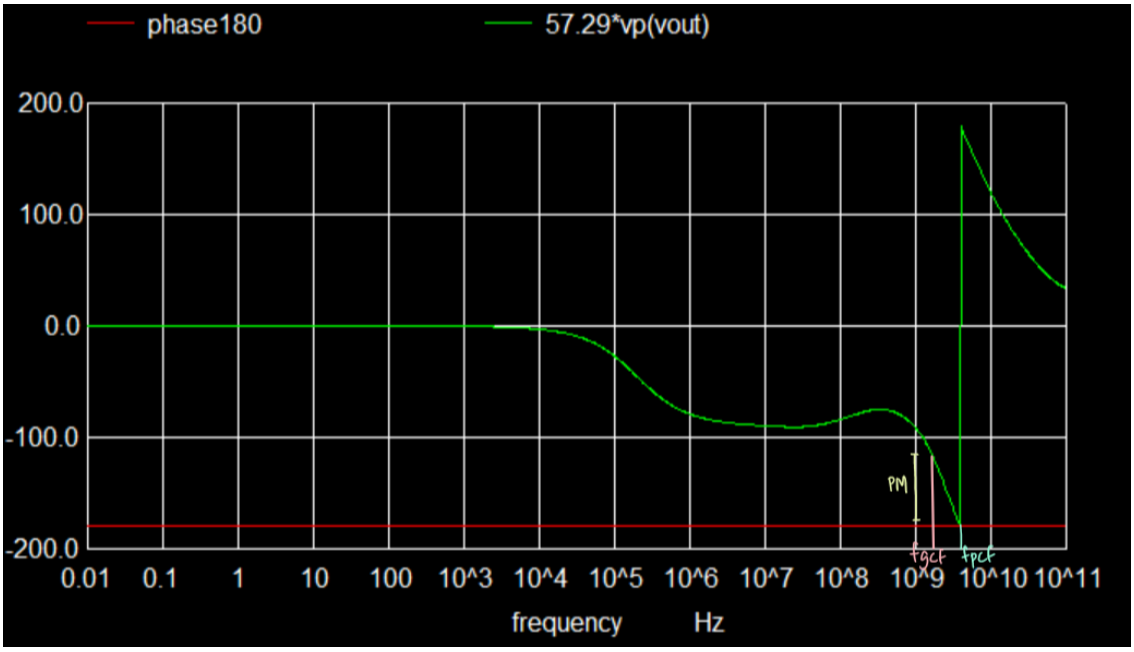

Figure 14: Bode phase plot with phase and gain crossover frequencies

6 Settling Time and Slew rate calculation

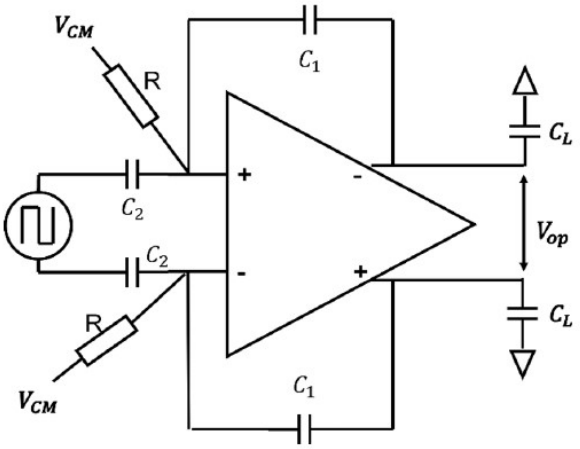

Figure 15: Slew Rate and Settling Time Measurement setup

6.1 Circuit specifications

The following values are arrived upon in the above circuit for measuring slew rate and settling time:

- $C_1 = C_2 = 0.01pF$
- R= 100 kΩ
- Resistors of value 1kΩ are placed in parallel with C_2 to achieve meaningful simulation results

6.2 Differential Output Voltage Plots

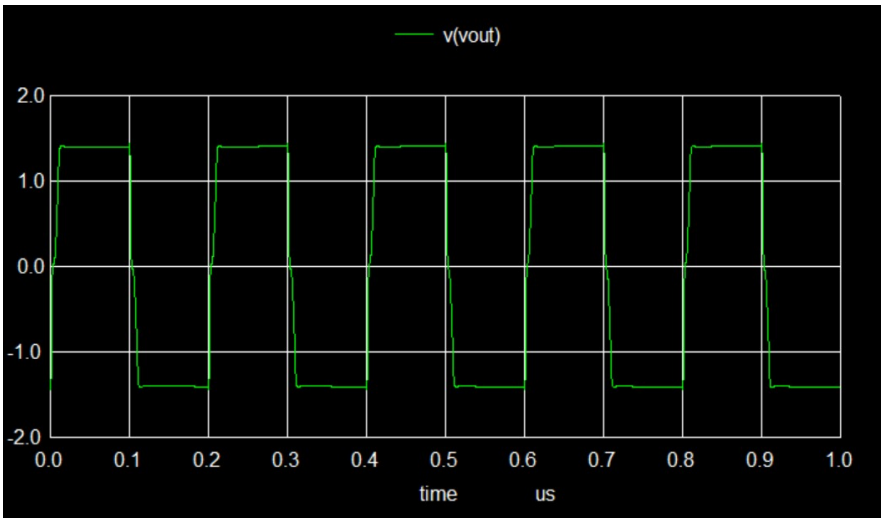

Figure 16: V_{op} for Pseudo class AB amplifier

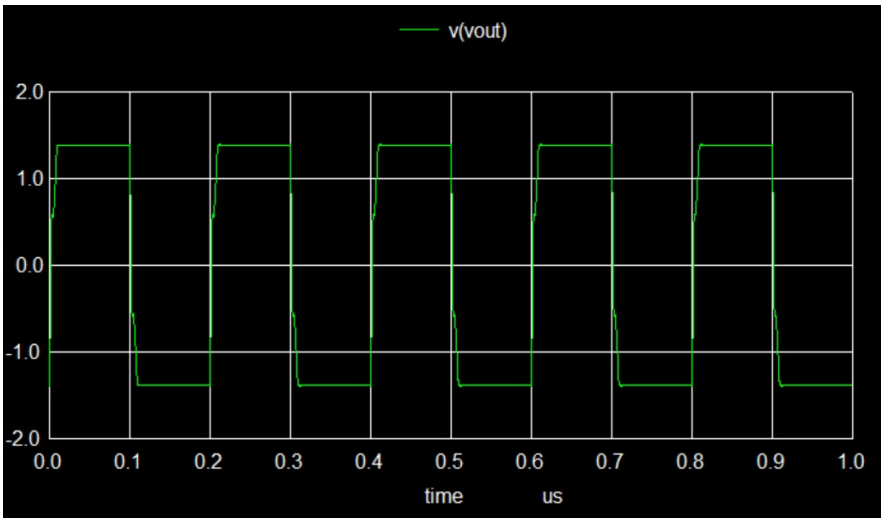

Figure 17: V_{op} for Pseudo class AB amplifier with auxiliary circuit

6.3 Slew rate calculation

Slew rate is calculated in the code as follows:

```
meas tran tp1 when v(vout)=0 RISE=3
meas tran tp2 when v(vout)=0.3 RISE=3
meas tran tn1 when v(vout)=0.5 FALL=3
meas tran tn2 when v(vout)=0.2 FALL=3

let srp = 0.3/(tp2-tp1)
let srn = 0.3/(tn2-tn1)
let sr_avg = (srp+srn)/2
print srp
print srn
print sr_avg
```

6.4 Average SR

- Average SR for class AB stage = $\boxed{404.44V/\mu s}$
- Average SR for class AB stage with SR booster = $\boxed{907.97V/\mu s}$

6.5 Settling Time

Settling time is computed for a unit step input, with the circuit settling at 1.389V.

- 1% settling time for class AB stage = $\boxed{5.02ns}$
- 1% settling time for class AB stage with SR booster = $\boxed{6.81ns}$

7 Noise Analysis

7.1 Input referred noise voltage plots

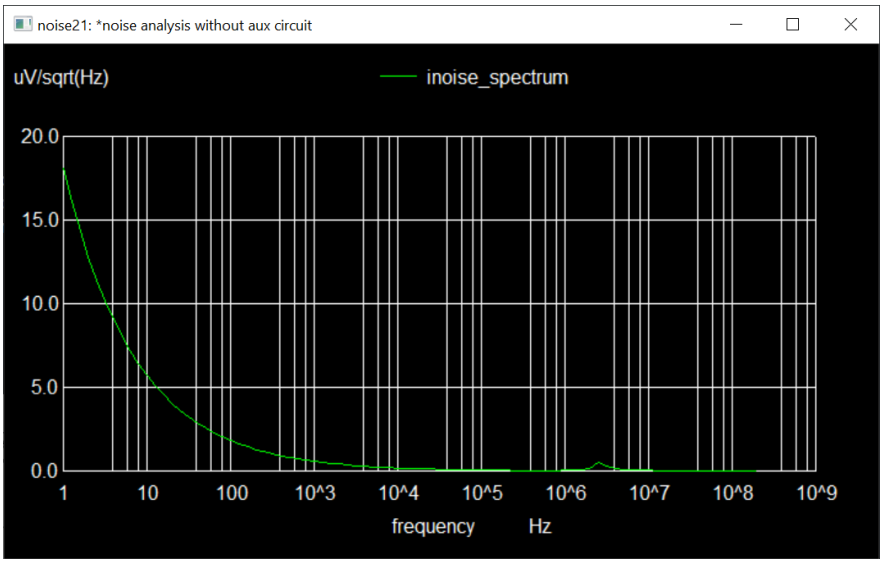

Figure 18: Input referred noise for Pseudo class AB amplifier

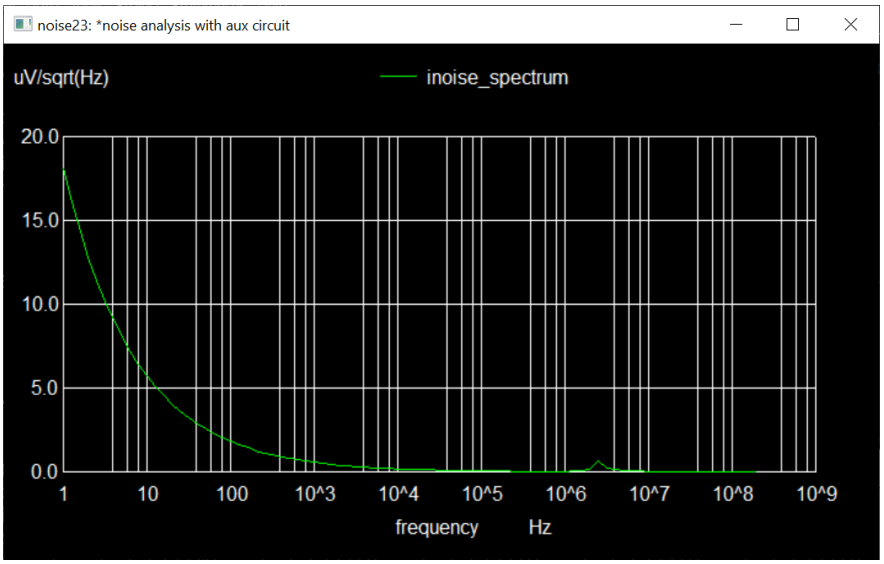

Figure 19: Input referred noise for Pseudo class AB amplifier with auxiliary circuit

7.2 Total Integrated input referred noise

From the NgSpice simulations, we get total input referred noise is 5.67×10^{-4} for the Pseudo Class AB stage and 5.44×10^{-4} for the Pseudo Class AB stage with auxiliary circuit.

7.3 Flicker Noise Corner Frequency

We only take contributions from the first stage for noise calculations as the later stages will be further divided by a gain term and hence be negligible in comparison. Let I_{n_i} be the noise current source of the i^{th} transistor.

7.3.1 Pseudo Class AB amplifier

For thermal noise:

$$\bar{v_{n_{in}}}^2 = \frac{I_{n_1}^2 + I_{n_2}^2 + I_{n_7}^2 + I_{n_8}^2}{g_{m1}^2}$$

Substituting for the above we get

$$\begin{aligned}\bar{v_{n_{in}}}^2 &= \frac{4KT\gamma(g_{m1} + g_{m2} + g_{m7} + g_{m8})}{g_{m1}^2} \\ &= \frac{8KT\gamma(g_{m1} + g_{m7})}{g_{m1}^2}\end{aligned}$$

Similarly, net flicker noise is given by

$$\begin{aligned}\bar{v_{n_{in}}}^2 &= (\frac{K}{W_1L_1C_{ox}} \cdot \frac{g_{m1}^2}{f_C} + \frac{K}{W_2L_2C_{ox}} \cdot \frac{g_{m2}^2}{f_C} + \frac{K}{W_7L_7C_{ox}} \cdot \frac{g_{m7}^2}{f_C} + \frac{K}{W_8L_8C_{ox}} \cdot \frac{g_{m8}^2}{f_C}) \cdot \frac{1}{g_{m1}^2} \\ &= (\frac{K}{W_1L_1C_{ox}} \cdot \frac{g_{m1}^2}{f_C} + \frac{K}{W_7L_7C_{ox}} \cdot \frac{g_{m7}^2}{f_C}) \cdot \frac{2}{g_{m1}^2}\end{aligned}$$

Equating the above 2 equations and solving f_C we get $\boxed{f_C = 1.64MHz}$

7.3.2 Pseudo class AB amplifier with auxiliary circuit

As above, thermal noise:

$$\bar{v_{n_{in}}}^2 = \frac{8KT\gamma(g_{m1} + g_{m7})}{g_{m1}^2} + \left(\frac{8KT\gamma g_{m1}}{g_{m1}^2}\right)_{aux}$$

Flicker noise:

$$\bar{v_{n_{in}}}^2 = (\frac{K}{W_1L_1C_{ox}} \cdot \frac{g_{m1}^2}{f_C} + \frac{K}{W_7L_7C_{ox}} \cdot \frac{g_{m7}^2}{f_C}) \cdot \frac{2}{g_{m1}^2} + \left(\frac{K}{W_1L_1C_{ox}} \cdot \frac{2}{f_C}\right)_{aux}$$

Equating the above 2 equations and solving f_C we get $\boxed{f_C = 2.23MHz}$

8 Common Mode Analysis

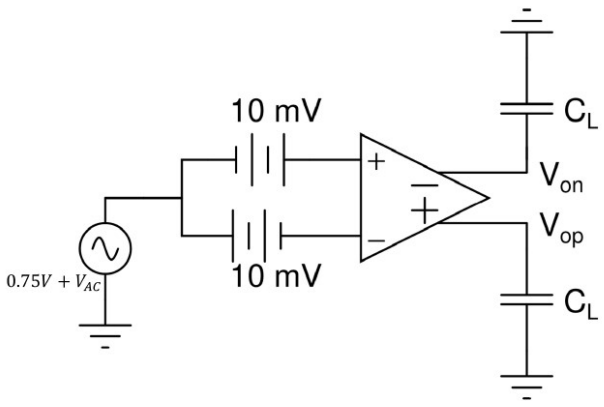

Figure 20: CMRR Measurement setup

8.1 Input Common Mode Range

We have the following constraints, given $V_{GST} = V_{DS,sat} = 0$:

$$\begin{aligned} V_{CM,min} &= V_{GST,MSS3} + V_{GS,1} = 2V_{GST} + V_{thn} = 0.3782V \\ V_{CM,max} &= V_{DD} - V_{GST,M7} - V_{GST,M5} - V_{GST,M3} - V_{GST,M3} + V_{GS,1} \\ &= V_{DD} - 3V_{GST} + V_{thn} = 1.8782V \end{aligned}$$

8.2 CMRR

For the above circuit, from the NgSpice simulations, we get:

$$A_{DM} = 2.420823/10^{-3} = 2.43 \times 10^3$$

$$A_{CM-DM} = 3 \times 10^{-6}/10^{-3} = 3 \times 10^{-3}$$

Therefore,

$$CMRR = 20log\left(\frac{A_{DM}}{A_{CM-DM}}\right) = 118\,dB$$

8.3 Bode Plots

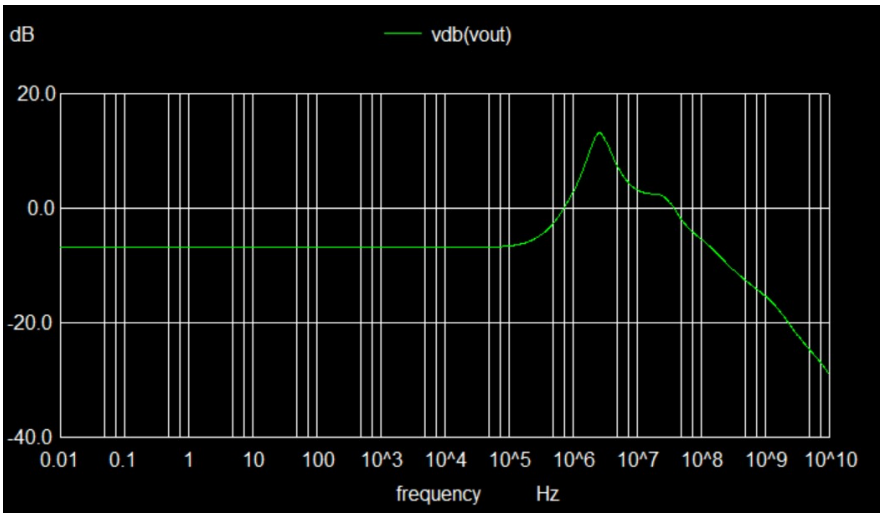

Figure 21: Common mode Magnitude Plot

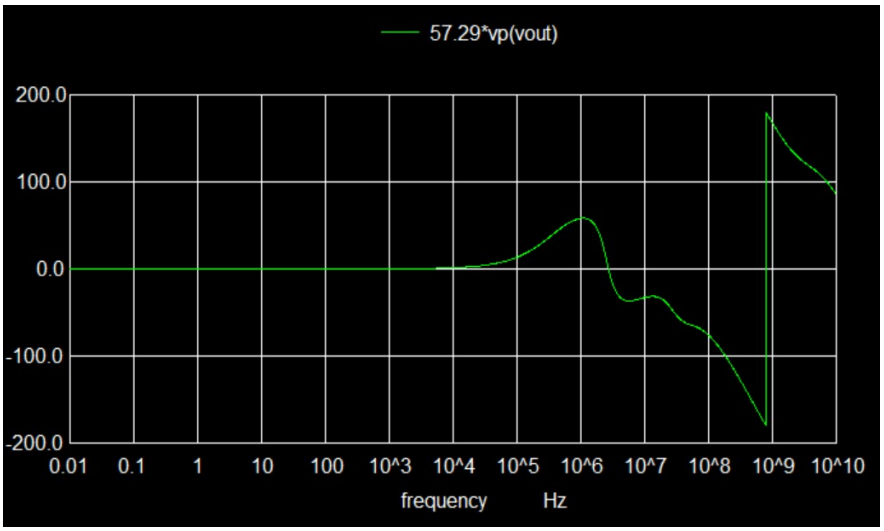

Figure 22: Common mode Phase Plot

9 Final Results

Parameters	Specifications
Static Power Consumption (Bias + AB)	4.18 mW
Static Power Consumption (Bias + AB + SR Boosting)	5.3 mW
Input DC Common Mode Voltage	0.75V
DC Voltage Gain	71.7 dB
UGF	1.61 GHz
Open Loop Phase Margin	66.17°
Load Capacitance	0.5 pF
Slew Rate AB Amplifier	404.44 $V/\mu s$
Slew Rate AB Amplifier with SR Boosting	907.97 $V/\mu s$
Input Referred Noise (1Hz to 250 MHz)	$544\mu V/\sqrt{Hz}$
Maximum Fully Differential Output Swing	1.32V
1% Settling Time AB Amplifier	5.02 ns
1% Settling Time AB Amplifier with SR Boosting	6.81 ns
CMRR for input offset = 20 mV	118 dB

Table 9: Final Results

Even as we increase the differential input, the output values at the two output nodes saturate at a value close to, and above 0V or close to, but below V_{DD}. The output swing for both the circuits - with and without auxiliary circuit is around 1.3V as calculated from the simulations, and the plot can be seen below.

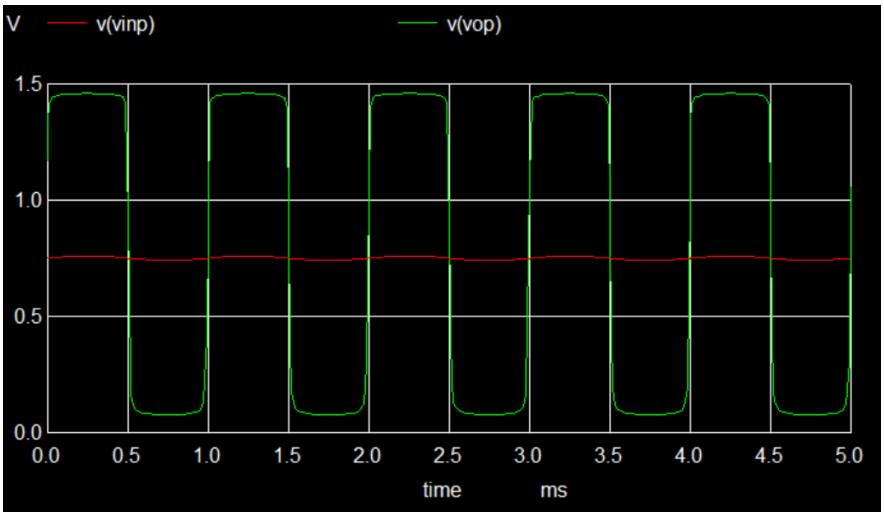

Figure 23: Maximum output swing

10 Work Contribution

Question Number	Saketika Chekuri	Suraj Samaga
1.1	✓(together)	✓(together)
1.2	✓(together)	✓(together)
1.3	✓(together)	✓(together)
1.4	✓(together)	✓(together)
2.1		✓
2.2		✓
2.3		✓
2.4		✓
3.1	✓	
3.2	✓	
3.3	✓	
4	✓(together)	✓(together)
5.1	✓(together)	✓(together)
5.2	✓(together)	✓(together)
6.1		✓
6.2		✓
6.3		✓
6.4		✓
6.5		✓
7.1	✓	
7.2	✓	
7.3	✓	
8.1	✓	
8.2	✓	
8.3	✓	