

# EE671: VLSI Design

## Assignment 2

Sai Saketika Chekuri  
190070054

September 5, 2022

### Question 1

The load capacitance  $C_L$  is 154fF.

#### Part a

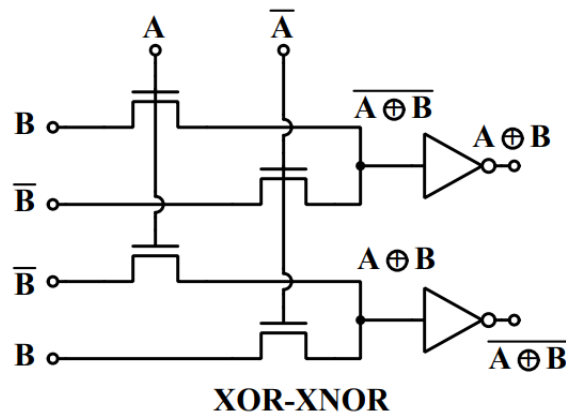


Figure 1: Circuit Diagram of CPL implementation of XOR-XNOR

- $I_{avg} = -52.76\mu A$  (-ve sign indicates current is being drawn from Vdd)
- The output swings between 0 and Vdd as per the XOR logic (the rise, and especially fall times are significant due to the load capacitance)
- The output of switch matrix only swings from 0 to approximately  $V_{dd} - V_{tn}$  due to the NMOS
- We see sudden peaks in current - this is during switching when dynamic power is high. At other times, current is low, but still non zero since PMOS of inverter never fully turns off as input is  $V_{dd} - V_{tn}$  at best.
- Fall time is high since NMOS has to pull down to 0 when PMOS isn't fully off.

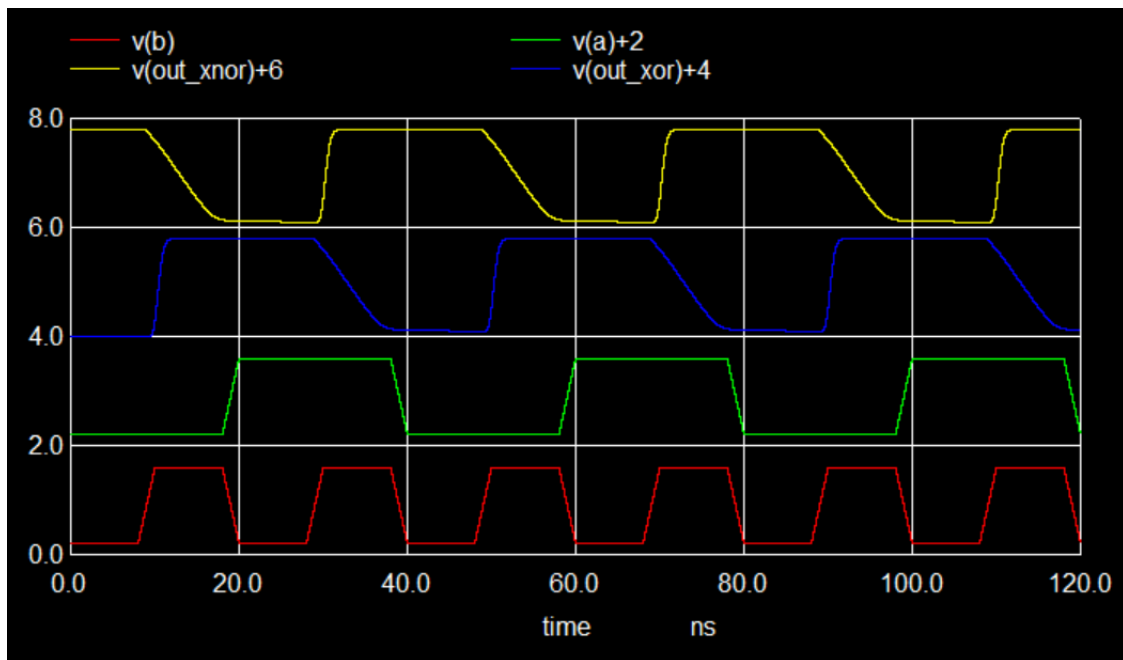


Figure 2: Input and output waveforms of CPL XOR gate

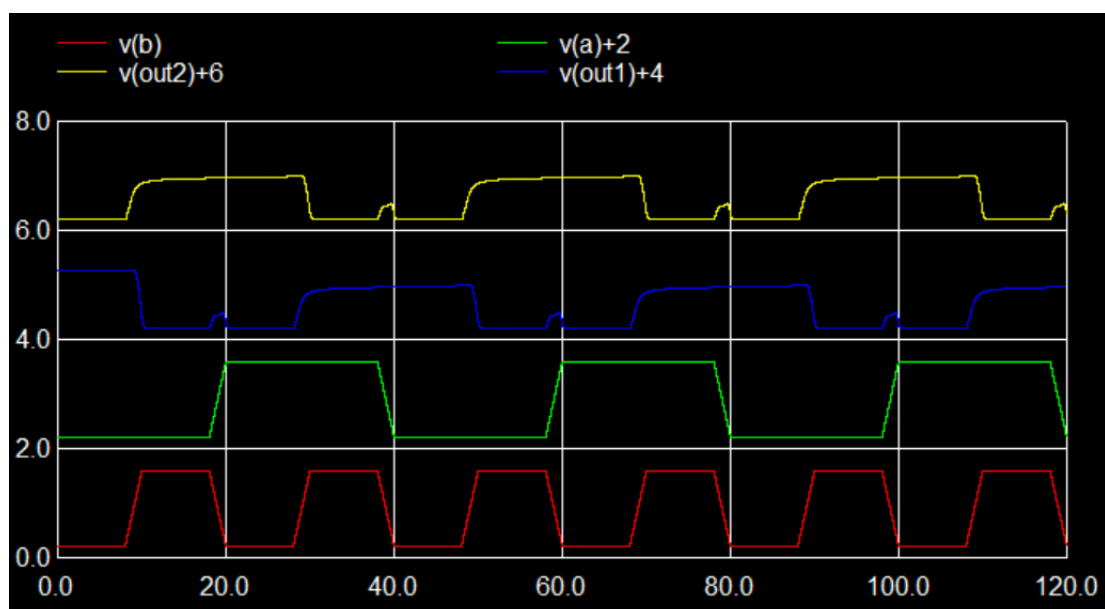


Figure 3: Voltages at output of switch matrix

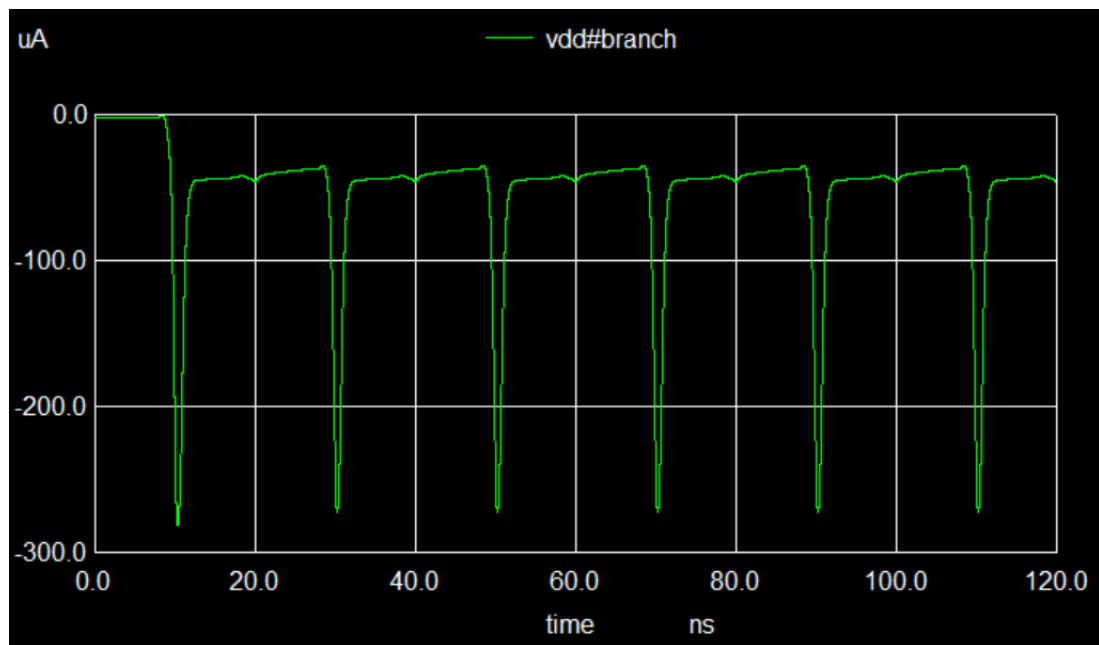


Figure 4: Current waveform

## Part b

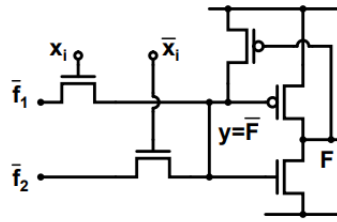


Figure 5: Pull-up PMOS connection

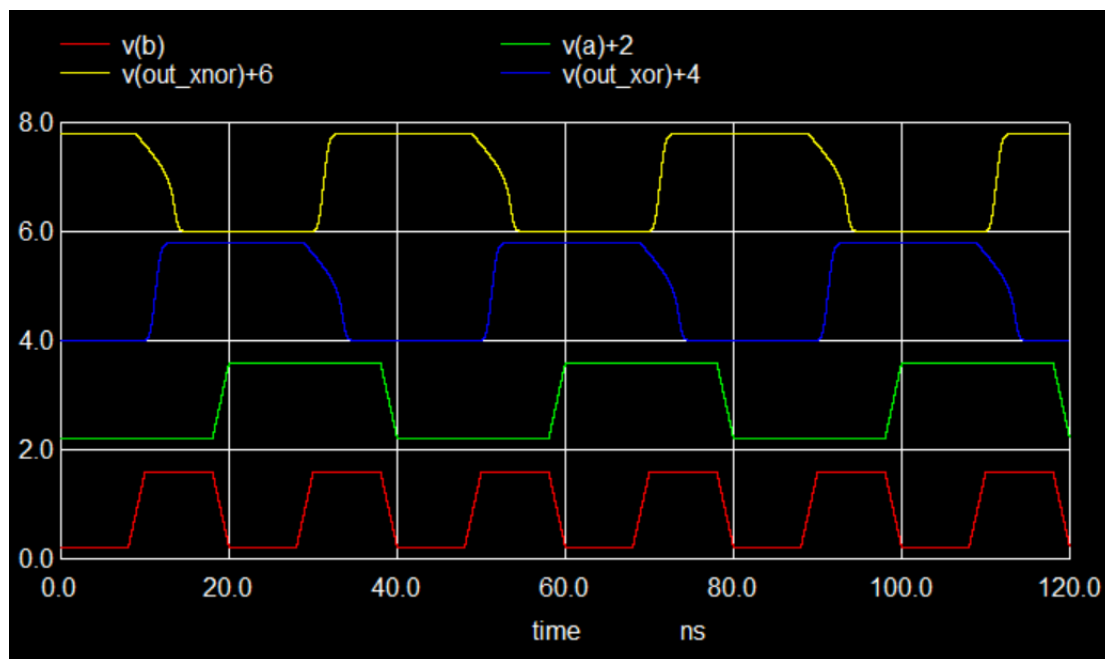


Figure 6: Input and output waveforms of CPL XOR gate after pull up PMOS

- $I_{avg} = -29.92\mu A$  (-ve sign indicates current is being drawn from Vdd)
- The output is now closer to the ideal XOR than previous case.
- The static power is now zero as the pull up transistor takes the input of inverter to Vdd, and the PMOS of inverter is therefore now fully off resulting in 0 static power.
- Outputs of switch matrix now swing rail to rail since PMOS fully brings input to Vdd (and also improves fall time).

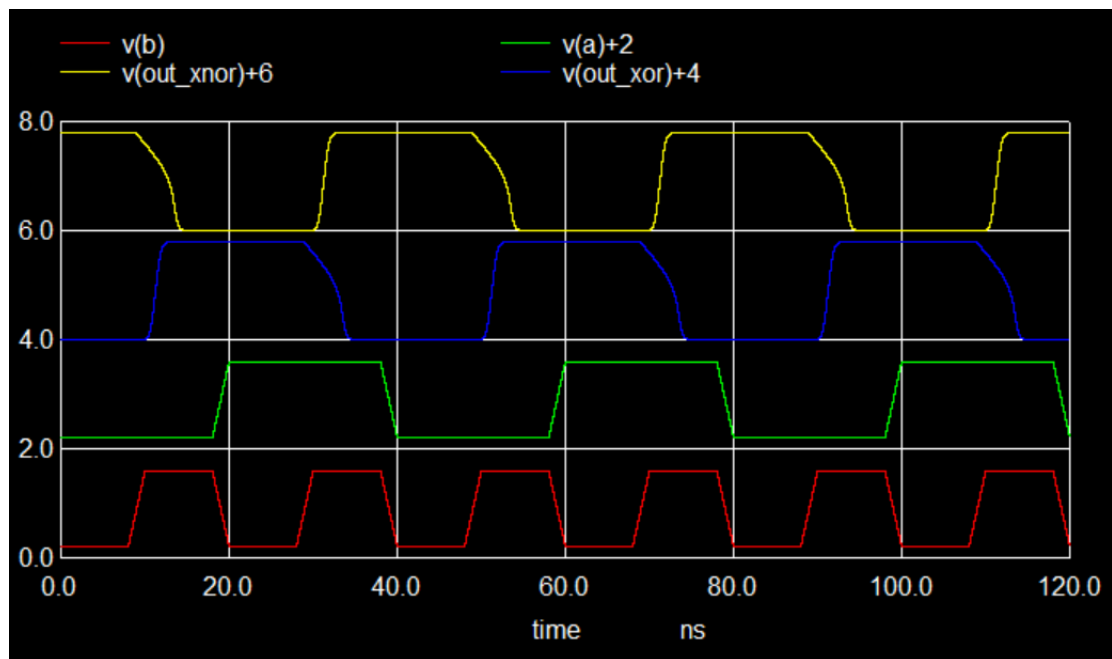


Figure 7: Voltages at output of switch matrix

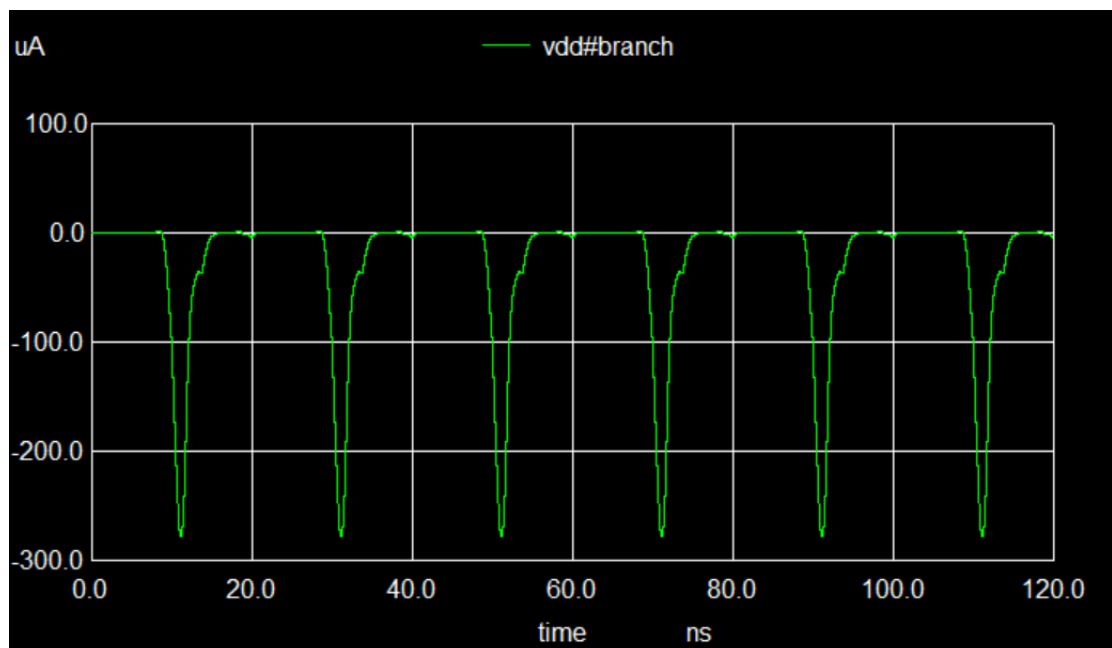


Figure 8: Current waveform

## Part c

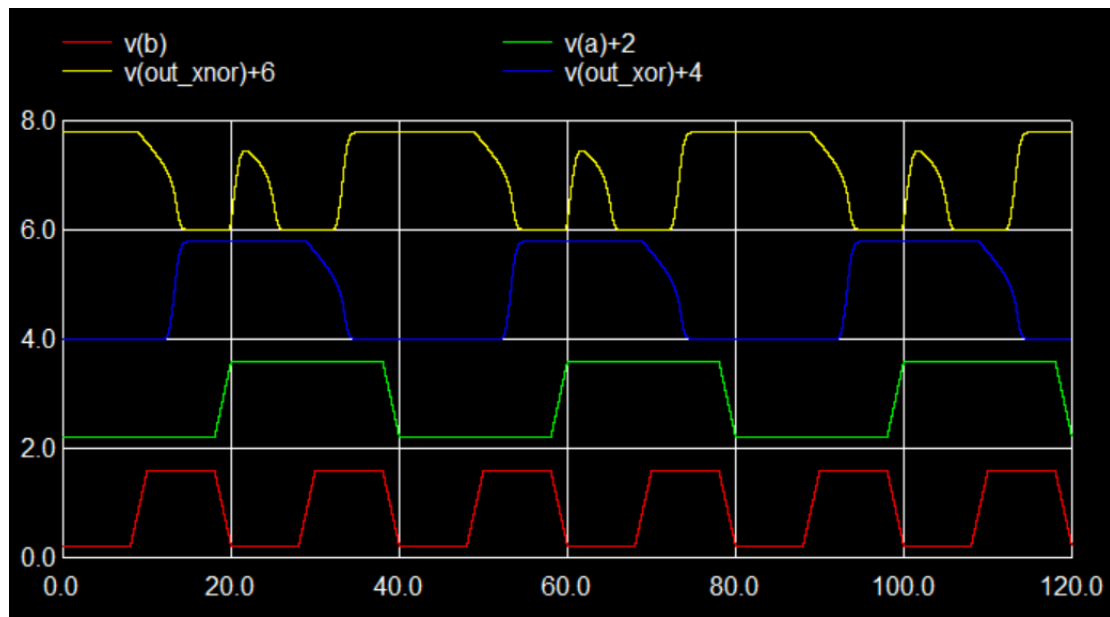


Figure 9: Input and output waveforms of CPL XOR gate after pull up PMOS and delayed complement inputs

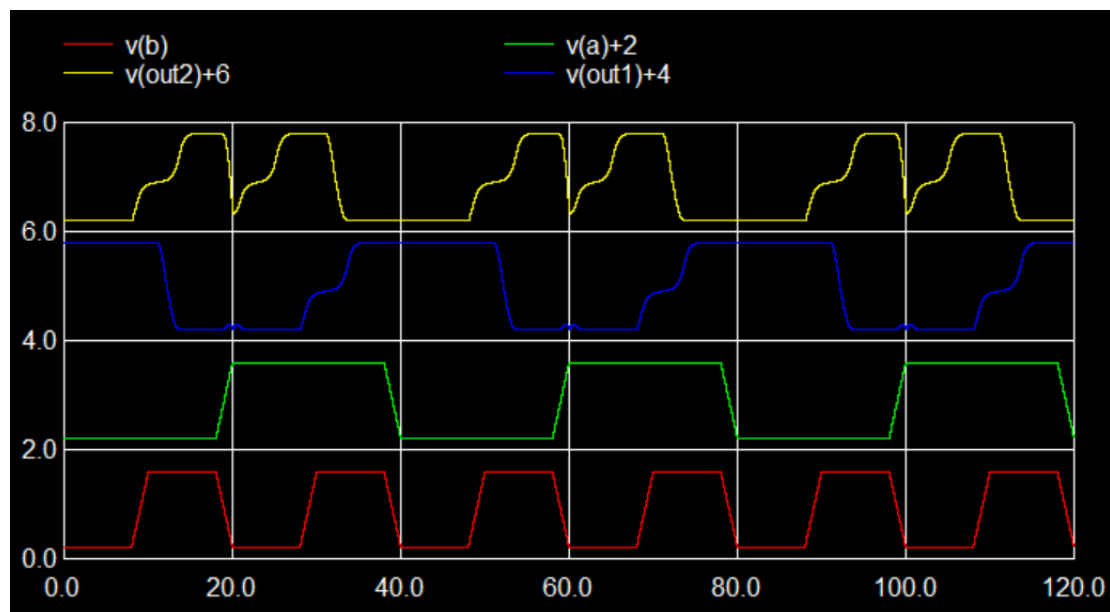


Figure 10: Voltages at output of switch matrix

- $I_{avg} = -42.66\mu A$  (-ve sign indicates current is being drawn from Vdd)
- The output has glitches– the delay in complement results in  $B$  and  $\bar{B}$  being shorted at input of inverter, which results in an undefined output for the short duration they overlap.
- The current is non zero when the inputs are shorted, leading to higher power consumption.

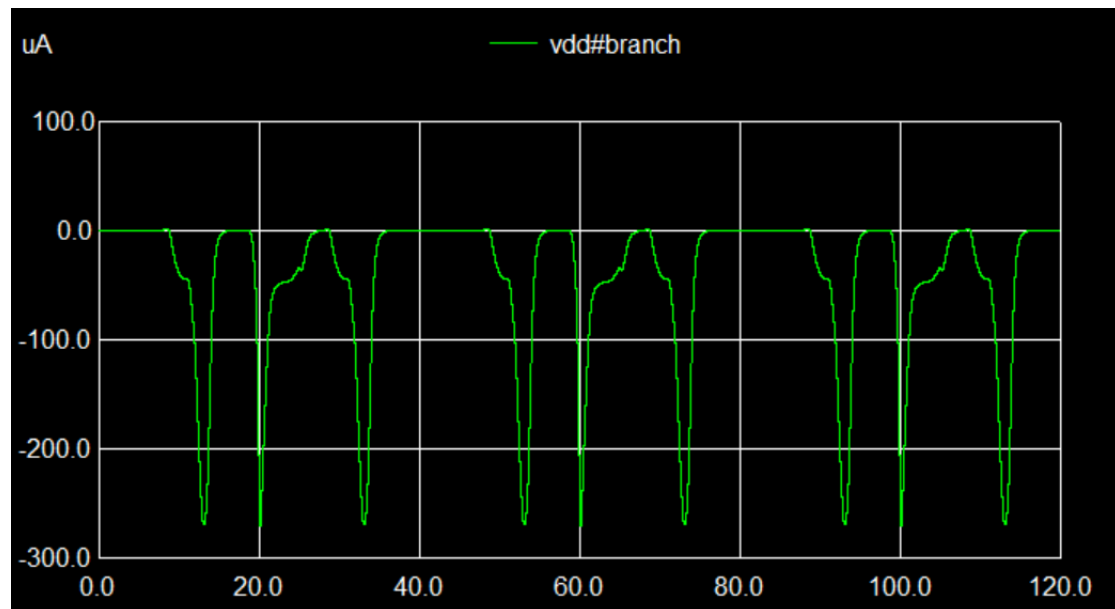


Figure 11: Current waveform

## Part d

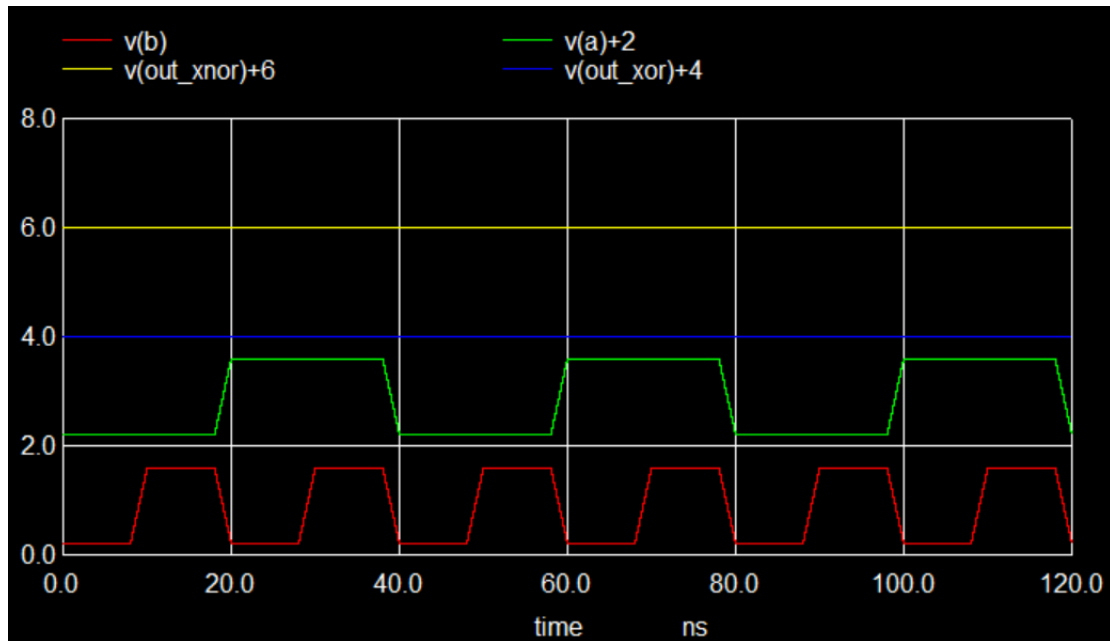


Figure 12: Input and output waveforms of CPL XOR gate after pull up PMOS with 4 times the minimum width

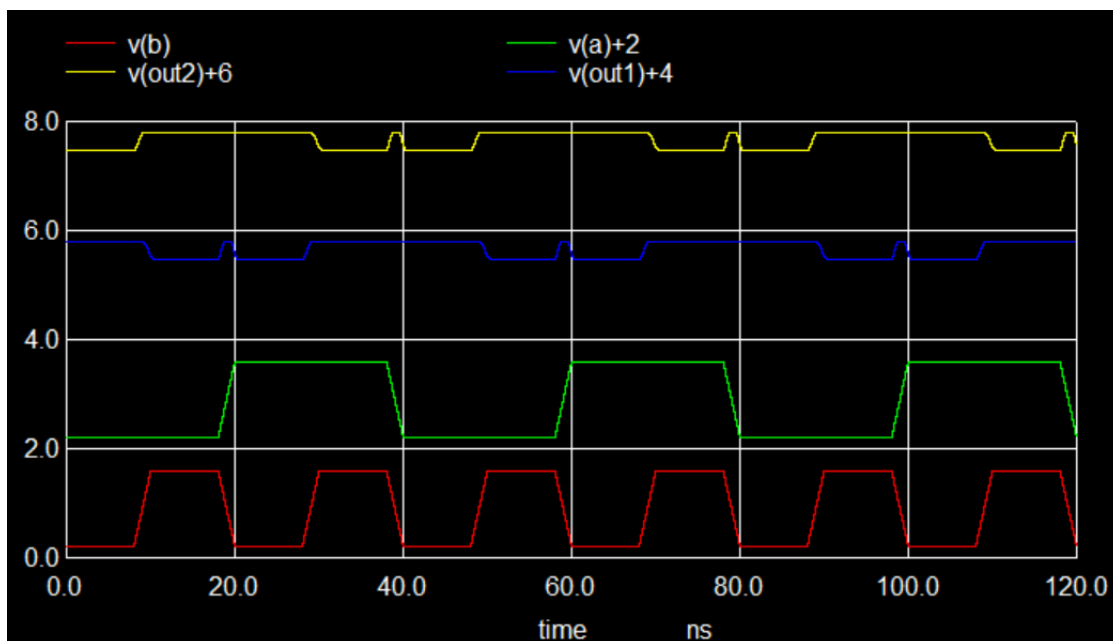


Figure 13: Voltages at output of switch matrix

- $I_{avg} = -111.565\mu A$  (-ve sign indicates current is being drawn from Vdd)
- The PMOS, being large, keeps the input of inverters permanently at almost Vdd, resulting in a constant 0 output at inverter.



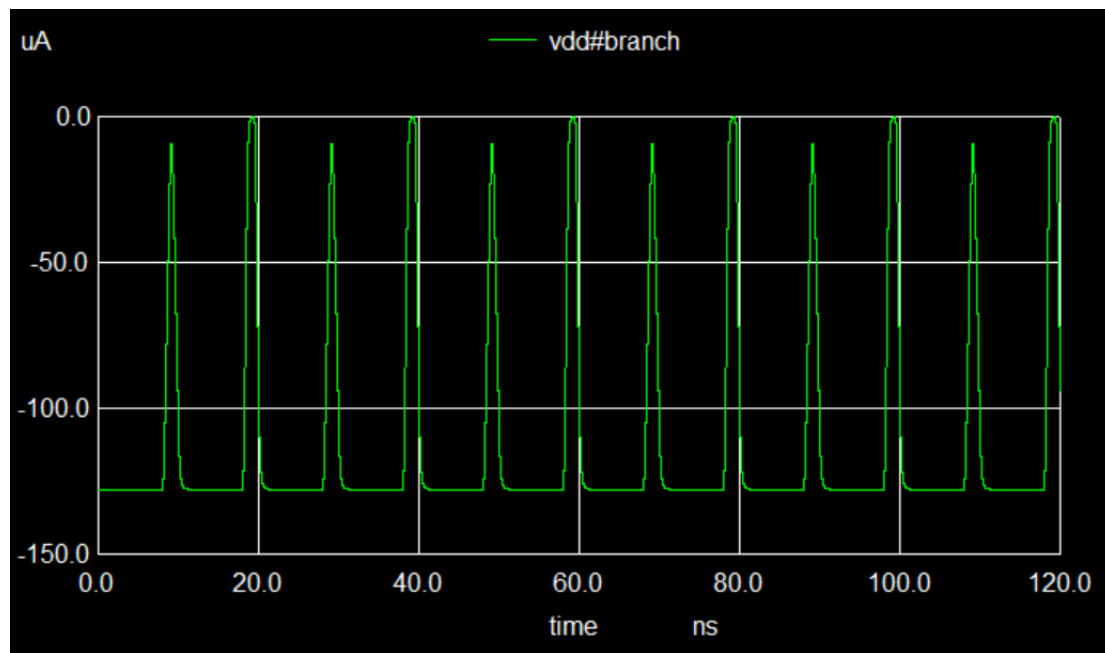


Figure 14: Current waveform

- The current is almost always high since it is essentially pseudo NMOS, and the pullup PMOS is always on along with the NMOS in switch matrix.

## Question 2

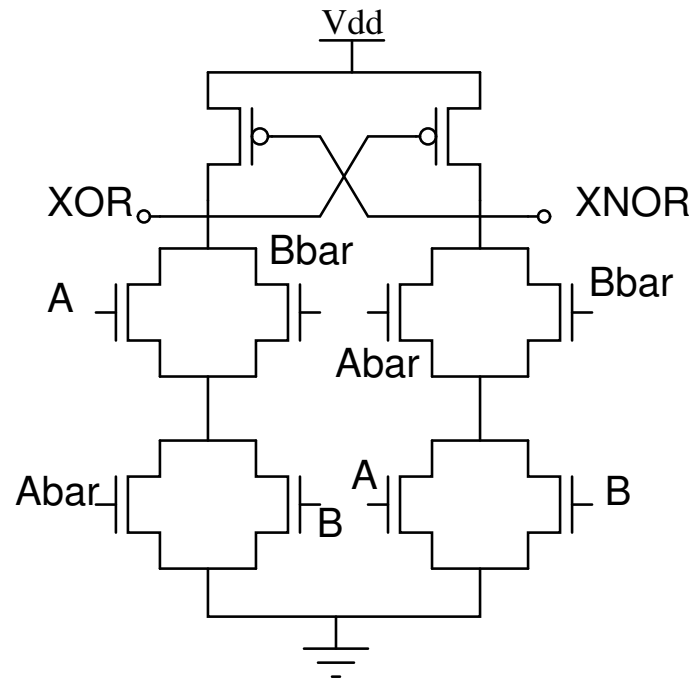


Figure 15: Circuit diagram

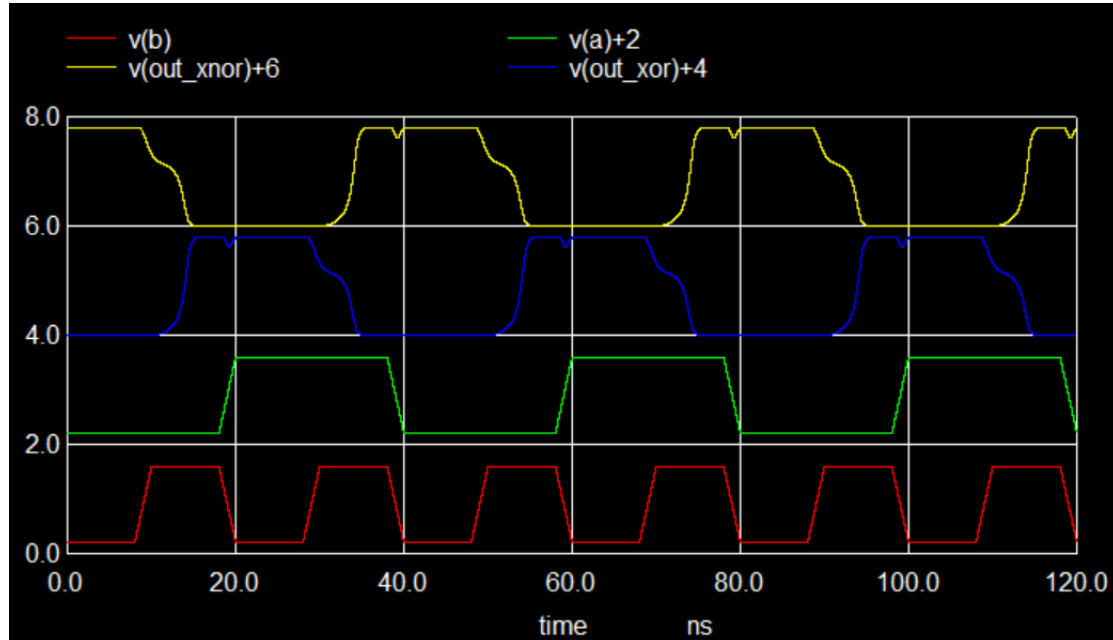


Figure 16: Input and output waveforms of CVSL XOR

- We see that the outputs are XOR and XNOR of inputs A and B.
- The NMOS transistors are all doubled in accordance to series parallel rules.

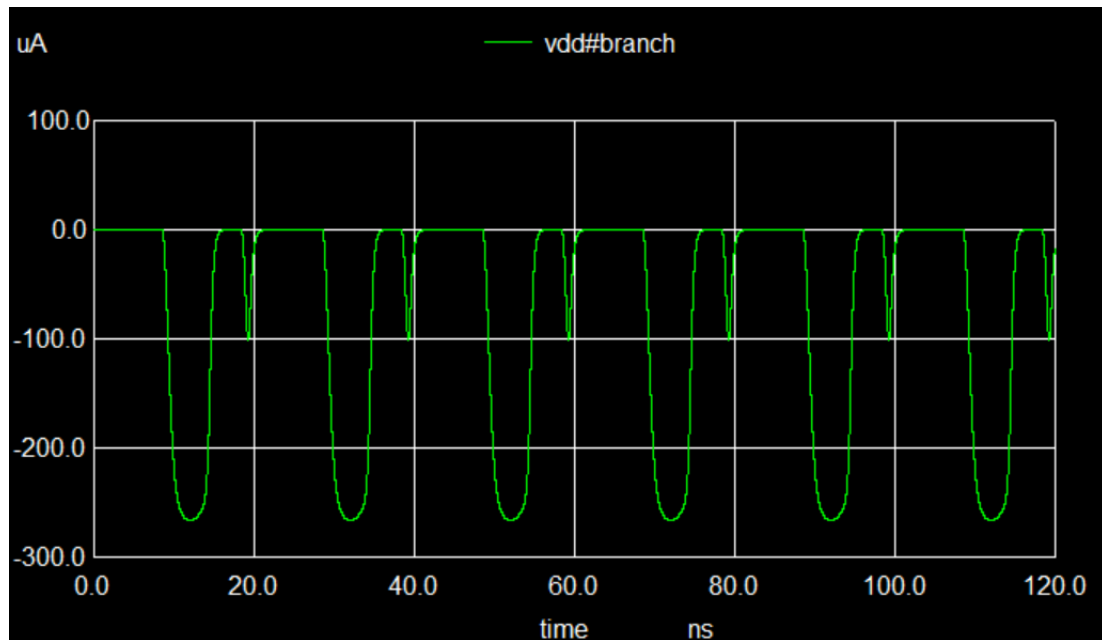


Figure 17: Current waveform

```

1 *CPL XOR
2 * Unit Inverter
3 .subckt inv supply Inp Output
4
5 .param Len = 0.18U
6 .param Wp = 1.275U Wn = 0.407U
7 .param Area_p = {2*Len*Wp} Area_n = {2*Len*Wn}
8 .param Per_p = {2*(Wp + 2*Len)} Per_n = {2*(Wn + 2*Len)}
9
10 MP1 Output Inp Supply Supply cmosp
11 + L = Len W = Wp AD = Area_p AS = Area_p PD = Per_p PS = Per_p
12 MN1 Output Inp 0 0 cmosn
13 + L = Len W = Wn AD = Area_n AS = Area_n PD = Per_n PS = Per_n
14 .ends
15
16
17 * Switch Matrix
18 .subckt swmat In1 In2 In3 In4 con conbar Out1 Out2
19 MN1 In1 con Out1 0 cmosn
20 + L=0.18U W=0.24U AD = 86.4fF AS = 86.4fF PD = 1.2U PS = 1.2U
21 MN2 In2 conbar Out1 0 cmosn
22 + L=0.18U W=0.24U AD = 86.4fF AS = 86.4fF PD = 1.2U PS = 1.2U
23 MN3 In3 con Out2 0 cmosn
24 + L=0.18U W=0.24U AD = 86.4fF AS = 86.4fF PD = 1.2U PS = 1.2U
25 MN4 In4 conbar Out2 0 cmosn
26 + L=0.18U W=0.24U AD = 86.4fF AS = 86.4fF PD = 1.2U PS = 1.2U
27 * Loads representing wiring capacitance
28 C1 Out1 0 50fF
29 C2 Out2 0 50fF
30 .ends
31
32 vdd supply 0 dc 1.8
33
34 * Device under test

```

```

35 x_swmat B Bbar Bbar B A Abar Out1 Out2 swmat
36 x_inv1 supply Out1 out_xor inv
37 x_inv2 supply Out2 out_xnor inv
38
39 * Load Capacitor
40 C3 out_xor 0 154f
41 C4 out_xnor 0 154f
42
43 .param Trep1= 40n
44 .param Trep2 = {Trep1/2.0}
45 .param Trf = {Trep1/20.0}
46 .param Tw1 = {Trep1/2.0 - Trf}
47 .param Tw2 = {Trep2/2.0 - Trf}
48 .param hival=1.6
49 .param loval=0.2
50 V1 A 0 DC 0 PULSE({loval} {hival} {Tw1} {Trf} {Trf} {Tw1} {Trep1})
51 V2 Abar 0 DC 0 PULSE({hival} {loval} {Tw1} {Trf} {Trf} {Tw1} {Trep1})
52 V3 B 0 DC 0 PULSE({loval} {hival} {Tw2} {Trf} {Trf} {Tw2} {Trep2})
53 V4 Bbar 0 DC 0 PULSE({hival} {loval} {Tw2} {Trf} {Trf} {Tw2} {Trep2})
54
55 .tran 1pS {3*Trep1} 0nS
56
57 .include models-180nm
58 .control
59 run
60 plot V(A)+2 V(B) V(out_xor)+4 V(out_xnor)+6
61 plot V(A)+2 V(B) V(out1)+4 V(out2)+6
62 plot vdd#branch
63 let i_vdd = vdd#branch
64 let t1 = 0ns
65 let t2 = 120ns
66 meas tran i_avg AVG i_vdd from = t1 to = t2
67 print i_avg
68 .endc
69 .options savecurrents
70 .end

```

```

1 * Unit Inverter
2 .subckt inv supply Inp Output
3
4 .param Len = 0.18U
5 .param Wp = 1.275U Wn = 0.407U
6 .param Area_p = {2*Len*Wp} Area_n = {2*Len*Wn}
7 .param Per_p = {2*(Wp + 2*Len)} Per_n = {2*(Wn + 2*Len)}
8
9 MP1 Output Inp Supply Supply cmosp
10 + L = Len W = Wp AD = Area_p AS = Area_p PD = Per_p PS = Per_p
11 MN1 Output Inp 0 0 cmosn
12 + L = Len W = Wn AD = Area_n AS = Area_n PD = Per_n PS = Per_n
13 .ends
14
15
16 * Switch Matrix
17 .subckt swmat In1 In2 In3 In4 con conbar Out1 Out2
18 MN1 In1 con Out1 0 cmosn
19 + L=0.18U W=0.24U AD = 86.4fF AS = 86.4fF PD = 1.2U PS = 1.2U
20 MN2 In2 conbar Out1 0 cmosn
21 + L=0.18U W=0.24U AD = 86.4fF AS = 86.4fF PD = 1.2U PS = 1.2U

```

```

22 MN3 In3 con Out2 0 cmosn
23 + L=0.18U W=0.24U AD = 86.4fF AS = 86.4fF PD = 1.2U PS = 1.2U
24 MN4 In4 conbar Out2 0 cmosn
25 + L=0.18U W=0.24U AD = 86.4fF AS = 86.4fF PD = 1.2U PS = 1.2U
26 * Loads representing wiring capacitance
27 C1 Out1 0 50fF
28 C2 Out2 0 50fF
29 .ends
30
31 vdd supply 0 dc 1.8
32
33 * Device under test
34 x_swmat B Bbar Bbar B A Abar Out1 Out2 swmat
35 x_inv1 supply Out1 out_xor inv
36 x_inv2 supply Out2 out_xnor inv
37
38 * Load Capacitor
39 C3 out_xor 0 154f
40 C4 out_xnor 0 154f
41
42 .param Len = 0.18U
43 .param Wp = 0.24U
44 .param Area_p = {2*Len*Wp}
45 .param Per_p = {2*(Wp + 2*Len)}
46
47 mp_out1 Out1 out_xor supply supply cmosp
48 + L = Len W = Wp AD = Area_p AS = Area_p PD = Per_p PS = Per_p
49
50 mp_out2 Out2 out_xnor supply supply cmosp
51 + L = Len W = Wp AD = Area_p AS = Area_p PD = Per_p PS = Per_p
52
53 .param Trep1= 40n
54 .param Trep2 = {Trep1/2.0}
55 .param Trf = {Trep1/20.0}
56 .param Tw1 = {Trep1/2.0 - Trf}
57 .param Tw2 = {Trep2/2.0 - Trf}
58 .param hival=1.6
59 .param loval=0.2
60 V1 A 0 DC 0 PULSE({loval} {hival} {Tw1} {Trf} {Trf} {Tw1} {Trep1})
61 V2 Abar 0 DC 0 PULSE({hival} {loval} {Tw1} {Trf} {Trf} {Tw1} {Trep1})
62 V3 B 0 DC 0 PULSE({loval} {hival} {Tw2} {Trf} {Trf} {Tw2} {Trep2})
63 V4 Bbar 0 DC 0 PULSE({hival} {loval} {Tw2} {Trf} {Trf} {Tw2} {Trep2})
64
65 .tran 1pS {3*Trep1} 0nS
66
67 .include models-180nm
68 .control
69 run
70 plot V(A)+2 V(B) V(out_xor)+4 V(out_xnor)+6
71 plot V(A)+2 V(B) V(out1)+4 V(out2)+6
72 plot vdd#branch
73 let i_vdd = vdd#branch
74 let t1 = 0ns
75 let t2 = 120ns
76 meas tran i_avg AVG i_vdd from = t1 to = t2
77 print i_avg
78 .endc
79 .options savecurrents

```

```

80 .end

1 * Unit Inverter
2 .subckt inv supply Inp Output
3
4 .param Len = 0.18U
5 .param Wp = 1.275U Wn = 0.407U
6 .param Area_p = {2*Len*Wp} Area_n = {2*Len*Wn}
7 .param Per_p = {2*(Wp + 2*Len)} Per_n = {2*(Wn + 2*Len)}
8
9 MP1 Output Inp Supply Supply cmosp
10 + L = Len W = Wp AD = Area_p AS = Area_p PD = Per_p PS = Per_p
11 MN1 Output Inp 0 0 cmosn
12 + L = Len W = Wn AD = Area_n AS = Area_n PD = Per_n PS = Per_n
13 .ends
14
15
16 * Switch Matrix
17 .subckt swmat In1 In2 In3 In4 con conbar Out1 Out2
18 MN1 In1 con Out1 0 cmosn
19 + L=0.18U W=0.24U AD = 86.4fF AS = 86.4fF PD = 1.2U PS = 1.2U
20 MN2 In2 conbar Out1 0 cmosn
21 + L=0.18U W=0.24U AD = 86.4fF AS = 86.4fF PD = 1.2U PS = 1.2U
22 MN3 In3 con Out2 0 cmosn
23 + L=0.18U W=0.24U AD = 86.4fF AS = 86.4fF PD = 1.2U PS = 1.2U
24 MN4 In4 conbar Out2 0 cmosn
25 + L=0.18U W=0.24U AD = 86.4fF AS = 86.4fF PD = 1.2U PS = 1.2U
26 * Loads representing wiring capacitance
27 C1 Out1 0 50fF
28 C2 Out2 0 50fF
29 .ends
30
31 vdd supply 0 dc 1.8
32
33 * Device under test
34 x_swmat B Bbar Bbar B A Abar Out1 Out2 swmat
35 x_inv1 supply Out1 out_xor inv
36 x_inv2 supply Out2 out_xnor inv
37
38 * Load Capacitor
39 C3 out_xor 0 154f
40 C4 out_xnor 0 154f
41
42 .param Len = 0.18U
43 .param Wp = 0.24U
44 .param Area_p = {2*Len*Wp}
45 .param Per_p = {2*(Wp + 2*Len)}
46
47 mp_out1 Out1 out_xor supply supply cmosp
48 + L = Len W = Wp AD = Area_p AS = Area_p PD = Per_p PS = Per_p
49
50 mp_out2 Out2 out_xnor supply supply cmosp
51 + L = Len W = Wp AD = Area_p AS = Area_p PD = Per_p PS = Per_p
52
53 .param Trep1= 40n
54 .param Trep2 = {Trep1/2.0}
55 .param Trf = {Trep1/20.0}
56 .param Tw1 = {Trep1/2.0 - Trf}

```

```

57 .param Tw2 = {Trep2/2.0 - Trf}
58 .param hival=1.6
59 .param loval=0.2
60 V1 A 0 DC 0 PULSE({loval} {hival} {Tw1} {Trf} {Trf} {Tw1} {Trep1})
61 V2 Abar 0 DC 0 PULSE({hival} {loval} {Tw1+2ns} {Trf} {Trf} {Tw1} {Trep1}
    })
62 V3 B 0 DC 0 PULSE({loval} {hival} {Tw2} {Trf} {Trf} {Tw2} {Trep2})
63 V4 Bbar 0 DC 0 PULSE({hival} {loval} {Tw2+2ns} {Trf} {Trf} {Tw2} {Trep2}
    })
64
65 .tran 1pS {3*Trep1} 0nS
66
67 .include models-180nm
68 .control
69 run
70 plot V(A)+2 V(B) V(out_xor)+4 V(out_xnor)+6
71 plot V(A)+2 V(B) V(out1)+4 V(out2)+6
72 plot vdd#branch
73 let i_vdd = vdd#branch
74 let t1 = 0ns
75 let t2 = 120ns
76 meas tran i_avg AVG i_vdd from = t1 to = t2
77 print i_avg
78 .endc
79 .options savecurrents
80 .end

```

```

1 * Unit Inverter
2 .subckt inv supply Inp Output
3
4 .param Len = 0.18U
5 .param Wp = 1.275U Wn = 0.407U
6 .param Area_p = {2*Len*Wp} Area_n = {2*Len*Wn}
7 .param Per_p = {2*(Wp + 2*Len)} Per_n = {2*(Wn + 2*Len)}
8
9 MP1 Output Inp Supply Supply cmosp
10 + L = Len W = Wp AD = Area_p AS = Area_p PD = Per_p PS = Per_p
11 MN1 Output Inp 0 0 cmosn
12 + L = Len W = Wn AD = Area_n AS = Area_n PD = Per_n PS = Per_n
13 .ends
14
15
16 * Switch Matrix
17 .subckt swmat In1 In2 In3 In4 con conbar Out1 Out2
18 MN1 In1 con Out1 0 cmosn
19 + L=0.18U W=0.24U AD = 86.4fF AS = 86.4fF PD = 1.2U PS = 1.2U
20 MN2 In2 conbar Out1 0 cmosn
21 + L=0.18U W=0.24U AD = 86.4fF AS = 86.4fF PD = 1.2U PS = 1.2U
22 MN3 In3 con Out2 0 cmosn
23 + L=0.18U W=0.24U AD = 86.4fF AS = 86.4fF PD = 1.2U PS = 1.2U
24 MN4 In4 conbar Out2 0 cmosn
25 + L=0.18U W=0.24U AD = 86.4fF AS = 86.4fF PD = 1.2U PS = 1.2U
26 * Loads representing wiring capacitance
27 C1 Out1 0 50fF
28 C2 Out2 0 50fF
29 .ends
30
31 vdd supply 0 dc 1.8

```

```

32
33 * Device under test
34 x_swmat B Bbar Bbar B A Abar Out1 Out2 swmat
35 x_inv1 supply Out1 out_xor inv
36 x_inv2 supply Out2 out_xnor inv
37
38 * Load Capacitor
39 C3 out_xor 0 154f
40 C4 out_xnor 0 154f
41
42 .param Len = 0.18U
43 .param Wp = 0.96U
44 .param Area_p = {2*Len*Wp}
45 .param Per_p = {2*(Wp + 2*Len)}
46
47 mp_out1 Out1 out_xor supply supply cmosp
48 + L = Len W = Wp AD = Area_p AS = Area_p PD = Per_p PS = Per_p
49
50 mp_out2 Out2 out_xnor supply supply cmosp
51 + L = Len W = Wp AD = Area_p AS = Area_p PD = Per_p PS = Per_p
52
53 .param Trep1= 40n
54 .param Trep2 = {Trep1/2.0}
55 .param Trf = {Trep1/20.0}
56 .param Tw1 = {Trep1/2.0 - Trf}
57 .param Tw2 = {Trep2/2.0 - Trf}
58 .param hival=1.6
59 .param loval=0.2
60 V1 A 0 DC 0 PULSE({loval} {hival} {Tw1} {Trf} {Trf} {Tw1} {Trep1})
61 V2 Abar 0 DC 0 PULSE({hival} {loval} {Tw1} {Trf} {Trf} {Tw1} {Trep1})
62 V3 B 0 DC 0 PULSE({loval} {hival} {Tw2} {Trf} {Trf} {Tw2} {Trep2})
63 V4 Bbar 0 DC 0 PULSE({hival} {loval} {Tw2} {Trf} {Trf} {Tw2} {Trep2})
64
65 .tran 1pS {3*Trep1} 0nS
66
67 .include models-180nm
68 .control
69 run
70 plot V(A)+2 V(B) V(out_xor)+4 V(out_xnor)+6
71 plot V(A)+2 V(B) V(out1)+4 V(out2)+6
72 plot vdd#branch
73 let i_vdd = vdd#branch
74 let t1 = 0ns
75 let t2 = 120ns
76 meas tran i_avg AVG i_vdd from = t1 to = t2
77 print i_avg
78 .endc
79 .options savecurrents
80 .end

```

```

1 *CVSL Half Ckt
2 .subckt halfckt g x y z w Supply out
3
4 .param Len = 0.18U
5 .param Wp = 1.275U Wn = 0.814U
6 .param Area_p = {2*Len*Wp} Area_n = {2*Len*Wn}
7 .param Per_p = {2*(Wp + 2*Len)} Per_n = {2*(Wn + 2*Len)}
8

```



```

9 MP1 out g Supply Supply cmosp
10 + L = Len W = Wp AD = Area_p AS = Area_p PD = Per_p PS = Per_p
11 MNx out x out1 0 cmosn
12 + L = Len W = Wn AD = Area_n AS = Area_n PD = Per_n PS = Per_n
13 MNy out y out1 0 cmosn
14 + L = Len W = Wn AD = Area_n AS = Area_n PD = Per_n PS = Per_n
15 MNz out1 z 0 0 cmosn
16 + L = Len W = Wn AD = Area_n AS = Area_n PD = Per_n PS = Per_n
17 MNw out1 w 0 0 cmosn
18 + L = Len W = Wn AD = Area_n AS = Area_n PD = Per_n PS = Per_n
19 .ends
20
21 vdd supply 0 dc 1.8
22 x1 out_xnor A Bbar Abar B Supply out_xor halfckt
23 x2 out_xor Abar Bbar A B Supply out_xnor halfckt
24
25 * Load Capacitor
26 C3 out_xor 0 154f
27 C4 out_xnor 0 154f
28
29 .param Len = 0.18U
30 .param Wp = 0.96U
31 .param Area_p = {2*Len*Wp}
32 .param Per_p = {2*(Wp + 2*Len)}
33
34 .param Trep1= 40n
35 .param Trep2 = {Trep1/2.0}
36 .param Trf = {Trep1/20.0}
37 .param Tw1 = {Trep1/2.0 - Trf}
38 .param Tw2 = {Trep2/2.0 - Trf}
39 .param hival=1.6
40 .param loval=0.2
41 V1 A 0 DC 0 PULSE({loval} {hival} {Tw1} {Trf} {Trf} {Tw1} {Trep1})
42 V2 Abar 0 DC 0 PULSE({hival} {loval} {Tw1} {Trf} {Trf} {Tw1} {Trep1})
43 V3 B 0 DC 0 PULSE({loval} {hival} {Tw2} {Trf} {Trf} {Tw2} {Trep2})
44 V4 Bbar 0 DC 0 PULSE({hival} {loval} {Tw2} {Trf} {Trf} {Tw2} {Trep2})
45
46 .tran 1pS {3*Trep1} 0nS
47
48 .include models-180nm
49 .control
50 run
51 plot V(A)+2 V(B) V(out_xor)+4 V(out_xnor)+6
52 plot vdd#branch
53 let i_vdd = vdd#branch
54 let t1 = 0ns
55 let t2 = 120ns
56 meas tran i_avg AVG i_vdd from = t1 to = t2
57 print i_avg
58 .endc
59 .options savecurrents
60 .end

```