Sai Saketika Chekuri

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Education

Indian Institute of Technology Bombay *Mumbai, India*
Bachelor of Technology in Electrical Engineering with Honors *[Jul. 2019 - Present]*

- **CGPA - 9.89/10**
- Ranked **1st** in the Electrical Engineering Department out of 164 students

Academic Achievements

- Extended a **full-time offer** as Silicon Engineer by **Google** on the basis of internship performance *[2022]*
- Awarded an **AP** grade (given to the top 2% of students) in 3 courses at IITB - **Mixed Signal VLSI Design**, **Analog Circuits** and **Electronic Devices** *[2020-22]*
- Recipient of the **OPJEMS** scholarship awarded to 80 engineering students in the country based on academic, entrepreneurial, and leadership potential *[2021]*
- Received **Urvish Medh** and **Aditya Choubey Memorial Prizes** for ranking 1st in the department *[2020]*
- Conferred with **Institute Academic Prize** for ranking 10th in the institute in first year *[2020]*
- Secured an **All India Rank** of **407** in JEE (Main) and **All India Rank** of **716** in JEE (Advanced) *[2020]*
- Ranked **1st** in the Common Entrance Test conducted by the state government of Karnataka *[2019]*
- Secured an **All India Rank** of **1** in VITEEE examination conducted by Vellore Institute of Technology *[2019]*
- Selected for the **KVPY** fellowship administered by **Indian Institute of Science** and the Department of Science and Technology of India by securing an **All India Rank** of **159** in SX stream and **418** in SA stream *[2018-19]*
- Selected as a **Japan-Asia Youth Exchange Student** by the Government of India to represent the country in **Sakura Science Program** organized by the Japan Science and Technology Agency *[2018]*
- Awarded the **National Talent Search** Scholarship by Government of India, with **Karnataka Rank 1** *[2017]*

Research Projects

Logarithmic SAR Analog to Digital Converter Design *[Jul. 2022 - Present]*
Prof. Rajesh Zele, EE, IITB | Bachelor's Project

- Conducted literature review and studied Cadence Rapid Adoption Kits (RAKs) to understand efficient design flow of low-power linear SAR ADC, and adapting it to implement **logarithmic quantization**
- Ideated an **area-efficient** SAR-based Logarithmic ADC topology with **high dynamic range** applications
- Implemented a novel algorithm with an optimum number of capacitors on MATLAB and verified proof of concept; introduced stochastic variations in the capacitor bank to ensure **INL**, **DNL** considerations are met
- Working on Cadence Virtuoso to create a schematic-level design and perform simulations

Two-Stage Differential OTA with Positive Feedback Compensation *[Jan. 2022 - May 2022]*
Prof. Rajesh Zele, EE, IITB | Research Project

- Designed an OTA in GPDK 45 nm on Cadence Virtuoso with 121 dB gain, 79 MHz unity gain bandwidth
- Employed **integrated active RC filters** in positive feedback to cancel a pole with generated LHP zero
- Obtained $3\times$ gain-bandwidth product and $7°$ higher phase margin than Miller compensation at 0.42 mW
- Performed TT, SS, FF **process corner** simulations to verify results over a range of temperatures

Variability in Memory Peripheral Circuits *[Jul. 2022 - Present]*
Prof. Souvik Mahapatra, EE, IITB | Research Project

- Performed HSpice simulations on circuits such as Sense Amplifier, 6T SRAM Cell with **Hot Carrier Degradation** and **Negative Bias Temperature Instability** effects to compute **threshold voltage shift**
- Observed effect of transistor-wise degradation on Read and Hold Static Noise Margins, and Flip Time in **6T SRAM Cell** using HSpice and CARAT simulation tools
- Analysed correlation of number of stages of **Ring Oscillator** with BTI, HCD aging due to interface traps

INTERNSHIPS

Formal Verification of UART Virtualization feature *[May 2022 - Jul. 2022]*

Google India | Summer Internship, Hardware Engineering Intern

- Wrote **glue logic** in SystemVerilog to serialize data from AXI Stream to UART protocol and vice versa for **virtualization** and **arbitration** in the debug hub between system CPU and AXI Stream interface
- Wrote testbenches for baud clock generator, UART FSMs, Bus Handler packetizers and packet decoders to perform formal verification using the **Cadence JasperGold** tool and integrated with functional testbenches

Bus Analyzer Tool *[May 2021 - Jul. 2021]*

Google India | Summer Internship, STEP (Student Training in Engineering Program) Intern

- Developed an **off-time tool** for SoC to analyze all **NoC interfaces** using the AXI-4 protocol
- Generated a statistical and analytical report for entire system using the raw transaction data of fabric interfaces, including inferences about timing-related parameters and critical transaction attributes
- Developed a web application using **Flask API**, **CSS**; presented results via interactive graphs using Chart.js

KEY TECHNICAL PROJECTS

8-bit Segmented Current Steering Digital to Analog Converter *[Jan. 2022 - Apr. 2022]*

Prof. Rajesh Zele, EE, IITB | Mixed-Signal VLSI Design (EE 719) Course Project

- Designed a DAC operating at **1 GSps** sampling frequency in GPDK 45 nm on Cadence Virtuoso
- Designed cascode current source biasing circuit, digital input driver for unit cell at transistor level, and integrated the scaled **thermometer cells** and digital decoder to implement the DAC from end-to-end
- Performed **Monte Carlo** and **FFT** simulations; achieved 50 dB SFDR, $<$ 1 LSB INL, and $<$ 0.5 LSB DNL
- Performed **LVS** and **DRC** checks on layout to meet design specifications after **parasitic extraction**

CMOS Reliability Modelling *[Aug. 2022 - Nov. 2022]*

Prof. Souvik Mahapatra, EE, IITB | Advanced CMOS Logic Devices (EE 788) Course Project

- Fabricated and scaled MOSFETs on TCAD to observe **DIBL**, **Subthreshold Swing**, $\mathbf{V_{th}}$ and $\mathbf{I_{off}}$ trends
- Simulated effects of lateral and vertical electric field to find **mobility degraded** I-V characteristics
- Characterized MOSFETs using Pao-Sah, Brews and Piecewise Linear models on MATLAB
- Fit device threshold voltage NBTI shift vs time data to find the **Interface**, **Hole** and **Bulk trap** components of voltage acceleration, power law time exponent and Arrhenius temperature activation factors

Common Source Low Noise Amplifier *[Jan. 2022 - Apr. 2022]*

Prof. Jayanta Mukherjee, EE, IITB | RF Microelectronics (EE 619) Course Project

- Designed a single-ended CS-LNA in UMC 180 nm on Cadence Virtuoso for operation in **2.3-2.4 GHz** range
- Utilized a cascoded configuration with **inductive degeneration**; matched impedances at 50 Ω and achieved 11 dBm IIP_3, noise figure $<$ 0.6 dB, forward voltage gain $>$ 15 dB, voltage reflection coefficients $<$ -12 dB

20 MHz Receiver Frontend PCB for POF Data Communications *[Jan. 2022 - Apr. 2022]*

Prof. Joseph John, EE, IITB | Electronics Design Lab (EE 344) Project

- Designed a 3-device **low-noise** transimpedance amplifier for use in plastic optical fiber communication
- Cascaded CS JFET and CE BJTs in a **closed-loop** configuration for 200 kΩ gain at frequencies up to 2 MHz

Pipelined RISC Processor Design *[Jan. 2022 - Apr. 2022]*

Prof. Virendra Singh, EE, IITB | Processor Design (EE 739) Course Project

- Designed a 6-stage, 8-register, 16-bit pipelined **mini-8085** RISC processor written in VHDL
- Optimized performance using **branch prediction**, **hazard mitigation**, and **data forwarding** techniques

VLSI Circuits *[Aug. 2022 - Nov. 2022]*

Prof. Dinesh Sharma, EE, IITB | VLSI Design (EE 671) Course Project

- Designed a 16-bit **Multiply and Accumulate Circuit** with 8x8 **Dadda** multiplication scheme on VHDL, implementing a 16-bit **Brent Kung** logarithmic adder for final addition
- Designed and analyzed logic gates using static CMOS, pseudo-NMOS, CVSL and CPL design styles

Slew Rate Boosted OTA *[Aug. 2021 - Nov. 2021]*

Prof. Maryam Baghini, EE, IITB | CMOS Analog VLSI Design (EE 618) Course Project

- Designed an OTA with auxiliary class-B **SR Boosting** Circuit using PTM 130 nm technology on Ngspice
- Implemented a 2-stage **telescopic cascoded** design with **common mode feedback** and frequency compensation techniques to obtain 71 dB gain, 66° phase margin, and 900 $V/\mu s$ slew rate for 5 pF load

Adaptive Control of Spacecraft with Reaction Wheels *[Aug. 2021 - Nov. 2021]*

Prof. Srikant Sukumar, SysCon, IITB | Adaptive Control (SC 617) Course Project

- Defined the **state space equations** and **tracking objectives** of a spacecraft with three reaction wheels
- Used adaptive control techniques such as **Signal Chasing** arguments and **Certainty Equivalence principle** to show convergence of dynamical system to desired orientation; verified results using MATLAB simulations

Technical Skills and Key Courses

- **Analog**: Mixed-Signal VLSI Design, CMOS Analog VLSI Design, Radio Frequency Microelectronics Chip Design
- **VLSI**: Advanced CMOS Logic and Flash Memory Devices, VLSI Design, Processor Design, Algorithmic Design of Digital Systems, Microprocessors
- **Controls**: Adaptive Control Theory, Mathematical Structures for Control, Control Systems
- **Miscellaneous**: Markov Chains and Queueing Systems, Error Correcting Codes, Communication Systems, Programming for Data Science, Electromagnetic Waves
- **Software**: Cadence Virtuoso, Cadence JasperGold, Sentaurus TCAD, Intel Quartus, EAGLE, GNU Radio, Keil
- **Programming**: Python, C++, MATLAB, VHDL, Verilog, Spice, Assembly, Embedded C, Arduino, LaTeX

Leadership Positions

Institute and Department Academic Mentor | *Student Mentorship Program* *[Jun. 2021 - Jun. 2022]*

- One among 13 third-year students selected based on a rigorous interview process and peer reviews
- Mentored **12 freshmen** and **4 sophomores** by guiding in academic and extracurricular endeavors
- Conducted **tutorials** and **doubt-solving sessions** for Analog Circuits and Power Engineering courses

Institute Academic Coordinator | *Student Support Services* *[Apr. 2020 - May 2021]*

- Among 12 selected out of 120+ applicants, addressing academic queries of 4500+ undergraduates
- Organized 20+ **Tutorial Service Center** sessions for 1200+ undergraduate freshmen and sophomores
- Compiled **Information Booklets** to ensure student awareness about institute academic policies

Core Team Member | *Electronics and Robotics Club* *[Apr. 2020 - May 2021]*

- Part of a 15 member team that aims to disseminate practical knowledge through technical hobby-activities
- Conducted **Arduino**, **Control Theory** bootcamps; contributed to **ERC Wiki** by writing articles on PID Control and Signal Processing
- Coordinated BLAH sessions where prominent alumni and students deliver talks on technical topics

Extracurriculars

- Part of **Hyperloop IITB** tech-team as a Junior Controls and Communication Engineer; qualified in the **top 5** university teams internationally for the finals of the **European Hyperloop Week** (EHW 2021)
- Won **Best Design Award** in **RC Plane competition** held by Aeromodelling Club, IIT Bombay: a remote controlled plane making competition using BLDC and servo motors for wing control
- Engineered an all-terrain **obstacle-maneuvering bot** controlled using a mobile application
- Completed one year of training in **Badminton** under **National Sports Organization** at IIT Bombay
- Participated in various state and district level competitions in roller skating, taekwondo, and painting