Sai Saketika Chekuri

Graduate Student at Stanford University

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Education

Stanford University *Stanford, USA*
Master of Science in Electrical Engineering, Specialization - Circuits *[Sep. 2023 - Jun. 2025]*

Indian Institute of Technology Bombay *Mumbai, India*
Bachelor of Technology in Electrical Engineering with Honors *[Jul. 2019 - Aug. 2023]*

- **CGPA - 9.91/10**; Department Rank 1 amongst 164 students - **Institute Silver Medalist**
- Received the **Sharad Maloo Gold Medal** for being the most outstanding student of the graduating batch in terms of academic performance and extracurricular activities
- Conferred the **Prof. K. C. Mukherjee** Award for the best undergraduate thesis in the department and the **Ramesh Chandra Sinha Academic Excellence** Award for being the best-performing woman student

Academic Achievements

- Extended a **full-time offer** as Silicon Engineer by **Google** on the basis of internship performance *[2022]*
- Awarded an **AP** grade (given to the top 2% of students) in 3 courses at IITB - **Mixed Signal VLSI Design**, **Analog Circuits** and **Electronic Devices** *[2020-22]*
- Among top 60 students in the country to receive the **K.C Mahindra** scholarship for higher studies *[2023]*
- Recipient of the **J.N. Tata Endowment** merit scholarship, among top 100 students in the country *[2023]*
- Received **Narotam Sekhsaria** undergraduate scholarship based on academic and leadership merit *[2023]*
- Conferred the **Academic Excellence** award in the EE department Valedictory function at IITB *[2023]*
- Recipient of the **OPJEMS** scholarship based on academic, entrepreneurial, and leadership potential, awarded to 80 engineering students in the country *[2021]*
- Received **Urvish Medh** and **Aditya Choubey Memorial Prizes** for ranking 1st in the department *[2020]*
- Conferred with **Institute Academic Prize** for ranking 10th in the institute *[2020]*
- Secured an **All India Rank** of **407** in JEE (Main) and **All India Rank** of **716** in JEE (Advanced) *[2020]*
- Ranked **1st** in the Common Entrance Test conducted by the state government of Karnataka *[2019]*
- Secured **All India Rank** of **1** in VITEEE examination conducted by Vellore Institute of Technology *[2019]*
- Selected for the **KVPY** fellowship administered by **Indian Institute of Science** and the Department of Science and Technology of India by securing an **All India Rank** of **159** in SX stream and **418** in SA stream *[2018-19]*
- Selected as a **Japan-Asia Youth Exchange Student** by the Government of India to represent the country in **Sakura Science Program** organized by the Japan Science and Technology Agency *[2018]*
- Awarded the **National Talent Search** Scholarship by Government of India, with **Karnataka Rank 1** *[2017]*

Research Projects

Logarithmic SAR Analog to Digital Converter Design *[Aug. 2022 - Present]*
Prof. Rajesh Zele, EE, IITB | Bachelor's Project

- Ideated a novel area-efficient SAR-based Logarithmic ADC topology with high dynamic range applications
- Designed a 5-bit differential Logarithmic SAR ADC on Cadence Virtuoso with 55 dB dynamic range, 4.6 mW power consumption; designed bootstrapped switch, bias generator, OTA and error amplifier circuit blocks

Two-Stage Differential OTA with Positive Feedback Compensation *[Jan. 2022 - May 2022]*
Prof. Rajesh Zele, EE, IITB | Research Project

- Designed a schematic of low-power high-gain OTA in GPDK 45 nm on Cadence Virtuoso
- Employed integrated active RC filters in positive feedback to cancel a pole with generated LHP zero
- Performed SS, TT, FF process corner simulations to verify results over a range of temperatures
- Obtained higher phase margin than Miller compensation without increasing power consumption

Variability in Memory Peripheral Circuits *[Aug. 2022 - Present]*

Prof. Souvik Mahapatra, EE, IITB | Research Project

- Performed HSpice simulations on circuits such as Sense Amplifier, 6T SRAM Cell with Hot Carrier Degradation and Negative Bias Temperature Instability effects to compute threshold voltage shift
- Observed effect of transistor-wise degradation on Read and Hold Static Noise Margins, and Flip Time in 6T SRAM Cell using HSpice and CARAT simulation tools
- Analysed correlation of the number of stages of Ring Oscillator with BTI, HCD aging due to interface traps

INTERNSHIPS

Formal Verification of UART Virtualization feature *[May 2022 - Jul. 2022]*

Google India | Summer Internship, Hardware Engineering Intern

- Wrote glue logic in SystemVerilog to serialize data from AXI Stream to UART protocol and vice versa for virtualization and arbitration in the debug hub between system CPU and AXI Stream interface
- Wrote testbenches for baud clock generator, UART FSMs, Bus Handler packetizers and packet decoders to perform formal verification using the Cadence JasperGold tool and integrated with functional testbenches

Bus Analyzer Tool *[May 2021 - Jul. 2021]*

Google India | Summer Internship, STEP (Student Training in Engineering Program) Intern

- Developed an off-time tool for SoC to analyze all NoC interfaces using the AXI-4 protocol
- Generated a statistical and analytical report for entire system using the raw transaction data of fabric interfaces, including inferences about timing related parameters and critical transaction attributes
- Developed a web application using Flask API, CSS; presented results via interactive graphs using Chart.js

KEY TECHNICAL PROJECTS

8-bit Segmented Current Steering Digital to Analog Converter *[Jan. 2022 - Apr. 2022]*

Prof. Rajesh Zele, EE, IITB | Mixed-Signal VLSI Design (EE 719) Course Project

- Designed a DAC operating at 1 GSps sampling frequency in GPDK 45 nm on Cadence Virtuoso
- Designed cascode current source biasing circuit, digital input driver for unit cell at transistor level, and integrated the scaled thermometer cells and digital decoder to implement the DAC from end-to-end
- Performed LVS and DRC checks on layout to meet design specifications after parasitic extraction

Decision Feedback Equalizer Design *[Jan. 2023 - Apr. 2023]*

Prof. Shalabh Gupta, EE, IITB | High Speed Interconnects (EE 800) Course Project

- Designed a DFE equalizer and achieved a 60% eye-opening improvement against no equalization
- Implemented a Phase Locked Loop with a Hogge phase detector for clock recovery in the DFE circuit
- Implemented the LMS algorithm in VerilogA for a 6-tap Feed Forward Equalization at the receiver for a 40% eye-opening improvement against no equalization, and characterized in Cadence Virtuoso

Delta Sigma Modulator Design *[Jan. 2023 - Apr. 2023]*

Prof. Laxmeesha Somappa, EE, IITB | Delta Sigma Data Converters (EE 699) Course Project

- Designed a Delta Sigma DAC operating at 512 MHz sampling rate for a signal bandwidth of 1 MHz
- Achieved 5.9 ENOB, 40 dB SFDR and 2.1 nV^2 input-referred noise power with 1.4 mW power consumption
- Designed OTA, comparator, bootstrapped switch on Cadence Virtuoso and integrated them in DSM loop

CMOS Reliability Modelling *[Aug. 2022 - Nov. 2022]*

Prof. Souvik Mahapatra, EE, IITB | Advanced CMOS Logic Devices (EE 788) Course Project

- Fabricated and scaled transistors on TCAD to observe correlation with Drain-Induced Barrier Lowering
- Simulated effects of lateral and vertical electric field to find mobility degraded I-V characteristics on TCAD
- Fit device threshold voltage NBTI shift vs time data to find the Interface, Hole and Bulk trap components of voltage acceleration, power law exponent and Arrhenius temperature activation factors

Common Source Low Noise Amplifier *[Jan. 2022 - Apr. 2022]*

Prof. Jayanta Mukherjee, EE, IITB | RF Microelectronics (EE 619) Course Project

- Designed a single-ended CS-LNA in UMC 180 nm technology on Cadence Virtuoso to operate at 2.4 GHz
- Utilized a cascoded configuration with inductive degeneration to meet the noise figure, IIP_3, forward voltage gain, and voltage reflection coefficients specifications with matched input and output impedance

20 MHz Receiver Frontend for POF Data Communications *[Jan. 2022 - Apr. 2022]*

Prof. Joseph John, EE, IITB | Electronics Design Lab (EE 344) Project

- Designed a 3-device low-noise transimpedance amplifier PCB for use in plastic optical fiber communication
- Cascaded CS JFET and CE BJTs in a closed-loop configuration for 200 kΩ gain at frequencies up to 2 MHz

Pipelined RISC Processor Design *[Jan. 2022 - Apr. 2022]*

Prof. Virendra Singh, EE, IITB | Processor Design (EE 739) Course Project

- Designed a 6-stage, 8-register, 16-bit pipelined mini-8085 RISC processor written in VHDL
- Optimized performance using branch prediction, hazard mitigation, and data forwarding techniques

Adaptive Control of Spacecraft with Reaction Wheels *[Aug. 2021 - Nov. 2021]*

Prof. Srikant Sukumar, SysCon, IITB | Adaptive Control (SC 617) Course Project

- Defined the state space equations and tracking objectives of a spacecraft with three reaction wheels
- Used adaptive control techniques such as Signal Chasing arguments and Certainty Equivalence principle to show convergence of dynamical system to desired orientation; verified results using MATLAB simulations

Technical Skills and Key Courses

- **Analog**: Mixed-Signal VLSI Design, CMOS Analog VLSI Design, Radio Frequency Microelectronics Chip Design, Delta-Sigma Converters, High Speed Interconnects
- **VLSI**: Advanced CMOS Logic and Flash Memory Devices, VLSI Design, Processor Design, Algorithmic Design of Digital Systems, Microprocessors
- **Controls**: Adaptive Control Theory, Mathematical Structures for Control, Control Systems
- **Miscellaneous**: Markov Chains and Queuing Systems, Error Correcting Codes, Communication Systems, Programming for Data Science, Electromagnetic Waves
- **Software**: Cadence Virtuoso, Cadence JasperGold, Sentaurus TCAD, Intel Quartus, EAGLE, GNU Radio, Keil
- **Programming**: Python, C++, MATLAB, VHDL, Verilog, Spice, Assembly, Embedded C, Arduino, LaTeX

Leadership Positions

Teaching Assistant | *Mixed-Signal VLSI Design* *[Jan. 2023 - May. 2023]*

- Served as a teaching assistant for a batch of 100 undergraduate and graduate students
- Designed Cadence Virtuoso assignments and final project for evaluation

Institute and Department Academic Mentor | *Student Mentorship Program* *[Jun. 2021 - Jun. 2022]*

- One among 13 third-year students selected based on a rigorous interview process and peer reviews
- Mentored 12 freshmen and 4 sophomores by guiding in academic/extracurricular endeavors
- Conducted tutorials and doubt-solving sessions for Analog Circuits and Power Engineering courses

Institute Academic Coordinator | *Student Support Services* *[Apr. 2020 - May 2021]*

- Among 12 selected out of 120+ applicants, addressing academic queries of 4500+ undergraduates
- Organized 20+ Tutorial Service Center sessions for 1200+ undergraduate freshmen and sophomores
- Compiled Information Booklets to ensure student awareness about institute academic policies

Core Team Member | *Electronics and Robotics Club* *[Apr. 2020 - May 2021]*

- Part of a 15 member team that aims to disseminate practical knowledge through technical hobby-activities
- Conducted Arduino, Control Theory bootcamps; contributed to ERC Wiki by writing articles on PID Control and Signal Processing
- Coordinated BLAH sessions where prominent alumni and students deliver talks on technical topics

EXTRACURRICULARS

- Part of Hyperloop IITB tech-team as a Junior Controls and Communication Engineer; qualified in the top 5 university teams internationally for the finals of the European Hyperloop Week (EHW 2021)
- Won Best Design Award in RC Plane competition held by Aeromodelling Club, IIT Bombay: a remote controlled plane making competition using BLDC and servo motors for wing control
- Engineered an all-terrain obstacle-maneuvering bot controlled using a mobile application
- Completed one year of training in Badminton under National Sports Organization at IIT Bombay
- Held the position of Head Girl in the school student council in the academic year 2015-16
- Participated in various state and district level competitions in roller skating, taekwondo, and painting