Sai Saketika Chekuri

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Education

Stanford University *Stanford, USA*
Master of Science in Electrical Engineering, Specialization - Circuits *[Sep. 2023 - Jun. 2025]*

Indian Institute of Technology Bombay *Mumbai, India*
Bachelor of Technology in Electrical Engineering with Honors *[Jul. 2019 - Aug. 2023]*

- **CGPA - 9.91/10**; Department Rank 1 amongst 164 students - **Institute Silver Medalist**
- Received the **Sharad Maloo Gold Medal** for being the most outstanding student of the graduating batch in terms of academic performance and extracurricular activities
- Conferred the **Prof. K. C. Mukherjee** Award for the best undergraduate thesis in the department

Research Projects

Logarithmic SAR Analog to Digital Converter Design *[Aug. 2022 - May 2023]*
Prof. Rajesh Zele, EE, IITB | Bachelor's Project

- Ideated a novel area-efficient SAR-based Logarithmic ADC topology with high dynamic range applications
- Designed a 5-bit differential Logarithmic SAR ADC on Cadence Virtuoso with 55 dB dynamic range, 4.6 mW power consumption; designed bootstrapped switch, bias generator, OTA and error amplifier circuit blocks

Two-Stage Differential OTA with Positive Feedback Compensation *[Jan. 2022 - May 2022]*
Prof. Rajesh Zele, EE, IITB | Research Project

- Designed a schematic of low-power high-gain OTA in GPDK 45 nm on Cadence Virtuoso, employing integrated active RC filters in positive feedback to cancel a pole with generated LHP zero
- Performed SS, TT, FF process corner simulations; obtained higher phase margin than Miller compensation

8-bit Segmented Current Steering Digital to Analog Converter *[Jan. 2022 - Apr. 2022]*
Prof. Rajesh Zele, EE, IITB | Mixed-Signal VLSI Design (EE 719) Course Project

- Designed a DAC operating at 1 GSps sampling frequency in GPDK 45 nm on Cadence Virtuoso
- Designed cascode current source biasing circuit, digital input driver for unit cell at transistor level, and integrated the scaled thermometer cells and digital decoder to implement the DAC from end-to-end
- Performed LVS and DRC checks on layout to meet design specifications after parasitic extraction

Decision Feedback Equalizer Design *[Jan. 2023 - Apr. 2023]*
Prof. Shalabh Gupta, EE, IITB | High Speed Interconnects (EE 800) Course Project

- Designed a DFE equalizer and achieved a 60% eye-opening improvement against no equalization
- Implemented a Phase Locked Loop with a Hogge phase detector for clock recovery in the DFE circuit
- Implemented the LMS algorithm in VerilogA for a 6-tap Feed Forward Equalization at the receiver for a 40% eye-opening improvement against no equalization, and characterized in Cadence Virtuoso

Internships

Formal Verification of UART Virtualization feature *[May 2022 - Jul. 2022]*
Google India | Summer Internship, Hardware Engineering Intern

- Wrote glue logic and testbenches in SystemVerilog to serialize data from AXI Stream to UART protocol and vice versa for virtualization and arbitration in debug hub between system CPU and AXI Stream interface
- Performed formal verification using the Cadence JasperGold tool for baud clock generator and UART FSMs

Bus Analyzer Tool *[May 2021 - Jul. 2021]*
Google India | Summer Internship, STEP (Student Training in Engineering Program) Intern

- Developed an off-time tool for SoC to analyze all NoC interfaces using the AXI-4 protocol and generate inferences about timing-related parameters and critical transaction attributes from raw transaction data

Technical Skills and Key Courses

- **VLSI**: Mixed-Signal VLSI Design, CMOS Analog VLSI Design, Radio Frequency Microelectronics Chip Design, Advanced CMOS Logic and Flash Memory Devices, Delta Sigma Data Converters, High Speed Interconnects
- **Software/Programming**: Cadence Virtuoso, Cadence JasperGold, Sentaurus TCAD, Intel Quartus, EAGLE, GNU Radio, Keil, Python, C++, MATLAB, VHDL, Verilog, Spice, Assembly, Embedded C